

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, NPN, SILICON, AMPLIFIER,
NON-HERMETIC (PLASTIC ENCAPSULATED), SURFACE MOUNT,
TYPES 2N3498, 2N3499, 2N3500, AND 2N3501,
QUALITY LEVELS JANP, JANPTX, AND JANPTXV

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for non-hermetic plastic encapsulated NPN, silicon, low-power amplifier and switching transistors. Three levels of product assurance (JANP, JANPTX, and JANPTXV) are provided for each encapsulated device.

1.2 Package outlines. The device package for the encapsulated device type is a TO-236AB (similar to SOT-23) in accordance with [figure 1](#).

1.3 Maximum ratings. Unless otherwise specified, at $T_A = +25^\circ\text{C}$.

Types	P_T $T_A = +25^\circ\text{C}$	P_T $T_C = +25^\circ\text{C}$	$R_{\theta JA}$	$R_{\theta JC}$	V_{CBO}	V_{CEO}	V_{EBO}	I_C	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C}/\text{W}$</u>	<u>$^\circ\text{C}/\text{W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>mA dc</u>	<u>$^\circ\text{C}$</u>
2N3498	1	5	175	30	100	100	6	500	-55
2N3499	1	5	175	30	100	100	6	500	to
2N3500	1	5	175	30	150	150	6	300	+150
2N3501	1	5	175	30	150	150	6	300	

Comments, suggestions, or questions on this document should be addressed to DLA Weapons Support, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

AMSC N/A

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FSC 5961



1.4 Primary electrical characteristics. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type	h_{FE} at	h_{FE} at	h_{FE} at	h_{FE} at	$ h_{fe} $	C_{obo}
	$V_{CE} = 10\text{ V dc}$ $h_{FE1} (1)$ $I_C = 0.1\text{ mA dc}$	$V_{CE} = 10\text{ V dc}$ $h_{FE4} (1)$ $I_C = 150\text{ mA dc}$	$V_{CE} = 10\text{ V dc}$ $h_{FE5} (1)$ $I_C = 300\text{ mA dc}$	$V_{CE} = 10\text{ V dc}$ $h_{FE6} (1)$ $I_C = 500\text{ mA dc}$	$V_{CE} = 20\text{ V dc}$ $I_C = 20\text{ mA dc}$ $f = 100\text{ MHz}$	$V_{CB} = 10\text{ V dc}$ $I_E = 0$ $100\text{ kHz} \leq f \leq 1\text{ MHz}$
	<u>Min</u> <u>Max</u>	<u>Min</u> <u>Max</u>	<u>Min</u> <u>Max</u>	<u>Min</u> <u>Max</u>	<u>Min</u> <u>Max</u>	<u>pF</u> <u>Min</u> <u>Max</u>
2N3498	20	40 120		15	1.5 8.0	10
2N3499	35	100 300		20	1.5 8.0	10
2N3500	20	40 120	15		1.5 8.0	8
2N3501	35	100 300	20		1.5 8.0	8

(1) Pulsed (see 4.5.1).

Types (1)	$V_{CE(sat)} (1)$	$V_{CE(sat)} (1)$	$V_{BE(sat)} (1)$	$V_{BE(sat)} (1)$	t_{on}	t_{off}
	$I_C = 10\text{ mA dc}$ $I_B = 1\text{ mA dc}$	$I_C = 300\text{ mA dc}$ $I_B = 30\text{ mA dc}$	$I_C = 10\text{ mA dc}$ $I_B = 1\text{ mA dc}$	$I_C = 300\text{ mA dc}$ $I_B = 30\text{ mA dc}$	$I_C = 150\text{ mA dc}$ $I_{B1} = 15\text{ mA dc}$ $V_{EB} = 5\text{ V dc}$	$I_C = 150\text{ mA dc}$ $I_{B1} = I_{B2} = 15\text{ mA dc}$
	<u>Min</u> V dc <u>Max</u> V dc	<u>Min</u> V dc <u>Max</u> V dc	<u>Min</u> V dc <u>Max</u> V dc	<u>Min</u> V dc <u>Max</u> V dc	<u>Max</u> ns	<u>Max</u> ns
2N3498		0.6		0.8	115	1,150
2N3499	0.2	0.6		0.8	115	1,150
2N3500	0.2			0.8	115	1,150
2N3501	0.2			0.8	115	1,150

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500 and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are "JANP", "JANPTX" and "JANPTXV".

1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follow: "3498", "3499", "3500", and "3501".

1.5.3 Suffix symbols. The following suffix letters are incorporated in the PIN in the order listed below.

1.5.3.1 First suffix symbol (package designators). The first set of suffix symbols designate the package outline for the devices covered by this specification sheet. The suffix letters "UJ3" are used on devices that use a plastic TO-236AB gullwing package.

1.5.3.2 Second suffix (terminal finish designator). The second set of suffix symbols designate the terminal finish. The available finishes are as follows:

-A	Hot solder dip
-C	Gold plate
-E	Gold flash palladium

2. APPLICABLE PUBLICATIONS

2.1 General. The publications listed in this section are specified in sections 3 and 4 of this specification. This section does not include publications cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of publications cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government publications.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these publications are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

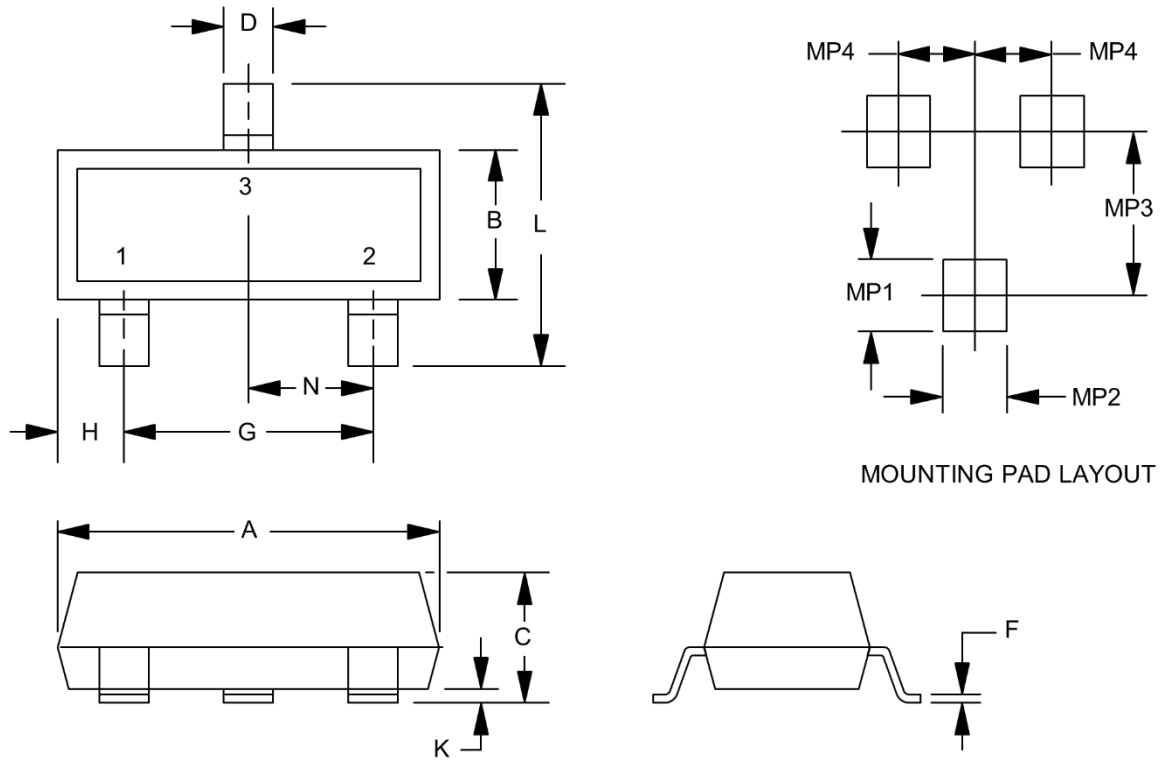
MIL-PRF-19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 – Test Methods for Semiconductor Devices.

(Copies of these publications are available online at <https://quicksearch.dla.mil/>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



Symbol	Dimensions				Symbol	Dimensions			
	inch		mm	mm		inch	inch	mm	mm
	Min	Max	Min	Max		Min	Max	Min	Max
A	.110	.122	2.8	3.1	K	.0004	.004	0.01	0.10
B	.047	.056	1.20	1.43	L	.094	.103	2.4	2.6
C	.035	.045	0.90	1.15	N	.037	.038	0.94	0.96
D	.012	.020	0.30	0.50	MP1	.035	.036	0.89	0.91
F	.003	.008	0.08	0.20	MP2	.031	.032	0.79	0.81
G	.074	.076	1.88	1.92	MP3	.078	.079	1.99	2.01
H	.018	.024	0.46	0.59	MP4	.037	.038	0.94	0.96

NOTES:

1. All dimensions are in inches. Millimeters are given for general information only.
2. Terminal numbers are shown for reference. 1 = Base, 2 = Emitter, 3 = Collector.

FIGURE 1. Physical dimensions of TO-236AB (similar to SOT-23) package.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows.

NGS	-	Non-Government Standard
UJ3	-	Unleaded, J-bend, 3 terminal plastic encapsulated (non-hermetic) package.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the PIN (see [1.5.3.2](#)) or acquisition document (see [6.2](#)).

3.4.2 Device construction. Devices shall be a non-hermetic, plastic encapsulated, with either a coated or uncoated die, wire bonded, non-cavity, construction in accordance with the requirements of [MIL-PRF-19500](#) and herein (see [figures 2](#) and [3](#)).

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.7 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (quality levels JANPTX and JANPTXV only). Screening shall be in accordance with table J-II of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements for JANPTX and JANPTXV levels
3c (1)	See 4.3.1
9	Not applicable.
11	I _{CBO2} and h _{FE4}
12	See 4.3.2
13	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE4} = ± 15 percent of initial value.

- (1) Shall be performed anytime after temperature cycling, screen 3a; JANPTX and JANPTXV levels do not need to be repeated in screening requirements.

4.3.1 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). The thermal impedance limit shall be less than the process determined statistical maximum limit as outlined in method 3131 of MIL-STD-750. See figure 4 for the layout of the substrate used for device mounting.

4.3.2 Power burn-in conditions. Power burn-in shall be performed in accordance with condition B of method 1039 of MIL-STD-750. The condition details shall be as follows: V_{CB} = 10 to 30 V dc; power shall be applied to achieve T_J = +135°C minimum using a minimum power dissipation = 75 percent of maximum rated P_T (see 1.3). No heat sink or forced air-cooling on the devices shall be permitted. Use method 3100 of MIL-STD-750 to measure T_J. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of subgroups 1 and 2 of table I herein, inspection only (table J-VIB, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection for quality levels JANP, JANPTX, and JANPTXV shall be conducted in accordance with the tests and conditions specified for subgroup testing in table J-VIC (small die flow) of MIL-PRF-19500 and herein. Delta measurements shall be taken after each step and shall be in accordance with 4.6 herein. The following details shall apply:

<u>Step</u>	<u>Method</u>	<u>Condition</u>
1	1026	Steady-state life: 1,000 hours minimum, $V_{CB} = 10$ V dc, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated P_T as defined in 1.3. $n = 45$ devices, $c = 0$. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, $T_A = +150^\circ\text{C}$, $V_{CB} = 80$ percent of rated voltage, 48 hours minimum. $n = 45$ devices, $c = 0$.
3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$. $n = 22$, $c = 0$.

4.4.2.1 Group B sample selection. Samples selected for group B inspection for JANP and JANPTX shall be selected randomly from a minimum of three wafers (or from each wafer in the lot). Separate samples may be used for each step.

4.4.2.2 Group B failures. All catastrophic failures during conformance inspection shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failure mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table J-V of MIL-PRF-19500 and herein. Delta limit measurements shall be in accordance with 4.6 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3 herein) $n = 22$, $c = 0$.
C6		Not applicable.

4.4.3.1 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table J-VI of MIL-PRF-19500 and as specified in table II herein. Delta measurements shall be in accordance with the applicable steps of 4.6.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

4.5.2 Safe operating area clamped switching test. The test shall be performed in accordance with condition B of method 3053 with the following details: The test circuit shall be in accordance with [figure 5](#); $T_A = +25^\circ\text{C}$; device fails if clamp voltage is not reached.

4.6 Delta measurements. Delta measurements shall be as specified below: 1/ 2/ 3/

Step	Inspection	MIL-STD-750		Symbol	Limit
		Method	Conditions		
1.	Collector to base cutoff current 2N3498, 2N3499 2N3500, 2N3501	3036	Bias condition D; $V_{CB} = 50\text{ V dc}$ $V_{CB} = 75\text{ V dc}$	ΔI_{CBO2}	± 100 percent of initial value or 10 nA dc, whichever is greater.
2.	Forward-current transfer ratio	3076	$V_{CE} = 10\text{ V dc}$; $I_C = 150\text{ mA dc}$; pulsed (see 4.5.1)	Δh_{FE4}	± 25 percent change from initial reading

- 1/ The delta measurements for group B inspection (table J-IVC of [MIL-PRF-19500](#)) shall be as follows: After each step in [4.4.2](#), steps 1 and 2.
- 2/ The delta measurements for group C inspection (table J-V of [MIL-PRF-19500](#)) shall be as follows: Subgroup 6, step 1.
- 3/ Devices which exceed the [table I](#), subgroup 2 limits shall not be returned to the lot, but will not be considered failures.

TABLE I. Group A inspection.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u> <u>2</u> /						
Small die flow inspections and tests.		See MIL-PRF-19500, table J-III, subgroup 1, for small die flow only.				
<u>Subgroup 2</u>						
Thermal impedance	3131	See 4.3.1	Z _{θJX}			°C/W
Collector to base cutoff current 2N3498, 2N3499 2N3500, 2N3501	3036	Condition D V _{CB} = 100 V dc V _{CB} = 150 V dc	I _{CBO1}		10 10	μA dc μA dc
Collector to emitter cutoff current 2N3498, 2N3499 2N3500, 2N3501	3041	Condition D; pulsed (see 4.5.1) V _{CE} = 80 V dc V _{CE} = 120 V dc	I _{CEO}		1 1	μA dc μA dc
Breakdown voltage, collector to emitter 2N3498, 2N3499 2N3500, 2N3501	3011	Bias condition D; pulsed (see 4.5.1) I _C = 10 mA dc	V _{(BR)CEO}	100 150		V dc V dc
Emitter to base, cutoff current	3061	Bias condition D; V _{EB} = 6 V dc	I _{EBO1}		10	μA dc
Collector to base cutoff current 2N3498, 2N3499 2N3500, 2N3501	3036	Bias condition D V _{CB} = 50 V dc V _{CB} = 75 V dc	I _{CBO2}		50 50	nA dc nA dc
Emitter to base cutoff current	3061	Bias condition D; V _{EB} = 4 V dc	I _{EBO2}		25	nA dc
Collector to emitter saturation voltage	3071	I _C = 10 mA dc; I _B = 1 mA dc; pulsed (see 4.5.1)	V _{CE(sat)1}		0.2	V dc
Collector to emitter saturation voltage (2N3500, 2N3501 only)	3071	I _C = 150 mA dc; I _B = 15 mA dc; pulsed (see 4.5.1)	V _{CE(sat)2}		0.4	V dc
Collector to emitter saturation voltage (2N3498, 2N3499 only)	3071	I _C = 300 mA dc; I _B = 30 mA dc; pulsed (see 4.5.1)	V _{CE(sat)3}		0.6	V dc

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
Subgroup 2 – continued						
Base emitter saturation voltage	3066	Test condition A; I _C = 10 mA dc; I _B = 1 mA dc; pulsed (see 4.5.1)	V _{BE(sat)1}		0.8	V dc
Base emitter saturation voltage (2N3500, 2N3501 only)	3066	Test condition A; I _C = 150 mA dc; I _B = 15 mA dc; pulsed (see 4.5.1)	V _{BE(sat)2}		1.2	V dc
Base emitter saturation voltage (2N3498, 2N3499 only)	3066	Test condition A; I _C = 300 mA dc; I _B = 30 mA dc; pulsed (see 4.5.1)			1.4	V dc
Forward-current transfer ratio 2N3498, 2N3500 2N3499, 2N3501	3076	V _{CE} = 10 V dc; I _C = 0.1 mA dc; pulsed (see 4.5.1)	h _{FE1}	20 35		
Forward-current transfer ratio 2N3498, 2N3500 2N3499, 2N3501	3076	V _{CE} = 10 V dc; I _C = 1.0 mA dc; pulsed (see 4.5.1)	h _{FE2}	25 50		
Forward-current transfer ratio 2N3498, 2N3500 2N3499, 2N3501	3076	V _{CE} = 10 V dc; I _C = 10 mA dc; pulsed (see 4.5.1)	h _{FE3}	35 75		
Forward-current transfer ratio 2N3498, 2N3500 2N3499, 2N3501	3076	V _{CE} = 10 V dc; I _C = 150 mA dc; pulsed (see 4.5.1)	h _{FE4}	40 100	120 300	
Forward-current transfer ratio 2N3500 2N3501	3076	V _{CE} = 10 V dc; I _C = 300 mA dc; pulsed (see 4.5.1)	h _{FE5}	15 20		
Forward-current transfer ratio 2N3498 2N3499	3076	V _{CE} = 10 V dc; I _C = 500 mA dc; pulsed (see 4.5.1)	h _{FE6}	15 20		

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High temperature operation		T _A = +150°C				
Collector to base cutoff current 2N3498, 2N3499 2N3500, 2N3501	3036	Bias condition D V _{CB} = 50 V dc V _{CB} = 75 V dc	I _{CBO3}		50	μA dc
Low temperature operation		T _A = -55°C				
Forward-current transfer ratio 2N3498, 2N3500 2N3499, 2N3501	3076	V _{CE} = 10 V dc; I _C = 150 mA dc	h _{FE7}	22 45		
<u>Subgroup 4</u>						
Magnitude of small-signal short- circuit forward current transfer ratio	3306	V _{CE} = 20 V dc; I _C = 20 mA dc; f = 100 MHz	h _{fe}	1.5	8	
Small-signal short-circuit forward current transfer ratio 2N3498, 2N3500 2N3499, 2N3501	3206	V _{CE} = 10 V dc; I _C = 10 mA dc; f = 1 kHz	h _{fe}	35 75	300 375	
Open circuit output capacitance 2N3498, 2N3499 2N3500, 2N3501	3236	V _{CB} = 10 V dc; I _E = 0; 100 kHz ≤ f ≤ 1 MHz	C _{obo}		10 8	pF pF
Input capacitance (output open-circuited)	3240	V _{EB} = 0.5 V dc; I _C = 0; 100 kHz ≤ f ≤ 1 MHz	C _{ibo}		80	pF
Noise figure (Test 1)	3246	V _{CE} = 10 V dc; I _C = 0.5 mA dc; R _g = 1 kΩ; f = 1 kHz	NF		16	dB
Noise figure (Test 2)	3246	V _{CE} = 10 V dc; I _C = 0.5 mA dc; R _g = 1 kΩ; f = 10 kHz	NF		6	dB
Turn-on time		V _{EB} = 5 V dc; I _C = 150 mA dc; I _{B1} = 15 mA dc; (see figure 6)	t _{on}		115	ns
Turn-off time		I _C = 150 mA dc, I _{B1} = I _{B2} = 15 mA dc; (see figure 6)	t _{off}		1150	ns

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u> Safe operating area (continuous dc) <u>Test 1</u> 2N3498, 3N3499 2N3500, 3N3501 <u>Test 2</u> 2N3498, 2N3499, 2N3500, 2N3501 <u>Test 3</u> 2N3498, 2N3499, 2N3500, 2N3501 Safe operating area (clamped switching) 2N3498, 2N3499 2N3500, 2N3501 Electrical measurements <u>Subgroup 6</u> Not required	3051	T _C = 25°C; t _r ≥ 10 ns; 1 cycle; (see figure 7); t = 1 s V _{CE} = 10 V dc; I _C = 500 mA dc V _{CE} = 16.67 V dc; I _C = 300 mA dc V _{CE} = 50 V dc; I _C = 100 mA dc V _{CE} = 80 V dc; I _C = 40 mA dc See 4.5.2 I _B = 85 mA dc; I _C = 500 mA dc I _B = 50 mA dc; I _C = 300 mA dc See table I, subgroup 2 herein.				
	3053					

1/ For sampling plan see [MIL-PRF-19500](#), unless otherwise specified.

2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests. A failure in [table I](#), subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not required for laser marked devices.

TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices, c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Electrical measurements		See table I , subgroup 2 and 4.6 herein.	
<u>Subgroup 2</u>			45 devices, c = 0
Intermittent life	1037	Intermittent operation life: $V_{CB} = 10$ V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	
Electrical measurements		See table I , subgroup 2 and 4.6 herein.	
<u>Subgroup 4</u>			10 devices, c = 0
Thermal resistance	3131	See figure 4 for substrate layout.	
Thermal impedance curves		See subgroup 4 of table E-IX of MIL-PRF-19500	Sample size N/A
<u>Subgroup 6</u>			
ESD	1020		

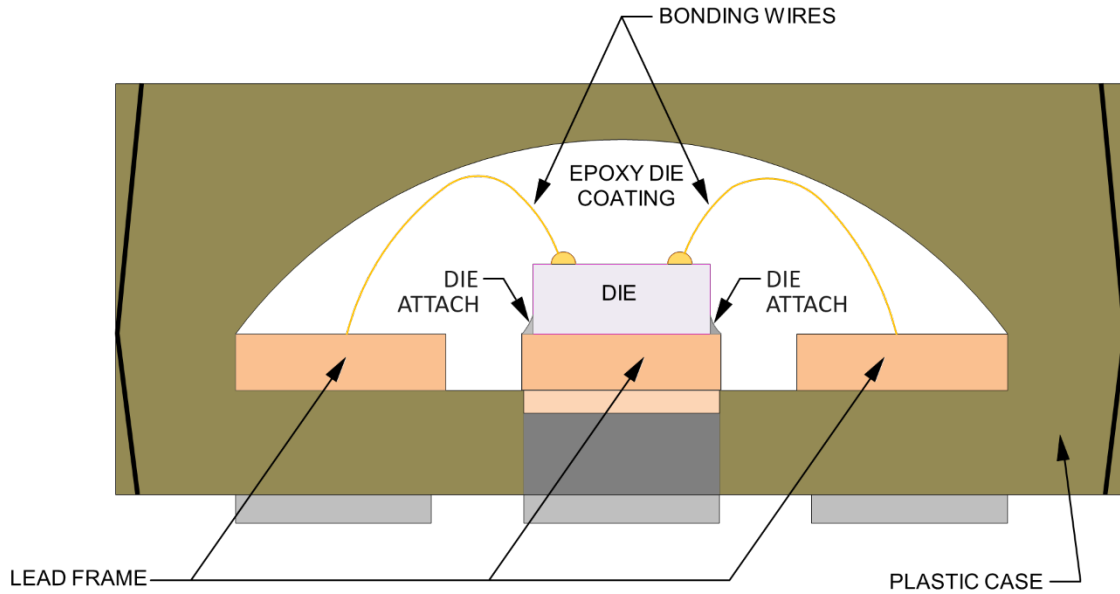


FIGURE 2. Sample construction using secondary die coating.

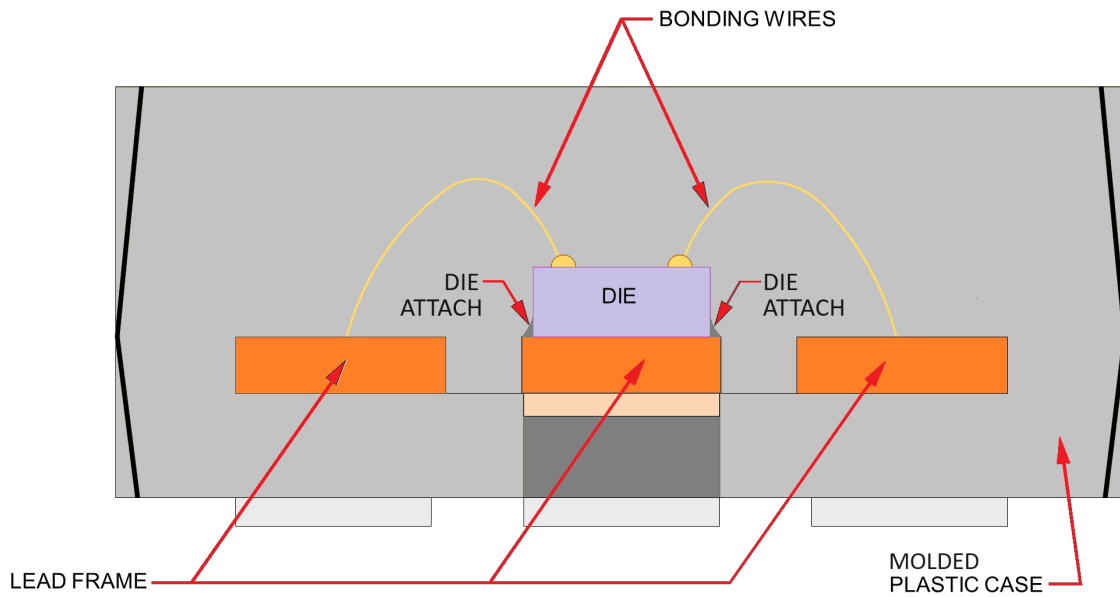


FIGURE 3. Sample construction without secondary die coating.

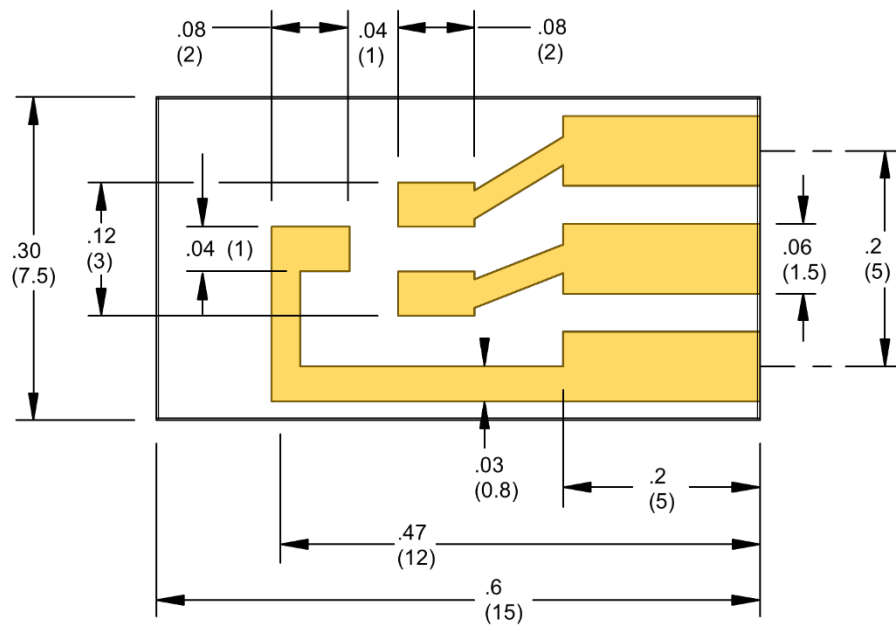
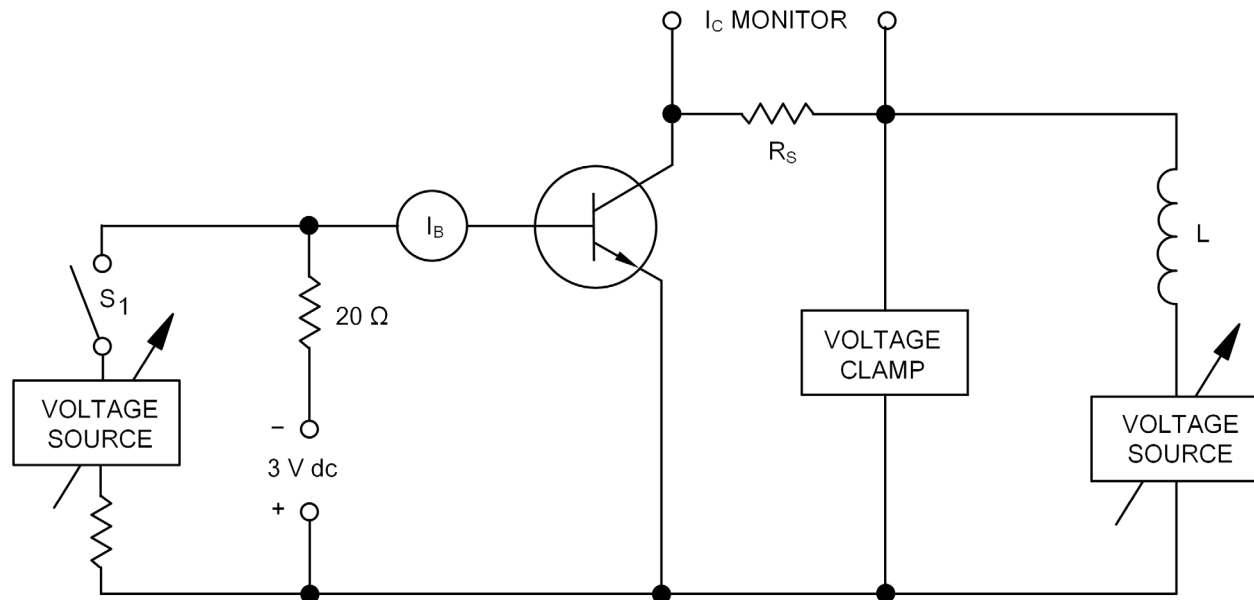


FIGURE 4. Layout for R_{6JA} test.



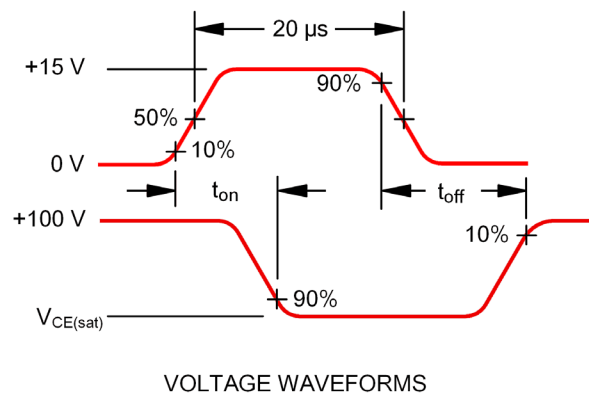
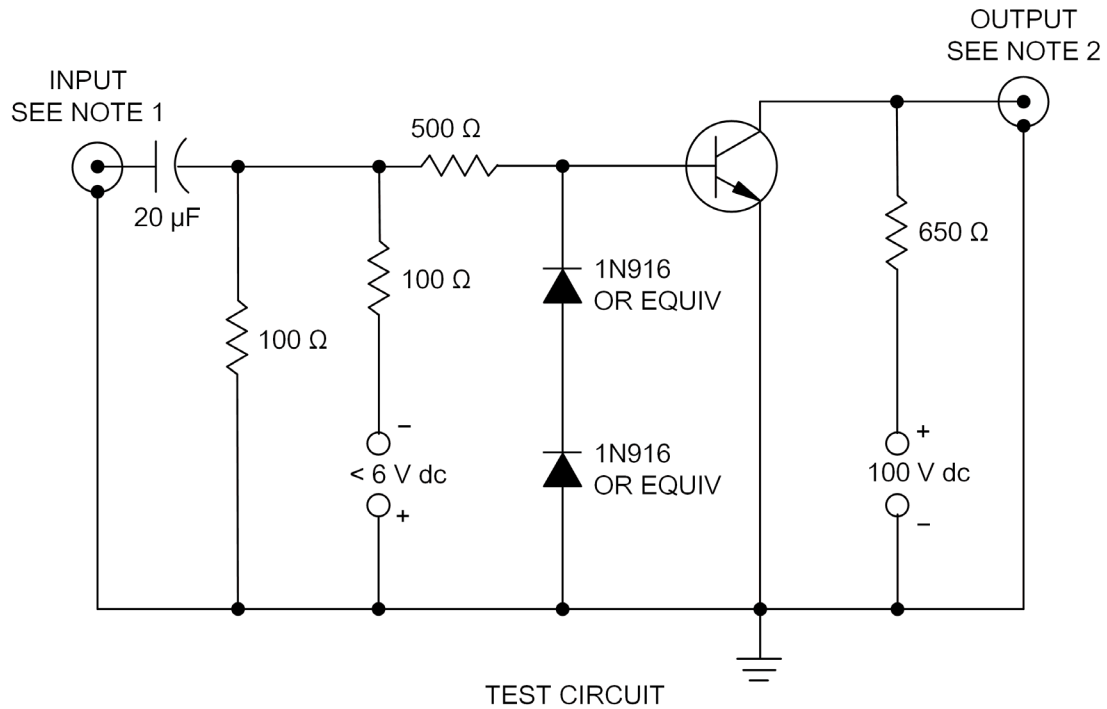
PROCEDURE:

1. With switch S_1 closed, set the specified test conditions.
2. Open S_1 .
3. Perform specified end-point tests.

NOTES:

1. Voltage clamp: 2N3498, 2N3499 = 100 V dc; 2N3500, 2N3501 = 150 V dc.
2. $R_S \leq 1.0$ ohm (noninductive).
3. $L = 25$ mH, 0.425Ω (STANCOR C-2686 or equivalent).

FIGURE 5. SOA clamped inductive sweep test circuit diagram.



NOTES:

1. The input waveform is supplied by a pulse generator with the following characteristics: Pulse width = 20 μ s, pulse repetition rate = 1 kHz, rise time (t_r) and fall time (t_f) $\leq$ 10 ns, duty cycle $\leq$ 2 percent.
2. The output waveform is monitored on a sampling oscilloscope with $Z_{in} \geq 1$ ms and $t_r \leq 1$ ns.

FIGURE 6. Turn-on, turn-off switching time test circuit.

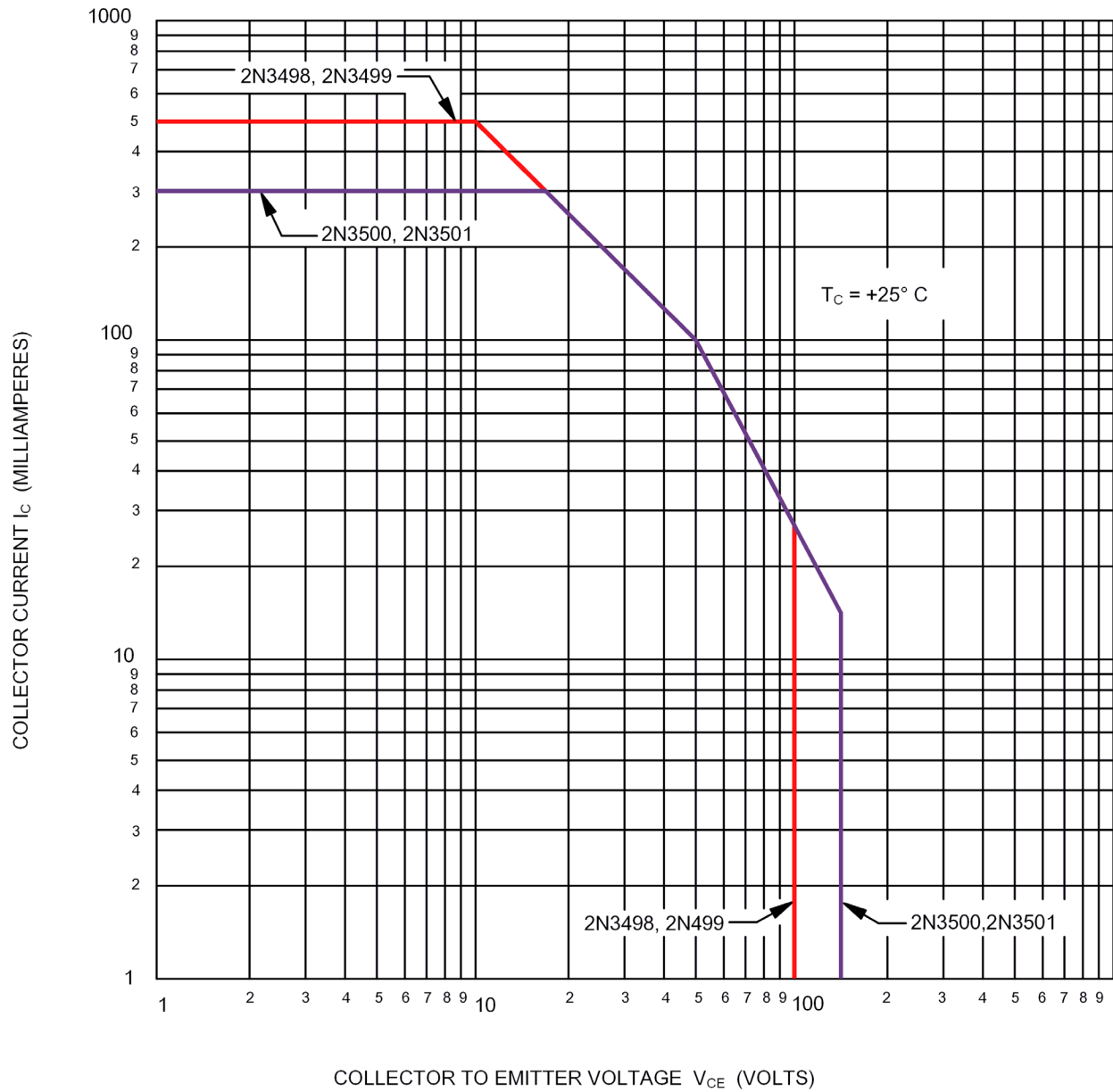


FIGURE 7. Maximum safe operating area (SOA).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

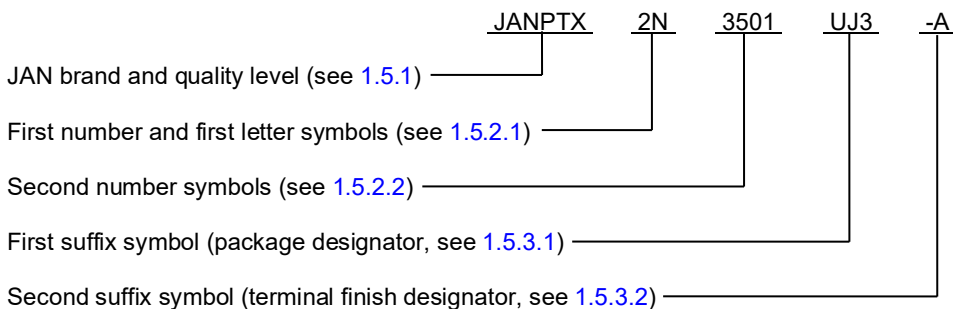
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. The complete PIN, see [1.5](#) and [6.5](#).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Weapons Support, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



6.5 List of PINs. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level
JANP2N3498UJ3-#	JANPTX2N3498UJ3-#	JANPTXV2N3498UJ3-#
JANP2N3499UJ3-#	JANPTX2N3499UJ3-#	JANPTXV2N3499UJ3-#
JANP2N3500UJ3-#	JANPTX2N3500UJ3-#	JANPTXV2N3500UJ3-#
JANP2N3501UJ3-#	JANPTX2N3501UJ3-#	JANPTXV2N3501UJ3-#

The number sign (#) represents a placeholder for one of the three terminal finish designators "A", "C" or "E" (see 1.5.3.2).

6.6 Alternate hermetic configurations. Alternate configurations of the devices covered by this specification sheet are available on [MIL-PRF-19500/366](#) as either hermetic packaged devices or unencapsulated die.

CONCLUDING MATERIAL

Custodians:
 Army – CR
 Navy – SH
 Air Force – 85
 NASA – NA
 DLA – CC

Preparing activity:
 DLA – CC

(Project 5961-2026-051)

Review activities:
 Army – AR, MI
 Navy – AS
 Air Force – 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.