

The documentation and process conversion measures necessary to comply with this document shall be completed by 26 November 2024.

INCH-POUND

MIL-PRF-19500/198F
w/AMENDMENT 1
26 June 2024
SUPERSEDING
MIL-PRF-19500/198F
28 October 2014

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, THYRISTORS,
TYPES 2N1870A, 2N1871A, 2N1872A, AND 2N1874A, JAN

Inactive for new design after 4 September 2007.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for silicon thyristors. One level of product assurance is provided for each device type as specified in [MIL-PRF-19500](#).

1.2 Physical dimensions. The device package outline is a TO-205AA (formerly TO-5) in accordance with [figure 1](#).

1.3 Maximum ratings. (1)

I_o $T_A = +100^\circ\text{C}$	$I_{f(\text{surge})}$	V_G V_{CG}	I_G	i_G	Operating and storage temperature	Operating altitude
<u>mA dc</u>	<u>a</u>	<u>V dc</u>	<u>mA dc</u>	<u>ma</u>	<u>°C</u>	<u>mm Hg</u>
220	15	5	25	250	-65 to +150	15

Type	V_{RM} (2)	V_{FBXM} (2)
	<u>V(pk)</u>	<u>V(pk)</u>
2N1870A	30	30
2N1871A	60	60
2N1872A	100	100
2N1874A	200	200

(1) For additional information on ratings see [figures 2 and 3](#).

(2) Blocking voltage ratings apply with gate connected through a resistor, $R_2 = 1 \text{ k}\Omega$, to cathode as shown on [figure 4](#).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dlamail. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

AMSC N/A

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FSC 5961



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1.4 Primary electrical characteristics.

Limits	V_f $I_f = 2A$	I_H	V_{GT} $V_{AC} = 5V$ $R_E = 1k\Omega$	I_{GT} $V_{AC} = 5V$ $R_E > 1k\Omega$
	<u>V</u>	<u>mA dc</u>	<u>V dc</u>	<u>μA dc</u>
Min		0.3	0.4	
Max	2.5	5.0	0.8	200

1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.4](#) for PIN construction example and [6.5](#) for a list of available PINs.

1.5.1 JAN certification mark and quality level. The only quality level designator for encapsulated devices that is applicable for this specification sheet is the base quality level "JAN" that uses no modifiers.

1.5.2 Device type. The designation system for the devices covered by this specification sheet is as follows.

1.5.2.1 First number and first letter symbols. The devices of this specification sheet use the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the devices covered by this specification sheet are as follows: "1870", "1871", "1872", and "1874".

1.5.3 Suffix symbols. The "A" suffix symbol indicates a modified version of the non-suffix device.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

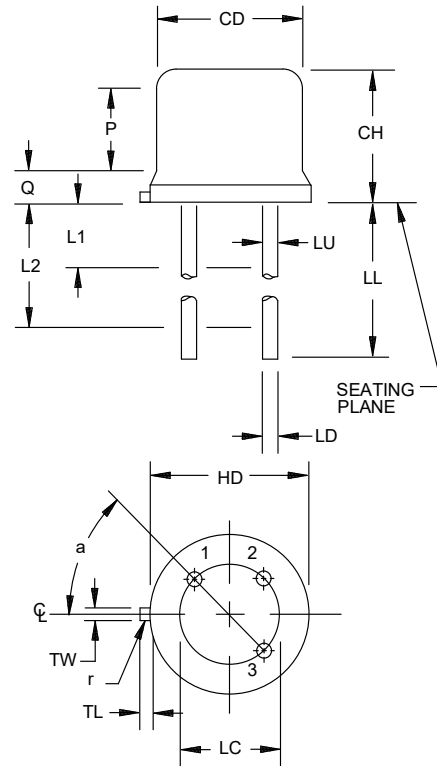
[MIL-STD-750](#) – Test Methods For Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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Symbol	Dimensions				Note
	Inch	Inch	mm	mm	
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	3
CH	.200	.260	5.08	6.60	
HD	.335	.370	8.51	9.40	3
LC	.200	TP	5.08	TP	4
LD	.016	.019	0.41	0.48	5, 6
LL	1.500	1.750	38.1	44.45	5, 6
LU	.016	.019	0.41	0.48	5, 6
L1		.050		1.27	5, 6
L2	.250		6.35		5, 6
P	.100		2.54		7
Q		.030		0.76	3, 8
TL	.029	.045	0.74	1.14	9
TW	.028	.034	0.71	0.86	9
r		.010		0.25	9, 10
α	45°		45°		4



NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Terminal 1 = cathode, terminal 2 = gate, terminal 3 = anode. All terminals are electrically insulated from the case.
3. Body contour optional within zone defined by dimensions CD, HD, and Q.
4. Leads at gauge plane $.054 + .001 - .000$ inch ($1.37 + 0.03 - 0.00$ mm) below seating plane shall be within $.007$ inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods.
5. Dimension LD applies between dimensions L2 and LL minimum. Diameter is uncontrolled in dimension L1 and beyond dimension LL minimum. Dimension LU applies between dimensions L1 and L2. Outside of these zones the lead diameter is not controlled.
6. All three leads.
7. This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed $.010$ inch (0.25 mm).
8. Details of outline in this zone are optional.
9. Tab is optional.
10. Dimension r (radius) applies to both inside corners of tab.
11. Leads may be soldered to within $.063$ inch (1.60 mm) of base. Heat sinking not required if temperature-time exposure is less than 230°C for 10 seconds.
12. This device is for socketed single-sided circuit-board, wire-in, and similar applications. Where used in double sided or eyeletted circuit-board, or similar applications where solder bridging may occur, a dielectric washer or other standoff device may be necessary.

FIGURE 1. Physical dimensions for TO-205AA package (formerly TO-5).

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3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#), and as follows:

I _{FBX}	DC forward blocking current with resistor R ₂ across gate and cathode.
I _{RBX}	DC reverse blocking current with resistor R ₂ across gate and cathode.
i _G	Peak gate current.
V _{AA}	Anode power supply voltage (dc).
V _{CG}	Reverse gate voltage.
V _{FBX}	Forward anode voltage.
V _G	Rated reverse gate voltage.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on [figure 1](#).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#). At the option of the manufacturer, marking of the country of origin may be omitted from the body of the transistor, but shall be retained on the initial container.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.7 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#) herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Conformance inspection (see [4.3](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.3 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.3.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#), [table I](#) herein, and as specified herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

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4.3.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN) of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1040	Operational life, see 4.6, test circuit on figure 6, $T_A = +100^{\circ}\text{C}$.
B6	1031	$T_A = +150^{\circ}\text{C}$.

4.3.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E, Lead fatigue.
C6	1031	$T_A = +150^{\circ}\text{C}$.

4.4 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.4.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5 Holding current. The holding current is measured by decreasing the anode current to the point where the device under test switches from the on-state to the off-state. The gate current shall be $-150\text{ }\mu\text{A}$ and the anode supply voltage shall be 5 volts. The test circuit shown on figure 5, or its equivalent, may be used. Resistor R_4 is increased, thereby decreasing device anode current, until the device switches to the off-state. The current measured by M_1 immediately prior to switching is the holding current. Switch S_1 is used to trigger the device to the on-state prior to making a holding current measurement.

4.6 Operational life test. The operational life test shall be performed in the test circuit shown on figure 6, or its equivalent. Transformer T_1 is adjusted such that the peak value of secondary voltage from T_3 equals the rated forward blocking voltage of the device under test. Transformer T_2 is adjusted such that meter reads 220 mA average rectified current. Transformer T_5 is selected to provide a maximum secondary peak voltage of 5 volts as read on meter M_3 . The device under test shall be in an oven at an ambient temperature of $+100^{\circ}\text{C} \pm 5^{\circ}\text{C}$.

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TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Forward blocking current 2N1870A 2N1871A 2N1872A 2N1874A	4206	DC method, bias condition B; $R_2 = 1,000 \Omega$, .25 watt $V_{FBX} = 30$ $V_{FBX} = 60$ $V_{FBX} = 100$ $V_{FBX} = 200$	I_{FBX}		10	μA dc
Reverse blocking current 2N1870A 2N1871A 2N1872A 2N1874A	4211	DC method, bias condition B; $R_2 = 1,000 \Omega$, .25 watt $V_{FBX} = -30$ $V_{FBX} = -60$ $V_{FBX} = -100$ $V_{FBX} = -200$	I_{RBX}		10	μA dc
Gate trigger current	4221	$V_2 = V_{FBX} = 5$ V dc $R_e = 1,000 \Omega$; $R_L = 100 \Omega$	I_{GT}		200	μA dc
Gate trigger voltage	4221	$V_2 = V_{FBX} = 5$ V dc $R_e = 1,000 \Omega$, $R_L = 100 \Omega$	V_{GT}	0.4	0.8	V dc
Forward "on" voltage	4226	$I_{FM} = 2$ a(pk) (pulse); pulse width = 8.5 ms; maximum; duty cycle = 2 percent maximum	V_f		2.5	V dc
Exponential rate of voltage rise	4231	Bias condition B; repetition rate = 60 pps; $50 \Omega \leq R_L \leq 400 \Omega$; $C = .001 \mu F$ min; $R_3 = 1,000 \Omega$ test duration = 15 sec	V_{FBX}			
2N1870A		$dv/dt = 100$ V/ μs ; $V_{AA} = 30$ V dc		25		V dc
2N1871A		$dv/dt = 60$ V/ μs ; $V_{AA} = 60$ V dc		55		V dc
2N1872A		$dv/dt = 40$ V/ μs ; $V_{AA} = 100$ V dc		95		V dc
2N1874A		$dv/dt = 30$ V/ μs ; $V_{AA} = 200$ V dc		190		V dc

See footnote at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued						
Reverse gate current	4219	V _{CG} = 5 V dc, anode open	I _{KG}		10	µA dc
Holding current	4201	Bias condition B, I _G = -150 µA dc, V _{AA} = 5 V dc, R ₂ = 100 Ω, I _{F1} = 100 mA dc, I _{F2} = 10 mA dc, trigger voltage source = 5 V dc; trigger pulse width = 25 µs (minimum)	I _H	0.3	5	mA dc
<u>Subgroup 3</u>						
High temperature operation:		T _A = +125°C				
Forward blocking current 2N1870A 2N1871A 2N1872A 2N1874A	4206	DC method, bias condition B, R ₂ = 1,000 Ω V _{FBX} = 30 V _{FBX} = 60 V _{FBX} = 100 V _{FBX} = 200	I _{FBX}		100	µA dc
Reverse blocking current 2N1870A 2N1871A 2N1872A 2N1874A	4211	DC method, bias condition B; R ₂ = 1,000 Ω V _{FBX} = -30 V _{FBX} = -60 V _{FBX} = -100 V _{FBX} = -200	I _{RBX}		100	µA dc
Gate trigger voltage	4221	V ₂ = V _{FBX} = 5 V, R _e = 1,000 Ω R _L = 100 Ω	V _{GT}	0.2		V dc
Holding current	4201	Bias condition B, I _G = -150 µA dc, V _{AA} = 5 V dc R ₂ = 100 Ω, I _{F1} = 100 mA dc, I _{F2} = 10 mA dc, trigger voltage source = 5 V dc; trigger pulse width = 25 µs (minimum)	I _H	0.2		mA dc
Low temperature operation:		T _A = -65°C				

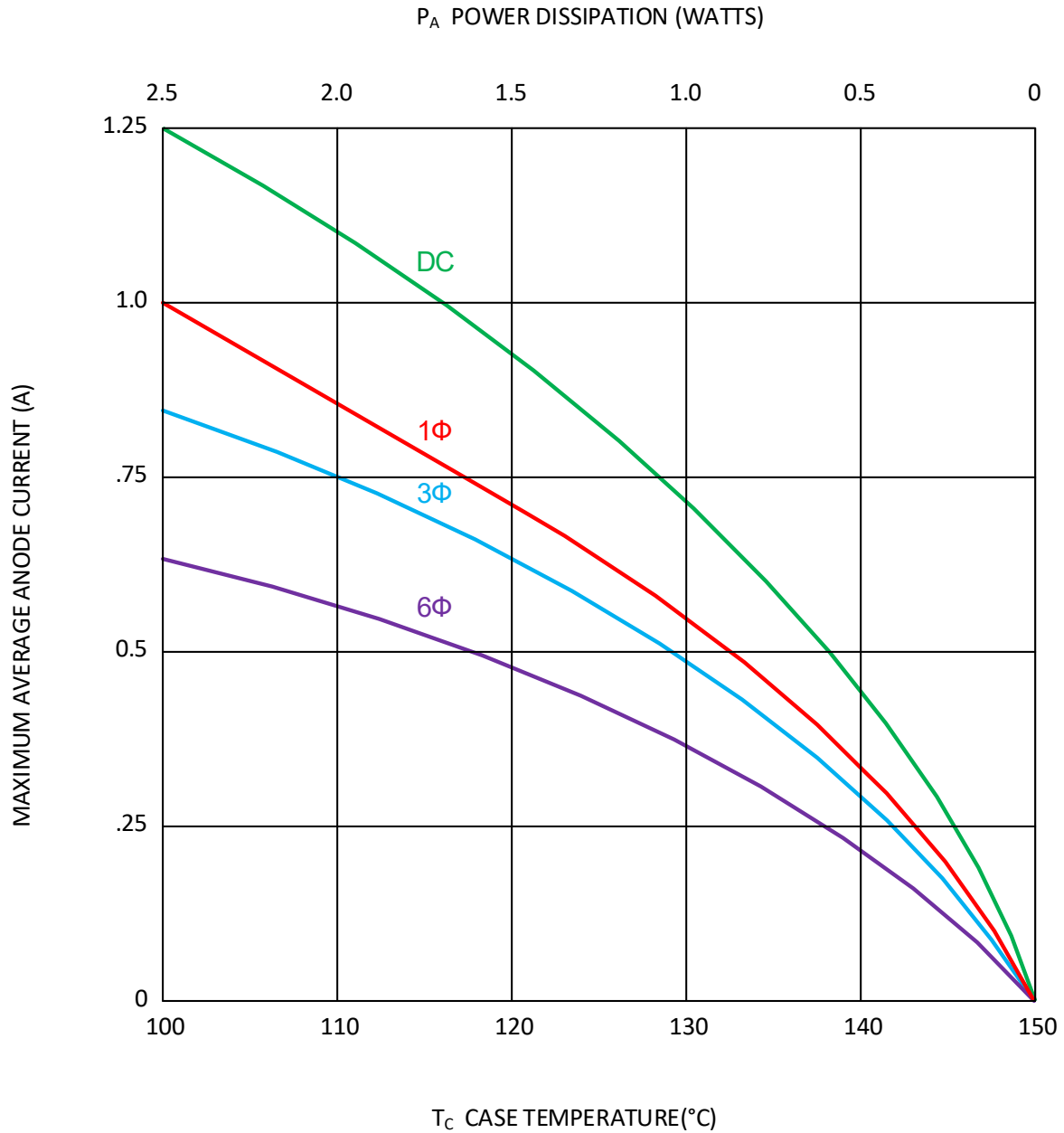
See footnote at end of table.

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TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - Continued						
Gate trigger voltage	4221	$V_2 = V_{FBX} = 5 \text{ V}$, $R_e = 1,000 \text{ } \Omega$; $R_L = 100 \text{ } \Omega$	V_{GT}		1.0	V dc
Gate trigger current	4221	$V_2 = V_{FBX} = 5 \text{ V}$, $R_e = 1,000 \text{ } \Omega$; $R_L = 100 \text{ } \Omega$	I_{GT}		500	μA dc
Holding current	4201	$I_G = -150 \text{ } \mu\text{A}$ dc, $V_{AA} = 5 \text{ V}$ dc	I_H		15	mA dc
<u>Subgroups 4 and 5</u>						
Not applicable						
<u>Subgroup 6</u>						
Surge current	4066	Condition A; $I_F = 15 \text{ A(pk)}$ (.5 sine wave); Ten surges per minute; $I_O = 250 \text{ mA}$ dc at rated V_{RRM} ; $T_C = +65^\circ\text{C}$; $f = 60 \text{ Hz}$; surge duration = 7 ms, minimum.				
Electrical measurements		See table I , group A, subgroup 2				

1/ For sampling plan, see [MIL-PRF-19500](#).



NOTES: Ratings apply for 50 to 400 Hz frequency.

FIGURE 2. Anode current rating as a function of operating case temperature.

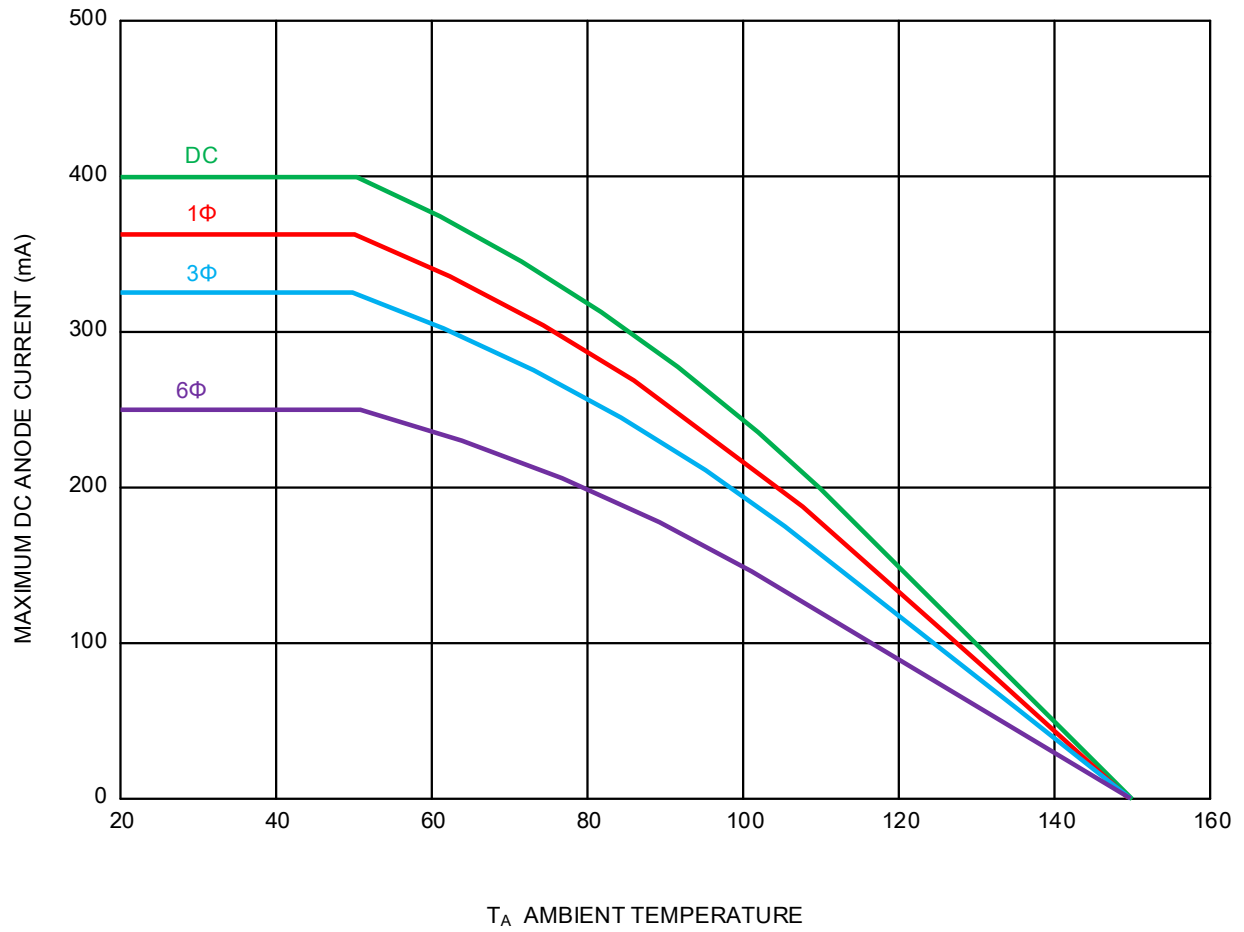


FIGURE 3. Anode current rating as a function of operating ambient temperature.

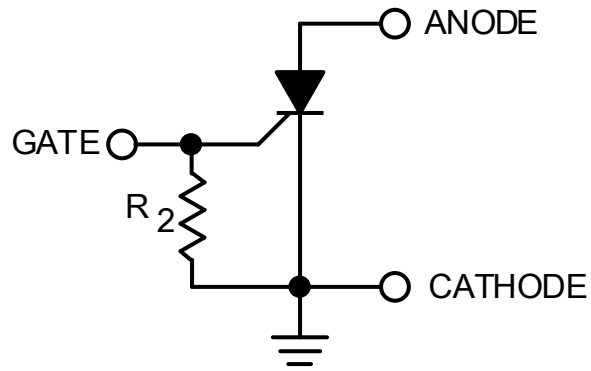
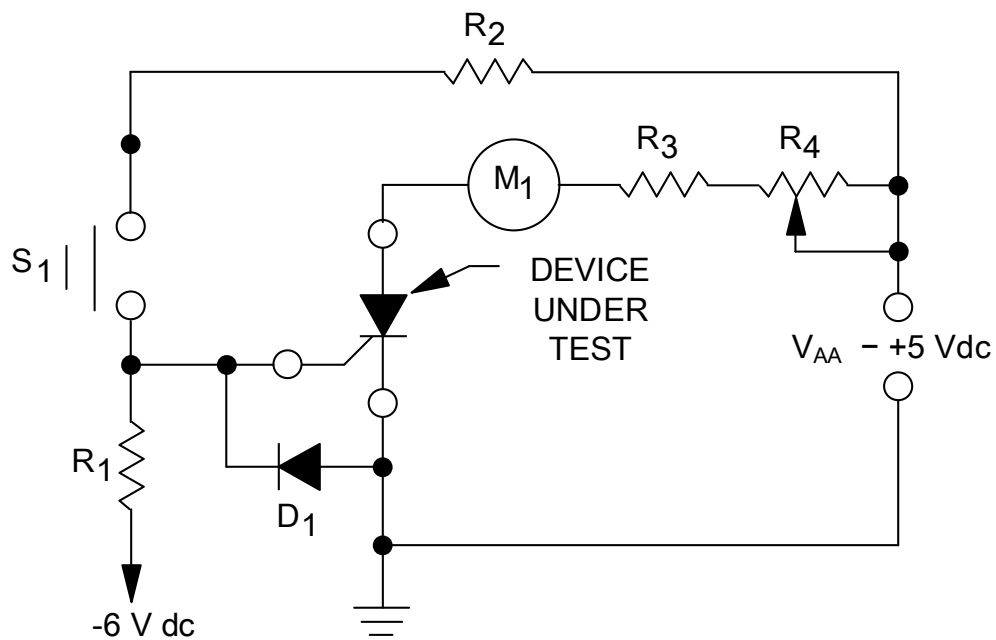
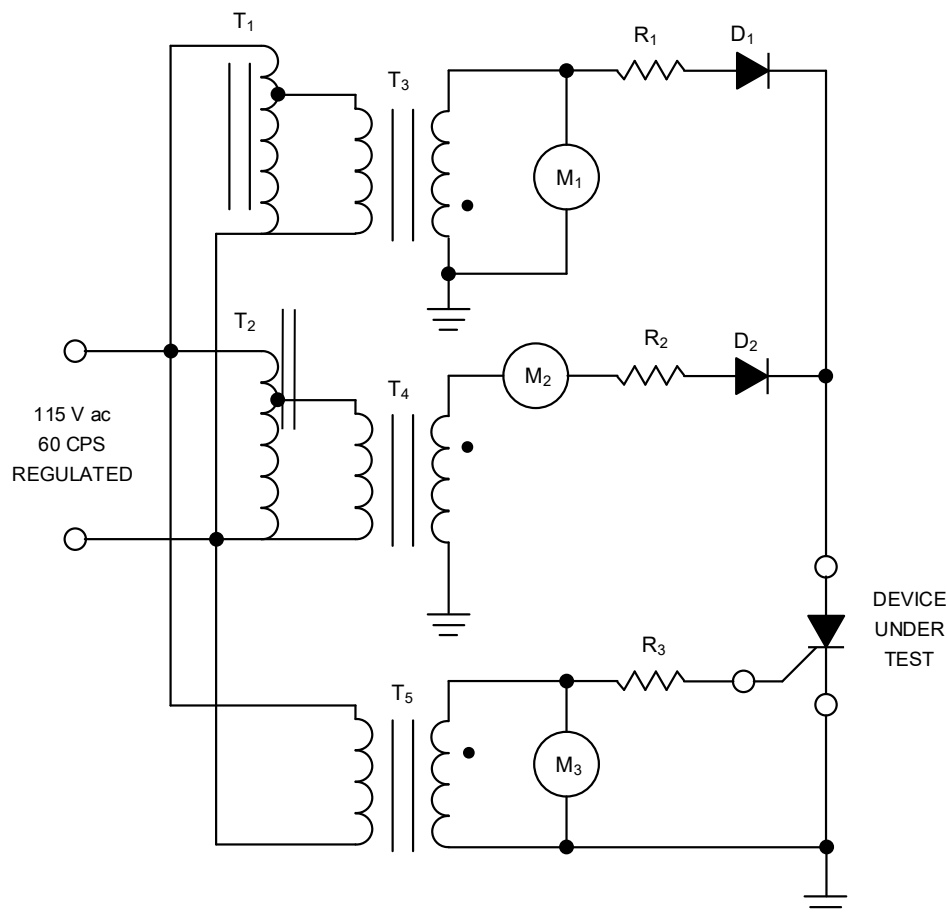


FIGURE 4. Condition for blocking voltage rating.



M ₁	DC milliammeter	R ₁	40 kΩ, 1/4 watt
S ₁	Trigger on switch, momentary type, normally open	R ₂	4,700 Ω, 1/4 watt
D ₁	1N457 diode	R ₃	270 Ω, 1/4 watt
		R ₄	25 kΩ potentiometer

FIGURE 5. Test circuit for holding current.



NOTES:

1. The dots adjacent to the secondary windings for T₃, T₄, and T₅ show their relative phase relationships.
2. The parameters for the components used in the test circuit are as follows:

D ₁ , D ₂	1N540
R ₁	20 kΩ, 1/2 watt
R ₂	20 Ω, 20 watt
R ₃	1,000 Ω, 1/4 watt
M ₁	Peak reading voltmeter or RMS equivalent (0 – 250 volts)
M ₂	DC millimeter 0 – 300 mA
M ₃	Peak reading voltmeter or RMS equivalent (0 – 10 volts)
T ₁ , T ₂	115 VAC adjustable transformer
T ₃	Step up transformer 115 VAC to 140 VAC
T ₄	Step down transformer 115 VAC to 12 VAC
T ₅	Step down transformer 115 VAC to 3.0 VAC

FIGURE 6. Operational life test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

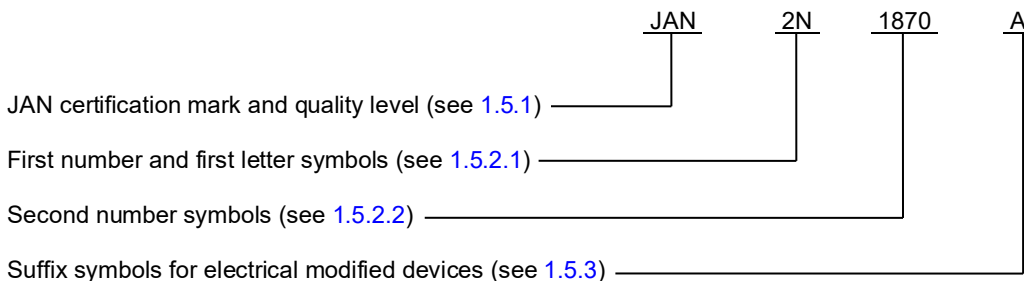
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.4.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: /VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 PIN construction example. The PINs are constructed using the following form.



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6.5 List of PINs. The following is a list of possible PINs available for devices covered by this specification sheet.

Quality level "JAN"	JAN2N1870A	JAN2N1871A	JAN2N1872A	JAN2N1874A
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6.6 Superseded PINs. The following supersession data applies to PINs associated with this document:

Superseded PIN by MIL-S-19500/198A(NAVY) dated 11 January 1969	Original PIN as specified within MIL-S-19500/198(NAVY) dated 13 June 1961
JAN2N1870A	USN-2N1870A
JAN2N1871A	USN-2N1871A
JAN2N1872A	USN-2N1872A
JAN2N1874A	USN-2N1874A

6.7 Amendment notations. The margins of this specification are marked with vertical lines to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
Army – CR
Navy – SH
Air Force – 11
DLA – CC

Preparing activity:
DLA – CC
(Project 5961-2024-040)

Review activities:
Army – MI
Navy – AS, MC
Air Force – 19

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