The documentation and process conversion measures necessary to comply with this document shall be completed by 13 January 2022.

INCH–POUND

MIL-PRF-19500/180E
w/AMENDMENT 3
13 October 2021
SUPERSEDING
MIL-PRF-19500/180E
w/AMENDMENT 2
5 September 2016

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, NPN, SILICON, MEDIUM-POWER,
THROUGH-HOLE MOUNT PACKAGE,
TYPES 2N1483, 2N1484, 2N1485, AND 2N1486,
QUALITY LEVELS JAN, JANTX, JANTXV

Inactive for new design after 7 June 1999.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an NPN, silicon, general purpose transistor for medium-power applications requiring high frequency switching. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for encapsulated devices.

1.2 Package outline. The device package outline for this specification sheet is a TO-8 in accordance with figure 1 for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Types	P_T (1) T_A = +25°C	P_T (2) T_C = +25°C	V_{CBO}	V_{CEO}	V_{EBO}	I_C	T_{STG}	T_J
	W	W	V dc	V dc	V dc	A dc	°C	°C
2N1483	1.75	25	60	40	12	3.0	–65 to +200	+200
2N1484	1.75	25	100	55	12	3.0	–65 to +200	+200
2N1485	1.75	25	60	40	12	3.0	–65 to +200	+200
2N1486	1.75	25	100	55	12	3.0	–65 to +200	+200

(1) Derate linearly 0.010 W/°C for T_A > +25°C.
(2) Derate linearly 0.143 W/°C for T_C > +25°C.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A
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FSC 5961

1.4 Primary electrical characteristics. Unless otherwise specified, T_C = +25ºC.

Limits	h_{FE} (1) V_{CE} = 4.0 V dc I_C = 750 mA dc		V_{BE} (1) V_{CE} = 4.0 V dc I_C = 750 mA dc	$V_{CE(SAT)}$ (1); I_C = 750 mA dc	
				I_B = 75 mA dc	I_B = 40 mA dc
	2N1483 2N1484	2N1485 2N1486		2N1483 2N1484	2N1485 2N1486
			V dc	V dc	V dc
Minimum	20	35			
Maximum	60	100	2.0	1.20	0.75

Limits	I_{CBO}		I_{EBO}	f_{hfb}
	V_{CB} = 30 V dc	V_{CB} = 50 V dc	V_{EB} = 12 V dc	V_{CB} = 28 V dc I_C = 5.0 mA dc
	2N1483 2N1485	2N1484 2N1486		
	µA dc	µA dc	µA dc	kHz
Minimum				600
Maximum	15	15	15	

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example, 6.5 for a list of available PINs, and 6.6 for supersession information.

1.5.1 JAN certification mark and quality level. The three quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: The base quality level "JAN" that uses no modifiers, "JANTX", and "JANTXV".

1.5.2 Type designation. The component designations for the medium power transistors covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "1483", "1484", "1485", and "1486".

1.5.3 Suffix symbols. Suffix symbols are not applicable for this specification sheet.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 – Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at https://quicksearch.dla.mil.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as specified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML-19500) before contract award (see 4.2 and 6.3).

3.3 Acronyms, symbols, and definitions. The acronyms, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

$$t_{off} - - - - - - - - - - t_s + t_f$$

3.4 Interface requirements and physical dimensions. The interface requirements and physical dimensions shall be as specified in MIL-PRF-19500 and herein. The device package styles shall be TO–8 in accordance with figure 1 for all device types.

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500, and herein. Unless otherwise specified (see 6.2), the lead finish shall be gold-plate. When a choice of lead formation is desired, it shall be specified in the acquisition document (see 6.2).

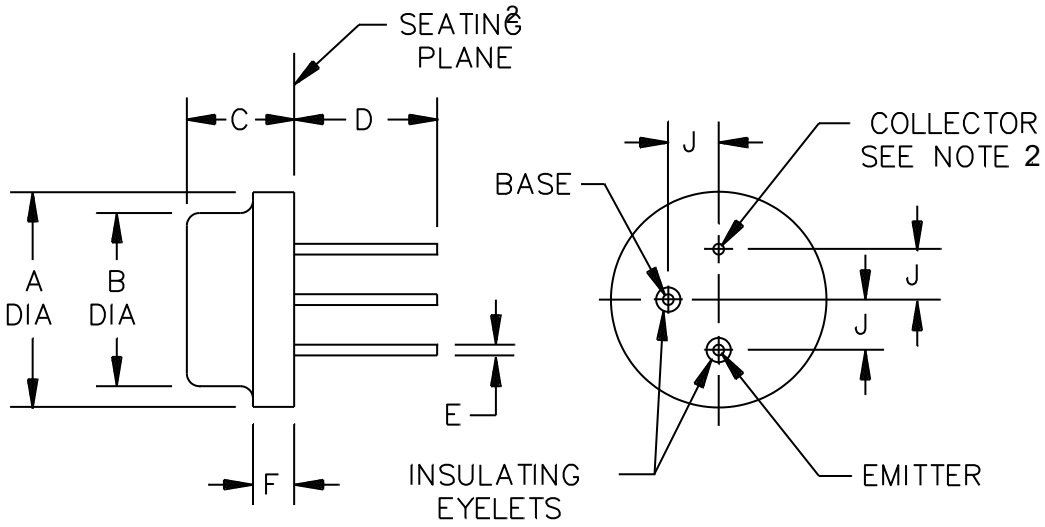
3.4.2 Pin-out. The pin-out of the device types shall be as shown on figure 1. The collector shall be electrically connected to the case.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics shall be as specified in 1.3, 1.4, and table I herein.

3.7 Workmanship. Transistors shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

*



LTR	Dimensions				Notes	LTR	Dimensions				Notes
	Inches		Millimeters				Inches		Millimeters		
	Min	Max	Min	Max			Min	Max	Min	Max	
A	.550	.650	13.97	16.51		E	.027	.033	0.69	0.84	3, 4
B	.444	.524	11.28	13.31		F		.115		2.92	
C	.270	.330	6.86	8.38		J	.136	.146	3.45	3.71	
D	.360	.440	9.14	11.18	3						

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. The collector shall be internally connected to the case.
3. All three leads.
4. Measured in the zone beyond .050 (1.27 mm) front the seating plane.

* FIGURE 1. Dimensions and configuration of TO-8 package.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANTX and JANTXV quality levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurement
	JANTX and JANTXV quality levels only
3c (1)	Thermal impedance, see 4.5.2
9	Not applicable
11	I_{CBO}, h_{FE1}
12	See 4.3.1
13	Subgroup 2 of table I herein. ΔI_{CBO} = ±100 percent of initial value or ±3 µA dc, whichever is greater. Δh_{FE1} = ±25 percent of initial value.

(1) This test shall be performed anytime after temperature cycling, screen 3a, and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions shall be as follows: V_{CE} = 32 V dc; power shall be applied to achieve T_J = +135°C minimum using a minimum P_D = 75 percent of P_T maximum, T_A ambient rated as defined in 1.3.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIB (JAN and JANTX) of MIL-PRF-19500 and herein. Delta requirements shall be in accordance with the applicable step of 4.6 herein.

Subgroup	Method	Conditions
B1	2026	Omit preconditioning.
B3	1026	V_{CE} = 32 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum P_D = 75 percent of P_T maximum, T_A ambient rated as defined in 1.3.
B6	1032	T_{stg} = +200ºC, t = 340 hours.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows herein. Delta measurements shall be in accordance with the applicable step of 4.6 herein.

Subgroup	Method	Conditions
C2	2036	Test condition A; weight = 10 lbs (4.54 Kg), t = 15s. Test condition D1; torque = 3 oz-in (2.12 N-cm), t = 15s.
C3	2006	10,000 G in each orientation X_1, Y_1, Y_2, Z_1.
C3	2016	Non-operating 500G, 1.0 msec, 5 blows in each orientation, X_1, Y_1, Y_2, Z_1.
C3	2056	Non-operating.
C6	1026	V_{CE} = 32 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum P_D = 75 percent of P_T maximum, T_A ambient rated as defined in 1.3.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-IX of MIL-PRF-19500 and as specified in table II herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with test method 3131 of MIL-STD-750 using the guidelines in that test method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). The thermal impedance limit used in screen 3c and table I, subgroup 2 herein shall be set statistically by the supplier. See subgroup 4 of table II (group E) herein.

4.6 Delta measurments. The delta measurements for groups B, C, and E shall be as specified below.

Step	Inspection (1) (2) (3) (4)	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1	Collector-base cutoff current 2N1483, 2N1485 2N1484, 2N1486	3036	Bias condition D, V_{CB} = 30 V dc V_{CB} = 50 V dc	ΔI_{CBO} (1)	100 percent of initial value or ±3 µA dc, whichever is greater.	
2	Forward current transfer ratio 2N1483, 2N1484 2N1485, 2N1486	3076	V_{CE} = 4.0 V dc; I_C = 750 mA dc; pulsed see 4.5.1	Δh_{FE} (1)	±25 percent change from initial reading.	

(1) Devices which exceed the group A limits for this test shall not be accepted.
(2) The delta electrical measurements for group B, product assurance levels JAN, JANTX, and JANTXV shall be as follows:
    a. In addition to the measurements specified for subgroup 3 of table E-VIB of MIL-PRF-19500, the measurements of all steps of this table shall also be taken.
    b. In addition to the measurements specified for subgroup 6 of table E-VIB of MIL-PRF-19500, the measurements of step 2 of this table shall also be taken.
(3) The delta electrical measurements for group C, all product assurance levels, shall be as follows:
    a. In addition to the measurements specified for subgroup 2 of table E-VII of MIL-PRF-19500, the measurements of step 1 of this table shall also be taken.
    b. In addition to the measurements specified for subgroup 3 of table E-VII of MIL-PRF-19500, the measurements of step 1 of this table shall also be taken.
    c. In addition to the measurements specified for subgroup 6 of table E-VII of MIL-PRF-19500, the measurements of steps 1 and of this table shall also be taken.
(4) The delta measurements for group E, all product assurance levels, shall be as follows: In addition to the measurements specified for subgroups 1 and 2 of table E–IX of MIL-PRF-19500, the measurements of all steps of this table shall also be taken.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance 2/	3131	See 4.5.2	$Z_{\theta JX}$		7.0	°C/W
Collector to emitter breakdown voltage	3011	Bias condition D, I_C = 100 mA dc, pulsed (see 4.5.1)	$V_{(BR)CEO}$			
2N1483, 2N1485				40		V dc
2N1484, 2N1486				55		V dc
Collector to base, breakdown voltage	3001	Bias condition D, I_C = 100 μA dc.	$V_{(BR)CBO}$			
2N1483, 2N1485				60		V dc
2N1484, 2N1486				100		V dc
Collector to emitter breakdown voltage	3011	Bias condition A, V_{EB} = 1.5 V dc, I_C = 0.25 m A dc	$V_{(BR)CEX}$			
2N1483, 2N1485					60	V dc
2N1484, 2N1486					100	V dc
Collector to emitter, cutoff current	3041	Bias condition A, V_{EB} = 1.5 V dc	I_{CEX}			
2N1483, 2N1485		V_{CB} = 60 V dc			.25	mA
2N1484, 2N1486		V_{CB} = 100 V dc			.25	mA
Collector to base, cutoff current	3036	Bias condition D.	I_{CBO1}			
2N1483, 2N1485		V_{CB} = 30 V dc			15	μA dc
2N1484, 2N1486		V_{CB} = 50 V dc			15	μA dc
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = 12 V dc	I_{EBO}		15	μA dc
Forward-current transfer ratio	3076	V_{CE} = 4.0 V dc, I_C = 750 mA dc; pulsed (see 4.5.1).	h_{FE1}			
2N1483, 2N1484				20	60	
2N1485, 2N1486				35	100	

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - continued						
Collector to emitter voltage (saturated)	3071	I_C = 750 mA dc; pulsed (see 4.5.1).	$V_{CE(sat)}$			
2N1483, 2N1484		I_B = 75 mA dc			1.20	V dc
2N1485, 2N1486		I_B = 40 mA dc			0.75	V dc
Base to emitter voltage (nonsaturated)	3066	Test condition B; V_{CE} = 4.0 V dc I_C = 750 mA dc; pulsed (see 4.5.1).	V_{BE}		2.0	V dc
Collector to base, cutoff current	3036	Bias condition D.	I_{CBO3}			
2N1483, 2N1485		V_{CB} = 60 V dc			100	µA dc
2N1484, 2N1486		V_{CB} = 100 V dc			100	µA dc
Subgroup 3						
High temperature operation:		T_A = +175°C				
Collector to base cutoff current	3036	Bias condition D	I_{CBO2}			
2N1483, 2N1485		V_{CB} = 30 V dc			1.0	mA dc
2N1484, 2N1486		V_{CB} = 50 V dc			1.0	mA dc
Low temperature operation:		T_A = –55°C				
Forward-current transfer ratio	3076	V_{CE} = 4.0 V dc; I_C = 750 mA dc; pulsed (see 4.5.1)	h_{FE2}			
2N1483, 2N1484				10		
2N1485, 2N1486				17		
Subgroup 4						
Small-signal, short-circuit, forward-current transfer ratio cutoff frequency	3301	V_{CB} = 28 V dc, I_C = 5.0 mA dc	f_{hfb}	600		kHz
Open circuit output capacitance	3236	V_{CB} = 10 V dc; I_E = 0 100 kHz ≤ f ≤ 1 MHz	C_{obo}		400	pF
Pulse response	3251	Test condition A; V_{CC} = +12 V dc, R_C = 15.9 ohms I_{B0} = I_{B2} = 35 mA dc; I_{B1} = 65 mA dc	$t_{on} + t_{off}$		25	µsec

See footnotes at end of table.

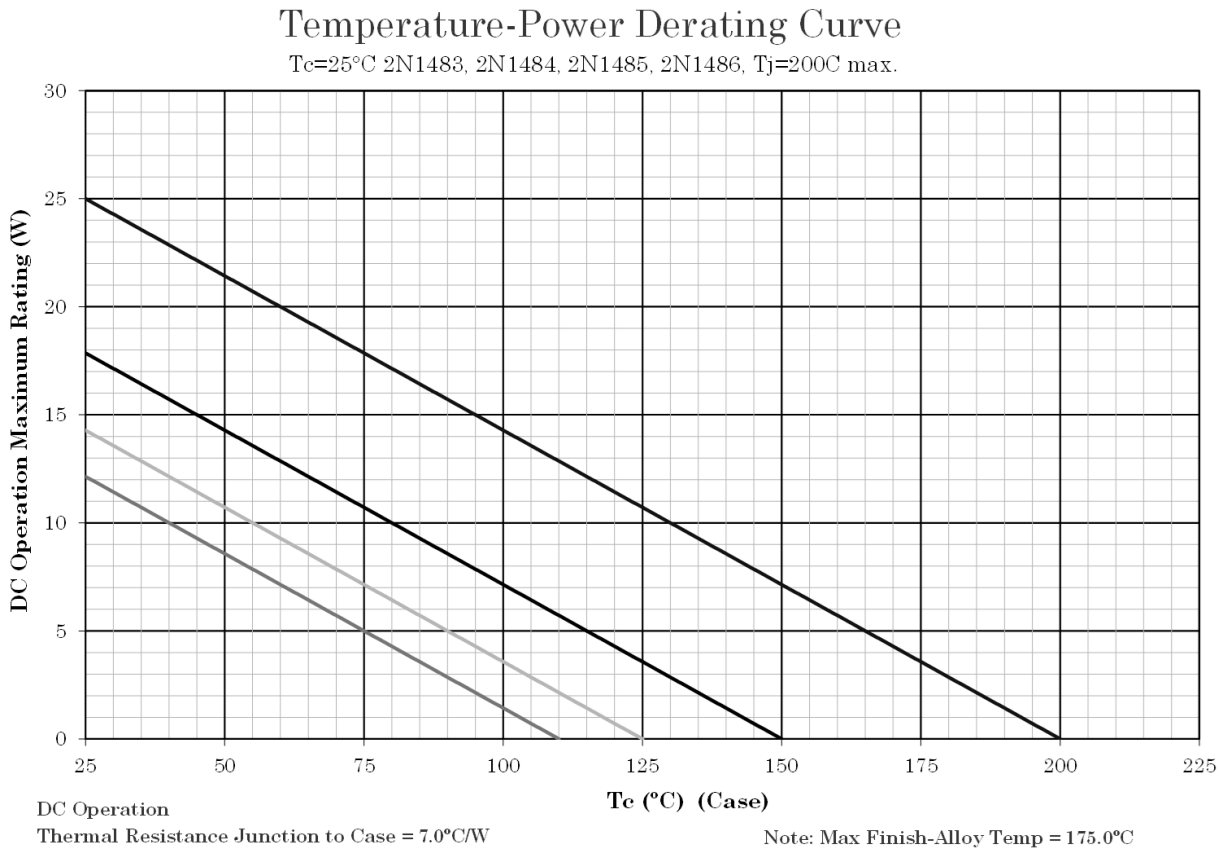
TABLE I. Group A inspection – Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroups 5, 6 and 7 Not applicable						

1/ For sampling plan, see MIL-PRF-19500.
2/ This test required for the following end-point measurements only:
Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group E inspection (all quality levels) - for qualification and requalification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal Fine leak Gross leak	1071		
End-point electrical measurements		See table I, subgroup 2 and 4.6 herein.	
Subgroup 2			45 devices c = 0
Intermittent operation life	1037		
End-point electrical measurements		See table I, subgroup 2 and 4.6 herein.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at less than or equal to T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 2. Temperature-power derating graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.) The notes specified in MIL-PRF-19500 are applicable to this specification.

6.1 Intended use. Transistors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

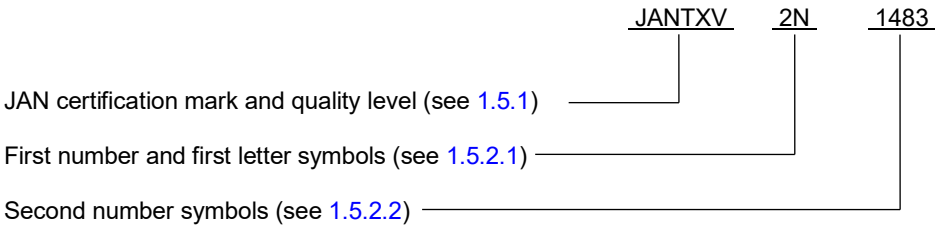
b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



6.5 List of PINs. The following is a list of possible PINs available for devices covered by this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level
JAN2N1483	JANTX2N1483	JANTXV2N1483
JAN2N1484	JANTX2N1484	JANTXV2N1484
JAN2N1485	JANTX2N1485	JANTXV2N1485
JAN2N1486	JANTX2N1486	JANTXV2N1486

6.6 Supersession information and superseded PINs. The non-TX types covered herein are interchangeable with the corresponding type covered by the superseded MIL-S-19500/180C(EL).

6.6.1 Lead finish. The original issue of this specification through MIL-S-19500/180C (12 December 1966) did not specify a lead finish. MIL-S-19500/180D (9 October 1967) specified that the lead finish as "gold plated". MIL-S-19500/180D with Amendment 1 (20 August 1973) modified the lead finish from "gold " to "gold or tin-plated". Tin is no longer acceptable as a lead finish.

6.6.2 Lead material. Because of the performance format of this document, a lead material is no longer specified.

6.7 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

* 6.8 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
Army - CR
* Navy - SH
Air Force - 85
* NASA - NA
DLA - CC

Review activities:
Army - AR, AV, MI, SM
* Navy - AS, CG, MC, OS
* Air Force - 19, 70

Preparing activity:
DLA - CC

(Project 5961-2021-088)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.