

The documentation and process conversion measures necessary to comply with this revision shall be completed by: 25 November 2024.

INCH-POUND

MIL-PRF-19500/168L
w/AMENDMENT 1
25 June 2024
SUPERSEDING
MIL-PRF-19500/168L
18 March 2019

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, THYRISTORS (CONTROLLED RECTIFIERS), SILICON,
TYPES 2N1771A, 2N1772A, 2N1774A, 2N1776A, 2N1777A, 2N1778A, AND 2N2619A,
QUALITY LEVELS JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP, silicon power, reverse-blocking triode thyristors. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for each device type as specified in [MIL-PRF-19500](#).

1.2 Package outline. The device package outline is a case mounted stud (TO-208AB, similar to TO-64) in accordance with [figure 1](#).

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^{\circ}\text{C}$.

Limits	I_o (1)	I_{TSM} (2)	V_{GM}	T_J	T_{STG}	dv/dt (4) (repetitive)
	<u>A</u>	<u>A</u>	<u>V(pk)</u>	<u>$^{\circ}\text{C}$</u>	<u>$^{\circ}\text{C}$</u>	<u>$\text{V}/\mu\text{s}$</u>
Min			(3)	-65	-65	5
Max	4.7	60	(3)	+150	+150	

- (1) This average forward current is for a maximum case temperature of $+105^{\circ}\text{C}$, and 180 electrical degrees of conduction.
- (2) Surge rating is non-recurrent and applies only with device in the "on" conducting state. The peak rate of surge current must not exceed 40 amperes/microsecond during the first 10 μs after switching from the "off" (blocking) state to the "on" (conducting) state. This time is measured from the point where the thyristor voltage has decayed to 90 percent of its initial blocking value.
- (3) Maximum peak positive gate voltage ($+V_{GM}$) = 10 V. Maximum peak negative gate voltage ($-V_{GM}$) = 5 V.
- (4) $T_C = -65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

AMSC N/A

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1.4 Primary electrical characteristics.

1.4.1 Common to all types.

Limits	V _{TM}	I _H	V _{GT} (1)	I _{GT} (1)	t _{off} (1)	t _{on}
	<u>V</u>	<u>mA dc</u>	<u>V dc</u>	<u>mA dc</u>	<u>μs</u>	<u>μs</u>
Min			0.2			
Max	1.85	25	2.0	30	30	5

(1) T_C = -65° to +150°C.

1.4.2 Individual ratings.

Types	V _{RRM} (1)	V _{DRM}
	<u>V(pk)</u>	<u>V(pk)</u>
2N1771A	50	50
2N1772A	100	100
2N1774A	200	200
2N1776A	300	300
2N1777A	400	400
2N1778A	500	500
2N2619A	600	600

(1) Values apply for zero or negative gate voltage (V_{GM}).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.4](#) for PIN construction example and [6.5](#) for a list of available PINs.

1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX" and "JANTXV".

1.5.2 Device type. The designation system for the devices covered by this specification sheet is as follows.

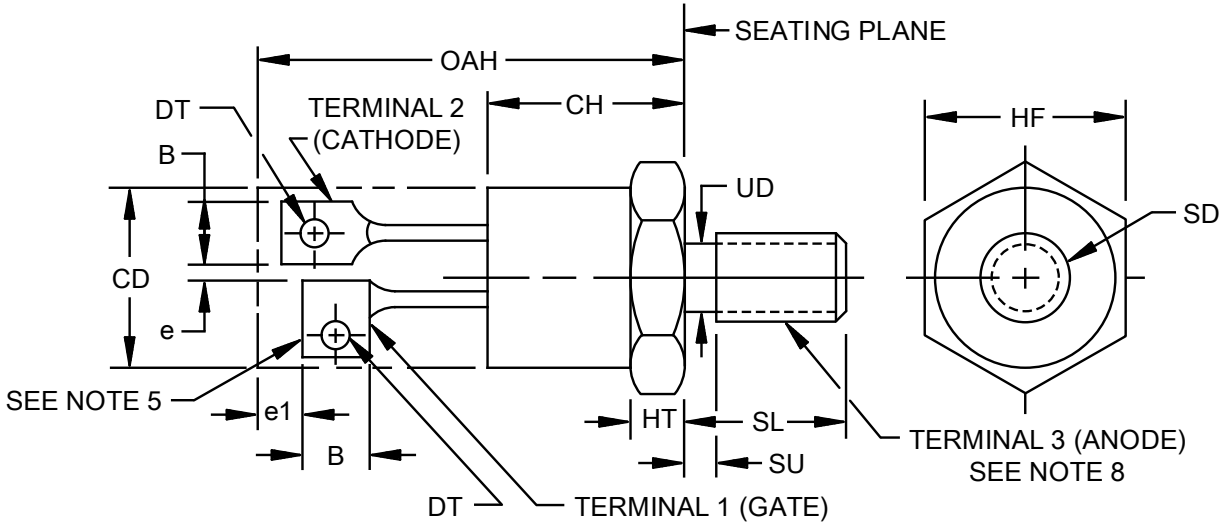
1.5.2.1 First number and first letter symbols. The devices of this specification sheet use the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the devices covered by this specification sheet are as follows: "1771", "1772", "1774", "1776", "1777", "1778" and "2619".

1.5.3 Suffix symbols. The "A" suffix symbol indicates a modified version of the non-suffix device.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

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Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
B	.080	.136	2.03	3.45	2
CD		.424		10.8	3
CH	.300	.400	7.62	10.2	
DT	.040	.075	1.02	1.9	
e	.013		0.33		4
e1	.060		1.52		5
HF	.424	.437	10.8	11.1	
HT	.060	.175	1.52	4.45	7
OAH	.700	.855	17.8	21.72	3
SD	.1658	.1697	4.21	4.310	8
SL	.400	.453	10.2	11.51	
SU		.078		1.98	
UD	.163	.189	4.14	4.80	

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Contour and angular orientation of terminals 1 and 2, with respect to hex portion and to each other, are optional.
3. Device contour, except on hex head and noted terminal dimensions, is optional within zone defined by dimensions CD and OAH.
4. Minimum spacing between terminals.
5. Square or radius on end of terminal is optional.
6. Minimum difference in terminal lengths to establish datum line for numbering terminals.
7. Chamfer, or undercut, on one or both ends of the hexagonal portion are optional.
8. Pitch diameter of threads is 10-32 NF-2A (coated). See FED-STD-H28, "Screw-Thread Standards for Federal Services".

FIGURE 1. Physical dimensions for TO-208AB package (similar to TO-64).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 – Test Methods For Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

V_{AA} Anode power supply voltage (dc).
V_{GG} Gate supply voltage.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Lead material. Where a choice of lead material is desired, it shall be specified in the acquisition document (see 6.2).

3.4.3 Construction. These devices shall be constructed in a manner and using materials which enable the thyristors to meet the applicable requirements of MIL-PRF-19500 and this document.

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3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.7 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#) herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [tables I, II, and III](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not require the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (Quality levels JANTX and JANTXV). Screening shall be in accordance with table E-IV of [MIL-PRF-19500](#), and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen	Measurements for JANTX and JANTXV levels
3a	Method 1051 of MIL-STD-750 , condition F, 10 cycles.
10	Not required.
11	I_{RRM1} , I_{DRM1} , V_{GT1} , V_{TM} .
12	Method 1040 of MIL-STD-750 , condition A, $T_C = +145^{\circ}\text{C}$ minimum, $R_{GK} \geq 1\text{K}\Omega$; V_{RRM} , $V_{DRM} = \text{rated}$ (see 1.4.2).
13	Subgroup 2 of table I herein, $\Delta I_{RRM1} = 100$ percent of initial value or $+1.0$ mA (pk), whichever is greater. $\Delta I_{DRM1} = 100$ percent of initial value or $+1.0$ mA (pk), whichever is greater.

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4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of table I, subgroups 1 and 2 inspection only (table E-VIB, group B, subgroup 1 of MIL-PRF-19500 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JANTX and JANTXV) of MIL-PRF-19500 and as follows. End-point electrical measurements shall be in accordance with the applicable steps of table II herein. Subgroups 3 and 6 of table E-VIB of MIL-PRF-19500, shall be performed on a sample from the subplot containing the highest voltage rated devices in the lot.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition F, 15 cycles.
B2	4066	Condition A; $I_{TSM} = 60 \text{ A(pk)}$ (0.5 sine wave); 10 surges 1 per minute; $I_O = 4.7 \text{ A}$ at rated V_{RRM} ; $T_C = +65^\circ\text{C}$; $f = 60 \text{ Hz}$; surge duration = 7 ms, minimum.
B3	1026	$T_C = +118^\circ\text{C}, \pm 5^\circ\text{C}$, 50 minutes "on", $I_O = 1.25 \text{ A}$, T_C uncontrolled, 10 minutes "off".
B5		Not applicable.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500. End-point electrical measurements shall be in accordance with the applicable steps of table II herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition A, weight 10 pounds (4.54 kg), application time = 15 seconds.
C3		Not applicable.
C6	1026	$T_C = +118^\circ\text{C}, \pm 5^\circ\text{C}$, 50 min "on", $I_O = 1.25 \text{ A}$, T_C uncontrolled, 10 minutes "off".

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of MIL-PRF-19500, and table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

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TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Reverse blocking current	4211	AC method, bias condition D; f = 60 Hz; V_{RRM} = rated (see 1.4.2)	I_{RRM1}		1	mA (pk)
Forward blocking current	4206	AC method, bias condition D; f = 60 Hz, V_{DRM} = rated (see 1.4.2)	I_{DRM1}		1	mA (pk)
Gate trigger voltage and current	4221	$V_2 = V_D = 6$ V dc; $T_C = +25^\circ\text{C}$ $R_g = 20\ \Omega$ maximum	V_{GT1} I_{GT1}		2 15	V dc mA dc
2N1771A, 2N1772A 2N1774A, 2N1776A 2N1777A, 2N1778A 2N2619A		$R_L = 50\ \Omega$ $R_L = 50\ \Omega$ $R_L = 50\ \Omega$ $R_L = 50\ \Omega$				
Forward "on" voltage	4226	$I_{TM} = 14.8$ A (pk) (pulse); pulse width = 8.5 ms maximum; duty cycle = 2 percent maximum	V_{TM}		1.85	V (pk)
Holding current	4201	Bias condition D; $R_2 = 50\ \Omega$ $V_{AA} = 24$ V dc maximum; $I_{F1} = 1$ A dc; $I_{F2} = 100$ mA dc; trigger voltage source = 6 V dc; trigger PW = 25 μs (minimum)	I_H		25	mA dc
Reverse gate current	4219	$V_G = 10$ V dc	I_G		250	mA dc
<u>Subgroup 3</u>						
High temperature operation:		$T_C = +145^\circ\text{C}$ minimum				
Reverse blocking current	4211	AC method, bias condition D; f = 60 Hz; V_{RRM} = rated (see 1.4.2)	I_{RRM2}		2	mA (pk)
Forward blocking current	4206	AC method, bias condition D; f = 60 Hz; V_{DRM} = rated (see 1.4.2)	I_{DRM2}		2	mA (pk)

See footnote at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - Continued						
Gate trigger voltage and current 2N1771A, 2N1772A 2N1774A, 2N1776A 2N1777A, 2N1778A 2N2619A	4221	V ₂ = rated V _{DM} (see 1.4.2); T _C = + 125°C minimum; R _e = 20 Ω maximum R _L = 140 Ω R _L = 650 Ω	V _{GT2}	0.2		V dc
Low temperature operation:		T _C = -65°C maximum				
Reverse blocking current	4211	AC method, bias condition D; f = 60 Hz; V _{RRM} = rated (see 1.4.2)	I _{RRM3}		1	mA (pk)
Forward blocking current	4206	AC method, bias condition D; f = 60 Hz; V _{DRM} = rated (see 1.4.2)	I _{DRM3}		1	mA (pk)
Gate trigger voltage and current 2N1771A, 2N1772A 2N1774A, 2N1776A 2N1777A, 2N1778A 2N2619A	4221	V ₂ = V _D = 6 V dc; R _e = 20 Ω maximum R _L = 140 Ω R _L = 650 Ω R _L = 650 Ω R _L = 650 Ω	V _{GT3} I _{GT2}		2 30	V dc mA dc
<u>Subgroups 4, 5, and 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Exponential rate of voltage rise	4231	Bias condition D; T _C = +145°C; dv/dt = 5 V/μs; C = 10 μF; 50 Ω ≤ R _L ≤ 400 Ω; minimum repetition rate = 60 pps; test duration = 15 s				
2N1771A		V _{AA} = 50 V dc	V _D	47		V dc
2N1772A		V _{AA} = 100 V dc	V _D	95		V dc
2N1774A		V _{AA} = 200 V dc	V _D	190		V dc
2N1776A		V _{AA} = 300 V dc	V _D	285		V dc
2N1777A		V _{AA} = 400 V dc	V _D	380		V dc
2N1778A		V _{AA} = 500 V dc	V _D	475		V dc
2N2619A		V _{AA} = 600 V dc	V _D	570		V dc

See footnote at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 7</u> – Continued						
Circuit commutated turn-off time	4224	$T_C = +145^{\circ}\text{C}$ minimum; $I_{TM} = 5\text{ A}$ pk; $t_{on} = 100\text{ }\mu\text{s}$; $di/dt = 5\text{ A}/\mu\text{s}$ minimum; reverse voltage at $t_1 = 2\text{ V}$ minimum; repetition rate = 1 Hz ; $dv/dt = 5\text{ V}/\mu\text{s}$; gate bias conditions: gate source voltage = 0 V , gate source resistance = $100\text{ }\Omega$	t_{off}			
2N1771A		$V_{DM} = V_{DRM} = 50\text{ V(pk)}$; $V_{DRM} = 50\text{ V}$ maximum			30	μs
2N1772A		$V_{DM} = V_{DRM} = 100\text{ V(pk)}$; $V_{DRM} = 100\text{ V}$ maximum			30	μs
2N1774A		$V_{DM} = V_{DRM} = 200\text{ V(pk)}$; $V_{DRM} = 200\text{ V}$ maximum			30	μs
2N1776A		$V_{DM} = V_{DRM} = 300\text{ V(pk)}$; $V_{DRM} = 300\text{ V}$ maximum			30	μs
2N1777A		$V_{DM} = V_{DRM} = 400\text{ V(pk)}$; $V_{DRM} = 400\text{ V}$ maximum			30	μs
2N1778A		$V_{DM} = V_{DRM} = 500\text{ V(pk)}$; $V_{DRM} = 500\text{ V}$ maximum			30	μs
2N2619A		$V_{DM} = V_{DRM} = 600\text{ V(pk)}$; $V_{DRM} = 600\text{ V}$ maximum			30	μs
Gate controlled turn-on time	4223	$I_{TM} = 5\text{ A}$ dc; $V_{GG} = 10\text{ V}$ dc; $R_e = 50\text{ }\Omega$; $t_{P1} = 15 \pm 5\text{ }\mu\text{s}$; $2\text{ A}/\mu\text{s} \leq di/dt \leq 200\text{ A}/\mu\text{s}$	t_{on}		5	μs
2N1771A		$V_{AA} = V_{DRM} = 50\text{ V(pk)}$				
2N1772A		$V_{AA} = V_{DRM} = 100\text{ V(pk)}$				
2N1774A		$V_{AA} = V_{DRM} = 200\text{ V(pk)}$				
2N1776A		$V_{AA} = V_{DRM} = 300\text{ V(pk)}$				
2N1777A		$V_{AA} = V_{DRM} = 400\text{ V(pk)}$				
2N1778A		$V_{AA} = V_{DRM} = 500\text{ V(pk)}$				
2N2619A		$V_{AA} = V_{DRM} = 600\text{ V(pk)}$				

1/ For sampling plan, see [MIL-PRF-19500](#).

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TABLE II. Groups A, B, and C end-point electrical measurements. 1/ 2/

Step	Inspection	MIL-STD-750		Symbol	Limit	Limit	Unit
		Method	Conditions		Min	Max	
1.	Reverse blocking cutoff current	4211	AC method, bias condition D; f = 60 Hz; V_{RRM} = rated (see 1.4.2)	I_{RRM1}		1	mA (pk)
2.	Forward blocking current	4206	AC method, bias condition D; f = 60 Hz; V_{DRM} = rated (see 1.4.2)	I_{DRM1}		1	mA (pk)
3.	Reverse blocking cutoff current	4211	AC method, bias condition D; T_C = +125°C minimum; f = 60 Hz; V_{RRM} = rated (see 1.4.2)	I_{RRM2}		2	mA (pk)
4.	Forward blocking current	4206	AC method; bias condition D; T_C = +125°C minimum; f = 60 Hz; V_{DRM} = rated (see 1.4.2)	I_{DRM2}		2	mA (pk)
5.	Gate trigger voltage and current	4221	$V_2 = V_D = 6$ V dc; $R_L = 50$ Ω ; $R_e = 20$ Ω maximum	V_{GT1} I_{GT1}		2 15	V dc mA dc
6.	Forward "on" voltage transfer ratio	4226	$I_{TM} = 14.8$ A(pk) (pulse); pulse width = 8.5 ms maximum; duty cycle = 2 percent maximum	V_{TM}		1.85	V (pk)

1/ The end-point electrical measurements taken during group B inspection for quality levels JAN, JANTX and JANTXV (table E-VIB of MIL-PRF-19500) shall be as follows: In addition to the measurements specified for subgroups 2, 3 and 6, the measurements of steps 1, 2, 3, 4, 5 and 6 of this table shall also be taken.

2/ The end-point electrical measurements taken during group C inspection for all quality levels (table E-VII of MIL-PRF-19500) shall be as follows: In addition to the measurements specified for subgroups 2, 3, and 6, the measurements of steps 1, 2, 3, 4, 5 and 6 of this table shall also be taken.

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TABLE III. Group E inspection (all quality levels) for qualification and requalification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			n = 45, c = 0
Temperature cycling or Thermal shock	1051	500 cycles, -65°C to +150°C.	
Hermetic seal	1056	100 cycles, test condition B.	
Electrical measurement	1071	Gross leak only.	
		See table I , subgroup 2.	
<u>Subgroup 2</u>			
Intermittent operating life	1037	Test current $I_O \geq 4.7$ A, half sine wave or dc equivalent; $T_{ON} \geq 1$ minute; 6,000 cycles.	
Electrical measurements		See table I , subgroup 2.	
<u>Subgroups 4, 5, 6, 7, 8, and 9</u>			
Not applicable			

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

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6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

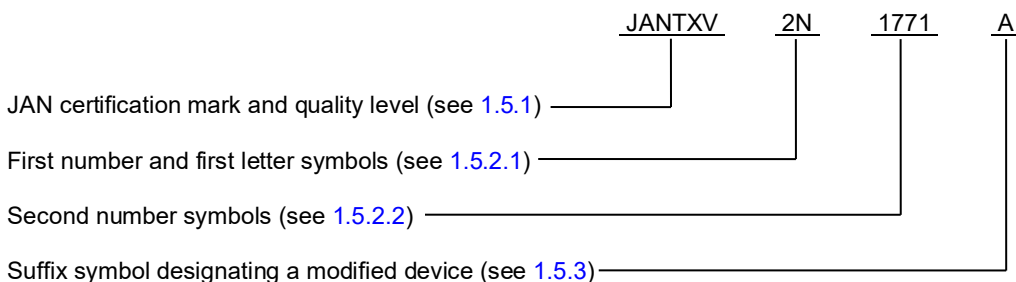
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish and material (see [3.4.1](#) and [3.4.2](#)).
- d. The complete PIN, see [1.5](#) and [6.4](#).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 PIN construction example. The PINs are constructed using the following form.



6.5 List of PINs.

Quality level JAN	Quality level JANTX	Quality level JANTXV
JAN2N1771A	JANTX2N1771A	JANTXV2N1771A
JAN2N1772A	JANTX2N1772A	JANTXV2N1772A
JAN2N1774A	JANTX2N1774A	JANTXV2N1774A
JAN2N1776A	JANTX2N1776A	JANTXV2N1776A
JAN2N1777A	JANTX2N1777A	JANTXV2N1777A
JAN2N1778A	JANTX2N1778A	JANTXV2N1778A
JAN2N2619A	JANTX2N2619A	JANTXV2N2619A

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6.6 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil.

6.7 Amendment notations. The margins of this specification are marked with vertical lines to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army – CR
Navy – SH
Air Force – 85
NASA – NA
DLA – CC

Preparing activity:
DLA – CC

(Project 5961–2024–039)

Review activities:

Army – AV, MI
Air Force – 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.