

The documentation and process conversion measures necessary to comply with this revision shall be completed by 15 May 2024.

INCH-POUND

MIL-PRF-19500/102C
w/AMENDMENT 1
15 February 2024
SUPERSEDING
MIL-PRF-19500/102C
12 January 2020

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, NPN, SILICON, HIGH-POWER
TYPES 2N1016, QUALITY LEVEL JAN

Inactive for new design after 7 June 1999.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a high-power, NPN, silicon transistor. One level of product assurance (JAN) is provided for each device type.

1.2 Physical dimensions. See [figure 1](#).

1.3 Maximum ratings. Unless otherwise specified $T_A = +25^\circ\text{C}$.

Types	P_T $T_C = +45^\circ\text{C}$ (1)	$R_{\theta JC}$	V_{CBO}	V_{EBO}	V_{CEO}	I_C	T_J and T_{STG}
	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>$^\circ\text{C}$</u>
2N1016B	150	0.7	100	25	100	7.5	65 to +150
2N1016C	150	0.7	150	25	150	7.5	
2N1016D	150	0.7	200	25	200	7.5	
2N1016B-2	150	0.7	100	20	100	7.5	
2N1016C-2	150	0.7	150	20	150	7.5	
2N1016D-2	150	0.7	200	20	200	7.5	

(1) Derate linearly 1.428 W/ $^\circ\text{C}$ for $T_C > +45^\circ\text{C}$. For temperature-power derating curves, see [figure 2](#).

1.4 Primary electrical characteristics. Unless otherwise specified $T_A = +25^\circ\text{C}$.

Limits	h_{FE} at $V_{CE} = 4.0$ V dc				$V_{CE(sat)}$ $I_C = 5$ A dc $I_B = 1$ A dc
	h_{FE1} $I_C = 2.0$ A dc	h_{FE2} $I_C = 5.0$ A dc	h_{fe} $I_C = 5$ A dc	f_{hfe} $I_C = 5$ A dc	
Min	20	10	5	<u>kHz</u>	<u>V dc</u>
Max	80	60		20	2.5

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AMSC N/A

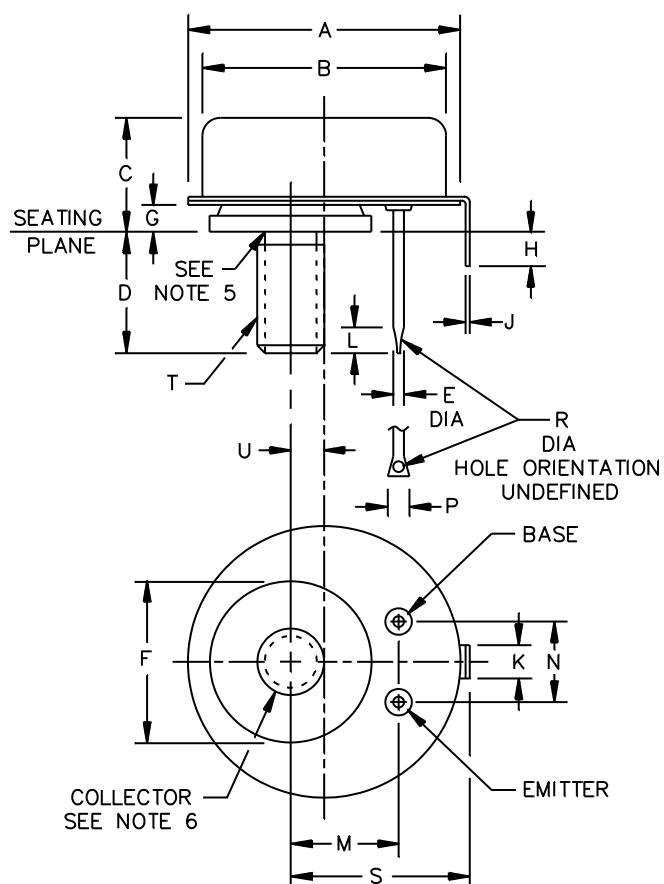
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FSC 5961



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Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	1.24	1.28	31.5	32.51	
B		1.130		28.7	
C	.50	.56	12.70	14.22	
D	.55	.58	13.97	14.73	
E	.045	.055	1.14	1.40	4
F	.73	.80	18.54	20.32	
G	.07	.14	1.78	3.56	
H	.13	.19	3.30	4.83	
J	.014	.024	0.36	0.61	
K	.14	.17	3.56	4.32	
L	.10	.14	2.54	3.56	
M	.48	.52	12.19	13.21	
N	.35	.40	8.89	10.16	
P	.09	.11	2.29	2.79	4
R	.050	.060	1.27	1.52	3
S	.81	.85	20.57	21.59	
T					2
U	.14	.17	3.56	4.32	



NOTES:

1. Dimension are in inches. Millimeters are given for general information only.
2. The ASME thread reference is 5/16-24 UNF-2A.
3. Diameter of hole or slot out either side of terminal.
4. Two terminals. Terminal diameter uncontrolled above the seating plane.
5. Reference point for temperature measurement.
6. The collector shall be internally connected to the mounting base.

* FIGURE 1. Physical dimensions for TO-82 package.

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1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.4](#) for PIN construction example and [6.5](#) for a list of available PINs.

1.5.1 JAN certification mark and quality level. The only quality level designator for encapsulated devices that is applicable for this specification sheet is the base quality level "JAN" that uses no modifiers.

1.5.2 Device type. The designation system for the devices covered by this specification sheet is as follows.

1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are "1016".

* 1.5.3 Suffix symbols. The suffix letters "B", "C" and "D" are incorporated in the PIN for this specification sheet to indicate an electrically modified version of the base type. The suffix symbol "-2" indicates a lower V_{EBO} maximum rating from the base type.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections [3](#) and [4](#) of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections [3](#) and [4](#) of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on [figure 1](#) herein.

3.4.1 Lead finish. Lead finish shall be solderable as defined in [MIL-PRF-19500](#). Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.6 Electrical test requirements. The electrical test requirements shall be the subgroups specified in [table I](#) herein.

3.7 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Conformance inspection (see [4.3](#) and [table I](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#) and as specified herein.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , t_{MD} (and V_H where appropriate). See [table II](#), group E, subgroup 4 herein.

4.3 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#), and as specified herein.

4.3.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#), and [table I](#) herein.

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4.3.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN) of [MIL-PRF-19500](#), and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1027	$V_{CB} = 30 \text{ V dc}$, $I_C = 2.39 \text{ A dc}$.

4.3.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#), and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition A; weight = 5 pounds ± 1 ounce (2.26 kg ± 28.3 g), application time = 15 s Test condition D2; torque = 40 inch-pound (4.5 N-m); application time = 15 s. Test condition D1; torque = 5 inch-ounce (0.035 N-m); application time = 15 s; tubulated leads only.
C5	3151	$R_{\theta JC}$ (see 1.3).
C6	1026	1,000 hours, $V_{CB} = 30 \text{ V dc}$, power and ambient temperature shall be applied to the device to achieve $T_J = +150^\circ\text{C}$ minimum, and minimum power dissipation of 75 percent of max rated P_T (see 1.3 herein); $n = 45$, $c = 0$. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

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TABLE I. Group A inspection.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2</u> /	3131	See 4.2.3	$Z_{\theta JX}$			°C/W
Breakdown voltage, collector to emitter 2N1016B 2N1016C 2N1016D	3011	Bias condition D, $I_C = 200$ mA dc	$V_{(BR)CEO}$	100 150 200		V dc V dc V dc
Collector to emitter cutoff current 2N1016B 2N1016C 2N1016D	3041	Bias condition A, $V_{EB} = -1.5$ V dc $V_{CE} = 100$ V dc $V_{CE} = 150$ V dc $V_{CE} = 200$ V dc	I_{CEX1}		1.0 1.0 1.0	mA dc mA dc mA dc
Collector to base cutoff current 2N1016B 2N1016C 2N1016D	3036	Bias condition D, $V_{EB} = 1.5$ V dc $V_{CB} = 100$ V dc $V_{CB} = 150$ V dc $V_{CB} = 200$ V dc	I_{CBO}		1.0 1.0 1.0	mA dc mA dc mA dc
Emitter to base cutoff current 2N1016B, 2N1016C, 2N1016D	3061	Bias condition D $V_{EB} = 25$ V dc	I_{EBO1}		1.0	mA dc
* 2N1016B-2, 2N1016C-2, 2N1016D-2		$V_{EB} = 20$ V dc			1.0	mA dc
Collector to emitter voltage (saturated)	3071	$I_C = 5$ A dc, $I_B = 1$ A dc	$V_{CE(sat)1}$		2.5	V dc
Base emitter voltage (saturated)	3066	Test condition A, $I_C = 5$ A dc, $I_B = 1$ A dc	$V_{BE(sat)1}$		4.0	V dc
Forward-current transfer ratio	3076	$V_{CE} = 4$ V dc, $I_C = 2$ A dc	h_{FE1}	20	80	
* Forward-current transfer ratio	3076	$V_{CE} = 4$ V dc, $I_C = 5$ A dc	h_{FE2}	10	60	
* Forward-current transfer ratio	3076	$V_{CE} = 4$ V dc, $I_C = 7.5$ A dc	h_{FE3}	6	45	

See footnote at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> – continued						
* Small-signal short- circuit forward-current transfer ratio	3206	$V_{CE} = 4 \text{ V dc}$, $I_C = 5 \text{ A dc}$ $f = 1 \text{ kHz}$	h_{fe}	5		
Small-signal short- circuit forward-current transfer ratio cutoff frequency	3301	$V_{CE} = 4 \text{ V dc}$, $I_C = 5 \text{ A dc}$	f_{hfe}	20		kHz
<u>Subgroup 3</u>						
High temperature operation		$T_C = +150^\circ\text{C}$				
Emitter to base cutoff current	3061	Bias condition D	I_{EBO2}			
* 2N1016B, 2N1016C, 2N1016D		$V_{EB} = 25 \text{ V dc}$			10	mA dc
* 2N1016B-2, 2N1016C-2, 2N1016D-2		$V_{EB} = 20 \text{ V dc}$			10	mA dc
Collector to emitter cutoff current	3041	Bias condition A, $V_{EB} = -1.5 \text{ V dc}$	I_{CEX2}			
2N1016B		$V_{CE} = 100 \text{ V dc}$			10	mA dc
2N1016C		$V_{CE} = 150 \text{ V dc}$			10	mA dc
2N1016D		$V_{CE} = 200 \text{ V dc}$			10	mA dc
Low-temperature operation		$T_C = -55^\circ\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = 4 \text{ V dc}$, $I_C = 5 \text{ A dc}$	h_{FE4}	10	35	
<u>Subgroup 4</u>						
Pulse response		See figure 3 . $I_C = 5 \text{ A dc}$, $V_{EB} = 6 \text{ V dc}$, $V_{CE} = 12 \text{ V dc}$; I_{B1} and $I_{B2} = 1.5 \text{ A dc}$	$t_d + t_r$		10	μs
Pulse response		See figure 3 . $I_C = 5 \text{ A dc}$, $V_{EB} = 6 \text{ V dc}$, $V_{CE} = 12 \text{ V dc}$; I_{B1} and $I_{B2} = 1.5 \text{ A dc}$	$t_s + t_f$		15	μs
<u>Subgroups 5, 6, and 7</u>						
Not applicable						

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:
Group B, subgroups 2 and 3 (JAN).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

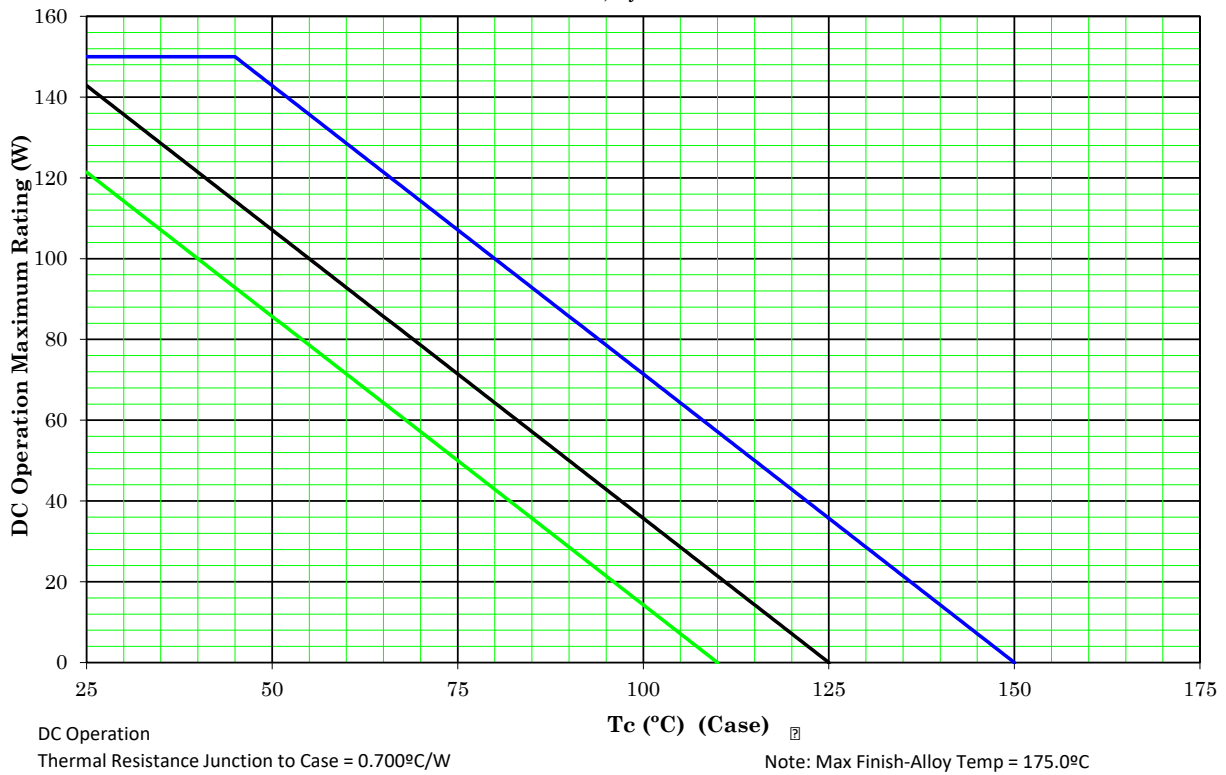
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TABLE II. Group E inspection (all quality levels) - for qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices, c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal	1071	Fine and gross leak	
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 2</u>			45 devices, c = 0
Blocking life	1048	T _A = +125°C, t = 1,000 hours +65, -0 hours; V _{CB} = 80 percent of rated voltage.	
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 4</u>			Sample size, N/A
Thermal impedance curves	3131	See MIL-PRF-19500 , table E-IX, group E, subgroup 4.	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 8</u>			45 devices, c = 0
Reverse stability	1033	Condition B.	

Temperature-Power Derating Curve

$T_c=25^{\circ}\text{C}$ 2N1016, $T_j=150^{\circ}\text{C}$ max.



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_j \leq +150^{\circ}\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curves chosen at $T_j \leq +125^{\circ}\text{C}$, and $+110^{\circ}\text{C}$ to show power rating where most users want to limit T_j in their application.

FIGURE 2. Derating for all devices.

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5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

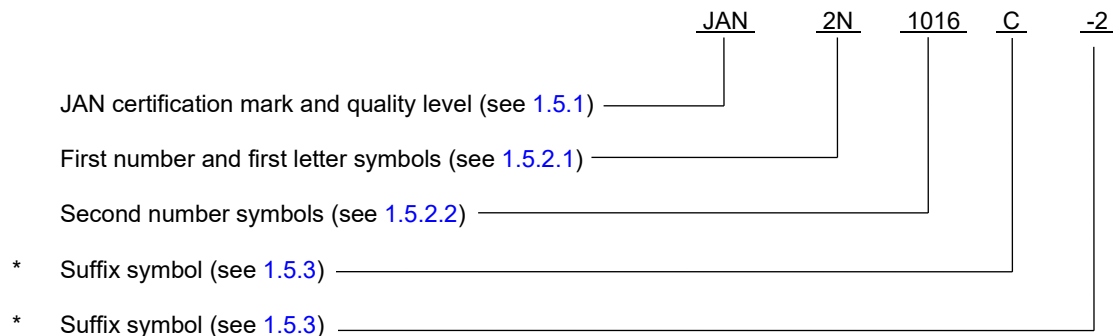
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.4.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 PIN construction example. The PINs for encapsulated devices and are constructed using the following forms.



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* 6.5 List of PINs. The following is a list of possible PINs available for encapsulated devices and covered by this specification sheet.

Quality level "JAN"	JAN2N1016B	JAN2N1016C	JAN2N1016D
	JAN2N1016B-2	JAN2N1016C-2	JAN2N1016D-2

* 6.6 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army – CR
Navy –SH
Air Force – 85
NASA – NA
DLA – CC

Preparing activity:

DLA – CC

(Project 5961-2024-011)

Review activities:

Army – AR, MI
Navy – AS, MC
Air Force – 19

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