

MILITARY SPECIFICATION

SEMICONDUCTOR DEVICE, TRANSISTORS, PN, SILICON UNJUNCTION

TYPES 2N489A THROUGH 2N494A, TX2N489A THROUGH TX2N494A,
2N2417A THROUGH 2N2422A, AND TX2N2417A THROUGH TX2N2422A

This specification is mandatory for use by all Depart-
ments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for silicon PN unijunction transistors. The prefix "TX" is used on devices submitted to and passing the special process-conditioning, testing, and screening as specified in 4.5 through 4.5.8.1. (see 6.5)

1.2 Physical dimensions. For types 2N489A through 2N494A, see figure 4.
For types 2N2417A through 2N2422A, see figure 6.

1.3 Maximum ratings.

P_T ^{1/} $T_A = 25^\circ C$		I_e	i_e ^{4/}	V_{B2E}	T_{stg}	T_J
2N489A through 2N494A	2N2417A through 2N2422A					
mW	mW	mA rms	A(pk)	Vdc	$^\circ C$	$^\circ C$
600 ^{2/}	350 ^{3/}	70	2	60	-65 to +175	+175

^{1/}Total interbase power dissipation must be limited by external circuitry (resistance in series with base two).

^{2/}Derate 4 mW/ $^\circ C$ for $T_A > 25^\circ C$.

^{3/}Derate 2.33 mW/ $^\circ C$ for $T_A > 25^\circ C$.

^{4/}This rating is for a capacitor discharge (into emitter) of 10 mfd or less with 30 Vdc or less on the capacitor.

TYPES	R_{BEO} (ohms)		η		$I_{B2(mod)}$ (mA dc)		$V_{EB1(sat)}$ (Vdc)	I_{EB20} (μ Adc)	V_{OB1} (Vpk)
	Min.	Max.	Min.	Max.	Min.	Max.	Max.	Max.	Min.
2N489A, 2N2417A	4700	6800	.51	.62	6.8	22	4.0	2	3
2N490A, 2N2418A	6200	9100	.51	.62	6.8	22	4.0	2	3
2N491A, 2N2419A	4700	6800	.56	.68	6.8	22	4.3	2	3
2N492A, 2N2420A	6200	9100	.56	.68	6.8	22	4.3	2	3
2N493A, 2N2421A	4700	6800	.62	.75	6.8	22	4.6	2	3
2N494A, 2N2422A	6200	9100	.62	.75	6.8	22	4.6	2	3

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of the specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-S-19500 - Semiconductor Devices, General Specification for.

STANDARDS

MILITARY

MIL-STD-202 - Test Methods for Electronic and Electrical Component Parts.

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 General. Requirements shall be in accordance with MIL-S-19500, and as specified herein.

3.2 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-S-19500, and as follows:

$I_{B2(mod)}$ - - - - Modulated interbase current. The resultant base-two (B2) current for specified values of emitter current and interbase voltage.

I_e - - - - - Emitter current, rms.

I_e - - - - - Instantaneous emitter current (capacitor discharge).

I_{EB20} - - - - Emitter reverse current (d. c.), base-one (B1) open-circuited.

I_p - - - - - Peak point emitter current. This is the minimum value emitter current for which the slope of the static emitter characteristic curve (see figure 1) is zero for a specified value of interbase voltage.

I_V - - - - - Valley point emitter current. This is the maximum value of emitter current for which the slope of the static emitter characteristic curve (see figure 1) is zero for a specified value of interbase supply voltage and base-two (B2) resistance.

η - - - - - (eta) Intrinsic standoff ratio. This is defined by the relationship.

$$\eta = \frac{V_p - V_D}{V_{B2B1}}$$

R_{B2} - - - - - Resistance in series with the base-two (B2) lead.

R_{BBO} - - - - Interbase resistance. The resistance measured between base-one (B1) and base-two (B2) with the emitter open circuited.

V_{BB} - - - - - Interbase power supply voltage (d. c.).

V_{B2B1} - - - - Interbase voltage, (d. c.) voltage from base-two (B2) to base-one (B1).

V_{B2E} - - - - - Voltage (d. c.) from base-two (B2) to emitter (E).

VEB1(sat) - Emitter saturation voltage. The resultant d. c. voltage measured between the emitter and base-one (B1) for specified values of emitter current and interbase voltage.

VOB1 - - - Base-one (B1) peak pulse voltage. The base-one (B1) peak pulse voltage is defined as shown in figure 2. This parameter is a relative indicator of the peak emitter current available for use in firing circuits.

Vp - - - - Peak point emitter voltage. The voltage from emitter to base-one (B1) when the peak point emitter current flows for a specified value of interbase voltage.

3.3 Symbol. The graphic symbol for the unijunction transistor shall be as shown in figure 3.

3.4 Design, construction, and physical dimensions. Transistors shall be of the design, construction, and physical dimensions shown on figures 4 and 6.

3.4.1 Lead arrangement shall be as follows (see figures 3, 4, and 6): Lead 1 - emitter (E); Lead 2 - base-one (B1); Lead 3 - omit; Lead 4 - base-two (B2).

3.4.2 Lead material and finish. Lead material and finish shall be gold-plated Kovar. (Leads may be tin-coated if specified in the contract or order, see 6.2.)

3.5 Performance characteristics. Performance characteristics shall be as specified in tables I, II, and III.

3.5.1 Process-conditioning, testing, and screening for "TX" types. Process-conditioning, testing, and screening for the "TX" types shall be as specified in 4.5.

3.6 Marking. The following marking specified in MIL-S-19500 may be omitted from the body of the transistor at the option of the manufacturer:

- (a) Country of origin.
- (b) Manufacturer's identification.

3.6.1 "TX" marking. Devices in accordance with the "TX" requirements shall include the additional marking "TX" preceding the type designation.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.2 Qualification inspection. Qualification inspection shall consist of the examinations and tests specified in tables I, II, and III.

4.2.1 Qualification testing. The non-TX types shall be used for qualification testing. (The "TX" types shall be procured from the sources listed in the QPL-19500 for the corresponding non-TX type.)

4.3 Quality conformance inspection. Quality conformance inspection shall consist of groups A and B inspections. When specified in the contract or order, one copy of the quality conformance inspection data, pertinent to the device inspection lot, shall be supplied with each shipment by the device manufacturer.

4.3.1 Group A inspection. Group A inspection shall consist of the examinations and tests specified in table I.

4.3.2 Group B inspection. Group B inspection shall consist of the examinations and tests specified in table II.

4.3.3 Group C inspection. Group C inspection shall consist of the examinations and tests specified in table III. This inspection shall be conducted on the initial lot and thereafter every 6 months during production.

4.3.4 Representative lot. A lot shall consist of transistors of only one family (2N489A through 2N494A or 2N2417A through 2N2422A). Group A shall be tested on a subplot basis. For subgroups 1 through 5 and subgroup 8 of group B, and group C, where a lot consists of more than one type, only one type need be tested as a representative of the lot for all types in the lot. For subgroups 6 and 7 of group B, the sample for each subgroup shall consist of all types within the lot in proportion to the distribution of the types within the lot.

4.4 Methods of examination and test. Methods of examination and test shall be as specified in tables I, II, and III.

4.5 Process-conditioning, testing, and screening for "TX" types. The procedure for process-conditioning, testing, and screening shall be in accordance with 4.5.1 through 4.5.8.1 and figure 13. Process-conditioning shall be conducted on 100 percent of the lot, prior to submission of the lot to the tests specified in tables I, II, and III. (At the option of the manufacturer, the non-TX type may be subjected to process-conditioning and testing).

4.5.1 Quality assurance (lot verification). Quality assurance shall keep lot records for three years minimum, monitor for compliance to the prescribed procedures, and observe that satisfactory manufacturing conditions and records on lots are maintained for these devices. The records shall be available for review by the customer at all times. The quality-assurance monitoring shall include, but not be limited to: process-conditioning, testing, and screening. (The conditioning and screening tests performed as standard production tests need not be repeated when these are acceptable to the Government beforehand as being equal to or more severe than the tests specified herein).

4.5.2 High-temperature storage. All devices shall be stored for at least 24 hours at a minimum temperature (T_A) of 200° C.

4.5.3 Thermal shock (temperature cycling). All devices shall be subjected to thermal shock (temperature cycling) in accordance with MIL-STD-750, method 1051, test condition C, except that 10 cycles shall be continuously performed and the time at the temperature extremes shall be 15 minutes, minimum.

4.5.4 Acceleration. All devices shall be subjected to acceleration test in accordance with MIL-STD-750, method 2008, with the following exceptions: The test shall be performed one time in the Y₁ orientation only, at a peak level of 20,000 G minimum. The one minute hold time requirement shall not apply.

4.5.5 Hermetic seal (fine-leak) test. All devices shall be fine-leak tested in accordance with MIL-STD-202, method 112, test condition C, procedure IIIa or IIIb (using the applicable condition of 4.5.5.1 or 4.5.5.2, except that the gross-leak test shall be as specified in 4.5.5.3).

4.5.5.1 Conditions for procedure IIIa. All devices shall be placed in a sealed chamber and pressurized to 50 psig minimum with helium gas for a minimum of 4 hours. The devices shall be removed from the chamber and within 30 minutes be subjected to a helium leak detection test. Devices that exhibit a leak rate of 5×10^{-7} cubic centimeters of helium per second when measured at a differential pressure of one atmosphere shall be rejected. All devices exhibiting this leakage rate or greater shall be removed from the lot.

4.5.5.2 Conditions for procedure IIIb. The devices shall be placed in a sealed chamber which shall be pressurized to 180 psig minimum with Krypton 85 tracer in a nitrogen solution for a minimum of 30 minutes. Within four hours after evacuation of the chamber, the device shall be tested with a counter capable of detecting leakage at the rate of 1×10^{-8} cc per second. All devices exhibiting this leakage rate or greater shall be removed from the lot.

4.5.5.3 Hermetic seal (gross-leak) test. All devices shall be tested for gross leaks by immersing in noncorrosive ethylene glycol at approximately 150° C for a minimum of 15 seconds and observed for bubbles. All devices that bubble shall be removed from the lot.

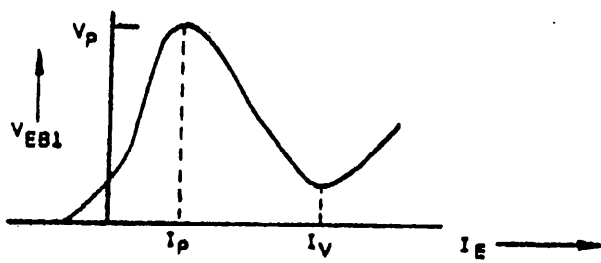


FIGURE 1. Unijunction transistor static emitter characteristic curve.

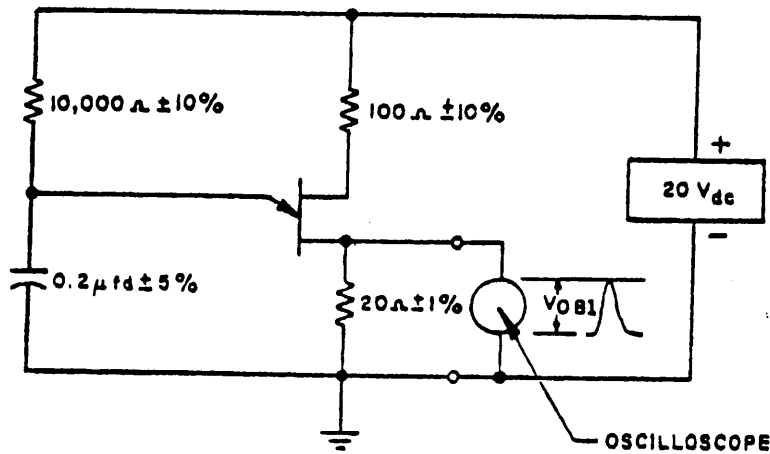


FIGURE 2. Base-one (B1) peak pulse voltage test circuit.

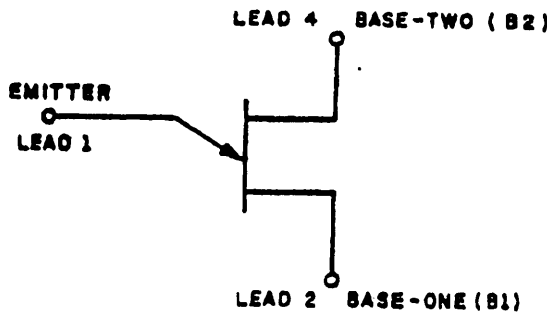
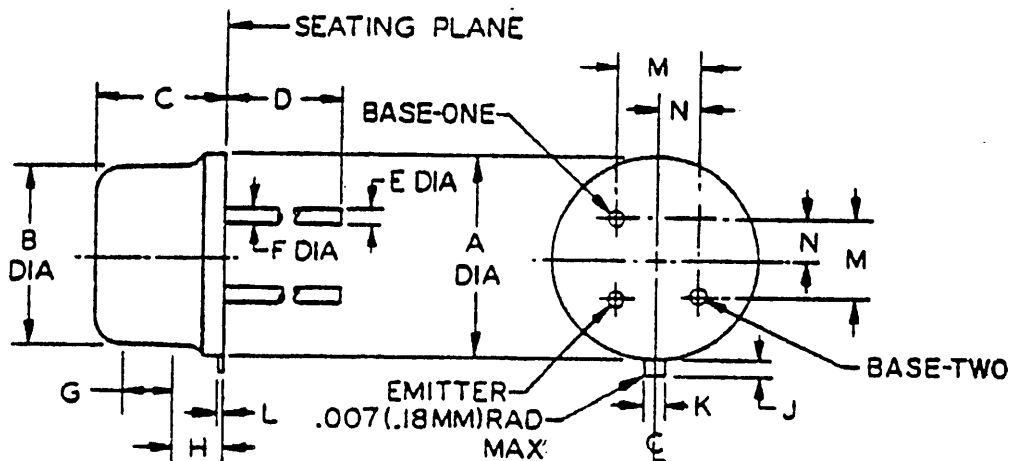


FIGURE 3. Graphic symbol for the unijunction transistor (see 3.4.1).

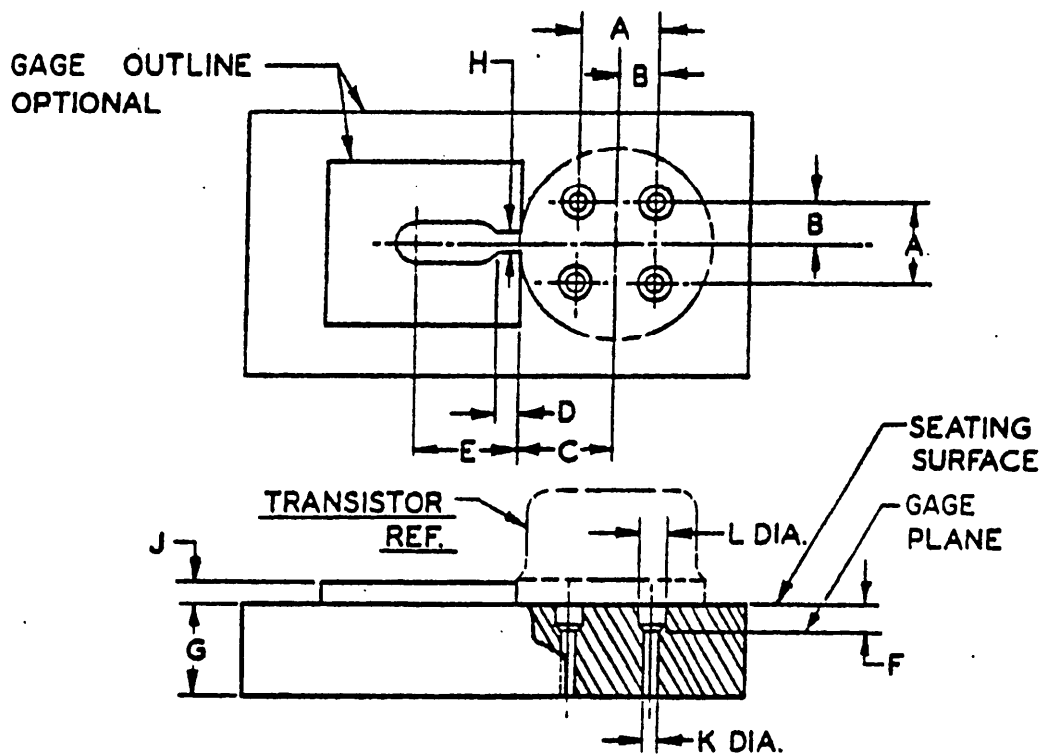


NOTES:

1. Metric equivalents (to the nearest .01 mm) are given for general information only and are based upon 1 inch = 25.4 mm.
2. Measured in the zone beyond .250 (6.35 mm) from the seating plane.
3. Measured in the zone .050 (1.27 mm) and .250 (6.35 mm) from the seating plane.
4. Variations on dim B in this zone shall not exceed .010 (.25 mm).
5. Outline in this zone is not controlled.
6. When measured in a gaging plane .054 $\pm$.001 (1.37 $\pm$.03 mm) below the seating plane of the transistor max dia leads shall be within .007 (.18 mm) of their true location. Smaller dia leads shall fall within the outline of the max dia lead tolerance. Fig. 5 preferred measured method.
7. All leads electrically isolated from case.
8. Measured from the maximum diameter of the actual device.
9. All three leads.

DIMENSIONS					NOTES
LTR	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	
A	.335	.370	8.51	9.40	
B	.305	.335	7.75	8.51	
C	.240	.260	6.10	6.60	
D	1.500	—	38.10	—	9
E	.016	.021	.41	.53	2,9
F	.016	.019	.41	.48	3,9
G	.100	—	2.54	—	4
H	—	—	—	—	5
J	.029	.045	.74	1.14	8
K	.028	.034	.71	.86	
L	.009	.125	.23	3.18	
M	.1414 Nom		3.59 Nom		6
N	.0707 Nom		1.80 Nom		6

FIGURE 4. Physical dimensions of transistor types (TX and non-TX) 2N489A thru 2N494A.

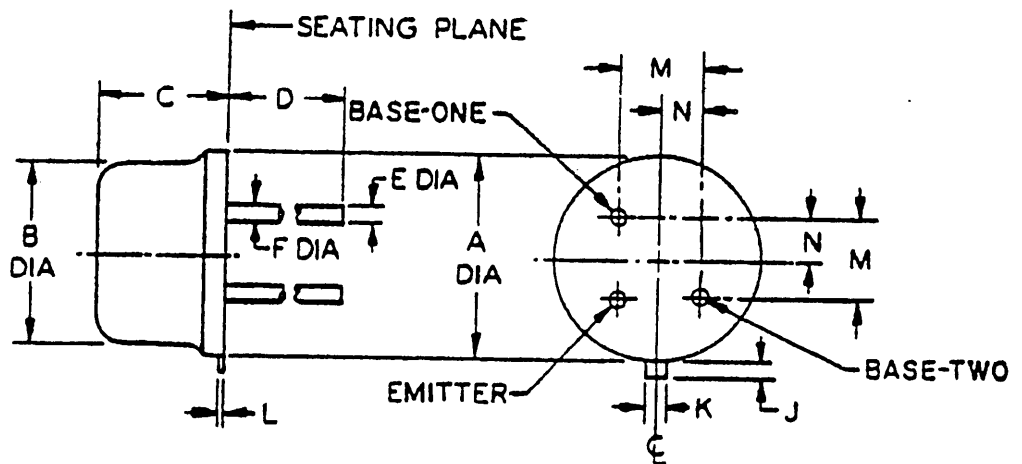


NOTES:

1. Metric equivalents (to the nearest .01 mm) are shown for general information only and are based upon 1 inch = 25.4 mm.
2. The following gaging procedure shall be used:
The use of a pin straightener prior to insertion in the gage is permissible. The device being measured shall be inserted until its seating plane is .125±.010 (3.18±.25 mm) from the seating surface of the gage. A spacer may be used to obtain the .125 (3.18 mm) distance from the gage seat prior to force application. A force of 8 oz ±.5 oz shall then be applied parallel and symmetrical to the device's cylindrical axis. When examined visually after the force application (the force need not be removed) the seating plane of the device shall be seated against the gage.
3. The location of the tab locator, within the limits of dimension C, will be determined by the tab and flange dimension of the device being checked.

DIMENSIONS				
LTR	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.1409	.1419	3.58	3.60
B	.0702	.0712	1.78	1.81
C	.182	.199	4.62	5.05
D	.009	.011	.23	.28
E	.125 Nom		3.18 Nom	
F	.054	.055	1.37	1.40
G	.372	.378	9.45	9.60
H	.0350	.0355	.89	.90
J	.150 Nom		3.81 Nom	
K	.0325	.0335	.83	.85
L	.0595	.0605	1.51	1.54

FIGURE 5. Gage for lead and tab location for transistor types (TX and non-TX) 2N489A thru 2N494A.

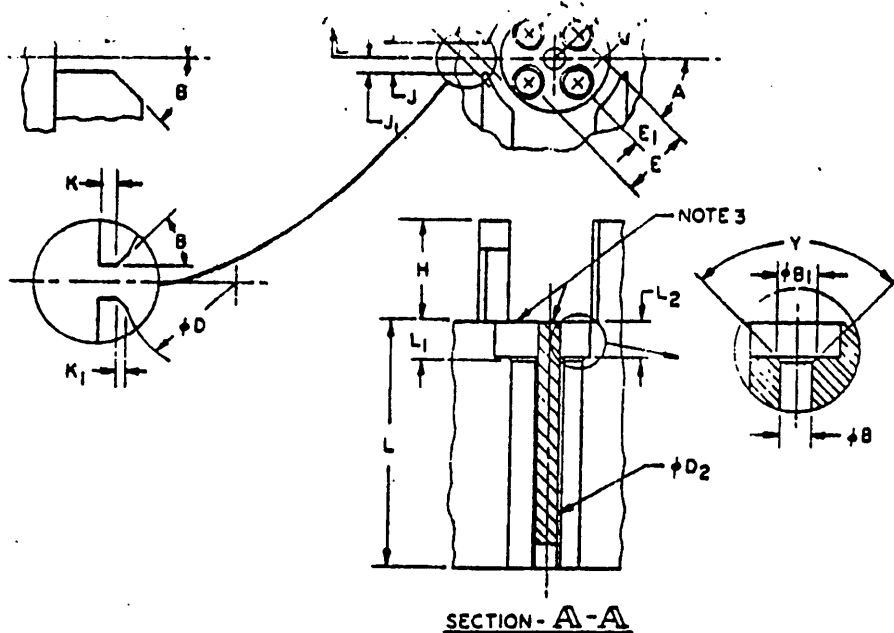


DIMENSIONS					NOTES
LTR	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	
A	.209	.230	5.31	5.84	
B	.178	.195	4.52	4.95	
C	.170	.210	4.32	5.33	
D	.500	—	12.70	—	7
E	—	.021	—	.53	2,7
F	.016	.019	.41	.48	3,7
J	.028	.048	.71	1.22	6
K	.036	.046	.91	1.17	
L	—	.020	—	.51	
M	.0707 Nom		1.80 Nom		4
N	.0354 Nom		.90 Nom		4

NOTES:

1. Metric equivalents (to the nearest .01 mm) are given for general information only and are based upon 1 inch = 25.4 mm.
2. Measured in the zone beyond .250 (6.35 mm) from the seating plane.
3. Measured in the zone .050 (1.27 mm) and .250 (6.35 mm) from the seating plane.
4. When measured in a gaging plane .054+.001 (1.37+.03 mm) below the seating plane of the transistor, max dia leads shall be within .007 (.18 mm) of their true location relative to a maximum width tab. Smaller dia leads shall fall within the outline of the max dia lead tolerance. Fig.7 preferred measured method.
5. All leads electrically isolated from case.
6. Measured from the maximum diameter of the actual device.
7. All 3 leads.

FIGURE 6. Physical dimensions of transistor types (TX and non-TX) 2N2417A thru 2N2422A.



Ltr	Dimensions in inches with metric equivalents (mm) in parentheses (see note 1)		Notes
	Minimum	Maximum	
ϕB	.0325 (.8255)	.0335 (.8509)	4
ϕB_1	.043 (1.09) Nom		4
ϕD	.2310 (5.867)	.2315 (5.880)	
ϕD_1	.159 (4.04)	.161 (4.09)	
ϕD_2	.040 (1.02) Nom		5
E	.0995 (2.527)	.1005 (2.553)	
E ₁	.0495 (1.257)	.0505 (1.283)	
H	.145 (3.68)	.155 (3.94)	
J	.0470 (1.194)	.0475 (1.207)	
J ₁	.0235 (.597)	.0245 (.622)	
K	.009 (.229)	.011 (.279)	
K ₁	.005 (.127) Nom		
L	.372 (9.45)	.378 (9.60)	
L ₁	.054 (1.37)	.055 (1.40)	
L ₂	.043 (1.09) Nom		
Q	.040 (1.02) Nom		
Q ₁	.123 (3.12)	.127 (3.23)	
A	44.90°	45.10°	
B	45° Nom		
Y	90° Nom		

NOTES:

1. Metric equivalents (to the nearest .01 mm) are given for general information only and are based upon 1 inch = 25.4 mm.
2. The following gaging procedure shall be used: The device being measured shall be inserted until its seating plane is .125 (3.18 mm) $\pm$.010 (.254 mm) from the seating surface of the gage. A force of 8 $\pm$ 5 oz. shall then be applied parallel and symmetrical to the device's cylindrical axis. When examined visually after the force application (the force need not be removed) the seating plane of the device shall be seated against the gage. The use of a pin straightener prior to insertion in the gage is permissible. A spacer may be used to obtain the .125 (3.18 mm) distance from the gage seat prior to force application.
3. These surfaces to be parallel and in same plane within $\pm$.001 (.025 mm).
4. Four holes.
5. Pressed in.

FIGURE 7. Gage for lead and tab location for transistor types (TX and non-TX) 2N2417A thru 2N2422A.

TABLE I. Group A inspection

Examination or test	MIL-STD-750		LTPD		Symbol	Limits		
	Method	Details	Non TX	TX		Min	Max	Unit
<u>Subgroup 1</u>			10	5				
Visual and mechanical examination	2071				---	---	---	---
<u>Subgroup 2</u>			5	2				
Intrinsic standoff ratio	See 4.7	$V_{B2B1} = 10 \text{ Vdc}$			η			
2N489A, 2N490A						0.51	0.62	---
2N2417A, 2N2418A						0.51	0.62	---
2N491A, 2N492A						0.56	0.68	---
2N2419A, 2N2420A						0.56	0.68	---
2N493A, 2N494A						0.62	0.75	---
2N2421A, 2N2422A						0.62	0.75	---
Interbase resistance	See 4.6	$V_{B2B1} = 3 \text{ Vdc}; I_E = 0$			R_{BBO}			
2N489A, 2N491A, 2N493A						4,700	6,800	ohms
2N2417A, 2N2418A, 2N2421A						4,700	6,800	ohms
2N490A, 2N492A, 2N494A						6,200	9,100	ohms
2N2418A, 2N2420A, 2N2422A						6,200	9,100	ohms
<u>Subgroup 3</u>			5	3				
Modulated interbase current	See 4.8	$V_{B2B1} = 10 \text{ Vdc}$ $I_E = 50 \text{ mAdc}$			$I_{B2}(\text{mod})$	6.8	22	mAdc
Emitter saturation voltage	See 4.8	$V_{B2B1} = 10 \text{ Vdc}$ $I_E = 50 \text{ mAdc}$			$V_{EB1}(\text{sat})$			
2N489A, 2N2417A						---	4.0	Vdc
2N490A, 2N2418A						---	4.0	Vdc
2N491A, 2N2419A						---	4.3	Vdc
2N492A, 2N2420A						---	4.3	Vdc
2N493A, 2N2421A						---	4.6	Vdc
2N494A, 2N2422A						---	4.6	Vdc
Emitter reverse current	3036 See 4.11	Bias cond. D; $V_{B2E} = 60 \text{ Vdc}; I_{B1} = 0$			I_{EB20}	---	-2.0	μAdc
<u>Subgroup 4</u>			10	5				
Valley point emitter current	See 4.10	$V_{BB} = 20 \text{ Vdc}$ $R_{B2} = 100 \text{ ohms}$			I_v	8	---	mAdc
Peak point emitter current	See 4.9	$V_{B2B1} = 25 \text{ Vdc}$			I_p	---	12	μAdc
Base-one peak pulse voltage	See fig. 2				V_{OB1}	3	---	V(pk)

TABLE I. Group A inspection - Continued

Examination or test	MIL-STD-750		LTPD		Symbol	Limits		
	Method	Details	Non TX	TX		Min	Max	Unit
<u>Subgroup 5</u>			10	5				
Low temperature operation:		$T_A = -65^\circ \text{C}$						
Interbase resistance	See 4.6	$V_{B2B1} = 3 \text{ Vdc}; I_E = 0$			RBBO			
2N489A, 2N491A, 2N493A						1,900	3,800	ohms
2N2417A, 2N2419A, 2N2421A						1,900	3,800	ohms
2N490A, 2N492A, 2N494A						2,500	4,800	ohms
2N2418A, 2N2420A, 2N2422A						2,500	4,800	ohms
Emitter reverse current	3036 See 4.11	Bias cond. D; $V_{B2E} = 50 \text{ Vdc}; I_{B1} = 0$			IEB20	---	-2	μAdc
High temperature operation:		$T_A = 150^\circ \text{C}$						
Interbase resistance	See 4.6	$V_{B2B1} = 3 \text{ Vdc}; I_E = 0$			RBBO			
2N489A, 2N491A, 2N493A						7,200	14,000	ohms
2N2417A, 2N2419A, 2N2421A						7,200	14,000	ohms
2N490A, 2N492A, 2N494A						10,800	18,000	ohms
2N2418A, 2N2420A, 2N2422A						10,800	18,000	ohms
Emitter reverse current	3036 See 4.11	Bias cond. D; $V_{B2E} = 10 \text{ Vdc}; I_{B1} = 0$			IEB20	---	-20	μAdc

TABLE II. Group B inspection

Examination or test	MIL-STD-750		LTPD		Symbol	Limits		
	Method	Details	Non TX	TX		Min	Max	Unit
<u>Subgroup 1</u>			20	20				
Physical dimensions	2086	See figures 4 and 6			---	---	---	---
<u>Subgroup 2</u>			15	15				
Solderability	2026				---	---	---	---
Thermal shock (temperature cycling)	1051	Test cond. C except high temp = $+175 \pm 5^\circ \text{C}$			---	---	---	---
Thermal shock (glass strain)	1056	Test cond. A			---	---	---	---
Moisture resistance	1021.				---	---	---	---
End points:								
Emitter reverse current	3036 See 4.11	Bias cond. D; $V_{B2E} = 30 \text{ Vdc}; I_{B1} = 0$			IEB20	---	-2.0	μAdc
Interbase resistance	See 4.6	$V_{B2B1} = 3 \text{ Vdc}; I_E = 0$			RBBO			
2N489A, 2N491A, 2N493A						4,200	7,500	ohms
2N2417A, 2N2419A, 2N2421A						4,200	7,500	ohms
2N490A, 2N492A, 2N494A						5,500	10,000	ohms
2N2418A, 2N2420A, 2N2422A						5,500	10,000	ohms

TABLE II. Group B inspection - Continued

Examination or test	MIL-STD-750		LTPD		Symbol	Limits		
	Method	Details	Non TX	TX		Min	Max	Unit
<u>Subgroup 2 - Continued</u>			15	15				
Intrinsic standoff ratio	See 4.7	VB2B1 = 10 Vdc			η			
2N489A, 2N490A						.48	.65	---
2N2417A, 2N2418A						.48	.65	---
2N491A, 2N492A						.53	.72	---
2N2419A, 2N2420A						.53	.72	---
2N493A, 2N494A						.59	.79	---
2N2421A, 2N2422A						.59	.79	---
<u>Subgroup 3</u>			15	15				
Shock	2016	Nonoperating; 1500 G for 0.5 msec; 5 blows in each orientation: X ₁ , Y ₁ , Y ₂ , and Z ₁ .			---	---	---	---
Vibration fatigue	2046	Nonoperating			---	---	---	---
Vibration, variable frequency	2056				---	---	---	---
Constant acceleration	2006	10,000 G; in each orientation: X ₁ , Y ₁ , Y ₂ , and Z ₁ .			---	---	---	---
End points: (Same as for subgroup 2)								
<u>Subgroup 4</u>			15	15				
Terminal strength (lead fatigue)	2036	Test cond. E			---	---	---	---
Seal (leak-rate)	---	Method 112 of MIL-STD-202, test cond. C, procedure III; test cond. A for gross leaks			---	---	5x10 ⁻⁷	atm cc/sec
<u>Subgroup 5</u>			15	15				
Salt atmosphere (corrosion)	1041				---	---	---	---
End points: (Same as for subgroup 2)								
<u>Subgroup 6</u>			$\lambda=15$	$\lambda=7$				
High-temperature life (nonoperating)	1031	T _{stg} = +175° C			---	---	---	---
End points:								
Emitter reverse current	3036 See 4.11	Bias cond. D; VB2E = 30 Vdc; IB1 = 0			IEB20	---	-4.0	μAdc

	Method	Details	Non TX	TX	Symbol	Min	Max	Unit
<u>Subgroup 6 - Continued</u>			$\lambda=15$	$\lambda=7$				
End points: Interbase resistance	See 4.6	$V_{B2B1} = 3 \text{ Vdc}; I_E = 0$			R_{BBO}			
2N489A, 2N491A, 2N493A						4,200	7,500	ohms
2N2417A, 2N2419A, 2N2421A						4,200	7,500	ohms
2N490A, 2N492A, 2N494A						5,500	10,000	ohms
2N2418A, 2N2420A, 2N2422A						5,500	10,000	ohms
Intrinsic standoff ratio	See 4.7	$V_{B2B1} = 10 \text{ Vdc}$			η			
2N489A, 2N490A						.48	.65	---
2N2417A, 2N2418A						.48	.65	---
2N491A, 2N492A						.53	.72	---
2N2419A, 2N2420A						.53	.72	---
2N493A, 2N494A						.59	.79	---
2N2421A, 2N2422A						.59	.79	---
<u>Subgroup 7</u>			$\lambda=10$	$\lambda=5$				
Steady state operation life	1028 See fig. 12	$T_A = 25^\circ \text{C}; I_E = 0$			---	---	---	---
2N489A through 2N494A		$1900 \Omega \leq R_{B2} \leq 16,750 \Omega$						
2N2417A through 2N2422A		$9500 \Omega \leq R_{B2} \leq 12,600 \Omega$						
All types		$V_{BB} = \text{per formula shown in figure 12}$						
End points: (Same as for subgroup 6)								
<u>Subgroup 8</u>			20	20				
Dew point	1066	$T_{\text{high}} = +25^\circ \text{C}$			---	---	---	---
Measurement during test: Emitter reverse current: 2N489A through 2N494A only	3036 See 4.11	Bias cond. D; $V_{B2E} = 30 \text{ Vdc}; I_{B1} = 0$			I_{EB20}	---	-2.0	μAdc

TABLE III. Group C inspection

Examination or test	MIL-STD-750		LTPD		Symbol	Limits		
	Method	Details	Non TX	TX		Min	Max	Unit
<u>Subgroup 1</u>			15	15				
Barometric pressure, reduced (altitude operation)	1001	Normal mounting; Pressure = 8±2 mm Hg for 60 sec min.			---	---	---	---
Measurement during test:								
Emitter reverse current	3036 See 4. 11	Bias cond. D; VB2E = 60 Vdc; IB1 = 0			IEB20	---	-2.0	μAdc

4.5.6 Pre burn-in tests. The parameters I_{EB20} , R_{BBO} , and η of table IV shall be measured and the data recorded for all devices in the lot. All devices shall be handled or identified such that the delta end points can be determined after the burn-in test. All devices which fail to meet these requirements shall be removed from the lot and the quantity removed shall be noted on the lot history.

TABLE IV. Burn-in test measurements

Examination or test	MTL-STD-750		Symbol	Limits		
	Method	Details		Min	Max	Unit
Emitter reverse current	3036 See 4.11	Bias cond. D; $V_{B2E} = 80 \text{ Vdc}$; $I_{B1} = 0$	I_{EB20}	---	-2.0	μAdc
Interbase resistance	See 4.6	$V_{B2B1} = 3 \text{ Vdc}$; $I_E = 0$	R_{BBO}			
2N489A, 2N491A, 2N493A				4,700	6,800	ohms
2N2417A, 2N2419A, 2N2421A				4,700	6,800	ohms
2N490A, 2N492A, 2N494A				6,200	9,100	ohms
2N2418A, 2N2420A, 2N2422A				6,200	9,100	ohms
Intrinsic standoff ratio	See 4.7	$V_{B2B1} = 10 \text{ Vdc}$	η			
2N489A, 2N490A				0.51	0.62	---
2N2417A, 2N2418A				0.51	0.62	---
2N491A, 2N492A				0.56	0.68	---
2N2419A, 2N2420A				0.56	0.68	---
2N493A, 2N494A				0.62	0.75	---
2N2421A, 2N2422A				0.62	0.75	---

4.5.7 Burn-in test. All devices shall be operated for 168 hours minimum under the following conditions:

$$T_A = 25 \pm 3^\circ \text{C}$$

$$V_{B2B1} = 10 \text{ Vdc}$$

$$I_E = 50 \text{ mAdc}$$

4.5.8 Postburn-in tests. The parameters I_{EB20} , R_{BBO} , and η of table IV shall be retested after burn-in and the data recorded for all devices in the lot. The parameters measured shall not have changed during the burn-in test from the initial value by more than the specified amount as follows:

$$\Delta I_{EB20} = 100 \text{ percent or } 50 \text{ nanoamperes, whichever is greater.}$$

$$\Delta R_{BBO} = \pm 20 \text{ percent.}$$

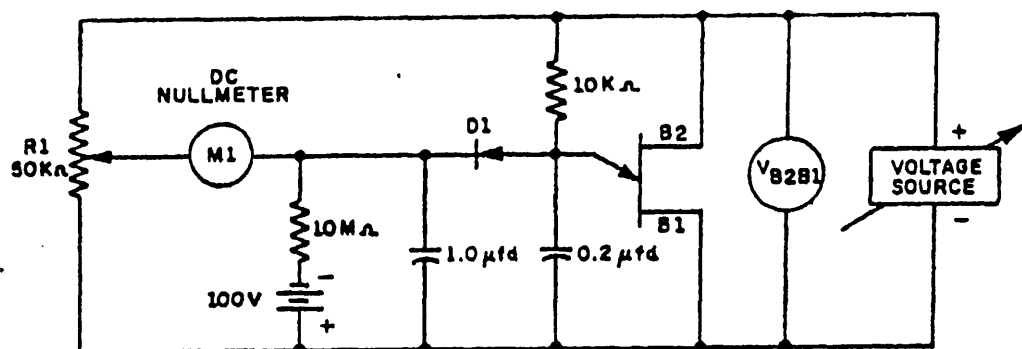
$$\Delta \eta = \pm 5 \text{ percent.}$$

4.5.8.1 Burn-in test failures (screening). All devices that exceed the delta (Δ) limits of 4.5.8 or the limits of table IV after burn-in, shall be removed from the inspection lot and the quantity removed shall be noted on the lot history. If the quantity removed after burn-in should exceed 10 percent of the total inspection lot on the burn-in tests, then the entire lot shall be unacceptable as the TX types.

4.6 Interbase resistance. The specified interbase voltage (see tables I and II) is applied and the corresponding resistance is measured for the emitter open circuited.

4.7 Intrinsic standoff ratio. Either of the two alternate methods below may be used at the option of the manufacturer.

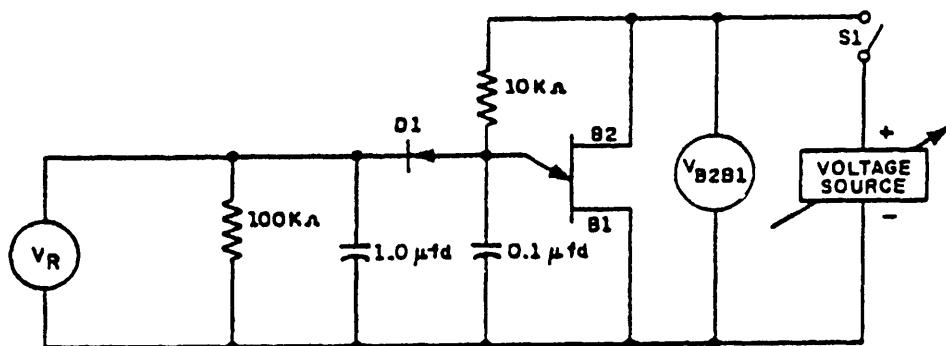
4.7.1 Method a. The circuit of figure 8a shall be used for this measurement. The specified interbase voltage (see tables I and II) shall be applied and the variable resistor shall be adjusted to obtain a null. η is then read directly from the calibration of the variable resistor. The equation $\eta = \frac{V_P - V_D}{V_{B2B1}}$ shall be used to calibrate the variable resistor.



NOTES:

1. R1 - Calibrated helipot (η).
2. Voltage source must have less than 10 mv ripple (peak to peak).
3. D1 - Silicon diode, forward voltage of $.672 \pm .010$ volts at forward current of .50 mA dc and a reverse leakage of less than 1μ A dc at 20 volts.

FIGURE 8a. Intrinsic standoff ratio test circuit. (Alternate A)



NOTES:

1. Voltage source must have less than 10 mv ripple (peak to peak) and be readily controllable to less than 10 mv.
2. D1 - Silicon diode, forward voltage of $.672 \pm .010$ volts at forward current of .50 mAdc and a reverse leakage of less than 1 μ Adc at 20 volts.

FIGURE 8b. Intrinsic standoff ratio test circuit. (Alternate B)

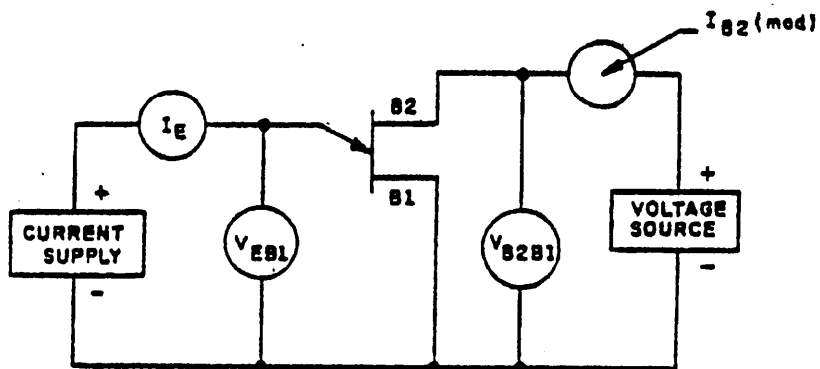
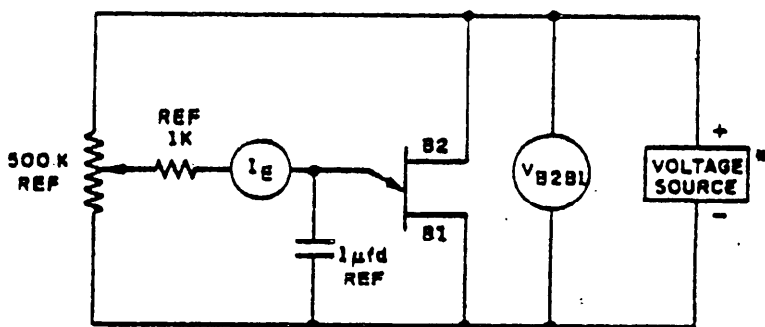


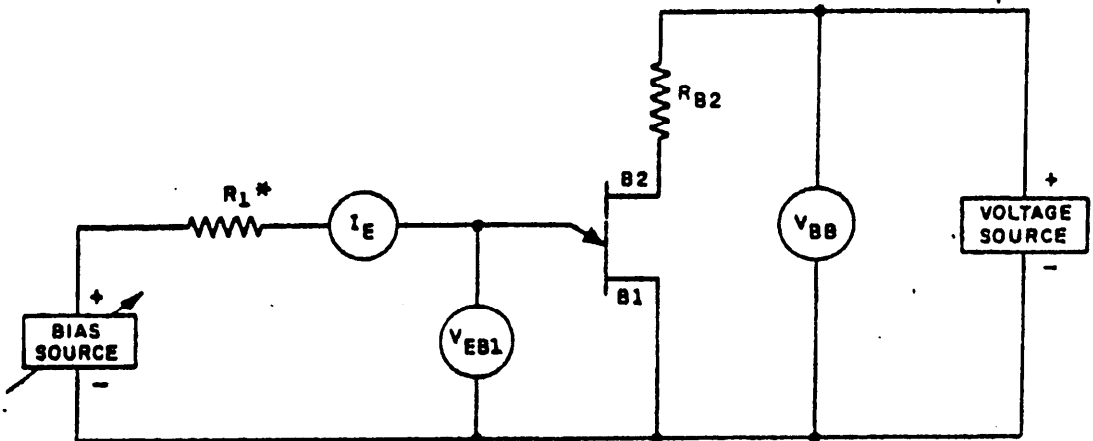
FIGURE 9. Modulated interbase current and emitter saturation voltage circuit.



NOTES:

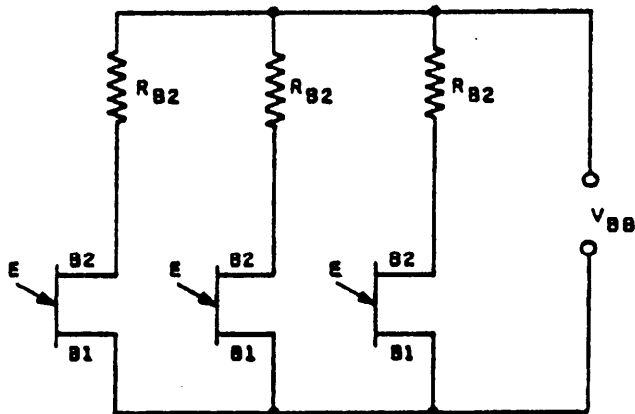
1. 500 K pot must be noiseless to prevent false triggering.
2. *Voltage source with less than 1 mv peak to peak ripple.

FIGURE 10. Peak point emitter current circuit.



* R_1 chosen to limit current to a safe value.

FIGURE 11. Valley point emitter current circuit.



Types 2N489A thru 2N494A

$$V_{BB} = \frac{12,333 + R_{B2}}{143.3}$$

R_{B2} must be between 1,900 and 16,750 ohms

Preferred value 12,333 ohms

Types 2N2417A thru 2N2422A

$$V_{BB} = \frac{12,000 + R_{B2}}{185}$$

R_{B2} must be between 9,500 and 12,600 ohms

Preferred value 12,000 ohms

R_{B2} shall be chosen by the manufacturer between the specified values. The V_{BB} to be used shall then be calculated. Extreme caution must be exercised to insure that excessive base to base transient voltages do not cause thermal runaway.

FIGURE 12. Life test circuit.

4.7.2 Method b. The circuit of figure 8b, or a suitable equivalent, shall be used for this measurement. Switch S is closed, applying the specified V_{B2B1} (see table I and II) and causing the unijunction to fire. The voltage across the 100 K ohm resistor, V_R , is measured and η ratio is computed as follows:

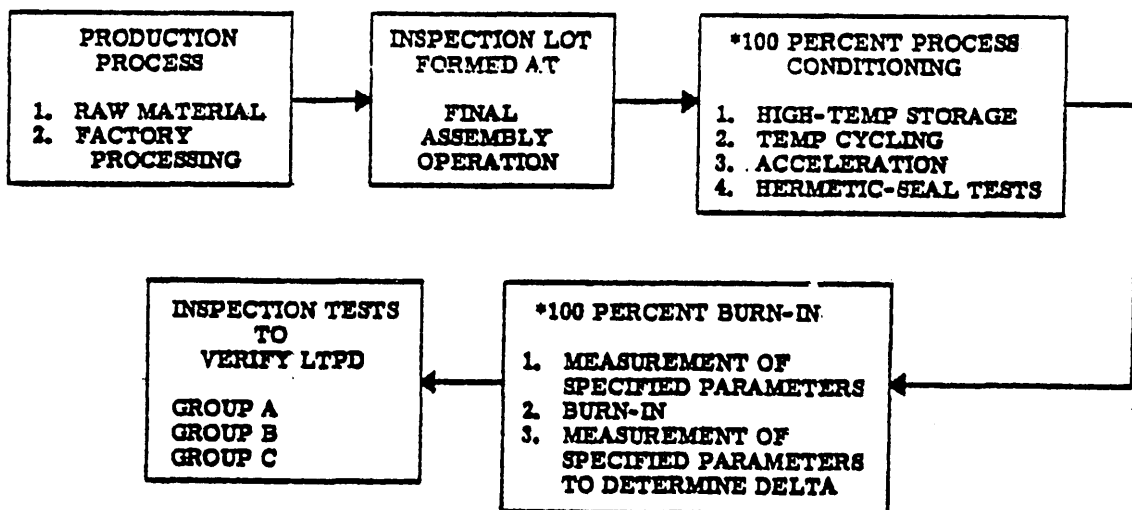
$$\eta = \frac{V_R}{V_{B2B1}} = \frac{V_P - V_D}{V_{B2B1}} \quad (V_D = 0.672 \text{ Vdc at } 0.5 \text{ mAdc and } T_A = 25^\circ \text{ C})$$

4.8 Modulated interbase current and emitter saturation voltage. The specified values (see table I) of interbase voltage and emitter current are applied. The base-two (B2) current is measured as the modulated interbase current. The emitter to base-one (B1) voltage is measured as the emitter saturation voltage. The test circuit of figure 9 may be used to measure these parameters.

4.9 Peak point emitter current. This parameter shall be measured in the circuit of figure 10 or a suitable equivalent. The variable resistor is adjusted to apply a low resistance between the emitter and base-one (B1). The specified V_{B2B1} (see table I) is applied and the resistance between the emitter and base-one (B1) is increased until the transistor fires as determined by oscillation of I_E . Peak point emitter current is the maximum value of I_E just prior to oscillation.

4.10 Valley point emitter current. For the specified interbase supply voltage (see table I) and base-two (B2) resistance the emitter current corresponding to the valley point operating condition is measured. The test circuit of figure 11, or suitable equivalent, shall be used for this measurement. The specified interbase supply voltage, V_{BB} , and base-two (B2) series resistance shall be applied. R_1 shall be of sufficient value to adequately control the emitter current. The bias voltage shall be gradually increased until the device fires and then shall be varied to obtain a minimum value of V_{EB1} . The I_E corresponding to this minimum value of V_{EB1} is the I_V of the device under test.

4.11 Emitter reverse current. This test shall be conducted in accordance with method 3036 of MIL-STD-750 except that the words and symbols, collector (C), base (B), and emitter (E) shall be replaced with base-two (B2), emitter (E), and base-one (B1), respectively.



*ORDER OF THE TESTS IN THE BLOCKS SHALL BE PERFORMED AS SHOWN

FIGURE 13. Order of procedure diagram for TX types.

5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery. See MIL-S-19500, section 5.

6. NOTES

6.1 Notes. The notes specified in MIL-S-19500 are applicable to this specification.

6.2 Ordering data.

- (a) Lead finish if other than gold-plated Kovar. (See 3.4.2).
- (b) Inspection data (See 4.3).

6.3 Qualified sources for "TX" types. Procurement for "TX" types will be as specified in 4.2.1.

6.4 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

6.5 Substitution criteria. Transistor types 2N489A through 2N494A specified herein are substitute devices (unilateral) for transistor types 2N489 through 2N494 respectively, previously covered by MIL-T-19500/75 (USAF).

Custodians:

Army - EL
Navy - SH
Air Force - 11

Preparing activity:

Air Force - 11

(Project 5961-0008-14)

Review activities:

Army - EL, MU, MI
Navy - SH
Air Force - 11, 17, 85

User activities:

Army - SM, EL, MI
Navy - AS, OS, CG, MC
Air Force -