

MIL-S-19500/425 (USAF)
23 Sept 1969

MILITARY SPECIFICATION

SEMICONDUCTOR DEVICE, TRANSISTOR, PN, SILICON, UNIJUNCTION
JAN2N5431, and JANTX2N5431

1. SCOPE

1.1 Scope. - This specification covers the detail requirements for a PN, silicon, unijunction transistor. The prefix "TX" is used on devices submitted to and passing the special process-conditioning, testing, and screening tests specified in 4.5 through 4.5.8.1.

1.2 Physical dimensions. - See Figure 1.

1.3 Maximum ratings.

P_T 1/ $T_A = 25^\circ\text{C}$	I_e	i_e 2/	V_{B2E}	T_{stg}
$\underline{W}$	$\underline{\text{mA (rms)}}$	$\underline{A(pk)}$	$\underline{Vdc}$	$\underline{^\circ\text{C}}$
.300	50	1.5	30	-65 to +200

1/ Derate linearly 2.4 mW/°C for $T_A > 25^\circ\text{C}$.

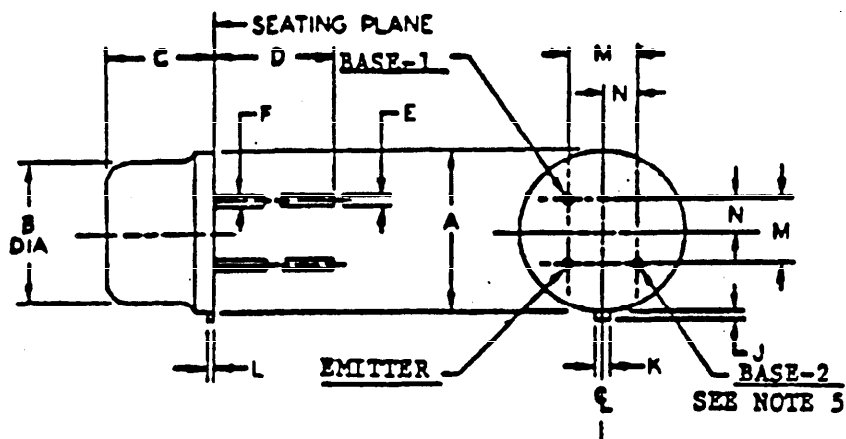
2/ This value applies for a capacitor discharge through the emitter-base-one diode. The current must fall to 0.37A within 3 ms and pulse-repetition rate must not exceed 10 pps.

1.4 Primary electrical characteristics.

R_{BBO} $V_{B2B1} = 3Vdc$ $I_E = 0$		n $V_{B2B1} = 10Vdc$ (see Figure 5)		$V_{EB1(sat)}$ 1/ $V_{B2B1} = 10Vdc$ $I_E = 50mAdc$	V_{OB1} See Figure 10	I_{EB20} $V_{EB2} = -30Vdc$ $I_{B1} = 0$	$I_{B2(mod)}$ 1/ $V_{B2B1} = 10Vdc$ $I_E = 50mAdc$	
k Ω				Vdc	V (pk)	nAdc	mAdc	
Min.	Max.	Min.	Max.	Max.	Min.	Max.	Min.	Max.
6.0	8.5	0.72	0.80	3.0	1.0	-10	5	30

1/ Pulsed see 4.4.1

FSC 5961



L I R	D I M E N S I O N S				N O T E S
	I N C H E S		M I L L I M E T E R S		
	M I N	M A X	M I N	M A X	
A	.209	.230	5.31	5.84	7 2,7 3,7 6
B	.178	.195	4.52	4.95	
C	.170	.210	4.32	5.33	
D	.500	--	12.70	--	
E	--	.021	--	.53	
F	.016	.019	.41	.48	
J	.028	.048	.71	1.22	
K	.036	.046	.91	1.17	4 4
L	--	.020	--	.51	
M	.0707 Nom		1.80 Nom		
N	.0354 Nom		0.90 Nom		

NOTES:

1. Metric equivalents (to the nearest .01 mm) are given for general information only and are based upon 1 inch = 25.4 mm.
2. Measured in the zone beyond .250 (6.35 mm) from the seating plane.
3. Measured in the zone .050 (1.27 mm) and .250 (6.35 mm) from the seating plane.
4. When measured in a gaging plane .054 $\pm$.001 (1.37 $\pm$.03 mm) below the seating plane of the transistor, maximum diameter leads shall be within .007 (.18 mm) of their true location relative to a maximum width tab. Smaller diameter leads shall fall within the outline of the maximum diameter lead tolerance. Figure 2 preferred measuring method.
5. Base-two shall be internally connected to the case.
6. Measured from the maximum diameter of the actual device.
7. All 3 leads.

Figure 1. Physical dimensions of transistor type (TX and non-TX) 2N5431

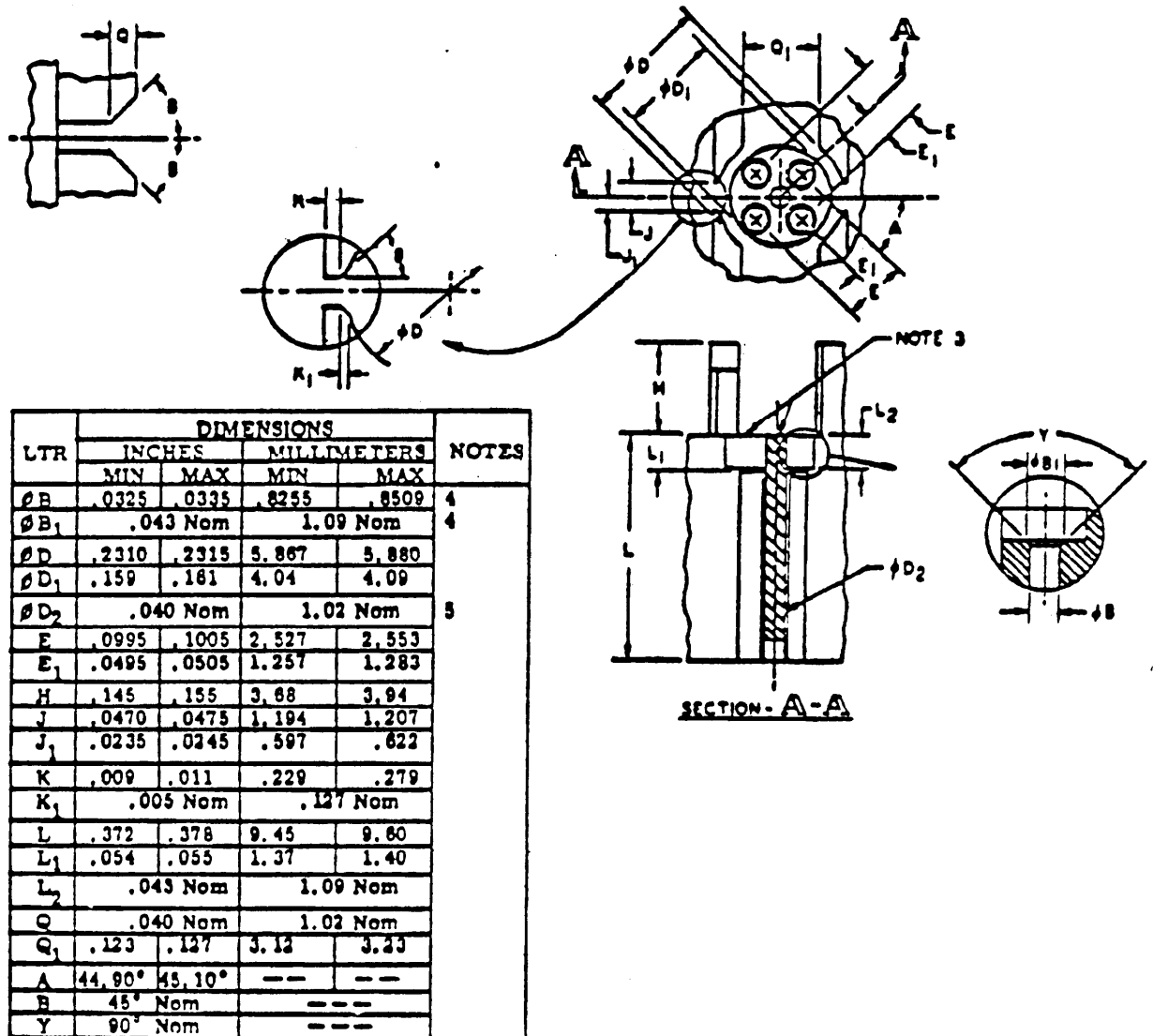


Figure 2. Gage for lead and tab location for transistor types (TX and non-TX) 2N5431.

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2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of the specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-S-19500--Semiconductor Devices, General Specification for.

STANDARDS

MILITARY

MIL-STD-202-Test Methods for Electronic and Electrical Component Parts.

MIL-STD-750-Test Methods for Semiconductor Devices.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 General. Requirements shall be in accordance with MIL-S-19500, and as specified herein.

3.2 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-S-19500, and as follows:

$I_{B2} \text{ (mod)}$ Modulated interbase current. The resultant base-two (B2) current for specified values of emitter current and interbase voltage.

I_e Emitter current, rms.

i_e Instantaneous emitter current (capacitor discharge).

I_{EB20} Emitter reverse current (d.c.), base-one (B1) open circuited.

- I_P Peak point emitter current. This is the minimum value emitter current for which the slope of the static emitter characteristic curve (see figure 3) is zero for a specified value of interbase voltage.
- I_V Valley point emitter current. This is the maximum value of emitter current for which the slope of the static emitter characteristic curve (see figure 3) is zero for a specified value of interbase supply voltage and base-two (B2) resistance.
- η (eta) Intrinsic standoff ratio. This is defined by the relationship:
- $$\eta = \frac{V_P - V_D}{V_{B2B1}}.$$
- R_{B2} Resistance in series with the base-two (B2) lead.
- R_{BBO} Interbase resistance. The resistance measured between base-one (B1) and base-two (B2) with the emitter open circuited.
- α_{RBBO} Interbase resistance temperature coefficient. This is determined by the following formula:
- $$\alpha_{RBBO} = \left[\frac{(R_{BBO} @ T_1) - (R_{BBO} @ T_2)}{(R_{BBO} @ 25^\circ C)} \right] \frac{100\%}{T_1 - T_2}.$$
- V_{BB} Interbase power supply voltage (d.c.).
- V_{B2B1} Interbase voltage, (d.c.) voltage from base-two (B2) to base-one (B1)
- V_{B2E} Voltage (d.c.) from base-two (B2) to emitter (E).
- V_D Emitter diode voltage, for intrinsic standoff ratio test. (0.565 $\pm$ 0.01 Vdc at 50 μ Adc, $T_A = 25^\circ C$.)

V_{EB1} . . . Voltage (d.c.) from emitter to base-one(B1).

$V_{EB1}(\text{sat})$. . . Emitter saturation voltage. The resultant d.c. voltage measured between the emitter and base-one (B1) for specified values of emitter current and interbase voltage.

V_{OB1} . . . Base-one (B1) peak pulse voltage. The base-one (B1) peak pulse voltage is defined as shown in figure 10. This parameter is a relative indicator of the peak emitter current available for use in firing circuits.

V_p . . . Peak point emitter voltage. The voltage from emitter to base-one (B1) when the peak point emitter current flows for a specified value of interbase voltage.

3.3 Symbol. The graphic symbol for the unijunction transistor shall be as shown in figure 4.

3.4 Design, construction, and physical dimensions. Transistors shall be of the design, construction, and physical dimensions shown on figure 1.

3.4.1 Lead arrangement. The lead arrangement shall be as follows (see Figure 1): Lead 1 - emitter (E); Lead 2 - base-one (B1); Lead 3 - omit; Lead 4 - base-two (B2).

3.4.2 Lead Material and finish. Lead material and finish shall be gold-plated Kovar. (leads may be tin-coated if specified in the contract or order, see 6.2).

3.5 Performance characteristics. Performance characteristics shall be as specified in Tables I, II, and III and as follows:

3.5.1 Process-conditioning, testing, and screening for "TX" types. Process-conditioning, testing, and screening for the "TX" types shall be as specified in 4.5.

3.6 Marking. The following marking specified in MIL-S-19500 may be omitted from the body of the transistor at the option of the manufacturer.

- a) Country of origin.
- b) Manufacturer's identification.

3.6.1 "TX" marking. Devices in accordance with the "TX" requirements shall include the additional marking "TX" preceding the type designation.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.2 Qualification inspection. Qualification inspection shall consist of the examinations and tests specified in Tables I, II, and III.

4.2.1 Qualification testing. The non-TX types shall be used for qualification testing. Upon request to the qualifying activity, qualification will be extended to include the TX type of the device.

4.3 Quality conformance inspection. Quality conformance inspection shall consist of Groups A, B, and C inspection. When specified in the contract or order, one copy of the quality conformance inspection data, pertinent to the device inspection lot, shall be supplied with each shipment by the device manufacturer.

4.3.1 Group A inspection. Group A inspection shall consist of the examinations and tests specified in Table I.

4.3.2 Group B inspection. Group B inspection shall consist of the examinations and tests specified in Table II.

4.3.3 Group C inspection. Group C inspection shall consist of the examinations and tests specified in Table III. This inspection shall be conducted on the initial lot, and thereafter every 6 months during production.

4.3.4 Group B and Group C life-test samples. Samples that have been subjected to Group B, 340 hour life-test, may be continued on test to 1,000 hours in order to satisfy group C life-test requirements. These samples shall be predesignated, and shall remain subjected to the Group C, 1,000 hour acceptance evaluation after they have passed the group B, 340-hour acceptance criteria. The cumulative total of failures found during 340-hour test and during the subsequent interval up to 1,000 hours shall be computed for 1,000 hour acceptance criteria, see 4.3.3.

4.4 Methods of examination and test. Methods of examination and test shall be as specified in Tables I, II and III, and as follows:

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4.4.1 Pulse measurements. Conditions for pulse measurements shall be as specified in section 4 of MIL-STD-750.

4.4.2 Interbase resistance. The specified interbase voltage (see Tables I, II, and IV) is applied and the corresponding resistance is measured for the emitter open circuited.

4.4.3 Intrinsic standoff ratio. Either of the two alternate methods below may be used at the option of the manufacturer.

4.4.3.1 Method a. The circuit of Figure 5a shall be used for this measurement. The specified interbase voltage (see Tables I,II, and IV) shall be applied and the variable resistor shall be adjusted to obtain a null. Eta is then read directly from the calibration of the variable resistor. The equation below shall be used to calibrate the variable resistor.

$$\eta = \frac{V_P - V_D}{V_{B2B1}}$$

4.4.3.2 Method b. The circuit of figure 5b or a suitable equivalent shall be used for this measurement. Switch S is closed, applying the specified V_{B2B1} (see Table I,II,and IV)and causing the unijunction to fire. The voltage acrosss the 100 K ohm resistor, V_R is measured and η ratio is computed as follows:

$$\eta = \frac{V_R}{V_{B2B1}} = \frac{V_P - V_D}{V_{B2B1}} \quad (V_D = 0.565 \text{ Vdc at } 50 \text{ } \mu\text{A dc and } T_A = -25^\circ\text{C})$$

4.4.4 Modulated interbase current and emitter saturation voltage. The specified values (see table I) of interbase voltage and emitter current are applied. The base-two (B2) current is measured as the modulated interbase current. The emitter to base-one (B1) voltage is measured as the emitter saturation voltage. The test circuit of Figure 6 may be used to measure these parameters.

4.4.5 Peak Point emitter current. This parameter shall be measured in the circuit of figure 7 or a suitable equivalent. The variable resistor is adjusted to apply a low resistance between the emitter and base-one (B1). The specified V_{B2B1} (see table I) is applied and the resistance between the emitter and base-one (B1) is increased until transistor fires as determined by oscillation of I_E . Peak point emitter current is the maximum value of I_E just prior to oscillation.

4.4.6 Valley point emitter current. For the specified interbase supply voltage (see table I) and base-two (B2) resistance the emitter current corresponding to the valley point operating condition is measured. The test circuit of figure 8, or suitable equivalent, shall be used for this measurement. The specified interbase supply voltage, V_{BB} , and base-two (B2) series resistance shall be applied. R_1 shall be of sufficient value to adequately control the emitter current. The bias voltage shall be gradually increased until the device fires and then shall be varied to obtain a minimum value of V_{EB1} . The I_E corresponding to this minimum value of V_{EB1} is the I_V of the device under test.

4.4.7 Emitter reverse current. This test shall be conducted in accordance with method 3036 of MIL-STD-750 except that the words and symbols, collector (C), base (B), and emitter (E) shall be replaced with base-two (B2), emitter (E), and base-one (B1), respectively.

4.4.8 Interbase resistance temperature coefficient. The interbase resistance temperature coefficient shall be determined by measuring the interbase resistance in accordance with paragraph 4.4.2 at the specified temperature and computing the temperature coefficient by the following formula:

$$\alpha_{RBBO} = \left[\frac{(RBBO @ T_1) - (RBBO @ T_2)}{(RBBO @ 25^\circ C)} \right] \times \frac{100\%}{T_1 - T_2}$$

4.4.9 Resistance to solvents. Transistors shall be subjected to tests in accordance with Method 215 of MIL-STD-202. The following details shall apply:

- (a) All areas of the transistor body where marking has been applied shall be brushed.
- (b) After subjection to the tests there shall be no evidence of mechanical damage to the device, and, markings shall have remained legible.

TABLE I. Group A inspection

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		UNIT
	METHOD	DETAILS	NON TX	TX		MIN.	MAX.	
<u>Subgroup 1</u>			10	5				
Visual and mechanical examination	2071				---	---	---	---
<u>Subgroup 2</u>			5	2				
Intrinsic standoff ratio	----	$V_{B2B1}=10Vdc$ (see 4.4.3)			n	0.72	0.80	---
Interbase resistance	----	$V_{B2B1}=3Vdc$; $I_E=0$ (see 4.4.2)			R_{BBO}	6	8.5	kohms
<u>Subgroup 3</u>			5	3				
Modulated interbase current	----	$V_{B2B1}=10Vdc$ (see 4.4.4) $I_E=50mAdc$ Pulsed (see 4.4.1)			$I_{B2(mod)}$	5	30	mAdc
Emitter saturation voltage	----	$V_{B2B1}=10Vdc$ (see 4.4.4) $I_E=50mAdc$ Pulsed (see 4.4.1)			$V_{EB1(sat)}$	--	3	Vdc
Emitter reverse current	3036	Bias Cond.D (see 4.4.7) $V_{EB2}=-30Vdc$ $I_{B1}=0$			I_{EB20}	--	-10	nAdc

TABLE I Group A inspection - Cont'd

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		UNIT
	METHOD	DETAILS	NON TX	TX		MIN.	MAX.	
<u>Subgroup 4</u>			10	5				
Valley point current	----	$V_{BB} = 20Vdc$ $R_{B2} = 100ohms$			I_V	2		mAdc
Peak point emitter current	----	$V_{B2B1} = 25Vdc$ (see 4.4.5)			I_p	—	0.4	μAdc
Base-one peak pulse voltage	----	$V_{B2B1} = 4Vdc$ (see 4.4.5) See figure 10			V_{OB1}	1	—	Vdc
<u>Subgroup 5</u>			10	5				
Interbase resistance temperature coefficient	----	$V_{B2B1} = 3Vdc$ $I_E = 0$ (see 4.4.8) $T_1 = 100^\circ C$ $T_2 = -65^\circ C$			α_{RBBO}	0.4	0.8	$\% / ^\circ C$
High temperature operation: Emitter reverse current	3036	$T_A = +125^\circ C$ Bias Cond.D (see 4.4.7) $V_{EB2} = -30Vdc$ $I_{B1} = 0$			I_{EB20}	--	-1	μAdc

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TABLE II. Group B inspection

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		UNIT
	METHOD	DETAILS	NON TX	TX		MIN.	MAX.	
<u>Subgroup 1</u>			20	20				
Physical dimensions	2066	See Figure 1			-----	---	---	---
<u>Subgroup 2</u>			15	15				
Solderability	2026	Omit Aging			----	---	---	---
Thermal shock (temperature cycling)	1051	Test Cond. C except temp. = 175 ⁺⁵ °C, -0 °C, 10 cycles, time at temp- erature ex- tremes = 15 minutes min.			----	---	---	---
Thermal shock	1056	Test Cond. A			----	---	---	---
Seal (Leak rate)	1071	Test Cond. H for fine leaks; Test Cond. C, D, or F for gross leaks.			----	---	5x10 ⁻⁷	atm cc/sec
Moisture resistance	1021				----	---	---	---
<u>End Points:</u>								
Emitter reverse current	3036	Bias Cond. D. (see 4.4.7) V _{EB2} = -30Vdc I _{B1} = 0			I _{EB20}	---	-10	nAdc

TABLE II. Group B inspection (Cont.)

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		UNIT
	METHOD	DETAILS	NON TX	TX		MIN.	MAX.	
<u>Subgroup 2</u> (Continued)								
Interbase resistance	----	$V_{B2B1} = 3V_{dc}$ $I_E = 0$ (See 4.4.3)			R_{BBO}	6.0	8.5	kohms
Intrinsic standoff ratio	----	$V_{B2B1} = 10V_{dc}$ (see 4.4.3)			η	0.72	0.80	----
<u>Subgroup 3</u>			15	15				
Shock	2016	Nonoperat- ing; 1500G for 0.5 msec; 5 blows in each orien- tation; X_1 , Y_1 , Y_2 , Z_1			----	----	----	----
Vibration variable frequency	2056				----	----	----	----
Constant acceleration	2006	10,000 G in each orien- tation: X_1 , Y_1 , Y_2 , Z_1						
End Points: (same as for sub-group 2)								

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TABLE II. Group B inspection - Cont'd

EXAMINATION or TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		UNIT
	METHOD	DETAILS	NON TX	TX		MIN.	MAX.	
<u>Subgroup 4</u>			15	15				
Terminal strength (lead fatigue)	2036	Test Cond. E.			---	--	--	---
Seal (leak-rate)	1071	Test Cond. H.			---	--	5×10^{-7}	atm cc/sec
<u>Subgroup 5</u>			15	15				
Salt atmosphere (corrosion)	1041				---	--	--	---
End Points: (same as for subgroup 2)								
<u>Subgroup 6</u>			15	2-7				
High temperature life (nonoperating) (non-TX types)	1032	$T_{stg} = +200^{\circ}\text{C}$ time = 340 hours (see 4.3.4)			---	--	--	---
High temperature Life (nonoperating) (TX types only)	1031	$T_{stg} = +200^{\circ}\text{C}$						
End Points:								
Emitter reverse current	3036	Bias cond. D (see 4.4.7) $V_{EB} = -30\text{Vdc}$ $I_{R1} = 0$			I_{EB20}	--	-20	nAdc

TABLE II. Group B inspection Cont'd

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		UNIT
	METHOD	DETAILS	NON TX	TX		MIN.	MAX.	
Subgroup 6 Cont'd) Interbase resistance	---	$V_{B2B1} = 3V_{dc}$ $I_E = 0$ (see 4.4.2)			R_{BBO}	5.4	9.4	Kohms
Intrinsic stand off ratio	---	$V_{B2B1} = 10V_{dc}$ (see 4.4.3)			η	0.65	0.88	---
Subgroup 7			10	$\lambda=5$				
Steady state operation life (non-TX types)	1027	$T_A = 25^\circ C$ $I_E = 0$ time = 340 hours, (see 4.3.4) $9500\Omega \leq R_{B2}$ $< 12,600 \Omega$ V_{BB} per formula shown in figure 9			---	---	---	---
Steady state operation life (TX types only)	1026	$T_A = 25^\circ C$ $I_E = 0$ $9500\Omega \leq R_{B2}$ $\leq 12,600 \Omega$ V_{BB} per formula shown in figure 9			---	---	---	---

TABLE III. Group C inspection

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		UNIT
	METHOD	DETAILS	NON TX	TX		MIN.	MAX.	
<u>Subgroup 1</u>			15	15				
Barometric pressure (reduced altitude operation)	1001	Normal mounting; pressure = 8 ± 2 mmHg for 60 seconds min.			---	---	---	---
Measurement during test:								
Emitter reverse current	3036	Bias cond.C (see 4.4.7) $V_{B2E} = 30Vdc$ $I_{B1} = 0$			I_{EB20}	---	-10	nAdc
<u>Subgroup 2</u>			15					
High temperature life (nonoperating) (non-TX types)	1032	$T_{stg} = +200^{\circ}C$ (see 4.3.4)			---	---	---	---
End Points: (same as for Subgroup 6, Group B)								
<u>Subgroup 3</u>			15					
Steady state operation life (non-TX types)	1027	$T_A = 25^{\circ}C$ $I_E = 0$ $9500\Omega \leq R_{B2} \leq 12,600\Omega$ V_{BB} per formula shown in Figure 9			---	---	---	---

TABLE III. GROUP C inspection Cont'd

EXAMINATION ---OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		UNIT
	METHOD	DETAILS	NON TX	TX		MIN.	MAX.	
<u>Subgroup 3</u> (Cont'd) <u>End Points</u> (same as for Subgroup 6, Group B) <u>Subgroup 4</u> Thermal shock (tem- perature cycling)	1051	Test Cond.C except temp= $+175^{+5}_{-0}$ °C, 25 cycles; Time at temp- erature ex- tremes = 15 minutes mini- mum. Total test time = 72 hr. max.	10	10				
<u>End Points:</u> Same as for subgroup 2, Gr. B.								
<u>Subgroup 5</u> Resistance to solvents	---	MIL-STD-202 Method 215 (see 4.4.9)	10	10	---	---	---	---

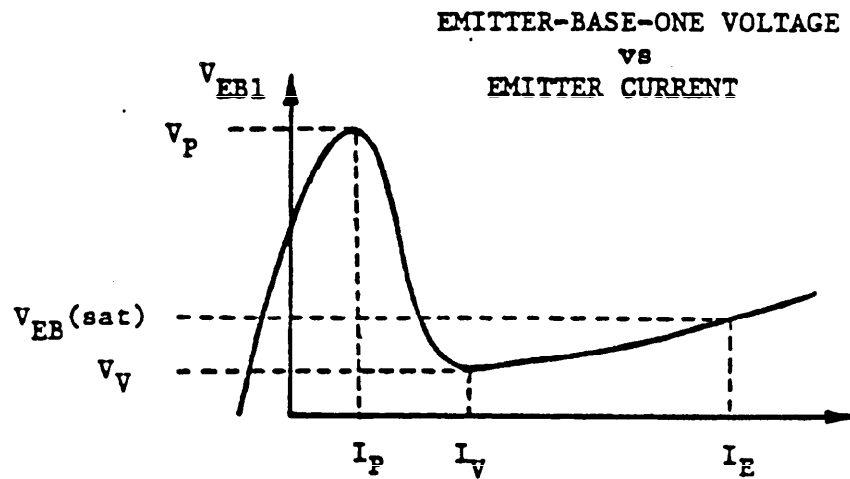


FIGURE 3. Unijunction transistor static emitter characteristic curve.

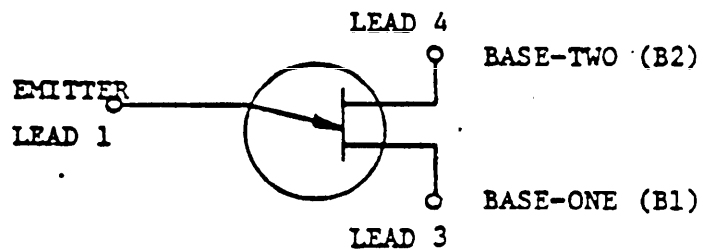
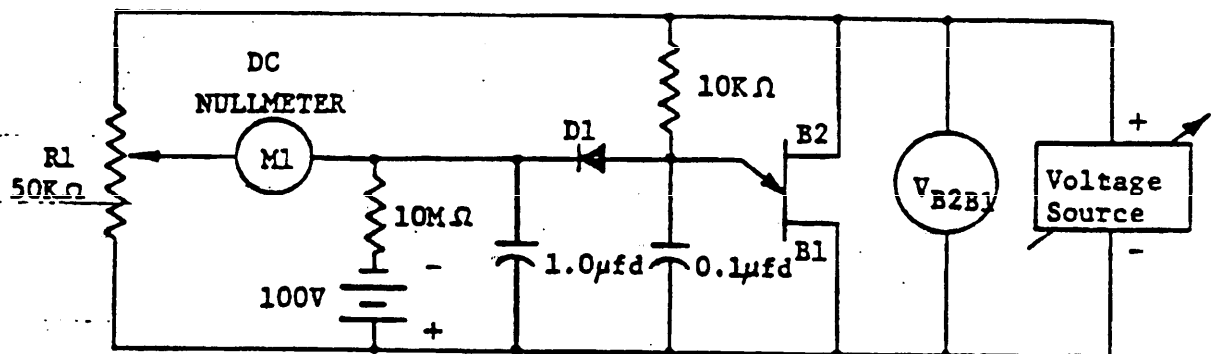


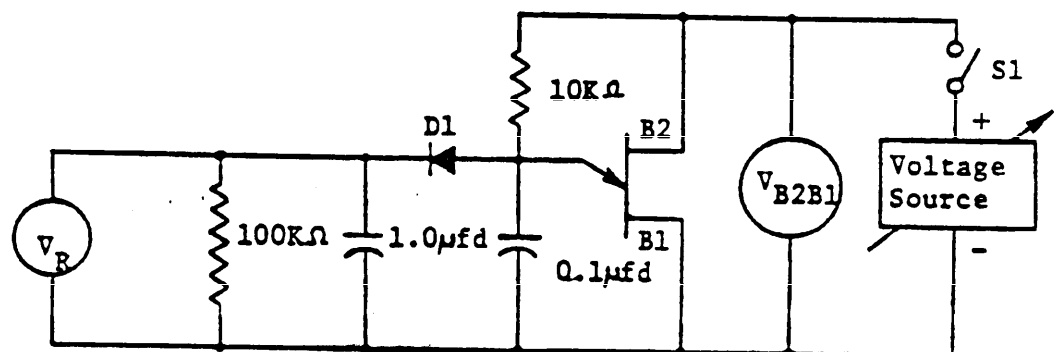
FIGURE 4. Graphic symbol for the unijunction transistor.



NOTES:

1. R1 - Calibrated helipot (η).
2. Voltage source must have less than 10mV ripple (peak to peak).
3. D1 - Silicon diode, forward voltage of $.490 \pm .010$ volts at forward current of 50μAdc and a reverse leakage of less than 1μAdc at 20 volts.

FIGURE 5a. Intrinsic standoff ratio test circuit. (Alternate A).



NOTES:

1. Voltage source must have less than 10mV ripple (peak to peak), and be readily controllable to less than 10mV.
2. D1 - Silicon diode, forward voltage of $.490 \pm .010$ volts at forward current of 50μAdc and a reverse leakage of less than 1μAdc at 20 volts.

FIGURE 5b. Intrinsic standoff ratio test circuit. (Alternate B).

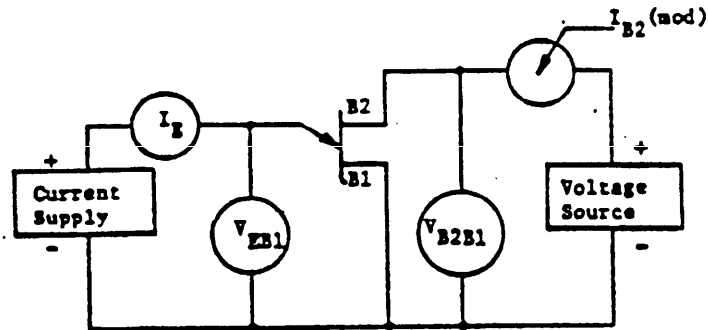
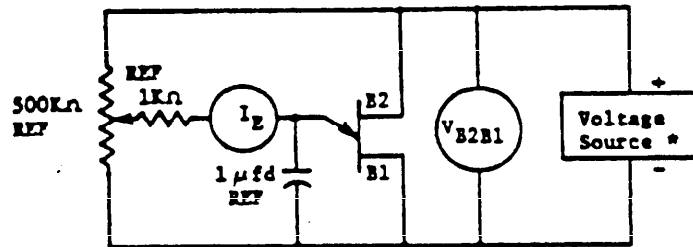


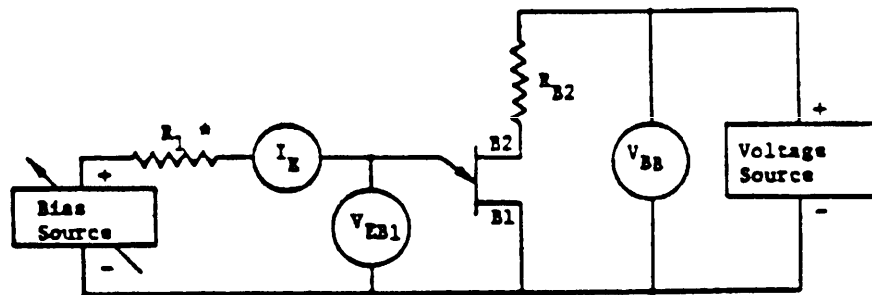
FIGURE 6 Modulated interbase current and emitter saturation voltage circuit.



NOTES:

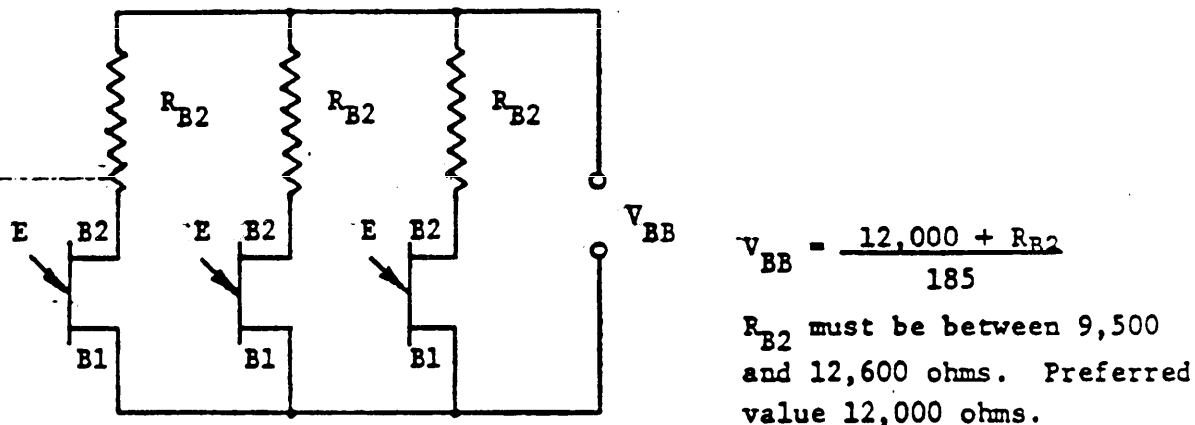
1. 500K pot must be noiseless to prevent false triggering.
2. *—Voltage source with less than 1 mV peak to peak ripple.

FIGURE 7. Peak point emitter current circuit.



* R_1 chosen to limit current to a safe value.

FIGURE 8. Valley point emitter current circuit.



R_{B2} shall be chosen by the manufacturer between the specified values. The V_{BB} to be used shall then be calculated. Extreme caution must be exercised to insure that excessive base to base transient voltages do not cause thermal runaway.

FIGURE 9. Life test circuit.

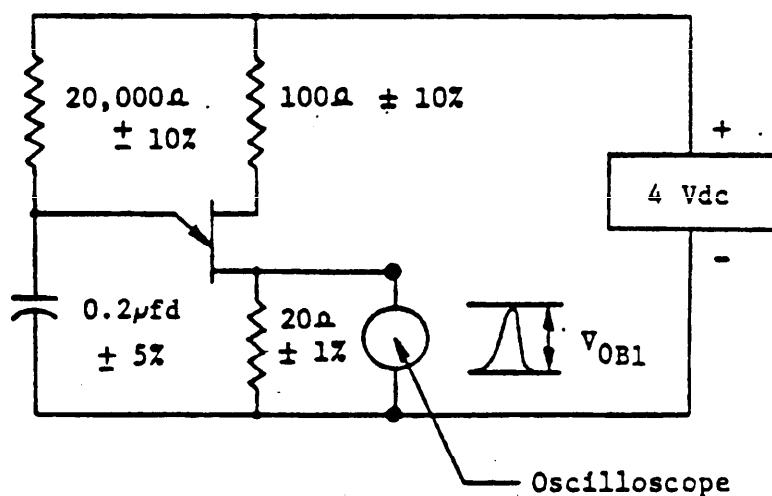


FIGURE 10. Base-one (B1) peak pulse voltage test circuit.

4.5 Process-conditioning, testing, and screening for TX types. The procedure for process-conditioning, testing, and screening shall be in accordance with 4.5.1 through 4.5.8.1 and Figure 11. Process-conditioning shall be conducted on 100% of the lot, prior to submission of the lot to the tests specified in Tables I, II, and III. (At option of the manufacturer, the non-TX type may be subjected to process-conditioning and testing).

4.5.1 Quality assurance (lot verification). Quality assurance shall keep lot records for three years minimum, monitor for compliance to the prescribed procedures, and observe that satisfactory manufacturing conditions and records on lots are maintained for these devices. The records shall be available for review by the customer at all times. The quality assurance monitoring shall include, but not be limited to: process-conditioning, testing, and screening. (The conditioning and screening tests performed as standard production tests need not be repeated when these are predesignated and acceptable to the Government as being equal to or more severe than the tests specified herein).

4.5.2 High-temperature storage. All devices shall be stored for at least 24 hours at a minimum temperature (T_A) of 200° C.

4.5.3 Thermal shock (temperature cycling). All devices shall be subjected to thermal shock (temperature cycling) in accordance with MIL-STD-750, Method 1051, Test Condition C, except that 10 cycles shall be continuously performed and the time at the temperature extremes shall be 15 minutes, minimum.

4.5.4 Acceleration. All devices shall be subjected to acceleration test in accordance with MIL-STD-750, Method 2006, with the following exceptions: The test shall be performed one time in the Y_1 orientation only at a peak level of 20,000 G minimum. The one minute hold requirement shall not apply.

4.5.5 Hermetic seal tests. All devices shall be subjected to hermetic seal tests (fine leak followed by gross leak) with test conditions as specified in 4.5.5.1 and 4.5.5.2. Failed devices from either test shall be removed from the lot.

4.5.5.1 Fine-leak test. All devices shall be fine-leak tested in accordance with MIL-STD-750, Method 1071, Test Condition H; except the leak rate rejection criterion shall be 5×10^{-7} cubic centimeters of helium per second when measured at a differential pressure of one atmosphere.

4.5.5.2 Gross leak test. All devices shall be tested for gross-leaks in accordance with MIL-STD-750, Method 1071, Test Condition D or F.

4.5.6 Pre Burn-in tests. The parameters I_{EB20} , R_{BBO} , and η of Table IV shall be measured and the data recorded for all devices in the lot. All devices shall be handled or identified such that the delta end points can be determined after the burn-in test. All devices which fail to meet these requirements shall be removed from the lot and the quantity removed shall be noted on the lot history.

TABLE IV. Burn-In test measurements

EXAMINATION OR TEST	MIL-STD-750		SYMBOL	MIN.	MAX.	UNIT
	METHOD	DETAILS				
Emitter reverse current	3036	Bias cond. D. (see 4.4.7) $V_{EB2} = -30Vdc$ $I_{B1} = 0$	I_{EB20}	—	-10	nAdc
Interbase resistance	—	$V_{B2B1} = 3Vdc$ $I_E = 0$ (see 4.4.2)	R_{BBO}	6	8.5	Kohms
Intrinsic standoff ratio	—	$V_{B2B1} = 10Vdc$ (see 4.4.3)	η	0.72	0.80	—

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4.5.7 Burn-in test. All devices shall be operated for 168 hours minimum under the following conditions:

$$T_A = 25 \pm 3^\circ\text{C}$$

$$V_{B2B1} = 10 \text{ Vdc}$$

$$I_E = 30 \text{ mAdc}$$

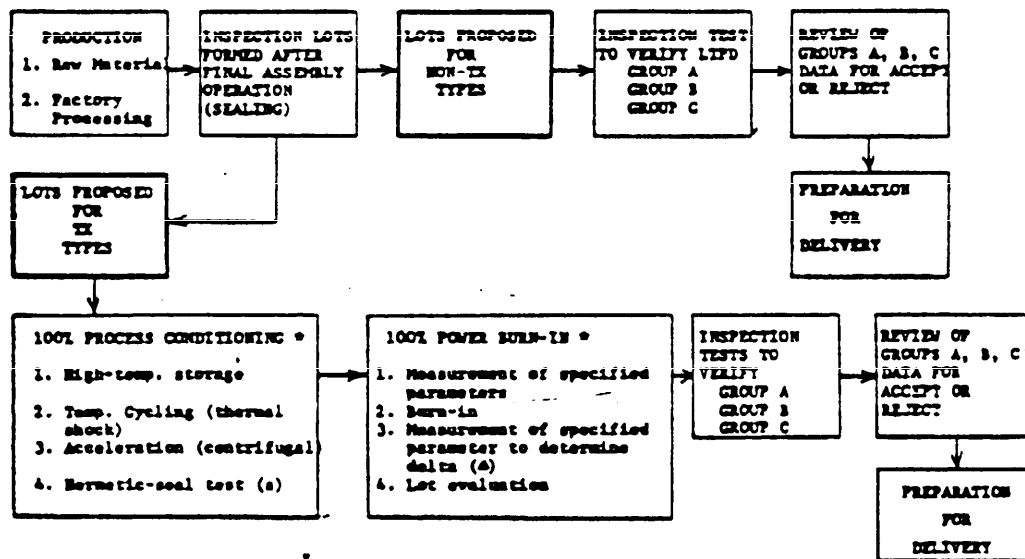
4.5.8 Post burn-in tests. The parameters I_{EB20} , R_{BBO} , and η of Table IV shall be retested after burn-in and the data recorded for all devices in the lot. The parameters measured shall not have changed during the burn-in test from the initial value by more than the specified amount as follows:

$\Delta I_{EB20} = 100$ percent or 5 nanoamperes, whichever is greater.

$\Delta R_{BBO} = \pm 20$ percent.

$\Delta \eta = \pm 10$ percent.

4.5.8.1 Burn-in test failures (screening). All devices that exceed the delta (Δ) limits of 4.5.8 or the limits of Table IV after burn-in, shall be removed from the inspection lot and the quantity removed shall be noted on the lot history. If the quantity removed after burn-in should exceed 10 percent of the total inspection lot on the burn-in tests, then the entire lot shall be unacceptable for TX types.



*ORDER OF THE TESTS IN THE BLOCKS SHALL BE PERFORMED AS SHOWN
FIGURE 11. Order of procedure diagram for TX types.

5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery. See MIL-S-19500, section 5.

6. NOTES

6.1 Notes. The notes specified in MIL-S-19500 are applicable to this specification.

6.2 Ordering data.

- a) Lead finish if other than gold-plated Kovar. (see 3.4.2)
- b) Inspection data (see 4.3)

6.3 The activity responsible for the Qualified Products List is Rome Air Development Center, Attn: ~~EMNEB~~, Griffiss Air Force Base, New York 13440; however, information pertaining to the qualification of products may be obtained from the Defense Electronics Supply Center, 1507 Wilmington Pike, Dayton, Ohio 45401.

Custodian:

Air Force - 17

Review activities:

Air Force - 11, 85

Preparing activity:

Air Force - 17

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