

MIL-S-19500/258A(NAVY)
 22 June 1964
 SUPERSEDING
 MIL-S-19500/258(NAVY)
 9 January 1963
 (See 6.2)

MILITARY SPECIFICATION
SEMICONDUCTOR DEVICE, TRANSISTOR TYPES
2N962 AND 2N964

1. SCOPE

1.1 Description.- This specification covers the detail requirements for PNP germanium epitaxial switching transistors and is in accordance with MIL-S-19500, except as otherwise specified herein.

1.2 Mechanical dimensions and outline.- T018 (see figure 1).

1.3 Absolute maximum ratings.-

P_T (mw)		V_{CB} (Vdc)	
$T_C = 25^\circ\text{C. } 1/$	$T_A = 25^\circ\text{C. } 2/$	2N962	2N964
300	150	-12	-15

V_{EB} (Vdc)		V_{CES} (Vdc)		I_C mA	T_J	T_{stg}
2N962	2N964	2N962	2N964			
-1.25	-2.5	-12	-15	200	100°C.	-55° to 100°C.

1/Derate 4 mw/°C above 25°C.

2/Derate 2 mw/°C above 25°C.

1.4 Primary electrical characteristics.

	h_{FE}				h_{fe}	$V_{CE} \text{ (sat) (Vdc)}$			
	$V_{CE} = -0.3$ $I_C = -10 \text{ ma}$		$V_{CE} = -1\text{Vdc}$ $I_C = -100 \text{ ma}$			$I_C = -10 \text{ mdc}$ $I_B = -1 \text{ mdc}$		$I_C = -100 \text{ mdc}$ $I_B = -10 \text{ mdc}$	
	2N962	2N964	2N962	2N964	$f = 100 \text{ mc}$ $I_C = -20 \text{ ma, V}$ $V_{CE} = -1\text{Vdc}$	2N962	2N964	2N962	2N964
Max.	20	40	20	40	3.0	---	---	---	---
	---	160	---	---	---	-0.20	-0.18	-0.70	-0.60

2. APPLICABLE DOCUMENTS

2.1 The following documents of the issue in effect on date of invitation for bids, or request for proposal, form a part of this specification to the extent specified herein:

FSC 5960

MIL-S-19500/258A(NAVY)

SPECIFICATIONS

MILITARY

MIL-S-19491 - Semiconductor Devices, Preparation for Delivery of.
MIL-S-19500 - Semiconductor Devices, General Specification for.

STANDARD

MILITARY

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 General.- Transistors shall be in accordance with MIL-S-19500 and as specified herein.

3.2 Design, construction and physical dimensions.- Transistors shall be of the design, construction and physical dimensions shown on figure 1.

3.3 Performance characteristics.- Performance characteristics shall be as specified in 4.2.1 and 4.2.2.

3.4 Marking.- The following marking specified in MIL-S-19500 may be omitted from the device:

- (a) Country of origin.
- (b) Manufacturer's identification.

3.4.1 The device shall be marked with the "USN" prefix in lieu of the "JAN" prefix.

4. QUALITY ASSURANCE PROVISIONS

4.1 Qualification tests.- Qualification tests shall be conducted at a laboratory satisfactory to the Bureau of Ships. Qualification tests shall consist of the tests specified in 4.2.1, and 4.2.2. (Application for Qualification tests shall be made in accordance with "Provisions Governing Qualification" (see 6.1)).

4.2 Quality conformance inspection.- Quality conformance inspection shall consist of the examinations and tests specified in 4.2.1 and 4.2.2.

4.2.1 Group A inspection.- Group A inspection shall consist of the examinations and tests shown in table I.

4.2.2 Group B inspection.- Group B inspection shall consist of the examinations and tests shown in table II.

4.2.2.1 Destructive tests.- Tests listed in subgroups 2, 3, 4, and 5 are considered destructive.

4.2.2.2 Salt atmosphere.- The device shall be examined for destructive corrosion and illegible marking.

4.2.4 Quality conformance inspection information.- When specified in the contract or order, one copy of the quality conformance inspection information pertinent to the transistor inspection lot shall be furnished by the transistor supplier and shall accompany each transistor shipment from the inspection lot to the equipment manufacturer.

4.3 Inspection of preparation for delivery.- Sample items and packs shall be selected and inspected in accordance with MIL-S-19491 to verify conformance with requirements in section 5 of this specification.

4.4 Collector latchup voltage.- Latch-up is the failure of the collector potential to return to the supply voltage upon turn-off. The collector latchup voltage is the minimum voltage that the collector must return to upon turn-off of the transistor.

4.5 Base leakage current.- I_{BL} is defined as base leakage current with both junctions reverse biased. I_C is always less than I_{BL} for $V_{BE} > V_T$. (V_{BE} is off condition base bias, V_T is base voltage at threshold of conduction.)

4.6 Total control charge.- When a transistor is held in a conductive state by a current, I_{BI} , a charge Q_s is developed in the active region. A charge Q_T can be stored on an external capacitor C to neutralize the internal charge of the transistor.

4.7 Methods of examination and test.-

4.7.1 Input capacitance.- Input capacitance shall be conducted in accordance with Method 3240 of MIL-STD-750 except that the capacitor in the output circuit shall be omitted.

4.7.2 All measurements and tests shall be made at an ambient temperature of $25^\circ \pm 3^\circ C$, unless otherwise specified.

4.7.3 Shock.- The shock waveform shall approximate one half-cycle of a sinewave with a rise time of $0.25^{+0.1}_{-0}$ msec and a decay time of $0.25^{+0.1}_{-0}$ msec. The acceleration of any secondary impacts shall not exceed 20 percent of each primary impact. The amplitude of any response waveform distortion shall not exceed 10 percent of the peak acceleration.

5. PREPARATION FOR DELIVERY

5.1 See MIL-S-19500.

6. NOTES

6.1 The activity responsible for the qualified products list is the Bureau of Ships, Department of the Navy, Washington, D. C. 20360, and information pertaining to qualification of products may be obtained from that activity. Application for Qualification tests shall be made in accordance with "Provisions Governing Qualification". (Copies of "Provisions Governing Qualification" may be obtained upon application to Commanding Officer, Naval Supply Depot, 5801 Tabor Avenue, Philadelphia 20, Pa.)

6.2 CHANGES FROM PREVIOUS ISSUE. THE EXTENT OF CHANGES (DELETIONS, ADDITIONS, ETC.) PRECLUDE THE ANNOTATION OF THE INDIVIDUAL CHANGES FROM THE PREVIOUS ISSUE OF THIS DOCUMENT.

Preparing activity:
Navy - Ships
(Project 5960-N461(NAVY))

Table I - Group A inspection.

EXAMINATION OR TEST	CONDITIONS		LTPD	MIN. REJ. NO.	SYMBOL	LIMITS		UNIT
	MIL-STD-750 METHOD	SPECIFIC CONDITIONS				MIN.	MAX.	
<u>Subgroup 1</u>								
Visual and mechanical examination	2071		10	5				
<u>Subgroup 2</u>								
Collector-base breakdown voltage	3001 Condition D	$I_C = -100\mu\text{A dc}$ $I_E = 0$	5	5	BV_{CBO}			
2N962						-12	---	Vdc
2N964						-15	---	Vdc
Collector latch-up voltage (see 4.4)		$V_{CC} = -11.5\text{V dc}$ (see figure 7)			V_{CEXL}	-11.5	---	Vdc
Emitter to base breakdown voltage	3026 Condition D	$I_E = -100\mu\text{A dc}$ $I_C = 0$			BV_{EBO}			
2N962						-1.25	---	Vdc
2N964						-2.5	---	Vdc
Collector to emitter breakdown voltage	3011 Condition D	$I_C = -10\text{mA dc}$ $I_B = 0$			BV_{CEO}	-7.0	---	Vdc
Collector to emitter cutoff current	3041 Condition C				I_{CES}			
2N962		$V_{CE} = -12\text{V dc}$ $V_{EB} = 0$				---	-100	$\mu\text{A dc}$
2N964		$V_{CE} = -15\text{V dc}$ $V_{EB} = 0$				---	-100	$\mu\text{A dc}$
Collector to base cutoff current	3036 Condition D	$V_{CB} = -6\text{V dc}$ $I_E = 0$			I_{CBO}	---	-3.0	$\mu\text{A dc}$
Base leakage current (see 4.5)		(See figure 6) $V_{CE} = -6\text{V dc}$ $V_{BE} = +0.5\text{V dc}$			I_{BL}	---	4	$\mu\text{A dc}$
		$V_{CE} = -6\text{V dc}$ $V_{BE} = +0.5\text{V dc}$ $T_J = +85^\circ\text{C.}$			I_{BL}	---	140	$\mu\text{A dc}$
<u>Subgroup 3</u>								
Static forward current transfer ratio	3076	$I_C = -10\text{mA dc}$ $V_{CE} = -0.3\text{V dc}$			h_{FE}			
2N962						20	---	
2N964						40	160	

Table I - Group A inspection (Cont'd).

EXAMINATION OR TEST	CONDITIONS		LTPD	MIN. REJ. NO.	SYMBOL	LIMITS		UNIT
	MIL-STD-750 METHOD	SPECIFIC CONDITIONS				MIN.	MAX.	
Static forward-current transfer ratio	3076	$I_C = -50\text{mA}_{dc}$ $V_{CE} = -1\text{V}_{dc}$			h_{FE}			
2N962						20	---	---
2N964						40	---	---
Static forward-current transfer ratio	3076	$I_C = -100\text{mA}_{dc}$ $V_{CE} = -1\text{V}_{dc}$			h_{FE}			
2N962						20	---	---
2N964						40	---	---
Collector saturation voltage	3071	$I_C = -10\text{mA}_{dc}$ $I_B = -1\text{mA}_{dc}$			$V_{CE(sat)}$			
2N962						---	-0.20	Vdc
2N964						---	-0.18	Vdc
Collector saturation voltage	3071	$I_C = -50\text{mA}_{dc}$ $I_B = -5\text{mA}_{dc}$			$V_{CE(sat)}$			
2N962						---	-0.40	Vdc
2N964						---	-0.35	Vdc
Collector saturation voltage	3071	$I_C = -100\text{mA}_{dc}$ $I_B = -10\text{mA}_{dc}$			$V_{CE(sat)}$			
2N962						---	-0.70	Vdc
2N964						---	-0.60	Vdc
Base saturation voltage	3066 Condition A	$I_C = -10\text{mA}_{dc}$ $I_B = -1\text{mA}_{dc}$			$V_{BE(sat)}$	-0.30	-0.50	Vdc
Base saturation voltage	3066 Condition A	$I_C = -50\text{mA}_{dc}$ $I_B = -5\text{mA}_{dc}$			$V_{BE(sat)}$	-0.40	-0.75	Vdc
Base saturation voltage	3066 Condition A	$I_C = -100\text{mA}_{dc}$ $I_B = -10\text{mA}_{dc}$			$V_{BE(sat)}$			
2N962						-0.40	-1.25	Vdc
2N964						-0.40	-1.00	Vdc
Subgroup 4								
Small-signal short cir- cuit forward-current transfer ratio	3206	$I_E = -20\text{mA}_{dc}$ $V_{CE} = -1.0\text{V}_{dc}$ $f = 100\text{mc}$	5	5	h_{fe}	3	---	---

Table I - Group A inspection (Cont'd).

EXAMINATION OR TEST	CONDITIONS		LTPD	MIN. REJ. NO.	SYMBOL	LIMITS		UNIT
	MIL-STD-750 METHOD	SPECIFIC CONDITIONS				MIN.	MAX.	
Input capacitance (output open-circuited)	3240 (See 4.7)	$V_{EB} = -1V_{dc}$ $I_C = 0$ $f = 100 \text{ kc}$			C_{ibo}	---	3.5	pf
Collector capacitance	3236	$V_{CB} = -1V_{dc}$ $I_E = 0$ $f = 1 \text{ mc}$			C_{obo}	---	5.0	pf
<u>Subgroup 5</u>								
Delay plus rise time		$I_C = -10\text{mA}_{dc}$ $I_{B1} = 1\text{mA}_{dc}$ $V_{BE(0)} =$ $+1.25V_{dc}$ (see figure 2)	5	5	$t_d + t_r$	---	50	nsec
Delay plus rise time		$I_C = -100\text{mA}_{dc}$ $I_{B1} = -5\text{mA}_{dc}$ $V_{BE(0)} =$ $1.25V_{dc}$ (see figure 3)			$t_d + t_r$	---	50	nsec
Storage plus fall time		$I_C = -10\text{mA}_{dc}$ $I_{B1} = -1\text{mA}_{dc}$ $I_{B2} = 0.25\text{mA}_{dc}$ $V_{BE(0)} =$ $1.25V_{dc}$ (see figure 2)			$t_s + t_f$			
2N962						---	100	nsec
2N964						---	85	nsec
Storage plus fall time		$I_C = -100\text{mA}_{dc}$ $I_{B1} = -5\text{mA}_{dc}$ $I_{B2} = 1.25\text{mA}_{dc}$ $V_{BE(0)} =$ 1.25mA_{dc} (see figure 3)			$t_s + t_f$			
2N962						---	180	nsec
2N964						---	85	nsec
Total control charge		$I_C = -10\text{mA}_{dc}$ $I_B = -1\text{mA}_{dc}$ (see figure 4)			QT			
2N962						---	90	pc
2N964						---	80	pc
Total control charge (see 4.6)		$I_C = -100\text{mA}_{dc}$ $I_B = -5\text{mA}_{dc}$ (see figure 5)			QT			
2N962						---	150	pc
2N964						---	125	pc

Table I - Group A inspection (Contd).

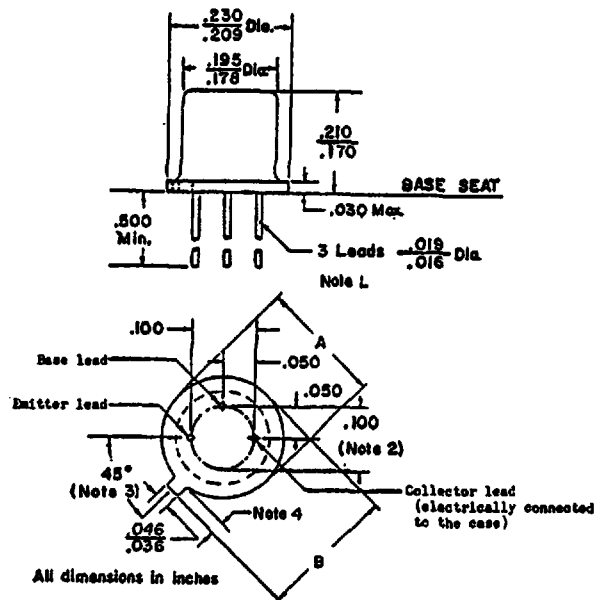
EXAMINATION OR TEST	CONDITIONS		LTPD	MIN. REJ. NO.	SYMBOL	LIMITS		UNIT
	MIL-STD-750 METHOD	SPECIFIC CONDITIONS				MIN.	MAX.	
<u>Subgroup 6</u>								
Collector to base cutoff current	3036 Condition D	$T_A = +55^\circ\text{C}$ $V_{CB} = -6\text{Vdc}$ $I_E = 0$	20	4	ICBO	---	-24	μAdc
Static forward-current transfer ratio	3076	$T_A = -55^\circ\text{C}$ $I_C = -10\text{mAdc}$ $V_{CE} = -0.3\text{Vdc}$			hFE			
2N962						10	---	---
2N964						20	---	---
Static forward-current transfer ratio	3076	$T_A = +85^\circ\text{C}$ $I_C = -100\text{mAdc}$ $V_{CE} = -1\text{Vdc}$			hFE			
2N962						16	---	---
2N964						35	---	---

Table II - Group B inspection.

EXAMINATION OR TEST	CONDITIONS		LTPD	MIN. REJ. NO.	SYMBOL	LIMITS		UNIT
	MIL-STD-750 METHOD	SPECIFIC CONDITIONS				MIN.	MAX.	
<u>Subgroup 1</u>								
Physical dimensions	2066		20	4				
<u>Subgroup 2</u>								
Solderability	2026		10	5				
Thermal shock (temperature cycling)	1051 Condition A							
Thermal shock (glass strain)	1056 Condition A							
Moisture resistance	1021							
<u>Subgroup 3</u>								
Shock (see 4.7.3)	2016	Nonoperating 1500G min. 5 blows each orientation: Y ₁ , Y ₂ , X ₁ and Z ₁	10	5				
Vibration fatigue	2046	Nonoperating						
Vibration, variable frequency	2056							

Table II - Group B inspection (Contd.).

EXAMINATION OR TEST	CONDITIONS		LTPD	MIN. REJ. NO.	SYMBOL	LIMITS		UNIT
	MIL-STD-750 METHOD	SPECIFIC CONDITIONS				MIN.	MAX.	
Constant acceleration	2006	20,000G each orientation: $\bar{Y}_1$, $\bar{Y}_2$, $\bar{X}_1$ and $\bar{Z}_1$						
<u>Subgroup 4</u>								
Terminal strength	2036 Condition E		20	4				
<u>Subgroup 5</u>			20	4				
Salt atmosphere (corrosion)	1041							
<u>Subgroup 6</u>								
High temperature life (nonoperating)	1031	$T_A = 100^\circ\text{C min.}$	$\lambda = 10$	5				
<u>Subgroup 7</u>								
Steady state operation life	1026	$T_A = 25^\circ\text{C}$ $V_{CB} = -5\text{Vdc}$ $I_C = -30\text{mAdc}$	$\lambda = 5$	5				
Endpoints for subgroups 2, 3, 5, 6, and 7:								
Static forward-current transfer ratio	3076	$I_C = 10\text{mAdc}$ $V_{CE} = -0.3\text{Vdc}$	---	---	h_{FE}			
2N962						16	---	---
2N964						32	---	---
Collector to base cutoff current	3036 Condition D	$V_{CE} = -6\text{Vdc}$ $I_E = 0$	---	---	I_{CBO}	---	-6.0	μAdc



Notes:

1. The specified lead diameter applies to the zone between 0.050 and 0.250 from the base seat. Between 0.250 and end of lead a maximum of 0.021 is held. Outside of these zones the lead diameter is not controlled.
2. Maximum diameter leads at a gaging plane $0.064^{+0.054}_{-0.000}$ below base seat to be within 0.007 of their true location relative to maximum width tab and to the maximum 0.230 diameter measured with a suitable gage. When gage is used, measurement will be made at base seat.
3. Index tab for visual orientation only.
4. Tab length shall be 0.028 minimum, 0.048 maximum, and will be determined by subtracting diameter A from Dimension B.

FIGURE 1 - MECHANICAL DIMENSIONS AND OUTLINE FOR TRANSISTOR TYPES 2N962 AND 2N964.

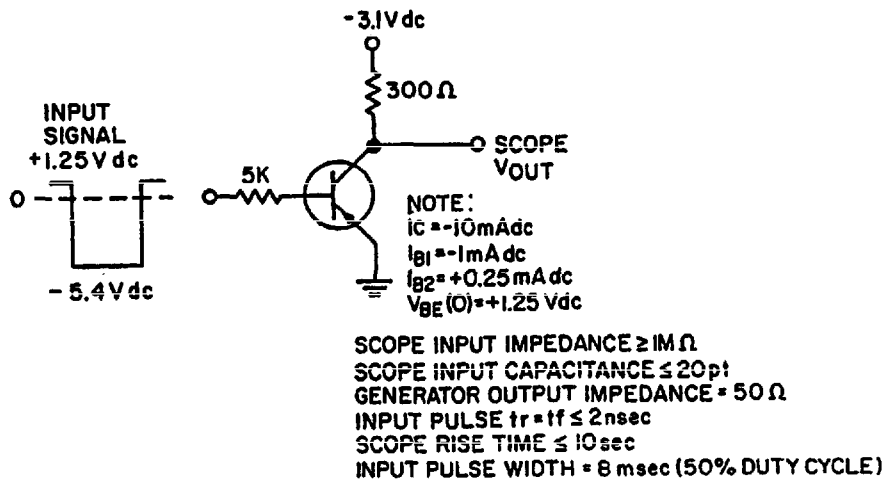


FIGURE 2 - 10 mA (Ic) SWITCHING TIME TEST CIRCUIT

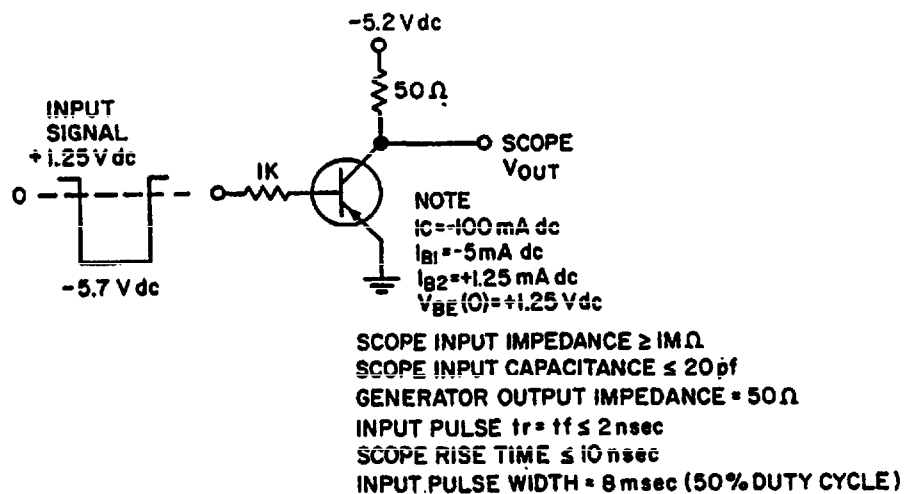


FIGURE 3 - 100 mA (Ic) SWITCHING TIME TEST CIRCUIT

*ADJUST V_{BB} FOR -5.4 VOLTS PULSE AT POINT A

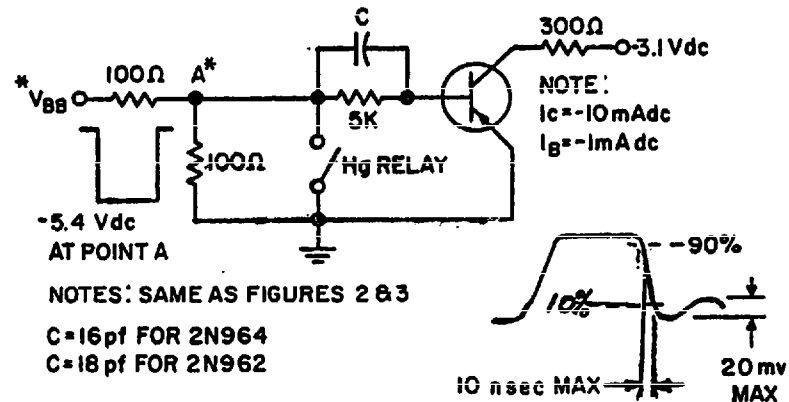


FIGURE 4 - 10mA (I_c) TOTAL CONTROL CHARGE TEST CIRCUIT

*ADJUST V_{BB} FOR -5.7 VOLTS PULSE AT POINT A

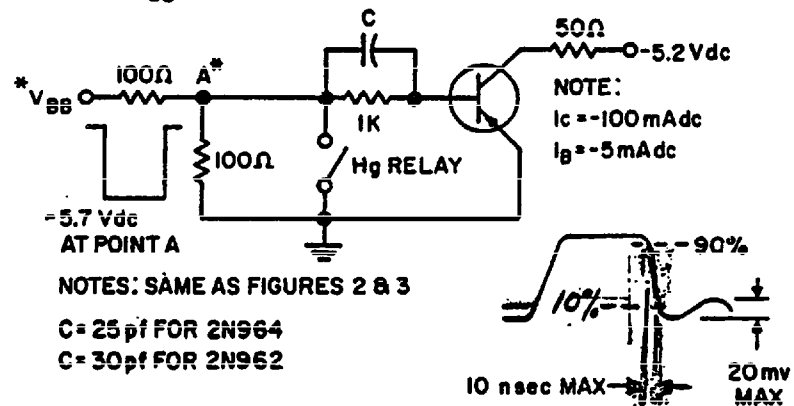


FIGURE 5 - 100mA (I_c) TOTAL CONTROL CHARGE TEST CIRCUIT

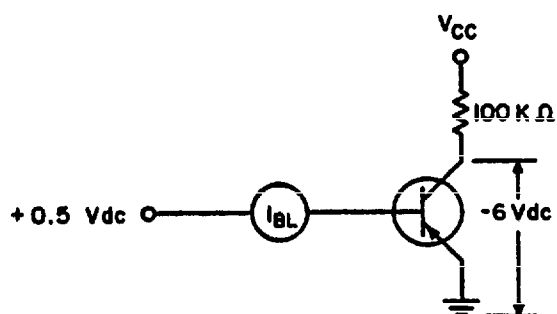
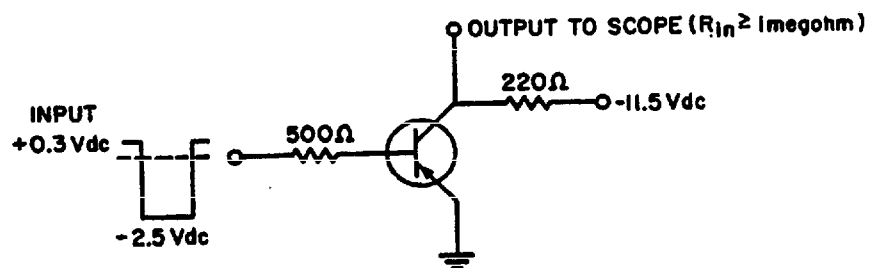


FIGURE 6 - BASE LEAKAGE CURRENT TEST CIRCUIT



NOTE:

GENERATOR OUTPUT IMPEDANCE $\leq 50 \Omega$

INPUT PULSE: $t_r = t_f \leq 2 \text{ nsec}$, $t_p \geq 500 \text{ nsec}$, DUTY CYCLE $\leq 50\%$

FIGURE 7 - COLLECTOR LATCH-UP VOLTAGE TEST CIRCUIT