



DEFENSE LOGISTICS AGENCY
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July 15, 2026

MEMORANDUM FOR MILITARY/INDUSTRY DISTRIBUTION

SUBJECT: Initial Draft of Performance Specification Sheet MIL-PRF-19500/733Fam4,
Project Number 5961-2026-071.

The initial draft for this subject document, dated July 15, 2026, is now available for viewing and downloading from the DLA Weapons Support-VA Web site:

<https://LandandMaritimeApps.dla.mil/Programs/MilSpec/DocSearch.aspx>

The initial draft of the subject document was generated to update the U2A case outline and to update it to the latest document format and various editorial changes to bring it into compliance with MIL-STD-961. Highlighting has been used for easy change recognition.

Concurrence or comments are required at this Center within 30 days from the date of this letter (August 14, 2026). Late comments will be held for the next coordination of the document. Comments from military departments must be identified as either "Essential" or "Suggested". Essential comments must be justified with supporting data. Military review activities should forward comments to their custodians of this office, as applicable, in sufficient time to allow for consolidating the department reply.

The point of contact for this document is Mr. Jason Hochstetler, DLA Weapons Support - VAC, Post Office Box 3990, Columbus, OH 43218-3990. Mr. Hochstetler can also be reached at 614-693-2825 / DSN 392-693-2825 or by e-mail to: Jason.hochstetler@dlamail.mil.

/ Signed /

MUHAMMAD AKBAR
Chief
Active Devices Branch

NOTE: This draft, dated 15 July 2026 prepared by DLA – CC, has not been approved and is subject to modification. DO NOT USE PRIOR TO APPROVAL.
(Project 5961-2026-071)
COMMENTS ARE DUE BY 14 August 2026.
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INCH-POUND

MIL-PRF-19500/733F
w/AMENDMENT 4
DRAFT
SUPERSEDING
MIL-PRF-19500/733F
w/AMENDMENT 3
22 October 2021

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED
P-CHANNEL, SILICON, DEVICE, ENCAPSULATED (THROUGH-HOLE, SURFACE MOUNT, AND
CARRIER BOARD PACKAGES), TYPES 2N7523, AND 2N7524, JANTXVR, F AND JANSR, F

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a P-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance (JANTXV and JANS) are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}) for use in particular power-switching applications. See 6.7 for JANHC and JANKC die versions. Provisions for radiation hardness assurance (RHA) to two radiation levels ("R" and "F") are provided for JANTXV and JANS product assurance levels.

1.2 Package outlines. The device package outlines are as follows: TO-254AA in accordance with figure 1, SMD2 TO-276AC (U2) in accordance with figure 2, and a modified (tab-less) TO-254AA in accordance with figure 3, SMD2 TO-276AC with lead option (U2L) in accordance with figure 4, SMD2 TO-276AC with carrier board option (U2S) in accordance with figure 5 for all encapsulated device types and surface mount (U2A) in accordance with figure 6 for all encapsulated device types. The dimensions and topography for JANHC and JANKC unencapsulated die are as listed in slash sheet MIL-PRF-19500/741.

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Type	P _T (1) T _C = +25°C	P _T T _A = +25°C (free air)	R _{θJC} (2)	R _{θJ} Carrier (3)	R _{θJ} Lid U2L (3)	V _{DS}	V _{DG}	V _{GS}	T _J and T _{STG}
	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>°C/W</u>	<u>°C/W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>°C</u>
2N7523T1, D4	208	2.60	0.60	N/A		-30	-30	±20	
2N7523U2, U2L, U2S, U2A	250	1.60	0.50	1.5	10	-30	-30	±20	-55 to +150
2N7524T1, D4	208	2.60	0.60	N/A		-60	-60	±20	
2N7524U2, U2L, U2S, U2A	250	1.60	0.50	1.5	10	-60	-60	±20	

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime Weapons Support, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

AMSC N/A

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FSC 5961



MIL-PRF-19500/733F
w/AMENDMENT 4

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1.3 Maximum ratings. - continued

Type	I _{D1} (4) (5) T _C = +25°C	I _{D2} (4) (5) T _C = +100°C	I _S	I _{DM} (6)
	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A(pk)</u>
2N7523T1, D4	-45	-45	-45	-180
2N7523U2, U2L, U2S, U2A	-56	-56	-56	-224
2N7524T1, D4	-45	-45	-45	-180
2N7524U2, U2L, U2S, U2A	-56	-56	-56	-224

- (1) Derate linearly by 2.00 W/°C (U2) or 1.67 W/°C (D4, T1) for T_C > +25°C.
(2) See figure 7, thermal impedance curves.
(3) The Thermal resistance is applicable for mounting methods where a heatsink is attached to the lid for U2L suffix devices.
(4) The following formula derives the maximum theoretical I_D limit. I_D is limited by package design and device construction, to 45 A for D4, T1 or to 56 A for U2, U2A, U2L, U2S.
- $$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$
- (5) See figure 8, maximum drain current graph.
(6) I_{DM} = 4 X I_{D1}, as defined in note (4).

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min V(BR)DSS V _{GS} = 0 I _D = 1.0 mA dc	V _{GS} (TH) V _{DS} ≥ V _{GS} I _D = 1.0 mA dc		Max I _{DSS1} V _{GS} = 0 V _{DS} = 80 percent of rated V _{DS}	Max r _{DS(ON)} (1) V _{GS} = 12 V dc		EAS at I _{D1}	I _{AS}
					T _J = +25°C at I _{D2}	T _J = +150°C at I _{D2}		
	<u>V dc</u>	<u>V dc</u>		<u>μA dc</u>	<u>ohm</u>	<u>ohm</u>	<u>mJ</u>	<u>A</u>
		Min	Max					
2N7523D4, T1	-30	-2.0	-4.0	-10	0.014	0.016	1250	-45
2N7523U2, U2L, U2S, U2A	-30	-2.0	-4.0	-10	0.013	0.015	1116	-56
2N7524D4, T1	-60	-2.0	-4.0	-10	0.018	0.027	890	-45
2N7524U2, U2L, U2S, U2A	-60	-2.0	-4.0	-10	0.016	0.026	725	-56

- (1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTXV" and "JANS".

1.5.2 JAN brand and quality level designators for unencapsulated devices (die). See 6.7 for unencapsulated devices.

1.5.3 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest for JANTXV and JANS quality levels are as follows: "R" and "F".

1.5.4 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.4.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

1.5.4.2 Second number symbols. The second number symbols for the transistor covered by this specification sheet are as follows: "7523" and "7524".

1.5.4.3 Suffix letters. The suffix letters "T1" are used on devices that are packaged in the TO-254AA package of figure 1. The suffix letters "U2" are used on devices that are packaged in the SMD2 TO-276AC package of figure 2. The suffix letters "D4" are used on devices that are packaged in the tab-less TO-254AA package of figure 3. The suffix letters "U2L" are used on devices that are packaged in the SMD2 TO-276AC package and have additional flat leads added, see figure 4. The suffix letters "U2S" are used on devices that are packaged in the SMD2 TO-276AC package mounted to a carrier board, see figure 5. The suffix letters "U2A" are used on devices that are packaged in the surface mount package of figure 6.

1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QML 19500.

* 1.6 Radiation features:

Maximum total ionizing dose (TID) available (Dose rate = 50-300 rad(Si)/s):

For device types 2N7523T1, 2N7523U2, 2N7523U2A, : 300 krad_s(Si) 1/
2N7524D4, 2N7524T1, 2N7524U2, and 2N7524U2A : 300 krad_s(Si) 1/

Heavy Ion Single Event Effect (SEE) SEB and SEGR test:

For device type 2N7523 (D4, T1, U2, U2A, U2L, U2S):

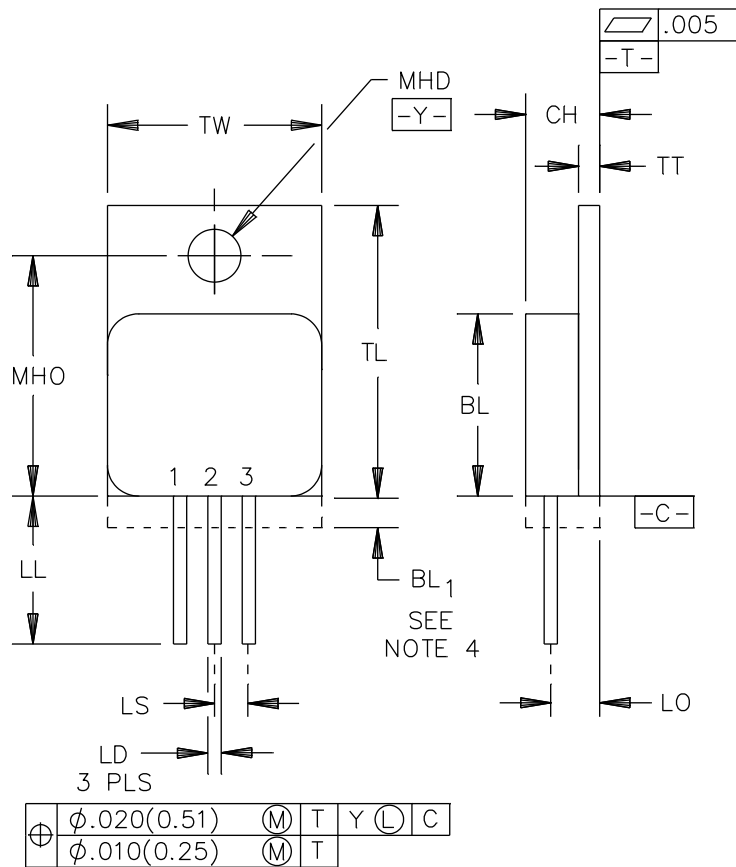
No SEB and SEGR were observed at surface LET (see table V) ≤ 85 MeV·cm²/mg 2/
(In-situ Bias V_{DS} = -30 V and V_{GS} = 10 V)
(In-situ Bias V_{DS} = -25 V and V_{GS} = 15 V)

For device type 2N7524 (D4, T1, U2, U2A, U2L, U2S):

No SEB and SEGR were observed at surface LET (see table V) ≤ 84 MeV·cm²/mg 2/
(In-situ Bias V_{DS} = -60 V and V_{GS} = 10 V)

1/ Manufacturer supplying device types 2N7523 and 2N7524 has performed characterization testing in accordance with MIL-STD-750, method 1019, condition A (dose rate = 50 - 300 rad(Si)/s). The radiation end point limits are guaranteed only for the conditions as specified in MIL-STD-750, method 1019, condition A to a maximum total ionizing dose level of 300 krad_s(Si).

2/ Manufacturer also performed heavy ion SEB and SEGR test at Brookhaven National Lab Accelerator for the MOSFET technology devices in accordance with TM1080 of MIL-STD-750. Limits are characterized at initial qualification and after any design or process changes which may affect the SEE (SEB/SEGR) characteristics. For more information on SEE (SEB/SEGR) test results, customers are requested to contact the manufacturer.



Ltr.	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.535	.545	13.59	13.84
BL ₁		.033		0.84
CH	.249	.260	6.32	6.60
LD	.035	.045	0.89	1.14
LL	.510	.570	12.95	14.48
LO	.150 BSC		3.81 BSC	
LS	.150 BSC		3.81 BSC	
MHD	.139	.149	3.53	3.79
MHO	.665	.685	16.89	17.40
TL	.790	.800	20.07	20.32
TT	.040	.050	1.02	1.27
TW	.535	.545	13.59	13.84
Term 1	Drain			
Term 2	Source			
Term 3	Gate			

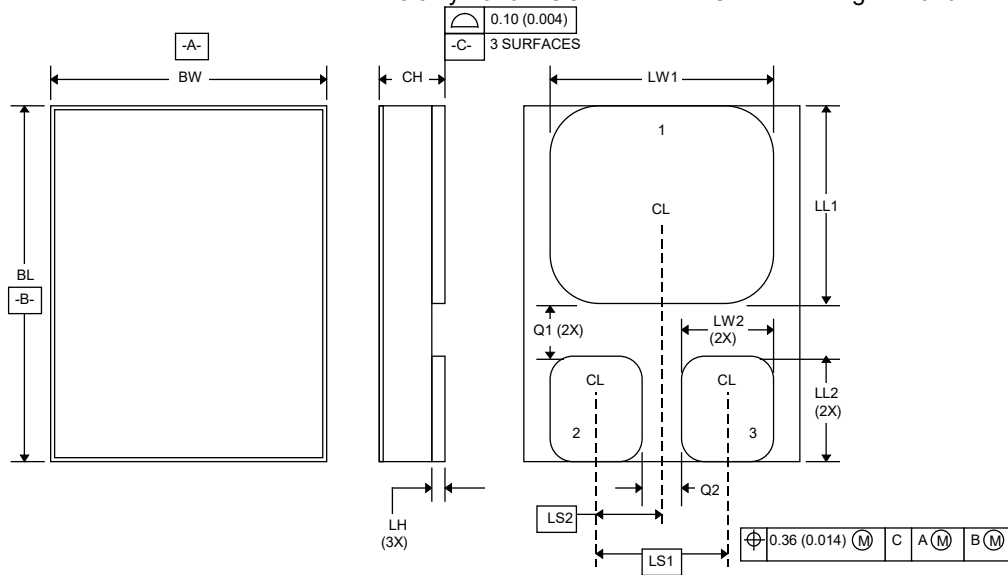
* NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
4. This area is for the lead feed-thru eyelets (configuration is optional, but will not extend beyond this zone).

* 5. In accordance with ASME Y14.5, diameters are equivalent to ϕ symbology.

FIGURE 1. Physical dimensions for TO-254AA (2N7523T1 and 2N7524T1).

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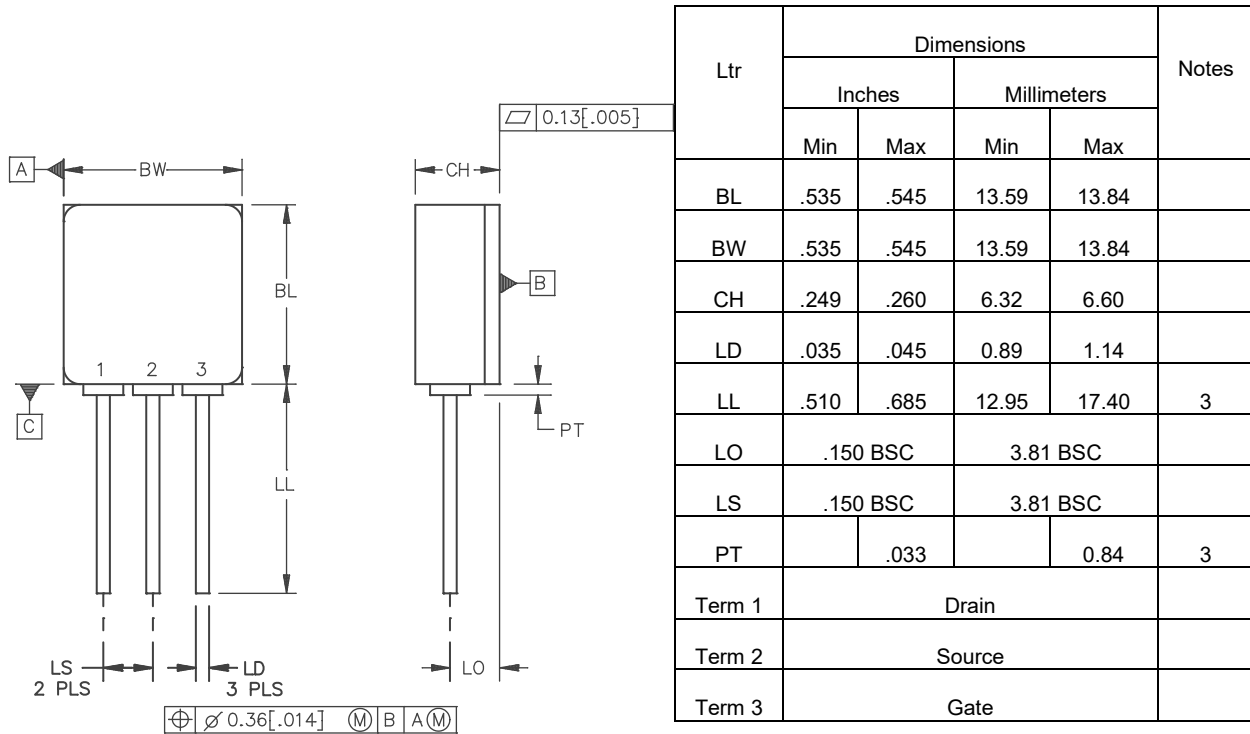
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.685	.695	17.40	17.65
BW	.520	.530	13.21	13.46
CH		.142		3.61
LH	.010	.020	0.25	0.51
LW1	.435	.445	11.05	11.30
LW2	.135	.145	3.43	3.68
LL1	.470	.480	11.94	12.19
LL2	.152	.162	3.86	4.12
LS1	.240 BSC		6.10 BSC	
LS2	.120 BSC		3.05 BSC	
Q1	.035		0.89	
Q2	.050		1.27	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

* NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.

* 4. In accordance with ASME Y14.5, diameters are equivalent to ϕ symbolology.

FIGURE 2. Physical dimensions for SMD2 TO-276AC (2N7523U2 and 2N7524U2).

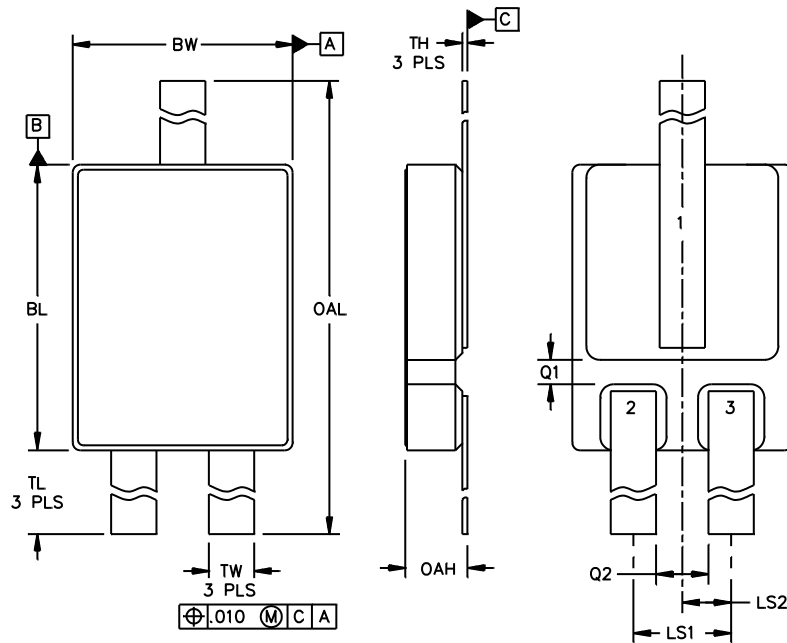


* NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness (PT) of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.

* 5. In accordance with ASME Y14.5, diameters are equivalent to ϕ x symbology.

FIGURE 3. Physical dimensions for TO-254AA tab-less package (2N7523D4 and 2N7524D4).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.685	.695	17.40	17.65
BW	.520	.530	13.21	13.46
LS1	.240 BSC		6.10 BSC	
LS2	.120 BSC		3.05 BSC	
Q1	.035		0.89	
Q2	.050		1.27	
TH	.005	.007	0.127	0.177
TL	.650	.675	16.52	17.14
TW	.095	.105	2.42	2.66
OAH		.150		3.81
OAL	1.985	2.045	50.42	51.94
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

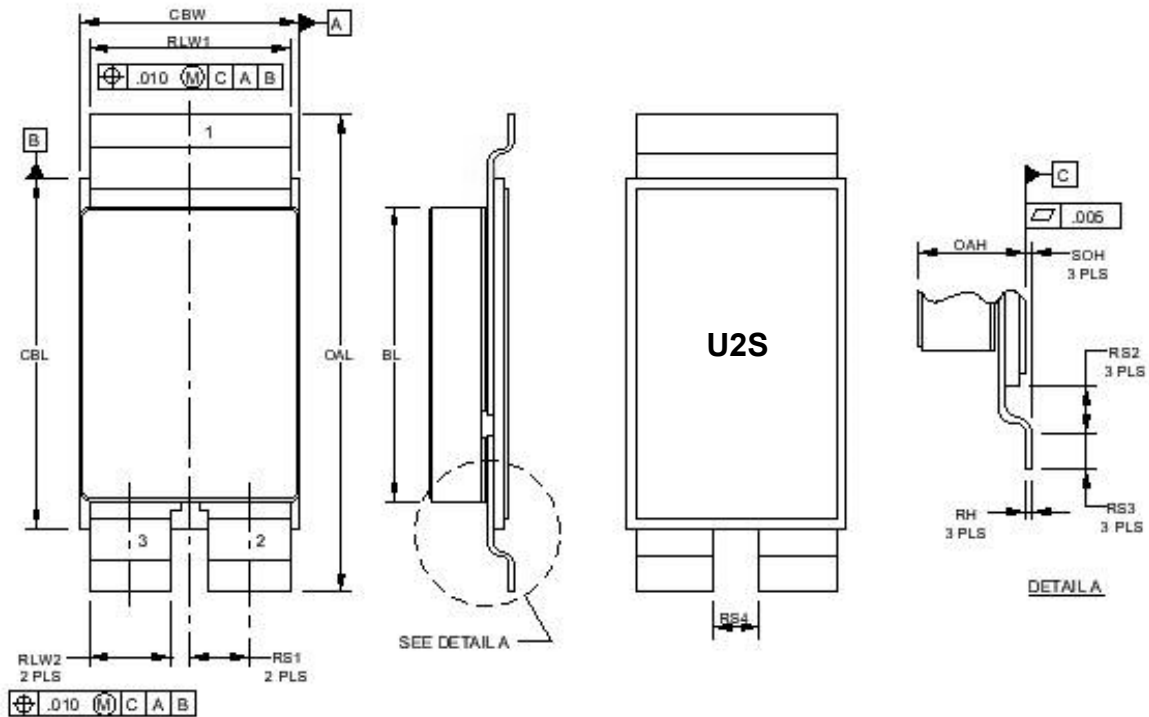
* NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.

* 4. In accordance with ASME Y14.5, diameters are equivalent to ϕ symbolology.

FIGURE 4. Physical dimensions, U2 with leaded option (U2L).

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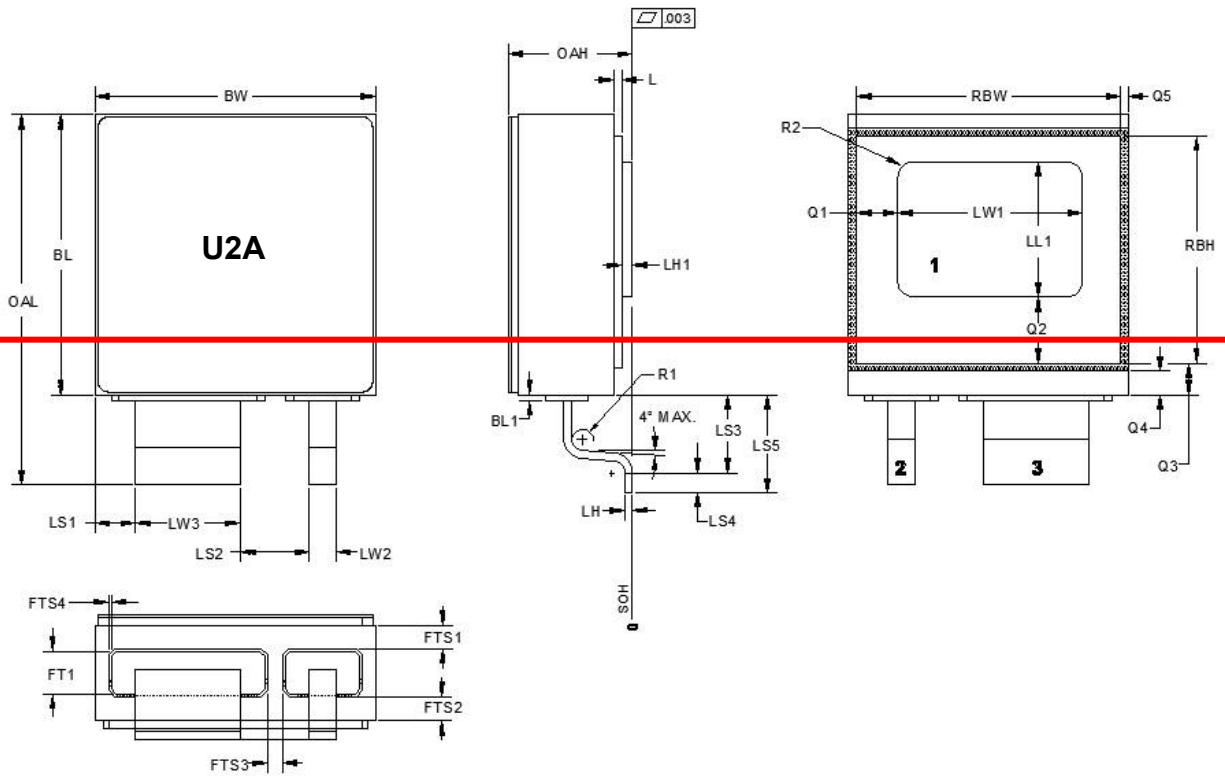
* NOTES:

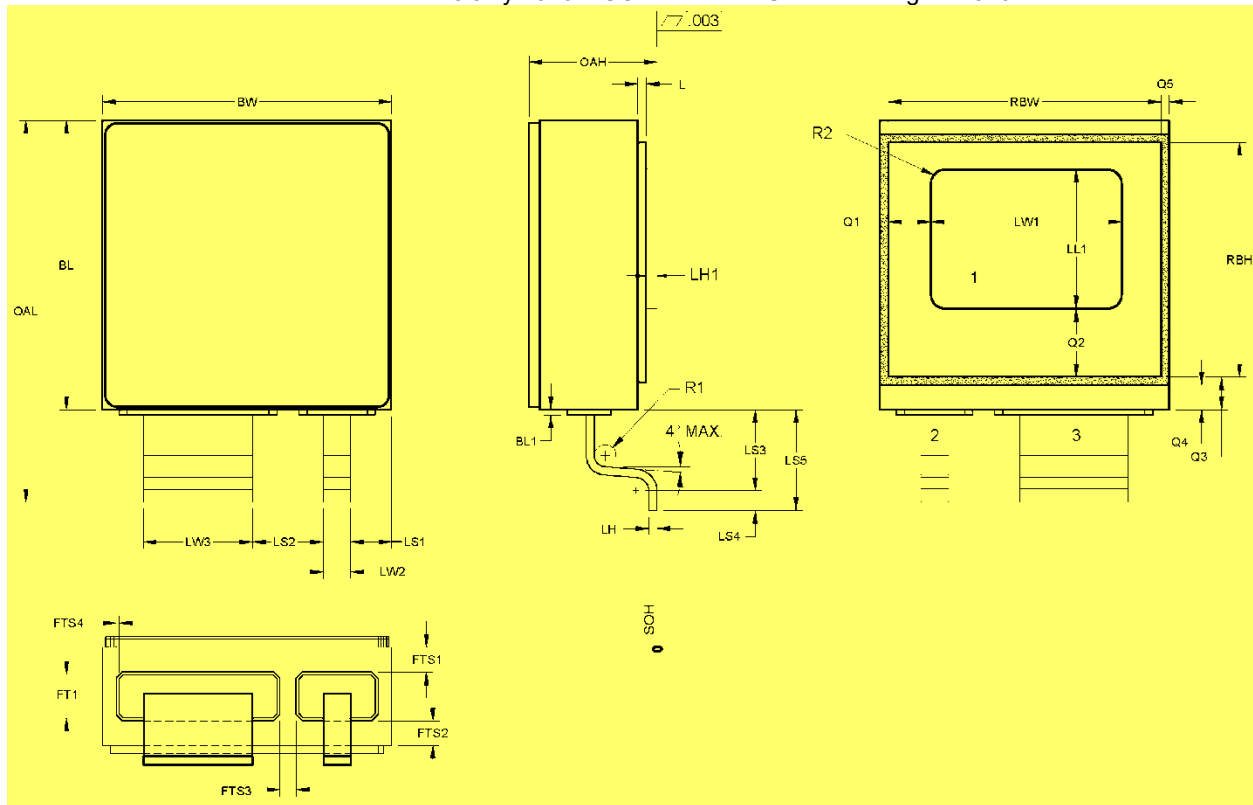
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.

* 4. In accordance with ASME Y14.5, diameters are equivalent to $\varnothing$ symbology.

* FIGURE 5. Physical dimensions, U2 with carrier board option (U2S).

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FIGURE 6. Physical dimensions, U2A surface mount.

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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.524	.536	13.31	13.61
BL1	.005	.015	0.13	0.38
BW	.524	.536	13.31	13.61
FT1	.075	.085	1.91	2.16
FTS1	.036		0.91	
FTS2	.036		0.91	
FTS3	.030		0.76	
FTS4	.005 TYP		0.127 TYP	
L	.013	.017	0.33	0.43
LH	.013	.017	0.33	0.43
LH1	.02	.024	0.51	0.61
LL1	.25	.26	6.35	6.60
LS1	.07	.08	1.78	2.03
LS2	.125	.135	3.18	3.43
LS3	~~.125~~ .130	~~.145~~ .140	~~3.18~~ 3.30	~~3.68~~ 3.56
LS4	.040	.050	1.02	1.27
LS5	.170	.190	4.32	4.83
LW1	.345	.355	8.76	9.02
LW2	.045	.055	1.14	1.4
LW3	.195	.205	4.95	5.21
OAH		.26		6.60
OAL	.71 TYP		18.03 TYP	
Q1	.073	.083	1.85	2.11
Q2	.12	.13	3.05	3.30
Q3	.055	.065	1.40	1.65
Q4	.04		1.02	
Q5	.010	.020	.25	.51
RBH	.425	.435	10.8	11.05
RBW	.495	.505	12.57	12.83
R1	.02		0.51	
R2	.025	.035	0.635	0.889
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.

*

FIGURE 6. Physical dimensions, U2A surface mount – continued.

* 2. APPLICABLE DOCUMENTS PUBLICATIONS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.
MIL-STD-883 - Test Method Standard Microcircuits

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1 (T1, TO-254AA), 2 (U2, surface mount TO-276AC), 3 (D4, tabless TO-254AA), 4 (U2L, surface mount TO-276AC with additional flat leads added), 5 (U2S, surface mount TO-276AC with additional flat leads added and mounted to a carrier board) herein, and 6 (U2A surface mount) herein.

3.4.1 Lead formation and finish. Lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500 and herein. Where a choice of finish is desired, it shall be specified in the acquisition document (see 6.2). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of MIL-PRF-19500 and 100 percent dc testing in accordance with table I, subgroup 2 herein.

3.4.2 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

3.4.3 Lead attach or carrier package. Alternations to the device shall be performed on devices that have passed all screening and QCI required per MIL-PRF-19500 and listed herein. When leads or carrier attach is added to the U2 package, as a minimum, the vendor shall perform the tests specified in 4.3.6 herein.

* 3.4.4 Silicone die coat. The use of a silicone die coat requires a successful completion of method 5011 of MIL-STD-883, method 5011 on each lot of silicone die coating lot for its intended applications, and as part of the full MIL-PRF-19500 qualification process.

3.5 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of MIL-PRF-19500 to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq$ or 100 k Ω , whenever bias voltage is applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container. Devices that have been altered with lead or carrier attached per the specification herein shall have the altered part number on the device or on the device packaging.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and table I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III (or table IV, as applicable) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.1.1 Single event effects (SEE). SEE (SEB/SEGR) shall be performed in accordance with TM1080 of MIL-STD-750 at initial qualification and after process or design changes which may affect radiation hardness (see table III and table V). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with table II. SEE (SEB/SEGR) characterization data shall be made available upon request of the qualifying or acquiring activity.

4.2.1.2 Lead or carrier attach. For devices that include a lead or carrier attach package configuration qualification shall be performed in accordance with table IV herein, at initial qualification and after process or design changes.

* 4.2.2 Silicone die coating. When silicone die coating is used, method 5011 of MIL-STD-883 shall be performed on that coating in the full MIL-PRF-19500 qualification process.

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4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurements for JANS level	Measurements for JANTXV level
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.4)	Not applicable
9	Subgroup 2 of table I herein; I _{GSSF1} , I _{GSSR1} , I _{DSS1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein; I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(on)1} , V _{GS(TH)1} ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein; I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(on)1} , V _{GS(TH)1}
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein; ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(on)1} = ±20 percent of initial value. ΔV _{GS(TH)1} = ±20 percent of initial value.	Subgroup 2 of table I herein; ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(on)1} = ±20 percent of initial value. ΔV _{GS(TH)1} = ±20 percent of initial value.
17	For TO-254 packages: Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein	For TO-254 packages: Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein

- (1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, V_{GS(th)1}, and r_{DS(on)1} shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV levels do not need to be repeated in screening requirements.

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4.3.1 Gate stress test. Apply $V_{GS} = 24 \text{ V}$, minimum for $t = 250 \mu\text{s}$, minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current $I_{AS} = I_{D1}$.
- b. Inductance $L = \left[\frac{2E_{AS}}{(I_{D1})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right] \text{ mH minimum.}$
- c. Gate to source resistor R_{GS} $25 \Omega \leq R_{GS} \leq 200 \Omega$.
- d. Supply voltage $V_{DD} \leq 30 \text{ V dc.}$
- e. Initial case temperature..... $T_C = +25^\circ\text{C}, -5^\circ\text{C}, +10^\circ\text{C}.$
- f. Gate voltage $V_{GS} = 12 \text{ V dc.}$
- g. Number of pulses to be applied 1 pulse minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). See [table III](#), group E, subgroup 4 herein.

4.3.4 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and be evaluated for root cause and lot integrity.

4.3.5 Dielectric withstanding voltage.

- a. Magnitude of test voltage..... 900 V dc.
- b. Duration of application of test voltage 15 seconds (min).
- c. Points of application of test voltage All leads to case (bunch connection).
- d. Method of connection..... Mechanical.
- e. Kilovolt-ampere rating of high voltage source 1,200 V/1.0 mA (min).
- f. Maximum leakage current..... 1.0 mA.
- g. Voltage ramp up time..... 500 V/second.

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4.3.6 Lead or carrier attach screening (All quality levels). All surface mount devices with added leads or carrier boards shall be screened as specified herein.

Screen	MIL-STD-750	
	Method	Conditions
1. Hermetic seal <u>1/</u> a. Fine leak b. Gross leak	1071	
2. Thermal response (see 4.3.3) A2 dc electrical <u>2/</u> <u>3/</u>	3161	Read and record.
3. Radiography	2076	The solder material coverage at the package lead pad/SMD carrier sub interfaces shall be 85% minimum
4. External visual examination	2071	Cracks or separation of materials shall not be evident on any device after the SMD lead attach assembly operation. Pad and Isolation areas shall be free from foreign matter and extraneous solder. Solder fillet coverage at the lead/package lead pad interfaces, along all visible sides, minimum of 75% solder fillet coverage.
5a. Physical dimensions	2066	6 piece sample, each device shall meet the requirements specified in figure 4 and 5 .
5b. Terminal strength	2036	3 piece sample.

1/ Evaluation of surface sorption in accordance with method 1071 shall be performed.

2/ Only DC electrical test specified herein.

3/ When lead carrier bend is requested, the electrical test is performed prior to the bend process

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#) and [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of [MIL-PRF-19500](#), and as follows.

4.4.2.1 Quality level JANS, table E-VIA of [MIL-PRF-19500](#).

Subgroup	Method	Condition
B3	1051	Test condition G, 100 cycles.
B3	2077	Scanning electron microscope (SEM) qualification may be performed anytime prior to lot formation.
B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
B4	1042	Condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} = \text{rated}$; $T_A = +175^\circ\text{C}$, $t = 24$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 48$ hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} = \text{rated}$; $T_A = +175^\circ\text{C}$, $t = 120$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 240$ hours minimum.

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4.4.2.2 Quality level JANTXV, table E-VIB of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition A; weight = 10 pounds; $t = 15$ s. (Not applicable to U2, U2L, U2S).
C3	2052	PIND, required if not performed in screening. (22 devices, $c = 0$ for large lots, 12 devices, $c = 0$ for small lots).
C5	3161	Thermal resistance, see 4.3.3 , $R_{\theta JC(max)} = 0.60$ °C/W (T1, D4) or 0.50 °C/W (U2, U2A), or 1.50 °C/W (U2L, U2S).
C6	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of [MIL-PRF-19500](#) and [table II](#) herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table III](#) herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source	3407	$V_{GS} = 0$ V dc, $I_D = -1$ mA dc, bias condition C	$V_{(BR)DSS}$	-30		V dc
2N7523D4, T1, U2, U2L, U2S, U2A				-60		V dc
2N7524D4, T1, U2, U2L, U2S, U2A						
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = -1$ mA dc	$V_{GS(TH)1}$	-2.0	-4.0	V dc
Gate reverse current	3411	$V_{GS} = +20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSF1}		+100	nA dc
Gate reverse current	3411	$V_{GS} = -20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSR1}		-100	nA dc
Drain current	3413	$V_{GS} = 0$ V dc, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS1}		-10	μA dc
Static drain to source on-state resistance	3421	$V_{GS} = -12$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)1}$			
2N7523D4, T1					0.014	Ω
2N7523U2, U2, U2L, U2S, U2A					0.013	Ω
2N7524D4, T1					0.018	Ω
2N7524U2, U2, U2L, U2S, U2A					0.016	Ω
Forward voltage	4011	Condition A, $I_D = I_{D1}$, $V_{GS} = 0$ V dc	V_{SD}		-5.0	V
<u>Subgroup 3</u>						
High-temperature operation:		$T_C = T_J = +125^\circ\text{C}$				
Gate reverse current	3411	$V_{GS} = -20$ V dc and $+20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSS2}		±200	nA dc
Drain current	3413	$V_{GS} = 0$ V dc, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS2}		-25	μA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits	Limits	Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - continued						
High-temperature operation:		T _C = T _J = +125°C				
Static drain to source on-state resistance	3421	V _{GS} = -12 V dc, condition A, pulsed (see 4.5.1), I _D = I _{D2}	r _{DS(on)3}		0.015 0.014	Ω Ω
2N7523D4, T1 2N7523U2, U2, U2L, U2S, U2A 2N7524D4, T1 2N7524U2, U2, U2L, U2S, U2A					0.026 0.024	Ω Ω
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS} , I _D = -1 mA dc	V _{GS(th)2}	-1.0		V dc
Low-temperature operation:		T _C = T _J = -55°C				
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS} , I _D = -1 mA dc	V _{GS(th)3}		-5.0	V dc
<u>Subgroup 4</u>						
Forward transconductance	3475	I _D = rated I _{D2} , V _{DD} = -15 V (see 4.5.1)	g _{FS}			
2N7523D4, T1 & 2N7524D4, T1				39		S
2N7523U2, U2, U2L, U2S & 2N7524U2, U2, U2L, U2S, U2A				40		S
Switching time test	3472	I _D = rated I _{D1} , V _{GS} = -12 V dc, R _G = 2.35 Ω (U2), V _{DD} = 50 percent of rated V _{DS}				
Turn-on delay time			t _{d(on)}		35	ns
Rise time			t _r		175	ns
2N7523D4, T1, U2, U2L, U2S, U2A 2N7524D4, T1, U2, U2L, U2S, U2A					150	ns
Turn-off delay time			t _{d(off)}		100	ns
Fall time			t _f		80	ns
2N7523D4, T1, U2, U2L, U2S, U2A 2N7524D4, T1, U2, U2L, U2S, U2A					35	ns

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 9 ; $t_p = 10$ ms, $V_{DS} = 80$ percent of rated V_{DS}				
Electrical measurements		See table I , subgroup 2 herein.				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B	$Q_{G(on)}$			
2N7523D4, T1					160	nC
2N7523, U2, U2L, U2S, U2A					240	nC
2N7524D4, T1					160	nC
2N7524, U2, U2L, U2S, U2A					200	nC
On-state gate charge			Q_{GS}			
2N7523D4, T1					60	nC
2N7523U2, U2A					60	nC
2N7524D4, T1					60	nC
2N7524U2, U2A					65	nC
Gate to drain charge			Q_{GD}			
2N7523D4, T1					65	nC
2N7523, U2, U2L, U2S, U2A					55	nC
2N7524D4, T1					65	nC
2N7524, U2, U2L, U2S, U2A					60	nC
Reverse recovery time	3473	$di/dt \leq 100A/\mu s$, $I_D = I_{D1}$, $V_{DD} \leq \text{Rated } V_{DS}$	t_{rr}			
2N7523D4, T1					150	ns
2N7523, U2, U2L, U2S, U2A					140	ns
2N7524D4, T1					110	ns
2N7524, U2, U2L, U2S, U2A					200	ns

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

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TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-Irradiation limits		Post-Irradiation limits		Post-Irradiation limits		Unit
	Method	Conditions		R, F		R		F		
				Min	Max	Min	Max	Min	Max	
<u>Subgroup 1</u> Not applicable										
<u>Subgroup 2</u>		T _C = +25°C								
Steady-state total dose irradiation (V _{GS} bias) 4/	1019	Condition A, V _{GS} = -12V V _{DS} = 0								
Steady-state total dose irradiation (V _{DS} bias) 4/	1019	Condition A, V _{GS} = 0 V _{DS} = 80 percent of rated V _{DS} (pre-irradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	V _{GS} = 0 I _D = -1 mA bias cond. C	V _{(BR)DSS}							
2N7523D4, T1, U2, U2L, U2S, U2A				-30		-30		-30		V dc
2N7524D4, T1, U2, U2L, U2S, U2A				-60		-60		-60		V dc
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS}	V _{GS(th)1}							
2N7523D4, T1, U2, U2L, U2S, U2A				-2.0	-4.0	-2.0	-4.0	-2.0	-4.0	V dc
2N7524D4, T1, U2, U2L, U2S, U2A				-2.0	-4.0	-2.0	-4.0	-2.0	-5.0	V dc
Gate reverse current	3411	V _{GS} = -20 V V _{DS} = 0 bias cond. C	I _{GSSR1}		-100		-100		-100	nA dc
Gate forward current	3411	V _{GS} = 20 V V _{DS} = 0 bias cond. C	I _{GSSF1}		100		100		100	nA dc
Drain current	3413	V _{GS} = 0 bias cond. C V _{DS} = 80 percent of rated V _{DS} (pre-irradiation)	I _{DSS1}		-10		-10		-10	µA dc

See footnotes at end of table.

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TABLE II. Group D inspection - Continued.

Inspection <u>1/</u> <u>2/</u> <u>3/</u>	MIL-STD-750		Symbol	Pre-Irradiation limits		Post-Irradiation limits		Post-Irradiation limits		Unit
	Method	Conditions		R, F		R		F		
				Min	Max	Min	Max	Min	Max	
Static drain to source on-state voltage 2N7523D4, T1 2N7523U2, U2L, U2S, U2A 2N7524D4, T1 2N7524U2, U2L, U2S, U2A	3405	V _{GS} = -12 V cond. A pulsed (see 4.5.1) I _D = I _{D2}	V _{DS(on)1}		0.630 0.784 0.765 0.952		0.630 0.784 0.765 0.952		0.630 0.784 0.765 0.952	V dc V dc V dc V dc
Forward voltage source to drain diode	4011	V _{GS} = 0, cond. A, I _D = I _{D1}	V _{SD}		-5.0		-5.0		-5.0	V dc

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in it's qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

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TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles.	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady state reverse bias	1042	Test condition A; 1,000 hours.	
Electrical measurements		See table I , subgroup 2.	
Steady-state gate bias	1042	Test condition B; 1,000 hours.	
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	
<u>Subgroup 11</u>			3 devices
SEE 2/ 3/	1080	See method 1080 of MIL-STD-750 .	

[1/](#) A separate sample for each test shall be pulled.

[2/](#) Group E qualification of testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

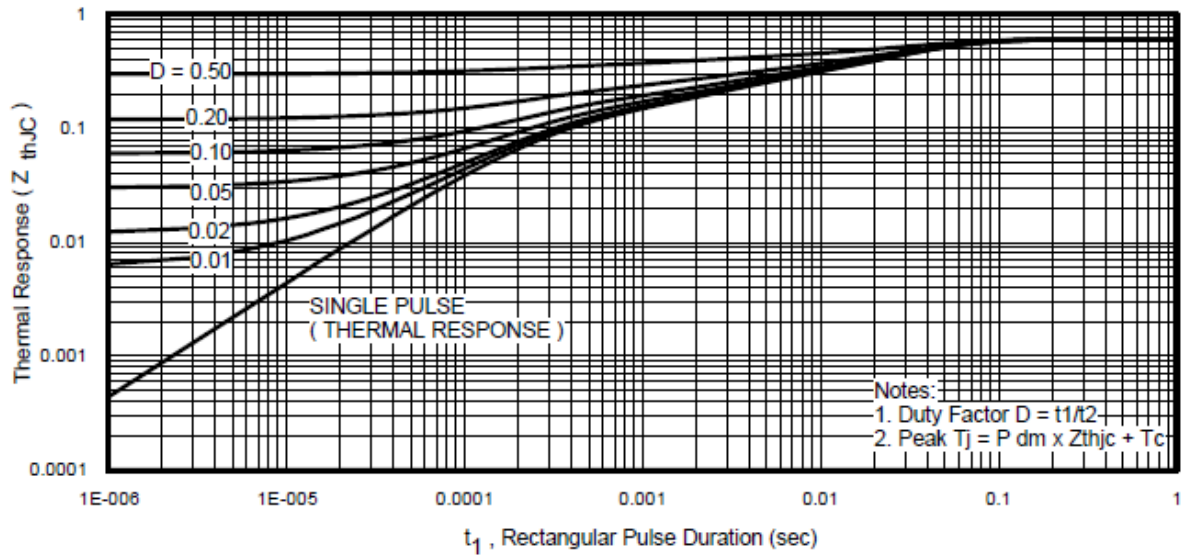
[3/](#) The sampling plan applies to each bias condition.

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TABLE IV. Lead alternation qualification inspection requirements.

Inspections <u>1/</u>	MIL-STD-750		Sample size
	Method	Conditions	
<u>Subgroup 1</u>			6 devices, c = 0
Temperature cycle	1051	100 Temp cycles, test condition G or maximum storage temperature.	
Hermetic seal Fine leak Gross leak	1071		
A2 dc electrical		Read and record.	
Thermal response	3161		
External visual examination	2071	Cracks or separation of materials shall not be evident on test samples.	
<u>Subgroup 2</u>			6 devices, c = 0
Intermittent operating life	1042	Condition D; 6,000 cycles.	
A2 dc electrical		Read and record.	
Thermal response	3161		
External visual examination	2071	Cracks or separation of materials shall not be evident on test samples.	
<u>Subgroup 3</u>			6 devices, c = 0
Terminal strength	2036	Tension; Condition A 10lbs for 10 seconds Fatigue; Condition E 3 arcs of 90 +/-5 degrees each 8.0 oz.	
A2 dc electrical		Read and record.	
External visual examination	2071	Cracks or separation of materials shall not be evident on test samples.	

1/ Qualification samples performed on non-formed leaded devices.



2N7523D4, T1 and 2N7524D4, T1

2N7523U2, U2A, and 2N7524U2, U2A

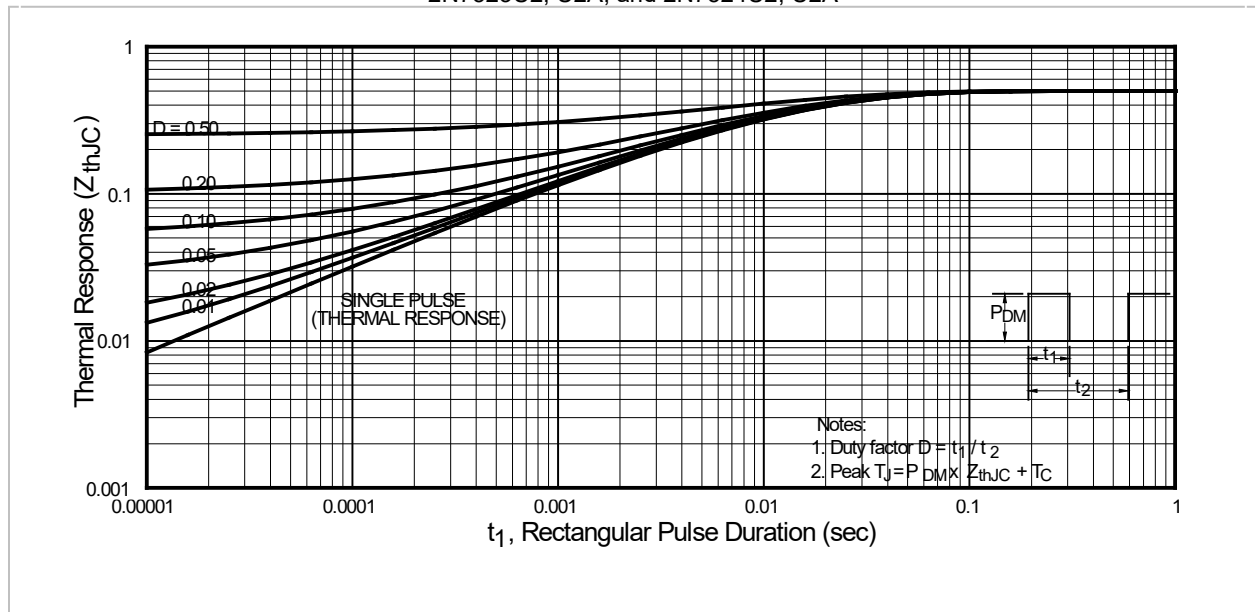


FIGURE 7. Thermal impedance curves.

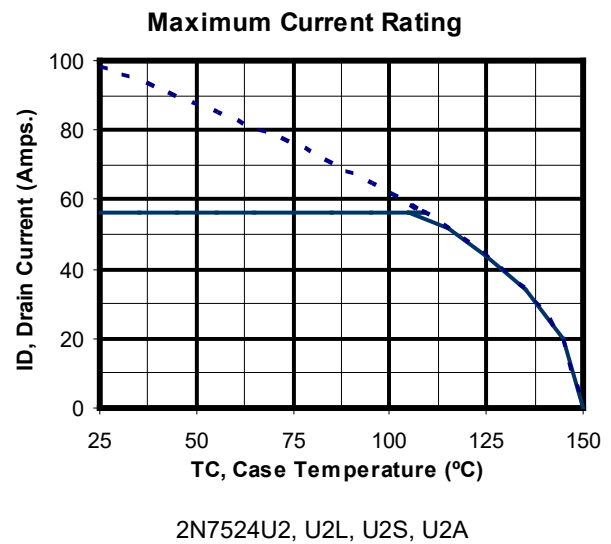
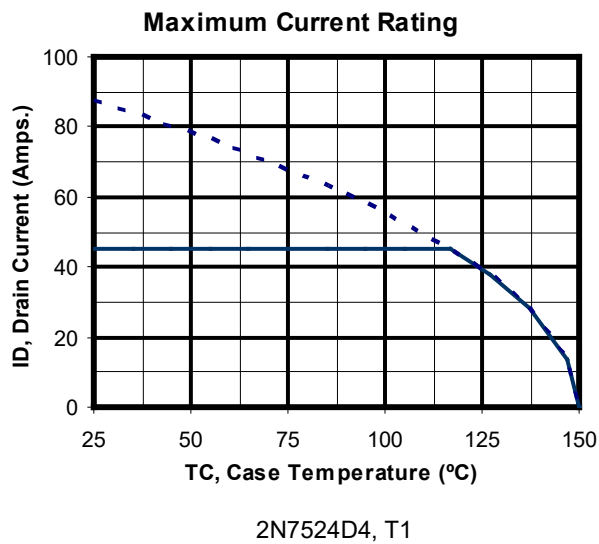
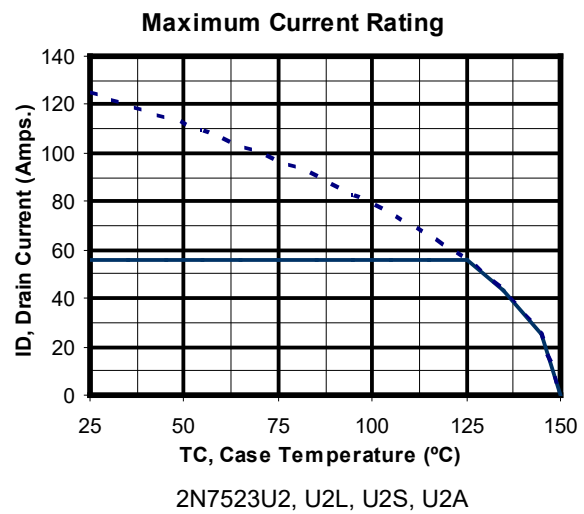
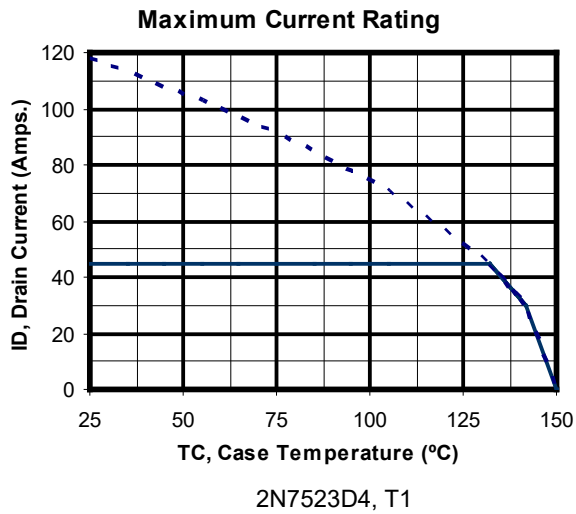


FIGURE 8. Maximum drain current vs case temperature graphs.

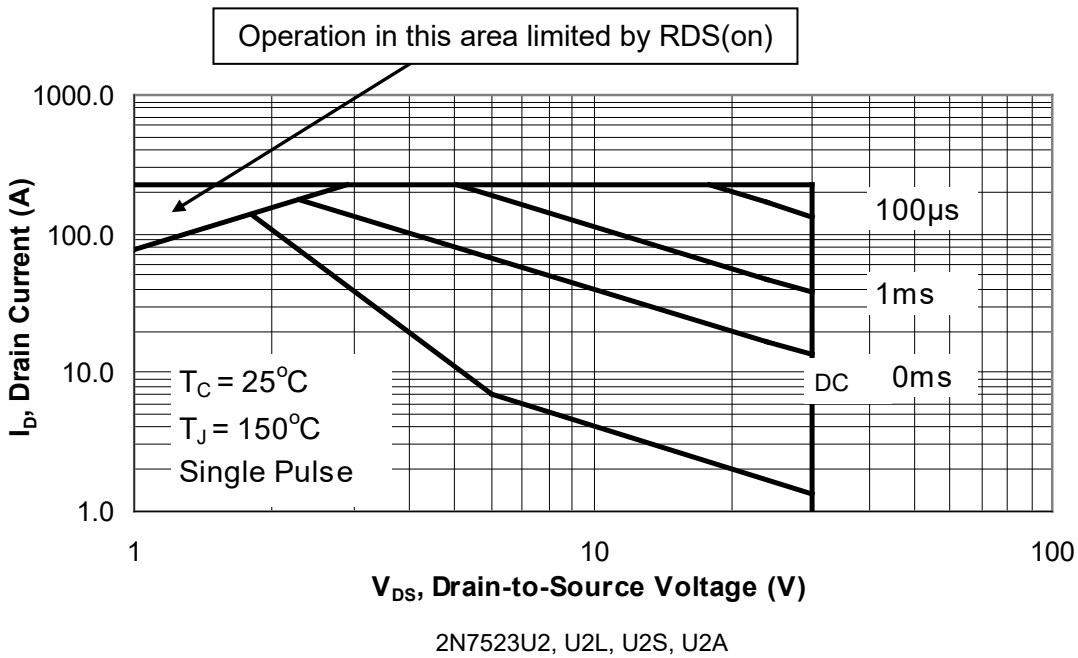
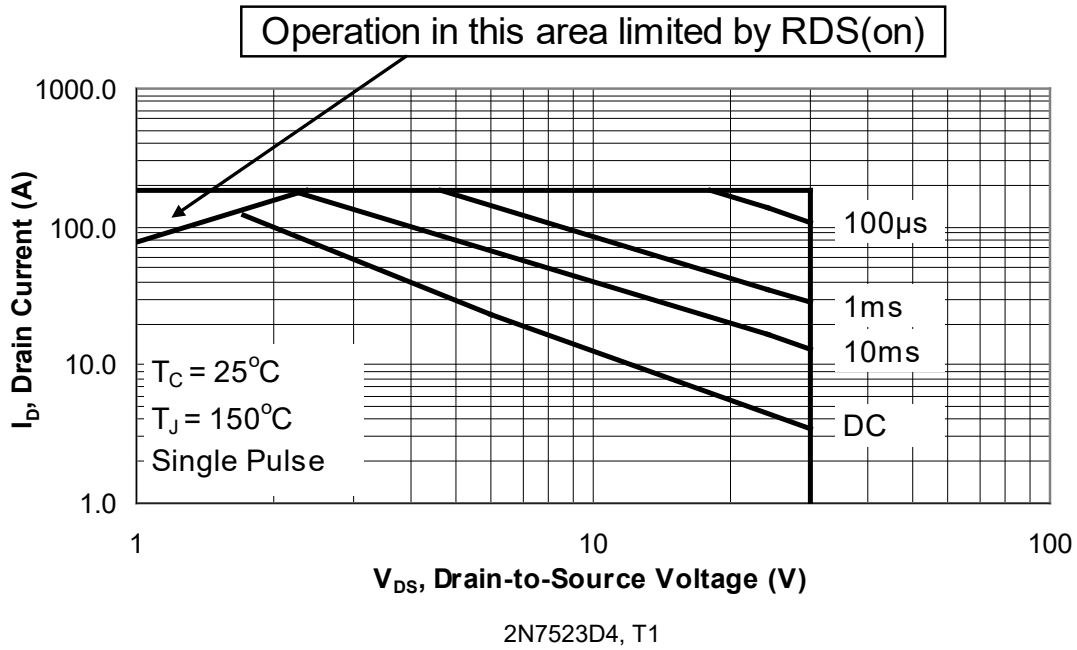
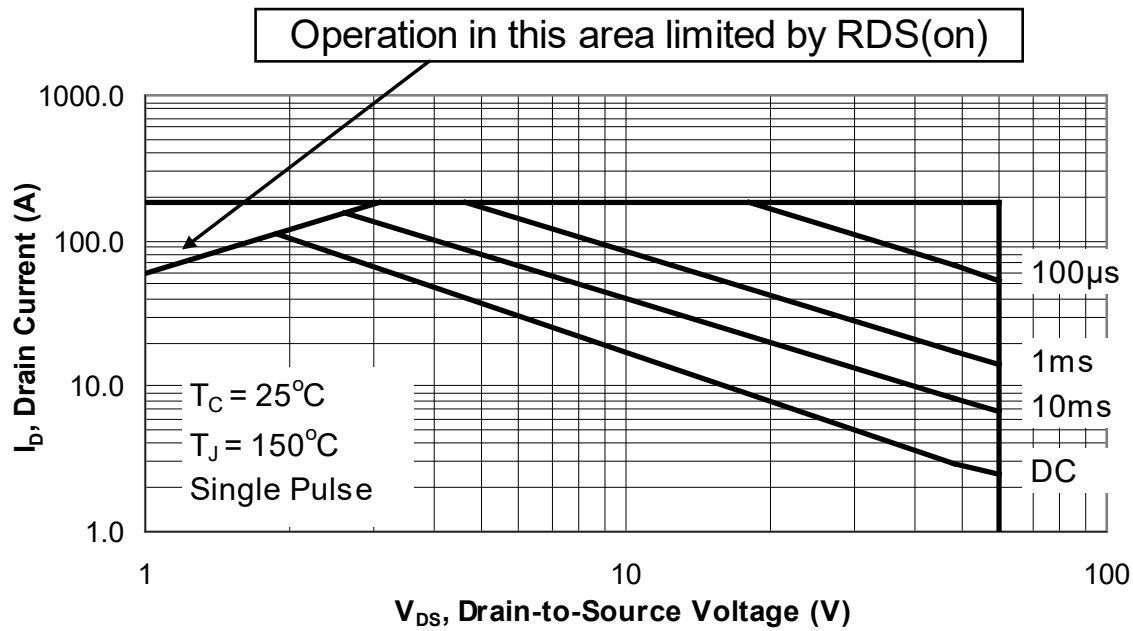
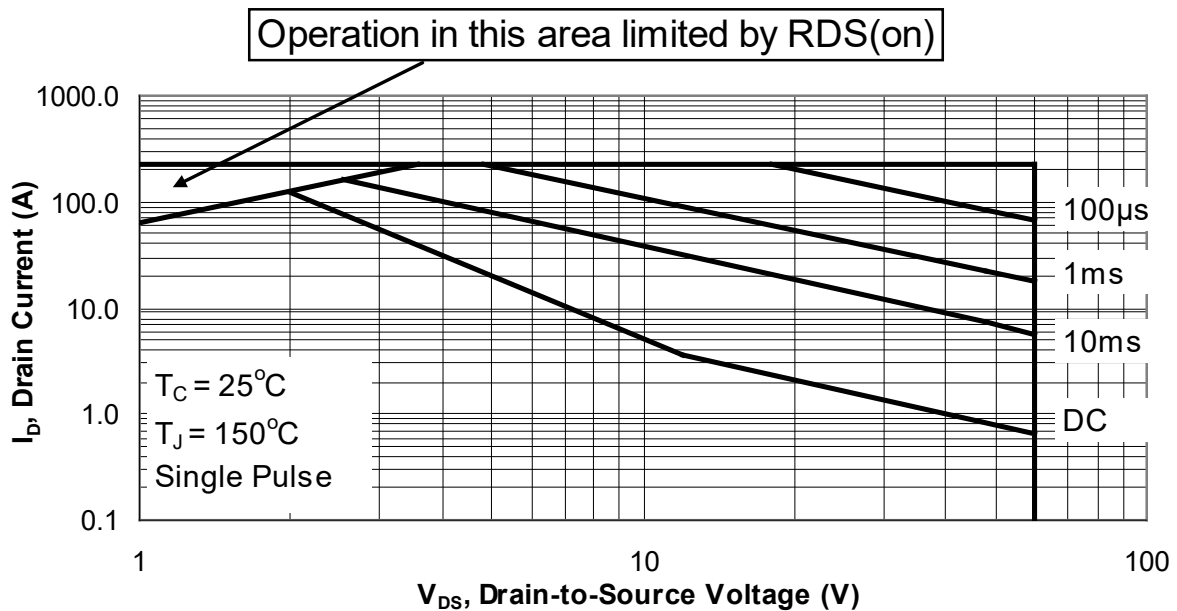


FIGURE 9. Safe operating area graphs.



2N7524D4, T1



2N7524U2, U2L, U2S, U2A

FIGURE 9. Safe operating area graphs - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

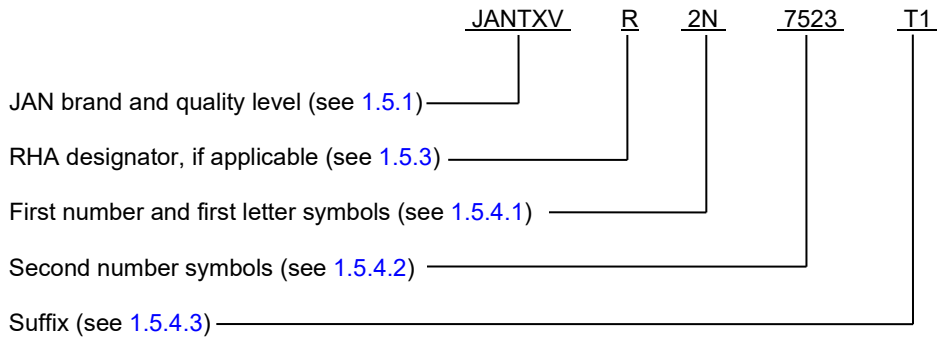
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead formation and finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.5.
- e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.
- f. If specific SEE characterization conditions are desired (see section 6.8 and table V), manufacturer's cage code should be specified in the contract or order.
- g. If SEE testing data is desired, it should be specified in the contract or order.
- h. If the leaded or carrier board configuration is desired for U2 devices (see 3.4.3), it should be specified in the contract. For acquisition of U2 devices, the default configuration is delivered without the carrier board.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime Weapons Support, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7523D4	JANTXV#2N7523D4	JANS2N7523D4	JANS#2N7523D4
JANTXV2N7523T1	JANTXV#2N7523T1	JANS2N7523T1	JANS#2N7523T1
JANTXV2N7523U2	JANTXV#2N7523U2	JANS2N7523U2	JANS#2N7523U2
JANTXV2N7523U2L	JANTXV#2N7523U2L	JANS2N7523U2L	JANS#2N7523U2L
JANTXV2N7523U2S	JANTXV#2N7523U2S	JANS2N7523U2S	JANS#2N7523U2S
JANTXV2N7523U2A	JANTXV#2N7523U2A	JANS2N7523U2A	JANS#2N7523U2A
JANTXV2N7524D4	JANTXV#2N7524D4	JANS2N7524D4	JANS#2N7524D4
JANTXV2N7524T1	JANTXV#2N7524T1	JANS2N7524T1	JANS#2N7524T1
JANTXV2N7524U2	JANTXV#2N7524U2	JANS2N7524U2	JANS#2N7524U2
JANTXV2N7524U2L	JANTXV#2N7524U2L	JANS2N7524U2L	JANS#2N7524U2L
JANTXV2N7524U2S	JANTXV#2N7524U2S	JANS2N7524U2S	JANS#2N7524U2S
JANTXV2N7524U2A	JANTXV#2N7524U2A	JANS2N7524U2A	JANS#2N7524U2A

(1) The number sign (#) represents one of two RHA designators available (R or F).

6.6 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix). Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types (military PIN)	Commercial PIN		
	TO-254AA	TO-276AC (SMD2)	U2A
2N7523T1	IRHMS59_Z60		
2N7523U2		IRHNA59_Z60	
2N7523U2A			IRHNS59_Z60
2N7524T1	IRHMS59_064		
2N7524U2		IRHNA59_064	
2N7524U2			IRHNS59_064

6.7 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet [MIL-PRF-19500/741](#).

6.8 Application data.

* 6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this specification sheet has characterized its devices to the requirements of [MIL-STD-750](#) method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the [MIL-STD-750](#) method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see [table V](#)) for information only. SEE (SEB and SEGR) conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

TABLE V. Manufacturers characterization conditions.

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
* 69210 (Applicable to devices with a date code of September 2009 and older)	SEE 1/	1080.0	See MIL-STD-750 method 1080	3 devices
	Electrical measurements		IGSSF1, IGSSR1, and IDSS1 in accordance with table I , subgroup 2	
	SEE irradiation:		Fluence = 3E5 ±20 percent ions/cm ² , Flux = 2E3 to 2E4 ions/cm ² /sec, Temperature = 25 ±5 °C	
	2N7523D4, T1, 2N7523U2, U2A		Surface LET = 38 MeV-cm ² /mg ±5%, range = 38 µm ±7.5%, energy = 300 MeV ±7.5%	
	2N7524D4, T1, 2N7524U2, U2A		In situ bias conditions: V _{DS} = -30 V and V _{GS} = 20 V (nominal 3.75 MeV/nucleon at Brookhaven National Lab Accelerator) Surface LET = 38 MeV-cm ² /mg ±5%, range = 35 µm ±7.5%, energy = 270 MeV ±7.5%	
	2N7523D4, T1, 2N7523U2, U2A		In situ bias conditions: V _{DS} = -60 V and V _{GS} = 20 V (nominal 3.38 MeV/nucleon at Brookhaven National Lab Accelerator) Surface LET = 62 MeV-cm ² /mg ±5%, range = 33 µm ±7.5%, energy = 355 MeV ±7.5%	
	2N7524D4, T1, 2N7524U2, U2A		In situ bias conditions: V _{DS} = -30 V and V _{GS} = 15 V V _{DS} = -25 V and V _{GS} = 20 V (nominal 2.80 MeV/nucleon at Brookhaven National Lab Accelerator) Surface LET = 61 MeV-cm ² /mg ±5%, range = 30 µm ±7.5%, energy = 330 MeV ±7.5%	
			In situ bias conditions: V _{DS} = -60 V and V _{GS} = 10 V V _{DS} = -45 V and V _{GS} = 15 V V _{DS} = -25 V and V _{GS} = 20 V (nominal 2.60 MeV/nucleon at Brookhaven National Lab Accelerator)	

See footnotes at end of table.

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TABLE V. Manufacturers characterization conditions - Continued.

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
* 69210 (Applicable to devices with a date code of September 2009 and older)	SEE 1/	1080.0	See MIL-STD-750 method 1080	3 devices
	Electrical measurements		IGSSF1, IGSSR1, and IDSS1 in accordance with table I , subgroup 2	
	SEE irradiation:		Fluence = 3E5 ±20 percent ions/cm ² , Flux = 2E3 to 2E4 ions/cm ² /sec, Temperature = 25 ±5 °C	
	2N7523D4, T1, 2N7523U2, U2L, U2S, U2A		Surface LET = 85 MeV-cm ² /mg ±5%, range =29 µm ±7.5%, energy = 380 MeV ±10% In situ bias conditions: V _{DS} = -30 V and V _{GS} = 10 V V _{DS} = -25 V and V _{GS} = 15 V (nominal 1.78 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7524D4, T1, 2N7524U2, U2L, U2S, U2A		Surface LET = 84 MeV-cm ² /mg ±5%, range =28 µm ±7.5%, energy = 350 MeV ±10% In situ bias conditions: V _{DS} = -60 V and V _{GS} = 10 V (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator)	
	Electrical measurements		IGSSF1, IGSSR1, and IDSS1 in accordance with table I , subgroup 2	
Upon qualification, all manufacturers will provide the verification test conditions to be added to this table.				

1/ IGSSF1, IGSSR1, and IDSS1 were examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with [table I](#), subgroup 2, may be performed at the manufacturer's option.

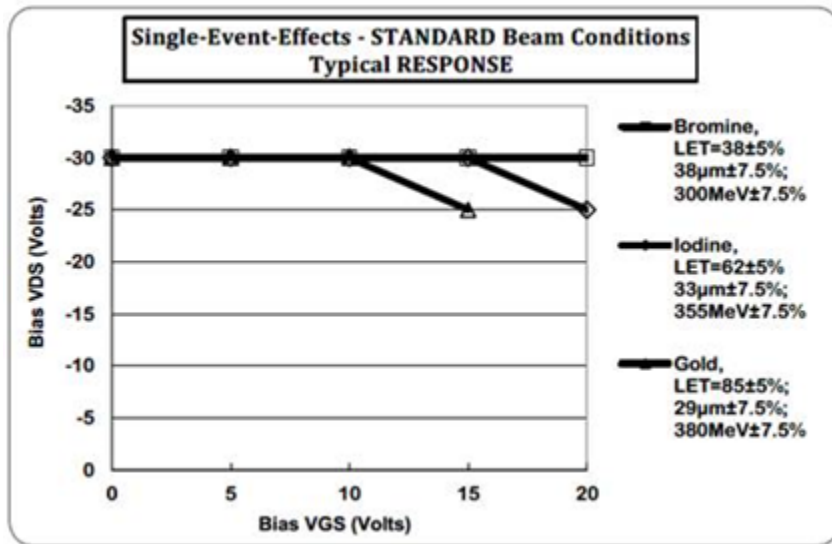


FIGURE 10. Cage 69210 typical SEE response graph, 2N7523.

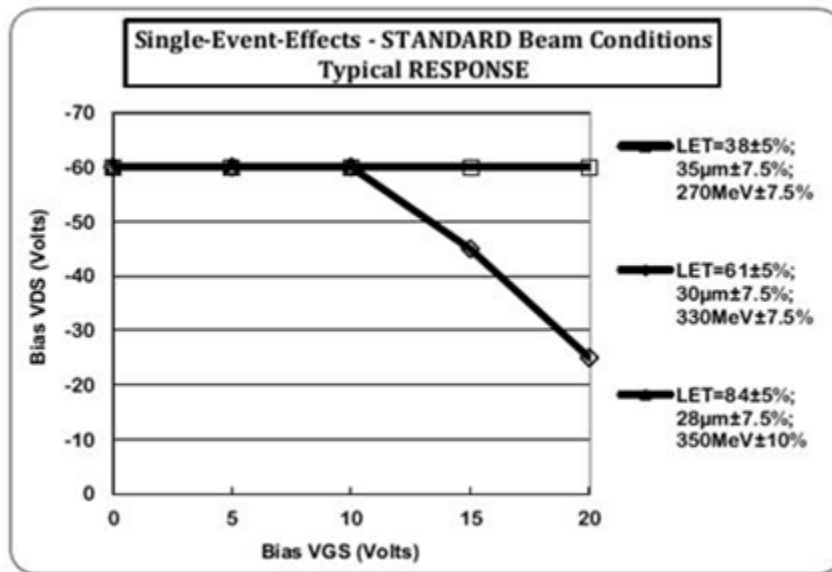


FIGURE 11. Cage 69210 typical SEE response graph, 2N7524.

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* 6.9 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime Weapons Support, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

6.10 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

CONCLUDING MATERIAL

Custodians:

Army - CR
* Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2026-071)

Review Activity:

Army - MI

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.