

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, HIGH SPEED, CMOS,
SHIFT REGISTER, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, high speed, CMOS, logic microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete Part or Identifying Number (PIN).

1.2 Classification. Microcircuits covered by this specification shall be of the following (see 6.2).

1.2.1 Device type. The device types shall be as follows:

<u>Device type</u>	<u>Circuit</u>
01	8 bit parallel-out shift register
02	8 bit parallel-in shift register with clock inhibit
03	8 bit parallel-in shift register with clear
04	4 bit bi-directional shift register
05	4 bit parallel-access shift register
06	8 bit bi-directional universal shift/storage register with three-state outputs
07	8 bit shift register with output latch and three-state outputs

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

<u>Outline letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
C	D-1 (14-lead, .785" x .310" x .200"), dual-in-line package
D	F-2 (14-lead, .280" x .260" x .085"), flat package
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
F	F-5 (16-lead, .440" x .285" x .085"), flat package
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .530" x .355" x .090"), flat package
Z	C-2 (20 terminal, .358" x .358" x .100"), square chip carrier package

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.3 Absolute maximum ratings.

Supply voltage (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage (V_{IN})	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage (V_{OUT})	-0.5 V dc to $V_{CC} + 0.5$ V dc
Clamp diode current (I_{IK}, I_{OK})	± 20 mA
DC output current per pin (I_{OUT}):	
Devices 01-07	± 25 mA
Devices 06-07	± 35 mA (see table 1, 3/)
DC V_{CC} or GND current per pin (I_{CC}):	
Devices 01-07	± 50 mA
Devices 06-07	± 70 mA (see table 1, 3/)
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	300 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance (θ_{JC}):	
Cases C, D, E, F, R, S, and 2	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Input low (V_{IL}) maximum voltage	0.3 V at $V_{CC} = 2$ V 0.9 V at $V_{CC} = 4.5$ V 1.2 V at $V_{CC} = 6$ V
Input high (V_{IH}) minimum voltage	1.5 V at $V_{CC} = 2$ V 3.15 V at $V_{CC} = 4.5$ V 4.2 V at $V_{CC} = 6$ V
Input rise and fall times (t_r, t_f) maximum:	
$V_{CC} = 2$ V	1000 ns
$V_{CC} = 4.5$ V	500 ns
$V_{CC} = 6$ V	400 ns
Case operating temperature range (T_C)	-55°C to +125°C
Minimum clock pulse width:	
Device types 01, 02, 03, 04, 05, and 07	24 ns
Device type 06	38 ns
Minimum clear pulse width:	
Device types 03 and 06	38 ns
Device type 01	30 ns
Device types 04, 05, and 07	24 ns
Minimum load pulse width:	
Device type 02	24 ns
Minimum setup time at mode control:	
Device type 07 (SR, CK)	30 ns
Device type 04 (S_1, S_0)	45 ns
Minimum setup time at shift/load:	
Device type 03	45 ns
Device types 02 and 05	30 ns
Minimum setup time at serial data:	
Device types 05 and 06	38 ns
Device type 07	45 ns
Minimum setup time at serial or parallel data:	
Device types 01, 02, 03, 04, and 05	30 ns
Device type 06	38 ns
Minimum setup time at inhibit:	
Device type 02 and 03	30 ns
Minimum hold time:	
Device types 01, 04, 05, 06, and 07	08 ns
Device type 02	11 ns
Device type 03	15 ns
Minimum enable or inhibit time of clock:	
Device type 03	15 ns
Maximum release time of shift/load:	
Device type 02	11 ns
Device type 03	08 ns
Minimum time of clear to clock (t_{rem}):	
Device types 01, 04, 05, and 06	30 ns
Device type 03	23 ns
Device type 07	15 ns

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications, specification sheets, or MS standards), the text of this document shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.1.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.1.2 Truth tables. The truth tables shall be as specified on figure 2.

3.1.3 Schematic circuits. The schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in this specification and shall be submitted to the qualifying activity as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained and available upon request.

3.2 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the case operating temperature range specified. A pin for pin conditions and testing sequence for table I parameters shall be maintained and available upon request from the qualifying activity, on qualified devices.

3.3 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.4 Correctness of indexing and marking. All devices shall be subjected to the final electrical tests specified in table II after PIN marking to verify that they are correctly indexed and identified by the PIN. Optionally, an approved electrical test may be devised especially for this requirement.

3.5 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 40 (see MIL-M-38510, appendix E).

TABLE I. Electrical performance characteristics test requirements.

Test	Symbol	Conditions 1/ unless otherwise specified	Device type	VCC	Group A subgroups (test method)	Limits -55/+25°C		Limits +125°C		Unit
						Min	Max	Min	Max	
High level output voltage	V_{OH1} <u>2/</u>	$V_{IH} = 1.5 \text{ V}$ $V_{IL} = 0.3 \text{ V}$ $I_{OH} = -20 \mu\text{A}$	A11	2.0 V	1,2,3 (3006)	1.95		1.95		V
	V_{OH2} <u>2/</u>	$V_{IH} = 3.15 \text{ V}$ $V_{IL} = 0.9 \text{ V}$ $I_{OH} = -20 \mu\text{A}$	A11	4.5 V		4.45		4.45		
	V_{OH3}	$V_{IH} = 4.2 \text{ V}$ $V_{IL} = 1.2 \text{ V}$ $I_{OH} = -20 \mu\text{A}$	A11	6.0V		5.95		5.95		
	V_{OH4} <u>2/</u>	$V_{IH} = 3.15 \text{ V}$ $V_{IL} = 0.9 \text{ V}$ $I_{OH} = -4.0 \text{ mA}$	01-07	4.5 V		3.98		3.7		
		$V_{IH} = 3.15 \text{ V}$ $V_{IL} = 0.9 \text{ V}$ $I_{OH} = -6.0 \text{ mA}$	06-07 <u>3/</u>			3.98		3.7		
	V_{OH5}	$V_{IH} = 4.2 \text{ V}$ $V_{IL} = 1.2 \text{ V}$ $I_{OH} = -5.2 \text{ mA}$	01-07	6.0 V		5.48		5.2		
	V_{OH5}	$V_{IH} = 4.2 \text{ V}$ $V_{IL} = 1.2 \text{ V}$ $I_{OH} = -7.8 \text{ mA}$	06-07 <u>3/</u>			5.48		5.2		
Low level output voltage	V_{OL1} <u>2/</u>	$V_{IH} = 1.5 \text{ V}$ $V_{IL} = 0.3 \text{ V}$ $I_{OL} = 20 \mu\text{A}$	A11	2.0 V	1,2,3 (3007)		0.05		0.05	V
	V_{OL2} <u>2/</u>	$V_{IH} = 3.15 \text{ V}$ $V_{IL} = 0.9 \text{ V}$ $I_{OL} = 20 \mu\text{A}$	A11	4.5 V			0.05		0.05	
	V_{OL3}	$V_{IH} = 4.2 \text{ V}$ $V_{IL} = 1.2 \text{ V}$ $I_{OL} = 20 \mu\text{A}$	A11	6.0V			0.05		0.05	

See footnotes at end of table.

TABLE 1. Electrical performance characteristics test requirements - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Device type	V _{CC}	Group A subgroups (test method)	Limits -55/+25°C		Limits +125°C		Unit
						Min	Max	Min	Max	
Low level output voltage	VOL4 2/	V _{IH} = 3.15 V V _{IL} = 0.9 V I _{OL} = 4.0 mA	01-07	4.5 V	1, 2, 3 (3007)		0.26		0.4	V
		V _{IH} = 3.15 V V _{IL} = 0.9 V I _{OL} = 6.0 mA	06-07 3/				0.26		0.4	
	VOL5	V _{IH} = 4.2 V V _{IL} = 1.2 V I _{OL} = 5.2 mA	01-07	6.0 V			0.26		0.4	
		V _{IH} = 4.2 V V _{IL} = 1.2 V I _{OL} = 7.8 mA	06-07 3/				0.26		0.4	
	Positive input clamp voltage	V _{CC} = GND I _{IN} = 1 mA T _C = +25°C	A11		1 (3022)	4/	1.5			
		Negative input clamp voltage	A11			-1.5				
Input current low	I _{IL} 5/	V _{IN} = GND	A11	6.0 V	1, 2 (3009)		-.05		-0.1	μA
Input current high	I _{IH} 5/	V _{IN} = 6.0 V	A11				.05		0.1	
Supply current quiescent	I _{CC} 5/	V _{IN} = V _{CC} or GND	01-05	6.0 V	1, 2 (3005)		0.1		10	μA
			06-07				0.2		20	
Supply current quiescent three-state	I _{CCZ} 5/	V _{IN} = V _{CC}	06-07				0.1		10	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics test requirements - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Device type	V _{CC}	Group A subgroups (test method)	Limits -55/+25°C		Limits +125°C		Unit	
						Min	Max	Min	Max		
Short circuit output current 6/	I _{OS1} 2/	V _O = GND V _I = GND or V _{CC} V _{I(enable)} = GND for (06-07) 3/	01-07	2.0 V	1,2,3 (3011)	-2	-50	-2	-50	mA	
			06-07			-2	-60	-2	-60		
	I _{OS2} 2/		01-07	4.5 V		-15	-150	-15	-150		
			06-07			-15	-165	-15	-165		
	I _{OS3} 2/		01-07	6.0 V		-25	-180	-25	-180		
			06-07			-25	-210	-25	-210		
	I _{OS4}		01-07	4.0 V		-10	-120	-10	-120		
			06-07			-10	-135	-10	-135		
Three-state output (low) leakage current	I _{OZL} 5/	V _I = 4.2 V 7/ V _{IN} , V _{OUT} = GND V _{I(enable)} = 6.0 V	06-07	6.0 V	1,2 (3020)		-.2		-2.0	μA	
Three-state output (high) leakage current	I _{OZH} 5/	V _{I(select)} = 4.2 V V _{I(enable)} = 6.0 V V _{OUT} = 6.0 V 7/	06-07		1,2 (3021)		.2		2.0		
Capacitance input	C _I	See 4.4.1c	A11		4 (3012)		10			pF	
Control	C _C	T _C = +25°C	A11				15				
Output	C _O		06-07	6.0 V			20				
Power dissipation capacitance	C _{PD}	See 4.4.1c T _C = +25°C 8/	01 02,05 03 04 06 07		4		150 100 50 65 240 400			pF	
Truth table test	9/	V _{IL} = .4 V V _{IH} = 3.7 V verify output V _O	A11	4.5 V	7,8 (3014)	L	H	L	H	V	

See footnotes at end of table.

TABLE I. Electrical performance characteristics test requirements - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Device type	VCC	Group A subgroups (test method)	Limits -55/+25°C		Limits +125°C		Unit
						Min	Max	Min	Max	
Propagation delay clock to Q	t _{PLH1} t _{PHL1}	C _L = 50 pF ±10% See figure 3 <u>10/ 11/</u>	01	4.5 V	9,10,11 (3003)	6	31	6	41	ns
			02			4	33	4	44	
			03			5	31	5	41	
			04,05			4	31	4	41	
			06			9	41	9	55	
			07			5	37	5	49	
			Propagation delay Clear to parallel Q			t _{PLH2} t _{PHL2}	01	7	36	
04	4	26		4	35					
05	4	28		4	37					
06	9	41		9	55					
Propagation delay parallel data to Q	t _{PLH3} t _{PHL3}	02	5	32	5	42				
Propagation delay latch clock to Q	t _{PLH4} t _{PHL4}	07	5	31	5	41				
Propagation delay SS/PL to Q	t _{PLH5} t _{PHL5}	02	4	35	4	47				
Propagation delay Clear to Q	t _{PLH6} t _{PHL6}	03	5	31	5	41				
		06	10	41	10	54				
		07	5	31	5	41				
Enable time OE to Q	t _{PZH1} t _{PZL1}	C _L = 50 pF ±10% R _L = 1 kΩ ±10% See figure 3 <u>10/ 11/</u>	06	4.5 V	9,10,11 (3003)	8	34	8	46	ns
			07			4	35	4	47	
Enable time select to Q	t _{PZH2} t _{PZL2}		06	5	54	5	70			
Disable time OE to Q	t _{PHZ1} t _{PLZ1}		06	8	35	8	47			
			07	4	35	4	47			
Disable time select to Q	t _{PHZ2} t _{PLZ2}	06	5	54	5	70				

See footnotes at end of table.

TABLE I. Electrical performance characteristics test requirements - Continued.

Test	Symbol	Conditions 1/ unless otherwise specified	Device type	V _{CC}	Group A subgroups (test method)	Limits -55/+25°C		Limits +125°C		Unit
						Min	Max	Min	Max	
Transition delay	t _{TLH1}	C _L = 50 pF ±10% V _I = GND or V _{CC} See figure 3 10/ 11/	01-05,07 06	4.5 V	9,10,11 (3004)	3	15	3	20	ns
	t _{THL1}					2	12	2	16	
Maximum clock frequency	f _{MAX}	C _L = 50 pF ±10% 11/	01-03	4.5 V	9,10,11	28		21		MHz
			04-05			34		26		
			06			23		17		
			07			31		23		

- 1/ For a power supply of 5 V ±10 percent the worst case output voltage (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V, respectively. The V_{IH} value at 5.5 V is 3.85 V. The worst case leakage current (I_{IH}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used. Each input/output, as applicable, shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

- a. V_{IC} (pos) tests, the GND terminal shall be open.
- b. V_{IC} (neg) tests, the V_{CC} terminal shall be open.
- c. I_{CC} tests, the output terminal shall be open.

Additional detailed information on qualified devices (i.e., pin for pin conditions and testing sequence) is available from the qualifying activity (DESC-EQM) upon request (see 3.2).

- 2/ Guaranteed but not tested.
- 3/ The serial outputs for device type 06 (Q_A' and Q_H') and device type 07 (Q_H') are standard outputs and not three-state bus outputs.
- 4/ For equipment that does not allow "GND" pin to be open during testing, a minimum limit of 0.4 V applies.
- 5/ Not tested at -55°C.
- 6/ Maximum limits in table I are for device testing only. Minimum limits are guaranteed for design. Only one output shall be shorted at a time.
- 7/ Three-state output conditions are required for I_{OZL}, set output to high state. For I_{OZH}, set output to low state. Set input pins to V_{IL} = V_{IL} (maximum) and V_{IH} = V_{IH} (minimum), as required.
- 8/ Power dissipation capacitance (C_{PD}) per package (device enabled). Power dissipation capacitance (C_{PD}), guaranteed but not tested, determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}2f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC}2f + I_{CC} (see JEDEC standard 7A, appendix E).

- 9/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Correct voltage outputs are ≥ 2.5 V for high logic levels and < 2.5 V for low logic levels. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. $H \geq 2.5$ V, $L < 2.5$ V; high inputs = 3.7 V and low inputs = 0.4 V.
- 10/ For class B devices tested at $V_{CC} = 4.5$ V at 125°C for sample testing and at $V_{CC} = 4.5$ V at $+25^{\circ}$ for screening guaranteed at other V_{CC} voltages and temperatures, see table IA as appropriate and 4.4.1d. Setup and hold times shall be as specified in the recommended operating conditions (see 1.4) and are referenced to the 50 percent points.
- 11/ See the formula for determining switching times shown in tables IA and IB.

TABLE IA. Calculated dynamic figures at $-55/+25$ case temperature ($^{\circ}\text{C}$).

V_{CC}	$T_C = (^{\circ}\text{C})$	
	+125	-55/+25
2.0 V	5	5×0.75
4.5 V	1	0.75
6.0 V	0.85	0.85×0.75

Normalized numbers
($+125^{\circ}\text{C}$ equals 1)

TABLE IB. Calculated f_{MAX} figures at $-55/+25$ case temperature ($^{\circ}\text{C}$).

V_{CC}	$T_C = (^{\circ}\text{C})$	
	+125	-55/+25
2.0 V	0.2X	0.2Y
4.5 V	$X = 1$	$1.33X = Y$
6.0 V	1.18X	1.18Y

Normalized numbers
($+125^{\circ}\text{C}$ equals 1)

NOTE: The 2.0 V and 6.0 V numbers are derived from their 4.5 V integer value (rounding off according 5/4).

TABLE II. Burn-in and electrical test requirements.

Line no.	Applicable tests and MIL-STD-883 test method	Class S device <u>1/</u>			Class B device <u>1/</u>		
		Reference paragraph	Table I subgroups <u>2/</u>	Table III delta limits <u>3/</u>	Reference paragraph	Table I subgroups <u>2/</u>	Table III delta limits <u>3/</u>
1	Interim electrical parameters (method 5004)		1				1
2	Static burn-in I (method 1015)	4.2b 4.5.2	Required			Not required	
3	Same as line 1		1	Δ			
4	Static burn-in II (method 1015)	4.2b 4.5.2	Required		4.2b 4.5.2	4/ Required	
5	Same as line 1	4.2d	1*	Δ	4.2d	1*	Δ
6	Dynamic burn-in (method 1015)	4.2b 4.5.2	Required			Not required	
7	Same as line 1	4.2d	1	Δ			
8	Final electrical parameters (method 5004)		1*, 2, 3, 7, 8, 9			1*, 2, 7, 9 4/	
9	Group A test requirements (method 5005)	4.4.1	1, 2, 3, 4, 7, 8, 9, 10, 11		4.4.1	1, 2, 3, 4, 7, 8, 9, 10, 11	
10	Group B end-point electrical parameters (method 5005)	4.4.2	1, 2, 3, 9, 10, 11	Δ			
11	Group C end-point electrical parameters (method 5005)				4.4.3	1, 2	Δ
12	Group D end-point electrical parameters (method 5005)	4.4.4	1, 2, 3		4.4.4	1, 2	

1/ Blank spaces indicate tests are not applicable.

2/ * indicates PDA applies to subgroup (see 4.2.1).

3/ Δ indicates delta limit shall be required only on table I subgroup 1, where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1).

4/ The device manufacturer may at his option either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).

Pin name									
Device	01	02	03	04	05	06	07		
Case	D,C	2	E,F	2	E,F	2	R,S,2	E,F	2
1	NC	SH/LD	NC	CLR	NC	SD	QB	NC	NC
2	AIN	CLK	SERINP	SR SER	CLR	G1	QC	QB	QB
3	BIN	E	A	AIN	J	G2	QD	QC	QC
4	QA	F	B	BIN	K	G/QG	QE	QD	QD
5	QC	G	C	CIN	AIN	E/QE	QF	QE	QE
6	QD	H	D	DIN	BIN	IC/QC	QG	NC	NC
7	GND	QH	CLK	SL SER	DIN	IA/QA	QH	QF	QF
8	CLK	GND	CLKINH	GND	GND	QA'	GND	QG	QG
9	CLR	QH	CLR	SL SER	SH/LD	CLR	QH'	QH	QH
10	QE	SERINP	E	SI	CLK	GND	SRCLR	GND	GND
11	QF	A	F	CLK	QD	SR	SRCK	NC	NC
12	QG	B	G	QD	SH/LD	CLK	RCK	QH'	QH'
13	QH	C	QH	QD	QD	IB/QB	G	SRCLR	SRCLR
14	VCC	D	SER	QD	QC	ID/QD	SER	SRCK	SRCK
15	NC	CLKINH	H	QA	QA	IF/QF	QA	RCK	RCK
16	QF	VCC	NC	VCC	VCC	H/QH	VCC	NC	NC
17	NC	C	QH	QC	QC	QH'	QC	G	G
18	QG	D	H	QB	QB	SL	SL	SER	SER
19	QH	CLKINH	SH/LD	QA	QA	SI	QA	QA	QA
20	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC

FIGURE 1. Terminal connections.

Device type 01

Inputs			Outputs		
$\overline{\text{Clear}}$	Clock	A B	Q_A	Q_B	... Q_H
L	X	X X	L	L	L
H	L	X X	Q_{A0}	Q_{B0}	Q_{H0}
H	$\uparrow$	H H	H	Q_{An}	Q_{Gn}
H	$\uparrow$	L X	L	Q_{An}	Q_{Gn}
H	$\uparrow$	X L	L	Q_{An}	Q_{Gn}

H = high level (steady state).

L = low level (steady state).

X = irrelevant (any input, including transitions).

$\uparrow$ = transition from low to high level.

Q_{A0} , Q_{B0} , Q_{H0} = the level of Q_A , Q_B , or Q_H , respectively, before the indicated steady-state input conditions were established.

Q_{An} , Q_{Gn} = the level of Q_A or Q_G before the most recent transition of the clock; indicates a one-bit shift.

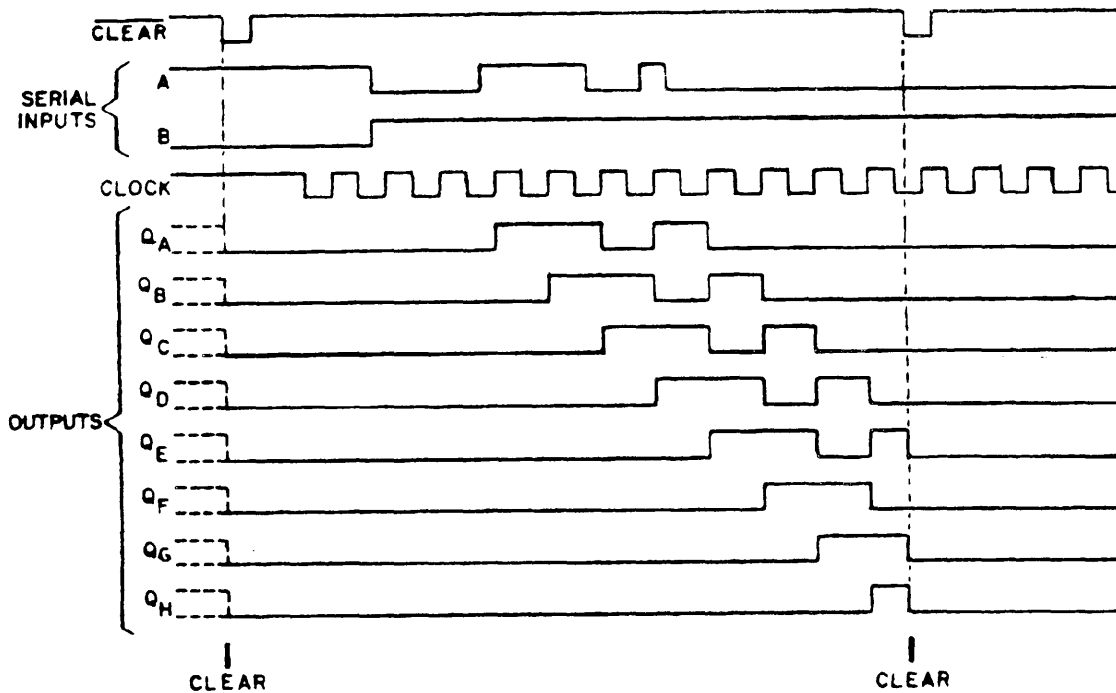


FIGURE 2. Truth tables and timing diagrams.

Device type 02

Inputs					Internal outputs		Output Q _H
Shift/ load	Clock inhibit	Clock	Serial	Parallel	Q _A	Q _B	
				A....H			
L	X	X	X	a....h	a	b	h
H	L	L	X	X	Q _{A0}	Q _{B0}	Q _{H0}
H	L	↑	H	X	H	Q _{An}	Q _{Gn}
H	L	↑	L	X	L	Q _{An}	Q _{Gn}
H	H	X	X	X	Q _{A0}	Q _{B0}	Q _{H0}

H = high level (steady state).

L = low level (steady state).

X = irrelevant (any input, including transitions).

↑ = transition from low to high level.

Q_{A0} , Q_{B0} , Q_{H0} = the level of Q_A , Q_B , or Q_H , respectively, before the indicated steady-state input conditions were established.

Q_{An} , Q_{Gn} = the level of Q_A or Q_G before the most recent transition of the clock; indicates a one-bit shift.

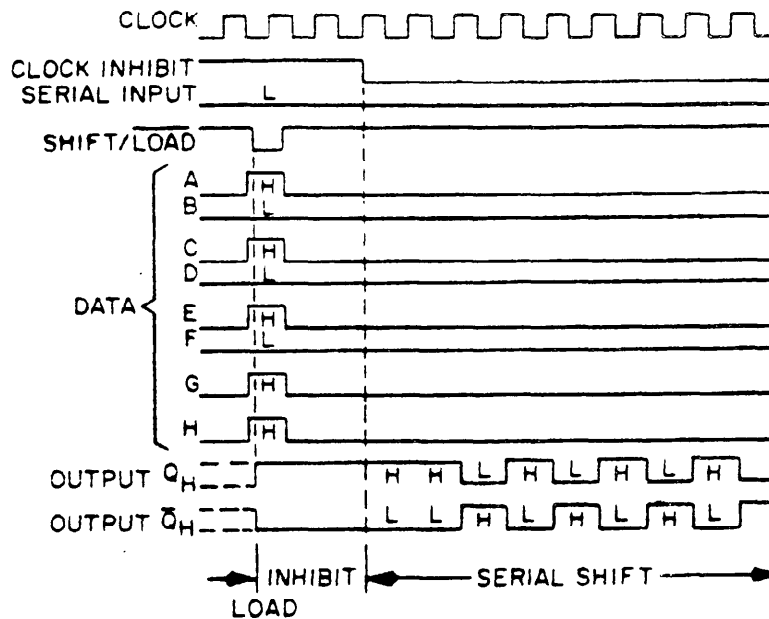


FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 03

Inputs						Internal outputs		Output
Clear	Shift/load	Clock inhibit	Clock	Serial	Parallel A....H	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	QA0	QB0	QH0
H	L	L	↑	X	a....h	a	b	h
H	H	L	↑	H	X	H	QAn	QGn
H	H	L	↑	L	X	L	QAn	QGn
H	X	H	↑	X	X	QA0	QB0	QH0

H = high level (steady state).

L = low level (steady state).

X = irrelevant (any input, including transitions).

↑ = transition from low to high level.

QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.

QAn, QGn = the level of QA or QG before the most recent transition of the clock;

indicates a one-bit shift.

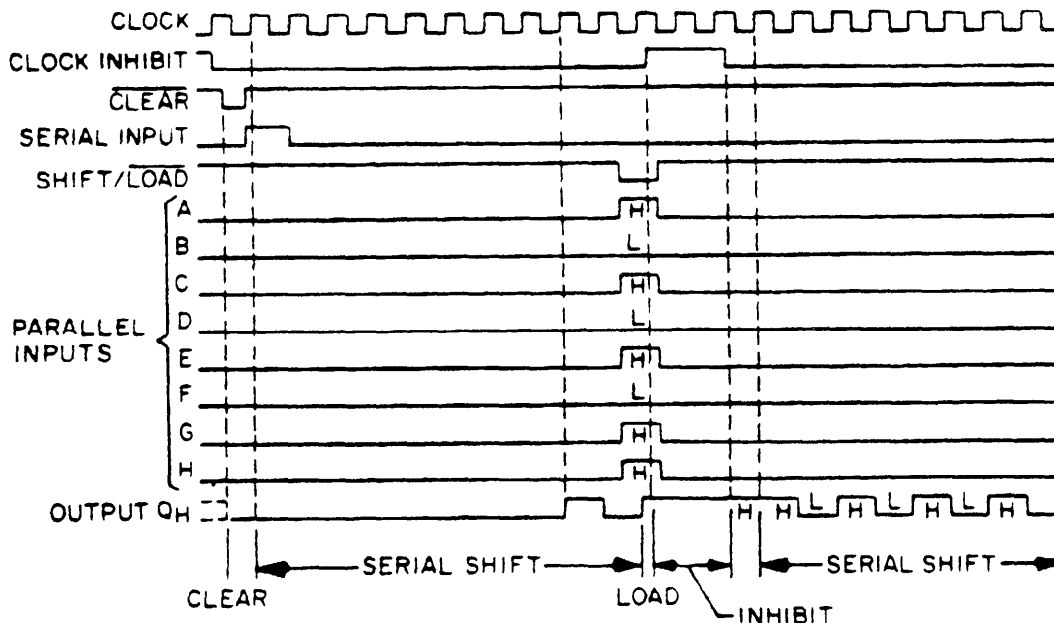


FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 04

Inputs									Outputs				
Clear	Mode		Clock	Serial		Parallel				QA	QB	QC	QD
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QAO	QBO	QCO	QDO
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	↑	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	↑	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QAO	QBO	QCO	QDO

H = high level (steady state).

L = low level (steady state).

X = irrelevant (any input, including transitions).

↑ = transition from low to high level.

a, b, c, d = the level of steady-state input at A, B, C, or D, respectively.

QAO, QBO, QCO, QDO = the level of QA, QB, QC, or QD, respectively, before

the indicated steady-state input conditions were established.

QAn, QBn, QCn, QDn = the level of QA, QB, QC, or QD, respectively, before the most recent transition of the clock.

FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 04

Typical clear, load, right-shift, left-shift, inhibit, and clear sequences.

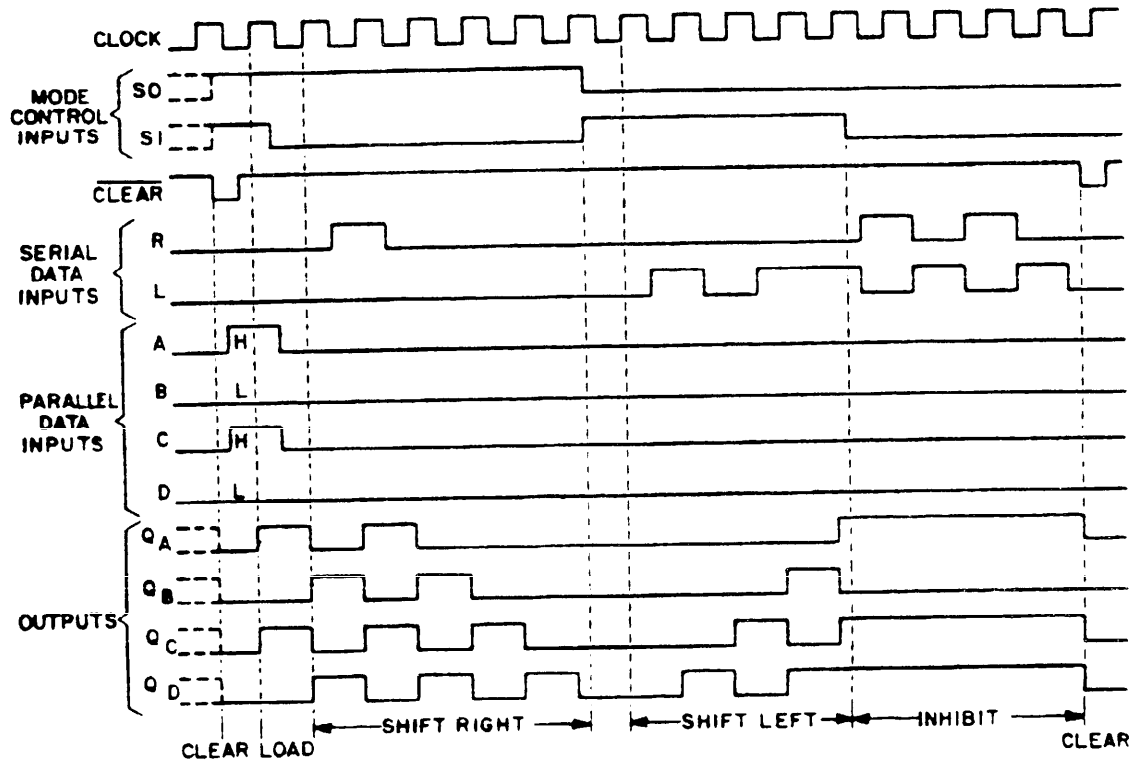


FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 05

Inputs					Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				$\bar{Q}_D$
			J	$\bar{K}$	A	B	C	D	
L	X	X	X	X	X	X	X	X	H
H	L	↑	X	X	a	b	c	d	$\bar{d}$
H	H	L	X	X	X	X	X	X	$\bar{Q}_{A0}$ $\bar{Q}_{B0}$ $\bar{Q}_{C0}$ $\bar{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	$\bar{Q}_{A0}$ $\bar{Q}_{A0}$ $\bar{Q}_{Bn}$ $\bar{Q}_{Cn}$ $\bar{Q}_{Dn}$
H	H	↑	L	L	X	X	X	X	L $\bar{Q}_{An}$ $\bar{Q}_{Bn}$ $\bar{Q}_{Cn}$ $\bar{Q}_{Dn}$
H	H	↑	H	H	X	X	X	X	H $\bar{Q}_{An}$ $\bar{Q}_{Bn}$ $\bar{Q}_{Cn}$ $\bar{Q}_{Dn}$
H	H	↑	H	L	X	X	X	X	$\bar{Q}_{An}$ $\bar{Q}_{An}$ $\bar{Q}_{Bn}$ $\bar{Q}_{Cn}$ $\bar{Q}_{Dn}$

H = high level (steady state).

L = low level (steady state).

X = irrelevant (any input, including transitions).

↑ = transition from low to high level.

a, b, c, d = the level of steady-state input at A, B, C, or D, respectively.

 $\bar{Q}_{A0}$, $\bar{Q}_{B0}$, $\bar{Q}_{C0}$, $\bar{Q}_{D0}$ = the level of $\bar{Q}_A$, $\bar{Q}_B$, $\bar{Q}_C$, or $\bar{Q}_D$, respectively, before the

indicated steady-state input conditions were established.

 $\bar{Q}_{An}$, $\bar{Q}_{Bn}$, $\bar{Q}_{Cn}$ = the level of $\bar{Q}_A$, $\bar{Q}_B$, or $\bar{Q}_C$, respectively, before the most recent transition of the clock.

Typical clear, shift, and load sequences.

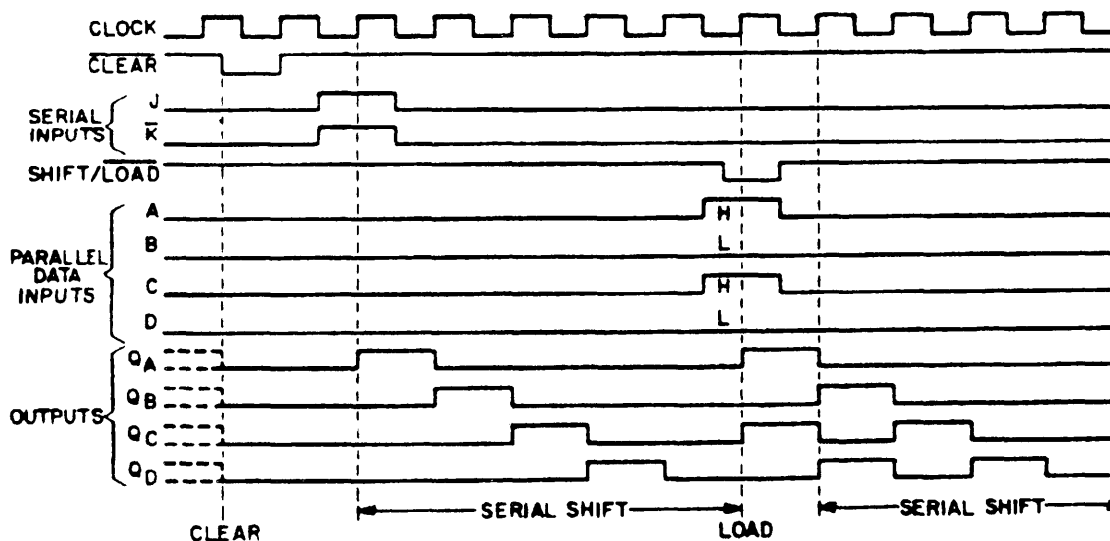


FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 06

Mode	Inputs				Inputs/outputs										Outputs	
	Clear SI	Function select SQ	Output control GI 1/ 02 1/	Clock SL	Serial SR	A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'	
Clear	L	X	L	X	X	L	L	L	L	L	L	L	L	L	L	
	L	L	L	X	X	L	L	L	L	L	L	L	L	L	L	
	L	H	X	X	X	X	X	X	X	X	X	X	X	L	L	
Hold	H	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0	
	H	X	L	L	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0	
	H	L	L	L	X	H	H	QA0	QB0	QC0	QF0	QG0	QH0	H	QH0	
Shift right	H	L	L	L	X	L	L	QA0	QB0	QC0	QF0	QG0	QH0	L	QH0	
	H	L	L	L	X	L	L	QA0	QB0	QC0	QF0	QG0	QH0	L	QH0	
	H	H	L	L	H	QA0	QB0	QC0	QD0	QE0	QF0	QH0	H	QA0	H	
Shift left	H	H	L	L	H	QA0	QB0	QC0	QD0	QE0	QF0	QH0	H	QA0	H	
	H	H	L	L	L	QA0	QB0	QC0	QD0	QE0	QF0	QH0	L	QA0	L	
	H	H	L	L	L	QA0	QB0	QC0	QD0	QE0	QF0	QH0	L	QA0	L	
Load	H	H	X	X	X	X	X	L	D	E	F	G	H	H	H	
	H	H	X	X	X	X	X	L	D	E	F	G	H	H	H	
	H	H	X	X	X	X	X	L	D	E	F	G	H	H	H	

1/ When one or both output controls are high the eight input/output terminals are disabled to the high impedance state; however, sequential operation or clearing of the register is not affected.

FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 06

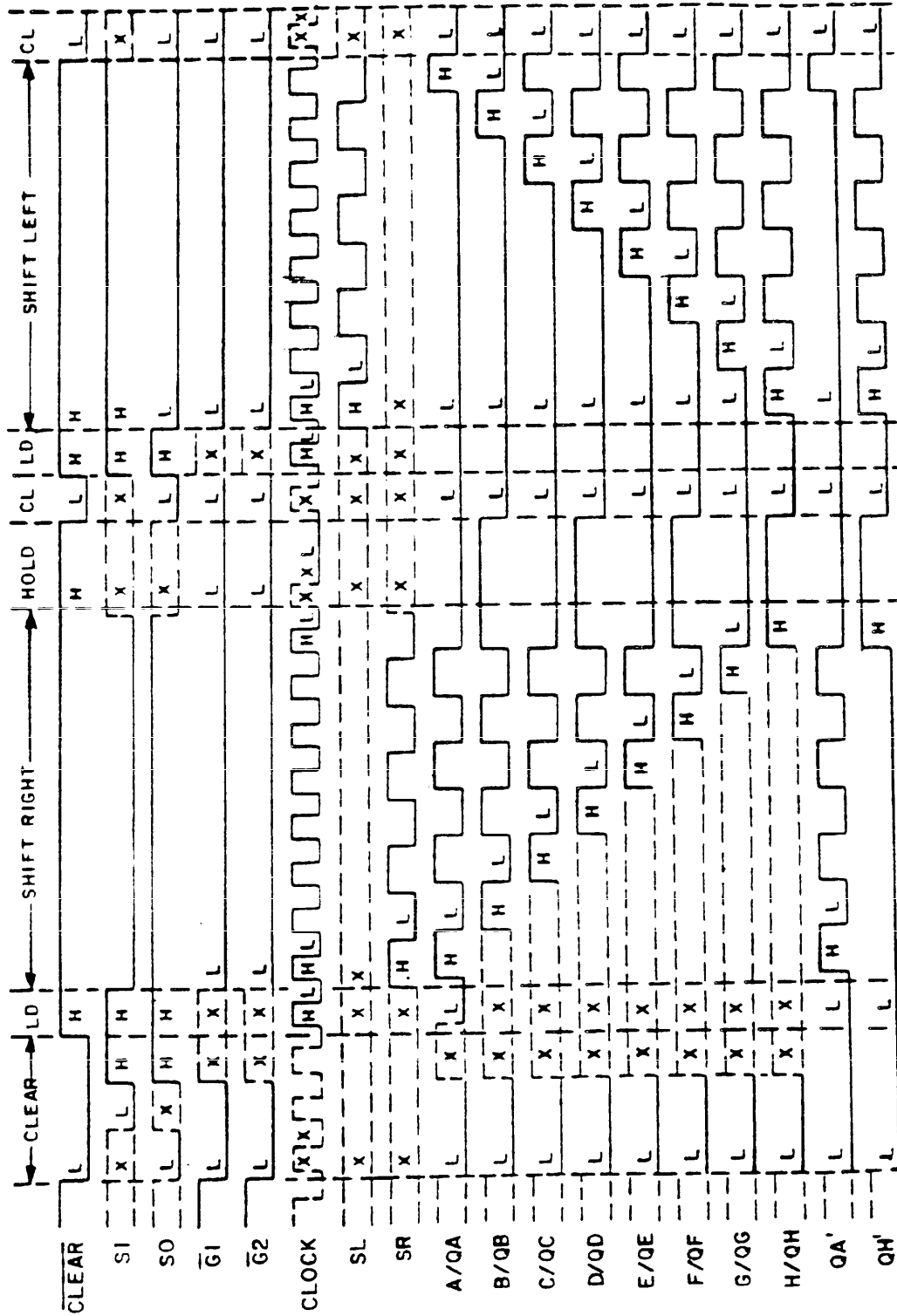


FIGURE 2. Truth tables and timing diagrams - Continued.

$\overline{\text{SRCLR}}$	SER	Inputs	$\text{SRCK} \diagdown \text{RCK}$		$\overline{\text{G}}$	Device type 07 Resulting function
			Shift Clock	Latch Clock		
$\overline{\text{Clear}}$	Data				Output Enable	
	L	X	X	X	X	Shift register contents are cleared.
	H	L	$\uparrow$	X	X	A low logic level is shifted into shift register.
	H	H	$\uparrow$	X	X	A high logic level is shifted into shift register.
	H	X	$\downarrow$	X	X	Shift register remains unchanged.
	H	X	L	$\uparrow$	X	Shift register data stored in the 8-bit latch.
	H	X	L	$\downarrow$	X	Data latch remains unchanged.
	H	X	L	L	L	Latch Outputs, QA - QH are enabled.
	H	X	L	L	H	Outputs QA - QH are in the high impedance state.
	H	X	L	L	H	

H = high level (steady-state)

L = low level (steady-state)

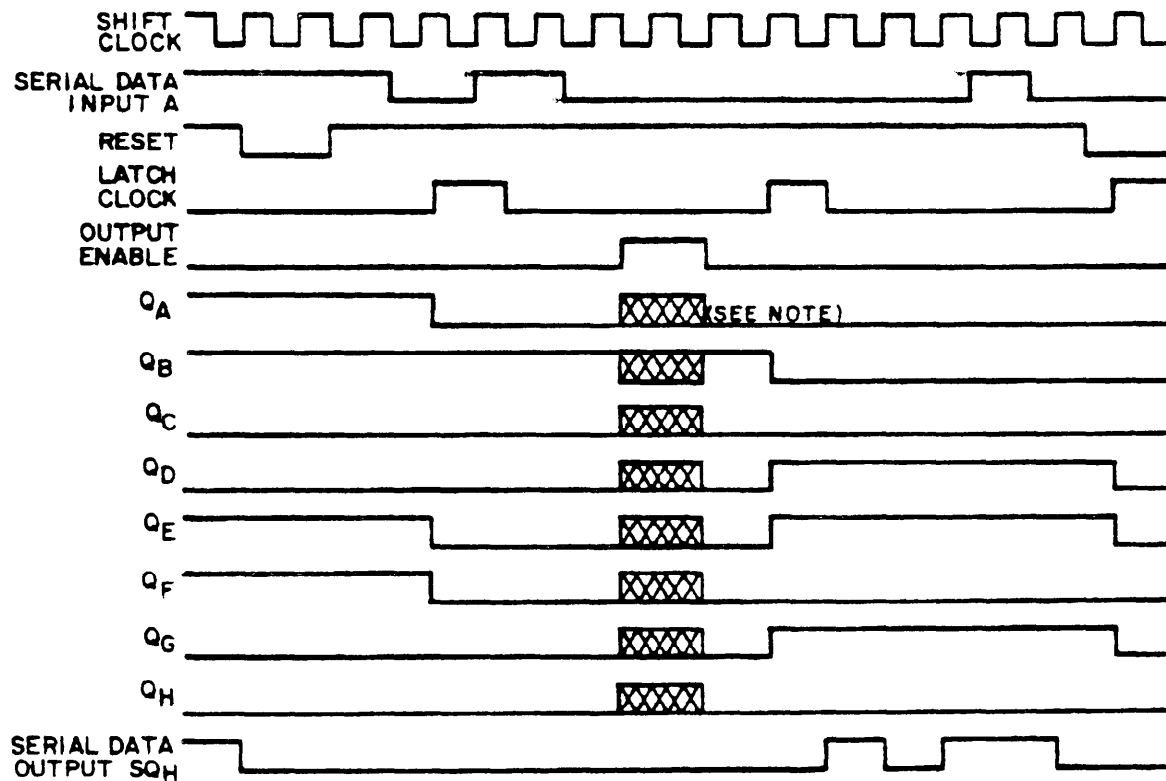
X = don't care

 $\uparrow$ = transition low to high level $\downarrow$ = transition high to low level

FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 07

TIMING DIAGRAM



NOTE: XXXXX implies that the output is in a high impedance state.

FIGURE 2. Truth tables and timing diagrams - Continued.

Device type 01

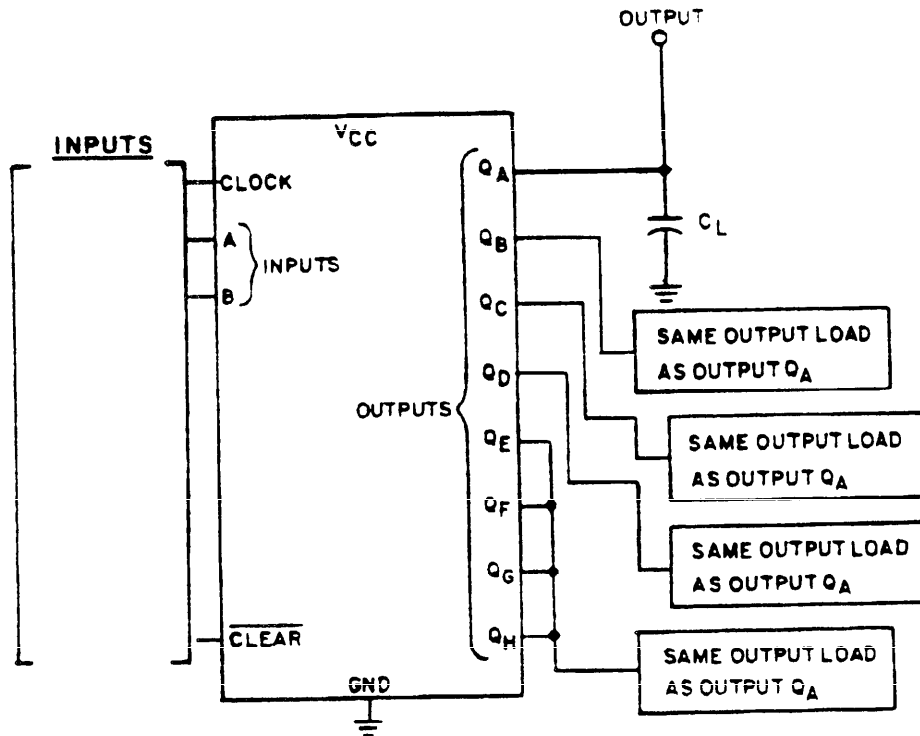


FIGURE 3. Switching test circuit and waveforms.

Device type 01

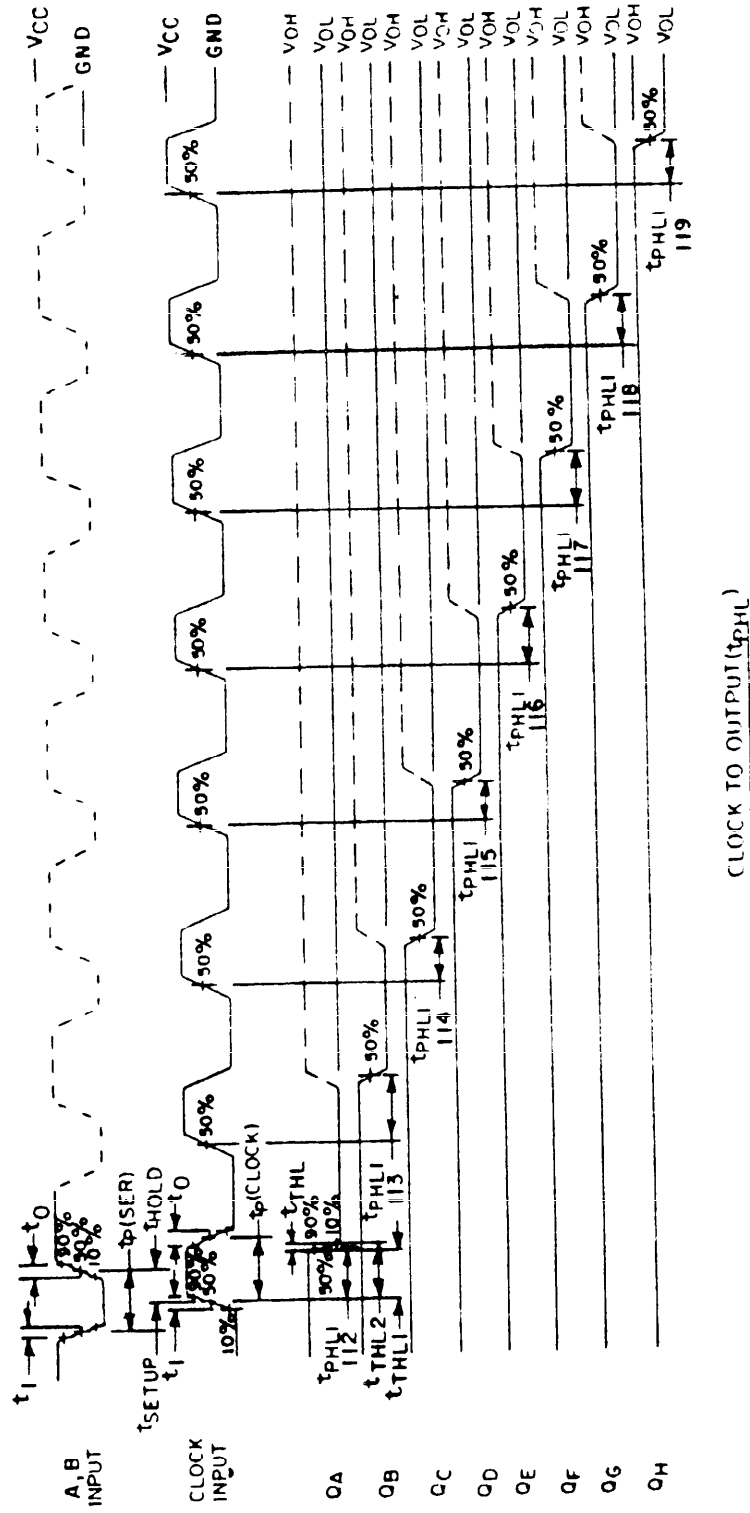
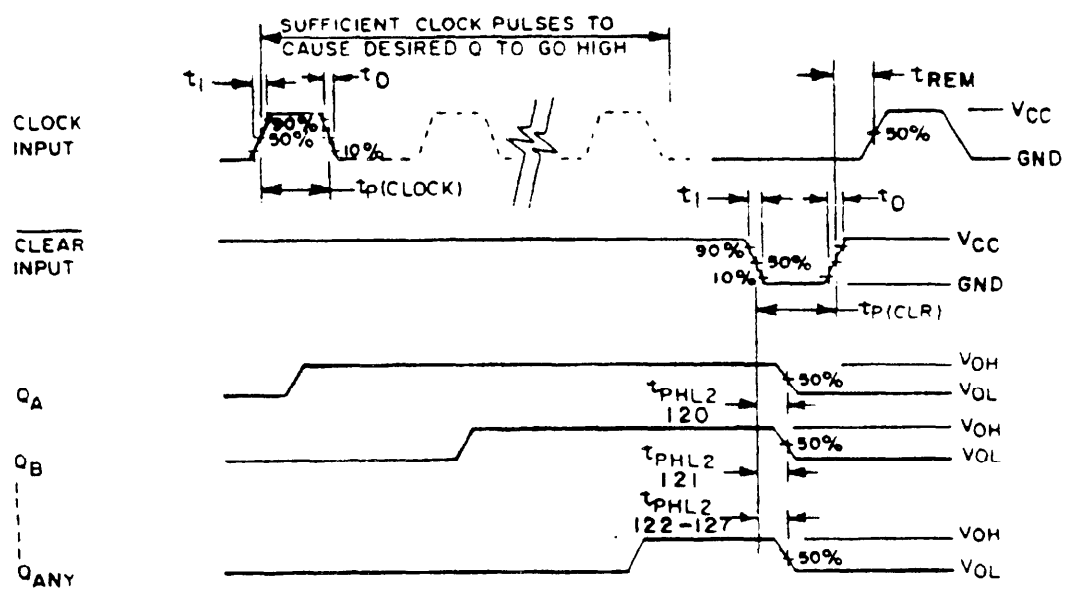
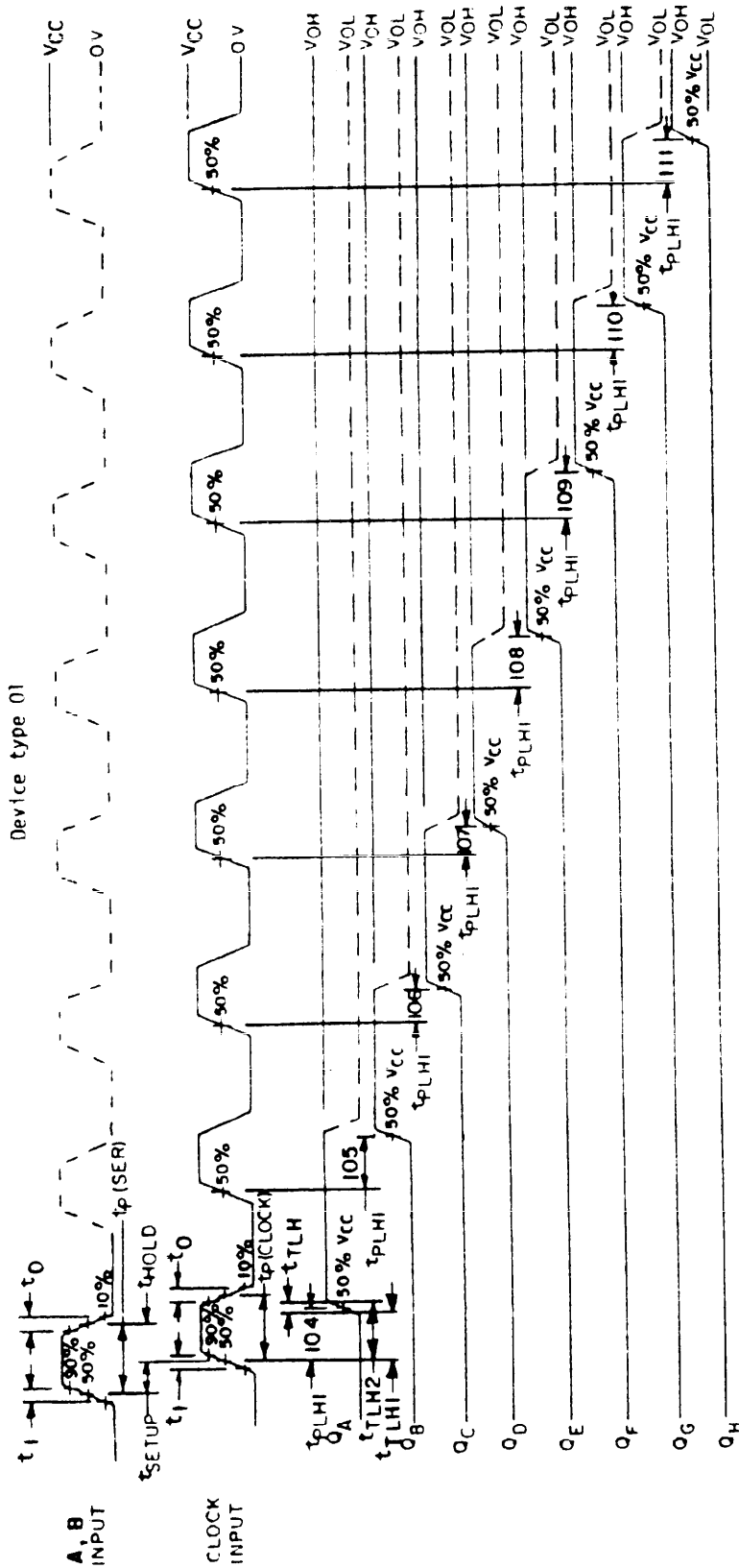


FIGURE 3. Switching test circuit and waveforms - Continued.

Device type 01

CLEAR TO OUTPUT WAVEFORMSFIGURE 3. Switching test circuit and waveforms - Continued.

CLOCK TO OUTPUT (t_{PLH})

NOTES:

1. Clock pulse characteristics: $t_1 \leq 6 \text{ ns}$, $t_0 \leq 6 \text{ ns}$, $16 \text{ ns} \leq t_p \text{ (clock)} \leq 24 \text{ ns}$.
2. Clear pulse characteristics: $t_1 \leq 6 \text{ ns}$, $t_0 \leq 6 \text{ ns}$, $20 \text{ ns} \leq t_p \text{ (clear)} \leq 30 \text{ ns}$, $20 \text{ ns} \leq t_{\text{REM}} \leq 30 \text{ ns}$.
3. Serial pulse characteristics: $t_1 \leq 6 \text{ ns}$, $t_0 \leq 6 \text{ ns}$, $25 \text{ ns} \leq t_p \leq 38 \text{ ns}$, $20 \text{ ns} \leq t_{\text{SETUP}} \leq 30 \text{ ns}$, $5 \text{ ns} \leq t_{\text{HOLD}} \leq 8 \text{ ns}$.
4. $C_L = 50 \text{ pF} \pm 10\%$ including scope, probe, wiring and stray capacitance without package in test fixture.
5. $t_{\text{THL}} = t_{\text{THL2}} - t_{\text{THL1}}$, $t_{\text{TLH}} = t_{\text{TLH2}} - t_{\text{TLH1}}$.
6. For f_{MAX} tests, clock PRR = 21 MHz, $t_p(\text{clock}) \geq 24 \text{ ns}$, $A_{\text{IN PRR}} = 11 \text{ MHz}$, $t_p(\text{data}) \geq 45 \text{ ns}$, $t_1 = t_0 \leq 6 \text{ ns}$.
7. Prior to initiating tests, the output shall be placed in the proper state.

FIGURE 3. Switching test circuit and waveforms - Continued.

Device type 02

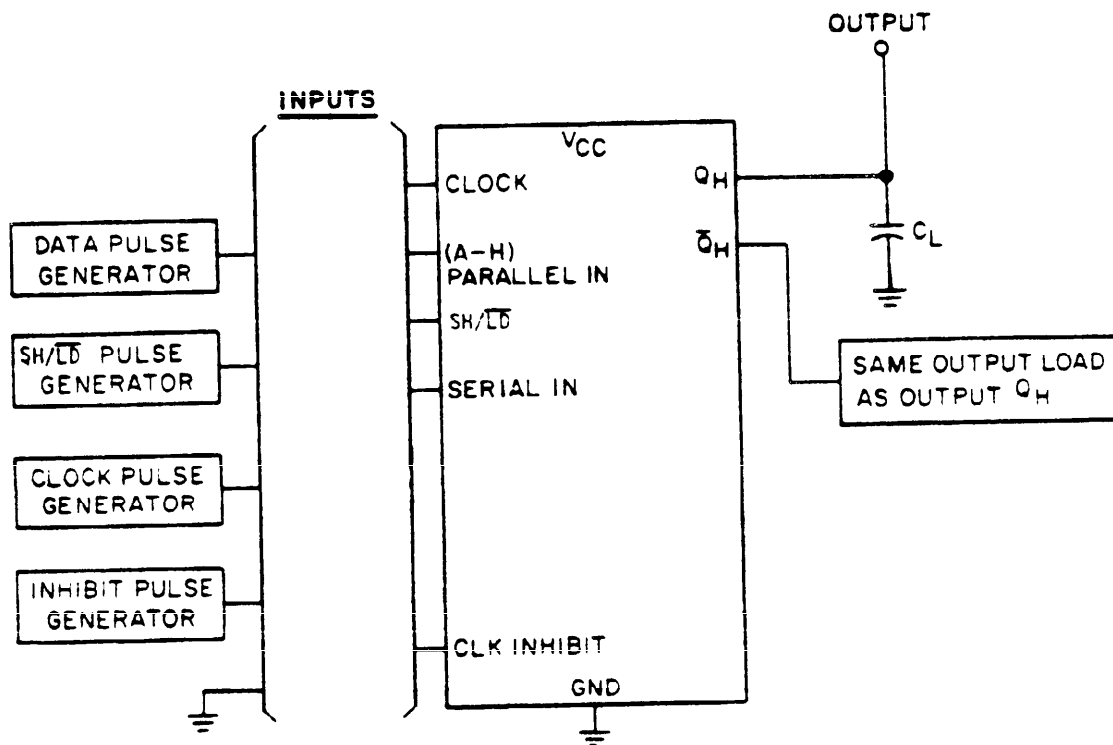
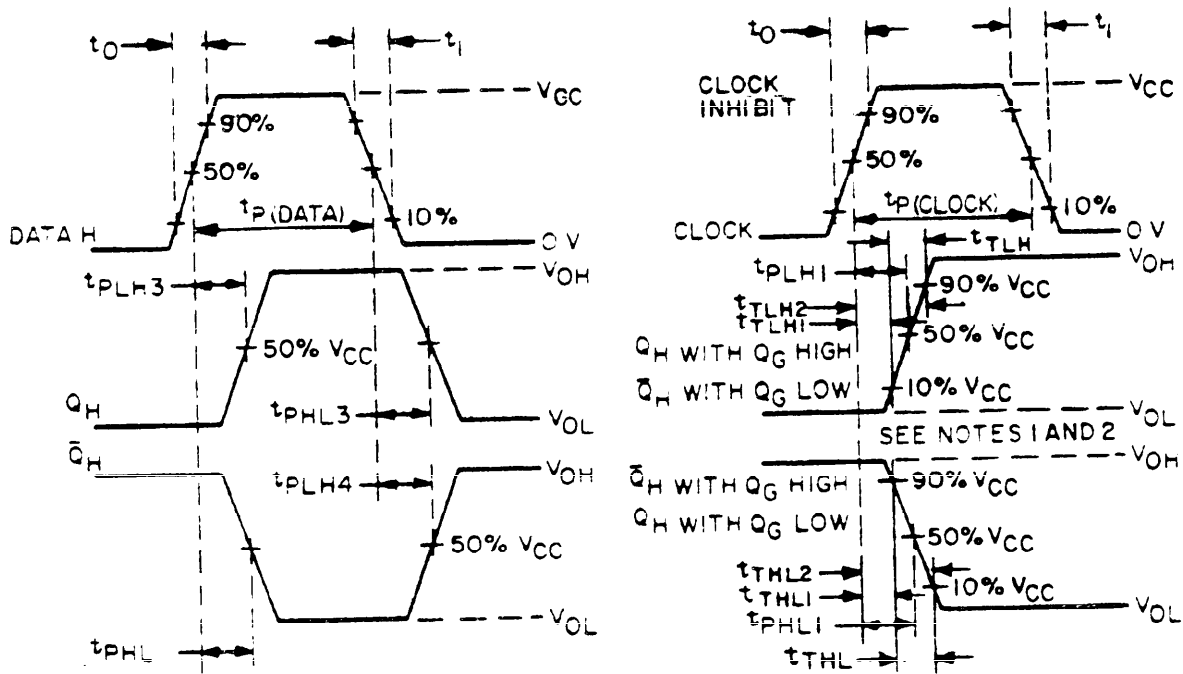
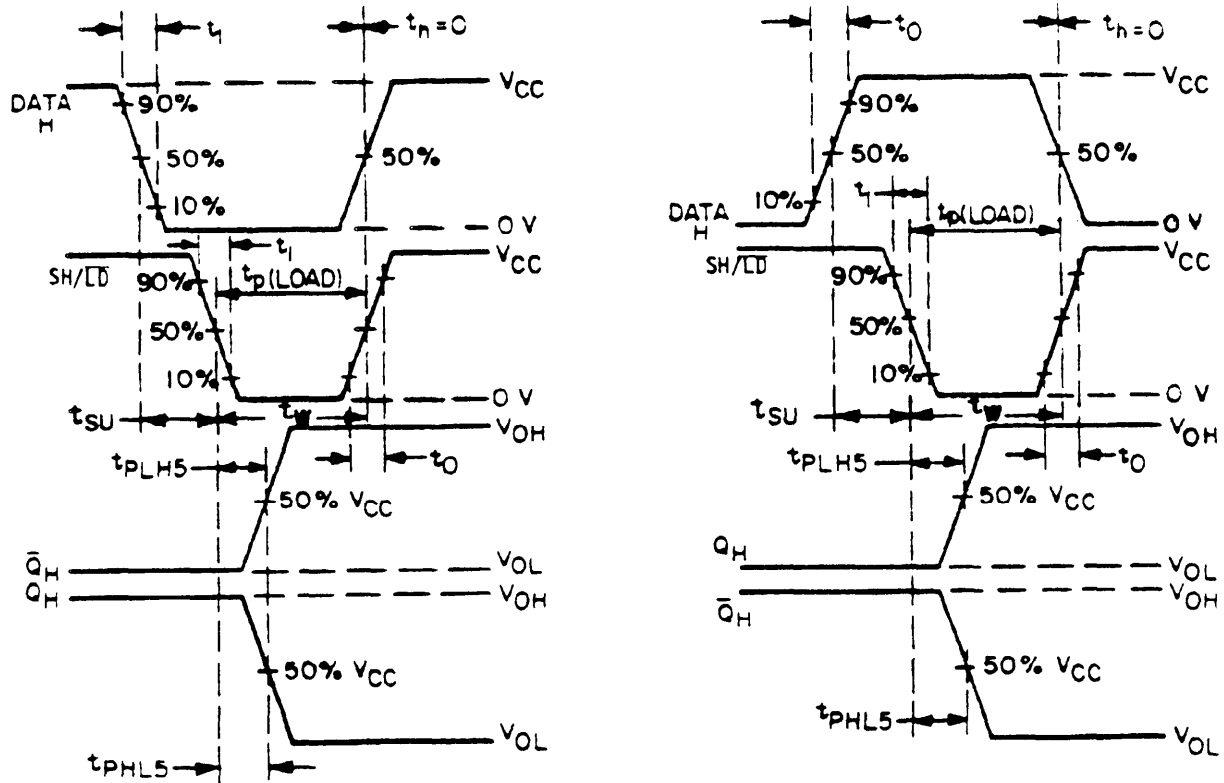


FIGURE 3. Switching test circuit and waveforms - Continued.

Device type 02


FIGURE 3. Switching test circuit and waveforms - Continued.

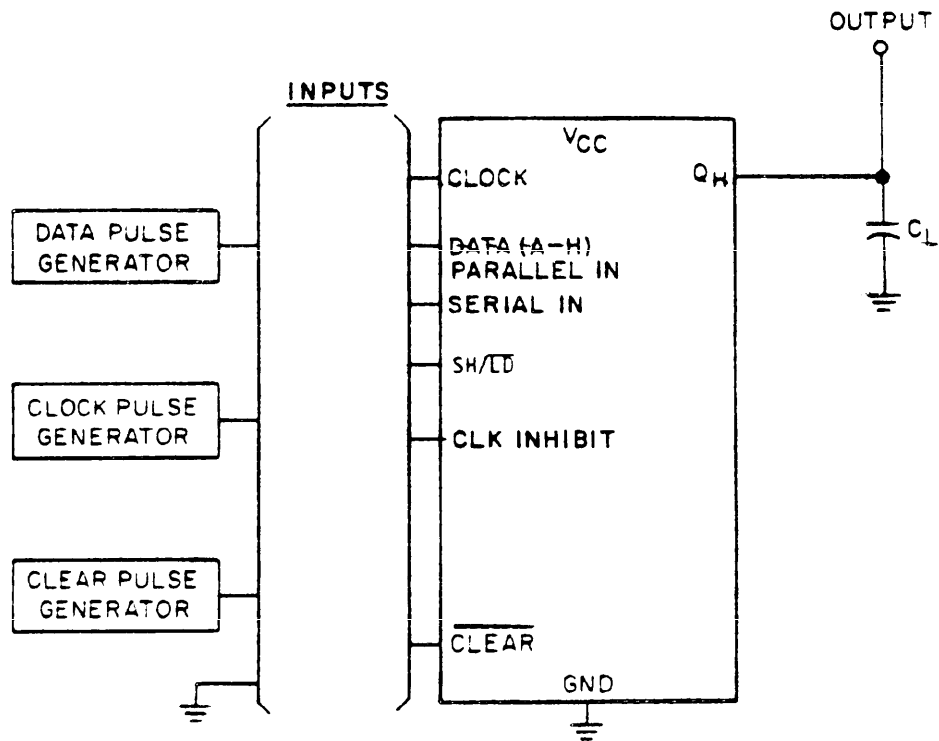


NOTES:

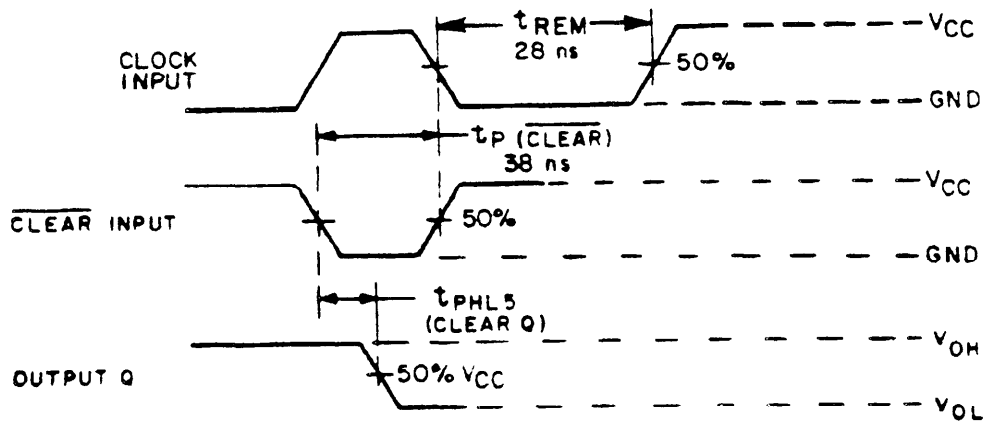
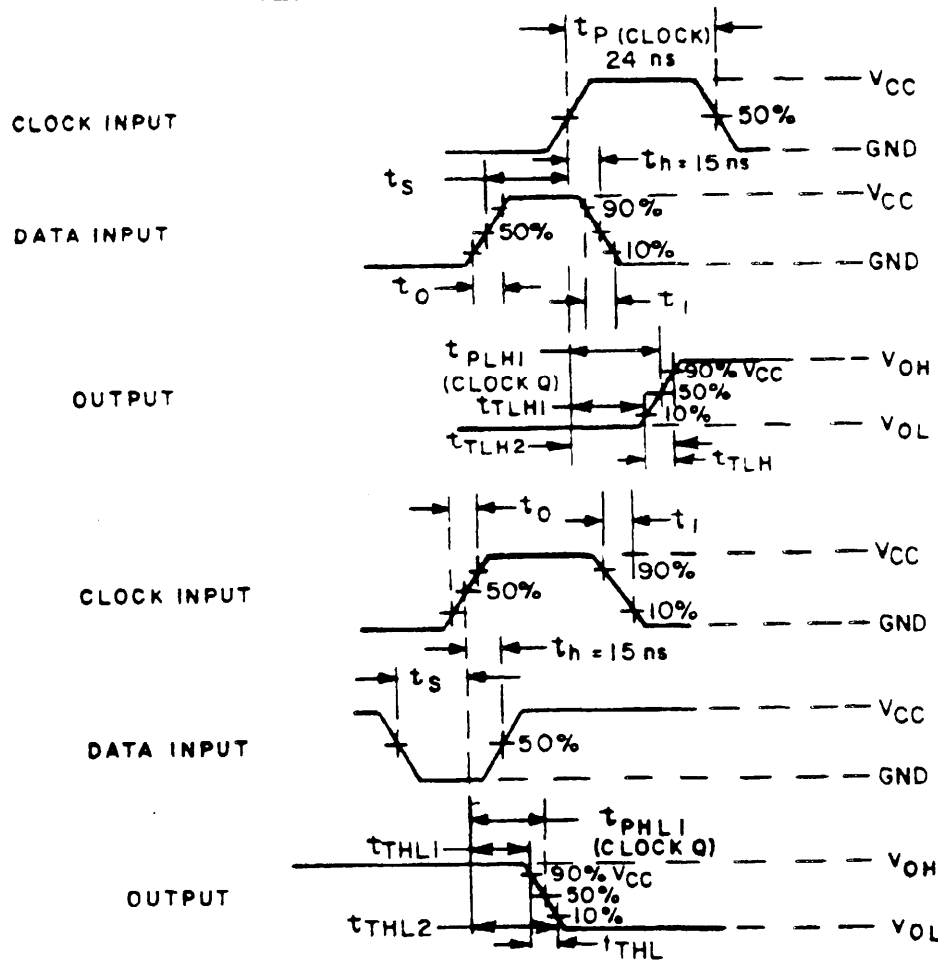
1. Clock pulse characteristics: clock, clock inhibit, $t_i \leq 6$ ns, $t_0 \leq 6$ ns, 16 ns $\leq t_p$ (clock, clock inhibit) ≤ 24 ns.
2. Data pulse characteristics: $t_i \leq 6$ ns, $t_0 \leq 6$ ns, 27 ns $\leq t_p$ (serial/parallel) ≤ 41 ns, 20 ns $\leq t_{SETUP} \leq 30$ ns, 7 ns $\leq t_{HOLD} \leq 11$ ns.
3. Shift/load pulse characteristics: $t_i \leq 6$ ns, $t_0 \leq 6$ ns, 16 ns $\leq t_p$ (load) ≤ 24 ns.
4. $C_L = 50$ pF $\pm 10\%$ including scope, probe, wiring and stray capacitance without package in test fixture.
5. Serial mode - clock inhibit: 20 ns $\leq t_S \leq 30$ ns.
6. Serial mode - load inhibit: 20 ns $\leq t_S \leq 30$ ns.
7. For f_{MAX} tests, clock PRR = 21 MHz, $t_p(\text{clock}) \geq 24$ ns, serial PRR = 11 MHz, $t_p(\text{data}) \geq 45$ ns, $t_i = t_0 \leq 6$ ns.
8. Prior to initiating tests, the output shall be placed in the proper state.
9. For t_{PHL1} measurements, internal output G must be set to a low and Q_H to a high prior to test.
10. For t_{PHL1} measurements, internal output G must be set to a high and Q_H to a low prior to test.
11. $t_{TLH} = t_{TLH2} - t_{TLH1}$, $t_{THL} = t_{THL2} - t_{THL1}$.

FIGURE 3. Switching test circuit and waveforms - Continued.

Device type 03

FIGURE 3. Switching test circuit and waveforms - Continued.

Device type 03

CLEAR TO OUTPUT WAVEFORMCLOCK TO OUTPUT WAVEFORMSFIGURE 3. Switching test circuit and waveforms - Continued.

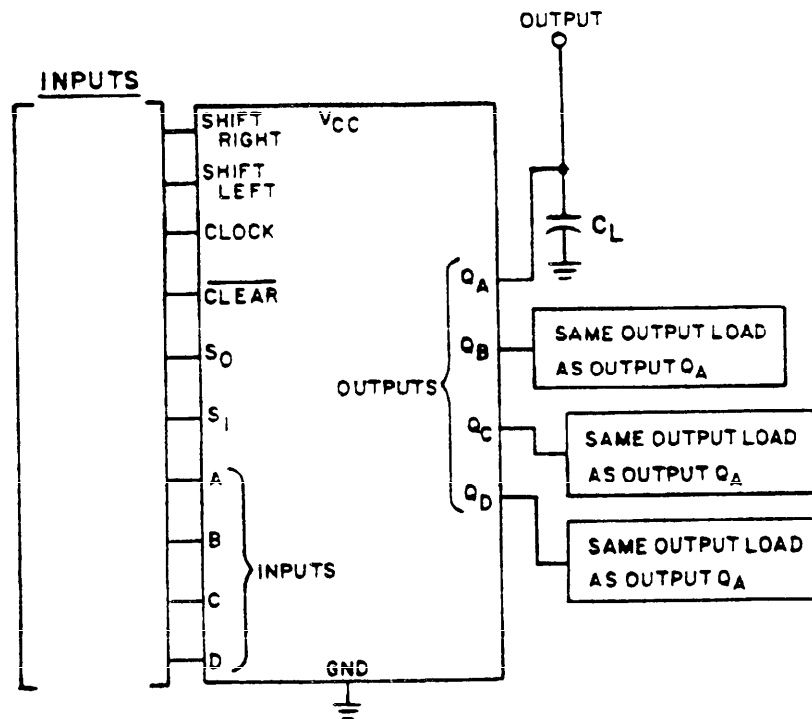
Device type 03

NOTES:

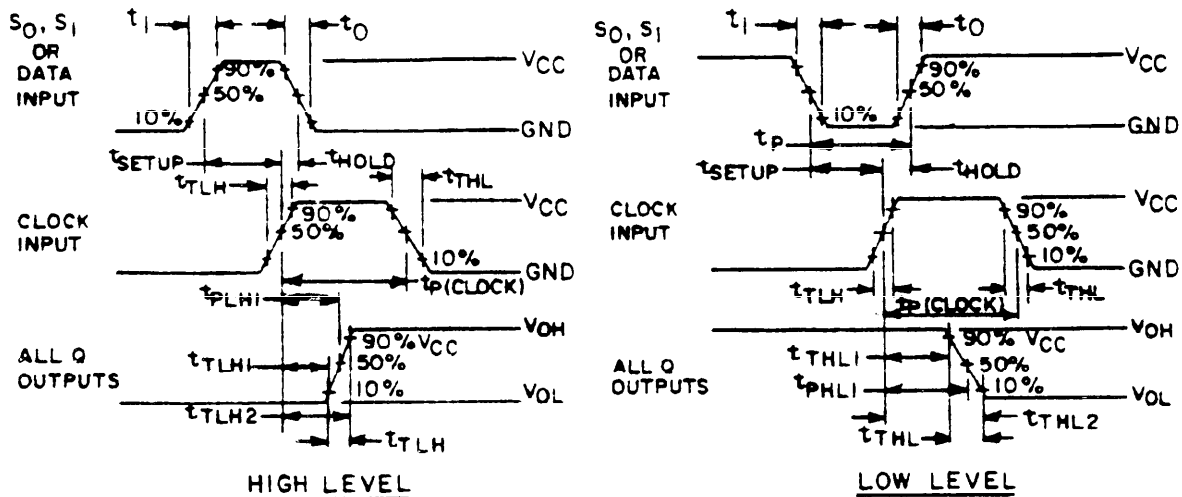
1. Clock pulse characteristics: clock, clock inhibit, $t_1 \leq 6$ ns, $t_0 \leq 6$ ns, 16 ns $\leq t_p$ (clock) ≤ 24 ns.
2. Serial or data pulse characteristics: $t_1 = t_0 \leq 6$ ns, 20 ns $\leq t_{SETUP} \leq 30$ ns, 10 ns $\leq t_{HOLD} \leq 15$ ns, 30 ns $\leq t_p$ (serial) or t_p (data) ≤ 45 ns.
3. Clear pulse characteristics: $t_1 = t_0 \leq 6$ ns, 25 ns $\leq t_p$ ($\overline{clear}$) ≤ 38 ns, 15 ns $\leq t_{REM} \leq 23$ ns.
4. Shift/ $\overline{Toad}$ pulse characteristics: $t_1 = t_0 \leq 6$ ns, 30 ns $\leq t_{SETUP} \leq 45$ ns, 5 ns $\leq t_{HOLD} \leq 8$ ns, 35 ns $\leq t_p$ ($\overline{Toad}$) ≤ 53 ns.
5. Clock inhibit pulse characteristics: $t_1 = t_0 \leq 6$ ns, 15 ns $\leq t_{SETUP} \leq 30$ ns, 10 ns $\leq t_{HOLD} \leq 15$ ns, 30 ns $\leq t_p$ (clock inhibit) ≤ 45 ns.
6. $C_L = 50$ pF $\pm 10\%$ including scope, probe, wiring and stray capacitance without package in test fixture.
7. For f_{MAX} tests, clock PRR = 21 MHz, 16 ns $\leq t_p$ (clock) ≤ 24 ns, serial, data PRR = 11 MHz, 30 ns $\leq t_p$ (data) ≤ 45 ns, $t_1 = t_0 \leq 6$ ns.
8. Prior to initiating tests, the output shall be placed in the proper state.
9. $t_{TLH} = t_{TLH2} - t_{TLH1}$, $t_{THL} = t_{THL2} - t_{THL1}$.

FIGURE 3. Switching test circuit and waveforms - Continued.

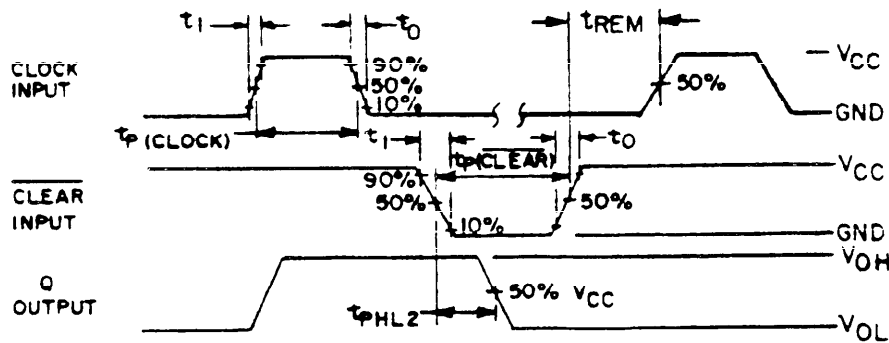
Device type 04

FIGURE 3. Switching test circuit and waveforms - Continued.

Device type 04



CLOCK TO OUTPUT WAVEFORMS (PARALLEL INPUT)



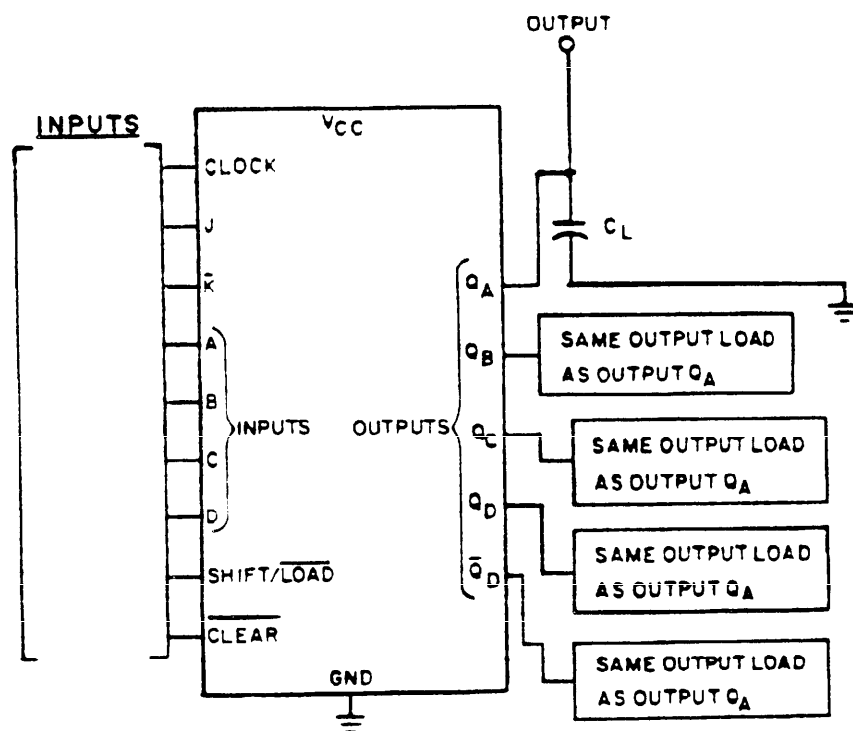
CLEAR TO OUTPUT WAVEFORMS

NOTES:

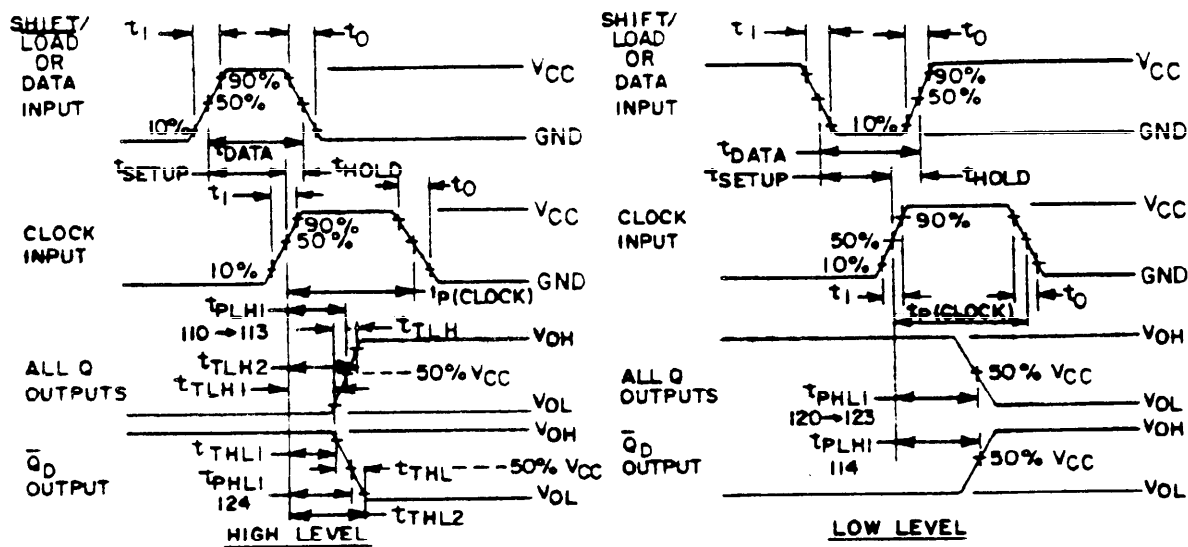
1. Clock pulse characteristics: $t_1 = t_0 \leq 6$ ns, 16 ns $\leq t_p$ (clock) ≤ 24 ns.
2. Mode (S_0, S_1), data pulse characteristics: $t_1 = t_0 \leq 6$ ns, 30 ns $\leq t_{SETUP} \leq 45$ ns, 5 ns $\leq t_{HOLD} \leq 8$ ns, 35 ns $\leq t_p$ (S_0, S_1) ≤ 53 ns, 25 ns $\leq t_p$ (data) ≤ 38 ns, 20 ns $\leq t_{SETUP}$ (data) ≤ 30 ns.
3. Clear pulse characteristics: $t_1 = t_0 \leq 6$ ns, 16 ns $\leq t_p$ (clear) ≤ 24 ns, 20 ns $\leq t_{REM} \leq 30$ ns.
4. $C_L = 50$ pF $\pm 10\%$ including scope, probe, wiring and stray capacitance without package in test fixture.
5. $t_{THL} = t_{THL2} - t_{THL1}$, $t_{TLH} = t_{TLH2} - t_{TLH1}$.
6. For f_{MAX} tests, clock PRR = 26 MHz, t_p (clock) ≥ 19 ns, data PRR = 13 MHz, t_p (data) ≥ 38 ns, $t_1 = t_0 \leq 6$ ns.
7. Prior to initiating tests, the output shall be placed in the proper state.

FIGURE 3. Switching test circuit and waveforms - Continued.

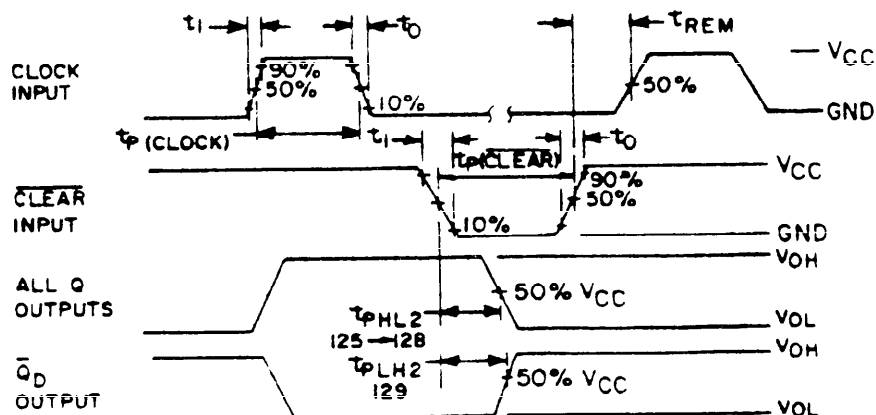
Device type 05

FIGURE 3. Switching test circuit and waveforms - Continued.

Device type 05



CLOCK TO OUTPUT WAVEFORMS (PARALLEL INPUT)



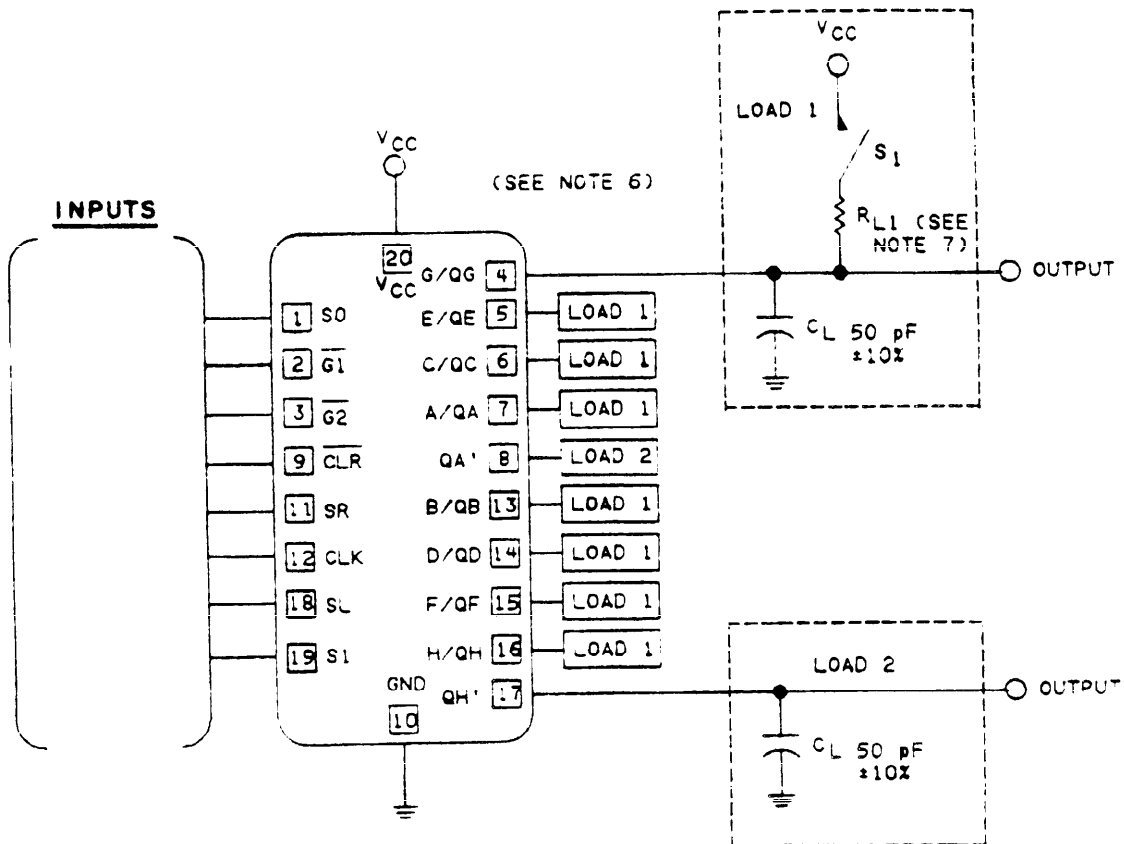
CLEAR TO OUTPUT WAVEFORMS

NOTES:

1. Clock pulse characteristics: $PRR = 1.0 \text{ MHz}$, $t_1 = t_0 \leq 6 \text{ ns}$, $16 \text{ ns} \leq t_p(\text{clock}) \leq 24 \text{ ns}$.
2. Data pulse characteristics: $t_1 = t_0 \leq 6 \text{ ns}$, $20 \text{ ns} \leq t_{SETUP} \leq 30 \text{ ns}$, $5 \text{ ns} \leq t_{HOLD} \leq 8 \text{ ns}$, $25 \text{ ns} \leq t_p(\text{shift/load}) \text{ or } t_p(\text{data}) \leq 38 \text{ ns}$.
3. Clear pulse characteristics: $t_1 = t_0 \leq 6 \text{ ns}$, $16 \text{ ns} \leq t_p(\text{clear}) \leq 24 \text{ ns}$, $20 \text{ ns} \leq t_{REM} \leq 30 \text{ ns}$.
4. $C_L = 50 \text{ pF} \pm 10\%$ including scope, probe, wiring and stray capacitance without package in test fixture.
5. For f_{MAX} tests, clock $PRR = 26 \text{ MHz}$, $t_p(\text{clock}) \geq 19 \text{ ns}$, data $PRR = 13 \text{ MHz}$, $t_p(\text{data}) \geq 38 \text{ ns}$, $t_1 = t_0 \leq 6 \text{ ns}$.
6. Prior to initiating tests, the output shall be placed in the proper state.
7. $t_{THL} = t_{THL2} - t_{THL1}$, $t_{TLH} = t_{TLH2} - t_{TLH1}$.

FIGURE 3. Switching test circuit and waveforms - Continued.

Device type 06



NOTES:

1. Clock pulse characteristics: $t_1 = t_0 \leq 6$ ns, 25 ns $\leq t_p$ (clock) ≤ 38 ns.
2. Serial input (SR/SL) pulse characteristics: $t_1 = t_0 \leq 6$ ns, 25 ns $\leq t_{\text{SETUP}} \leq 38$ ns, 5 ns $\leq t_{\text{HOLD}} \leq 8$ ns, 30 ns $\leq t_p$ data (serial) ≤ 46 ns.
3. Clear pulse characteristics: $t_1 = t_0 \leq 6$ ns, 25 ns $\leq t_p$ (clear) ≤ 38 ns, 20 ns $\leq t_{\text{REM}} \leq 30$ ns.
4. Three-state switching, the G, S0, or S1 input pulse characteristics: $t_1 = t_0 \leq 6$ ns, $t_p \geq 200$ ns.
5. For f_{MAX} tests, clock PRR = 17 MHz, $t_p(\text{clock}) \geq 29$ ns. The serial (SR/SL) input shall be one half the frequency of the clock and the serial $\uparrow$ and $\downarrow$ shall be coincident with the clock $\uparrow$ $t_1 = t_0 \leq 6$ ns.
6. $C_L = 50$ pF $\pm 10\%$ including scope, probe, wiring and stray capacitance without package in test fixture.
7. $R_{L1} = 1$ k Ω $\pm 5\%$.
8. Voltage measurements are to be made with respect to network ground terminal.

FIGURE 3. Switching test circuit and waveforms - Continued.

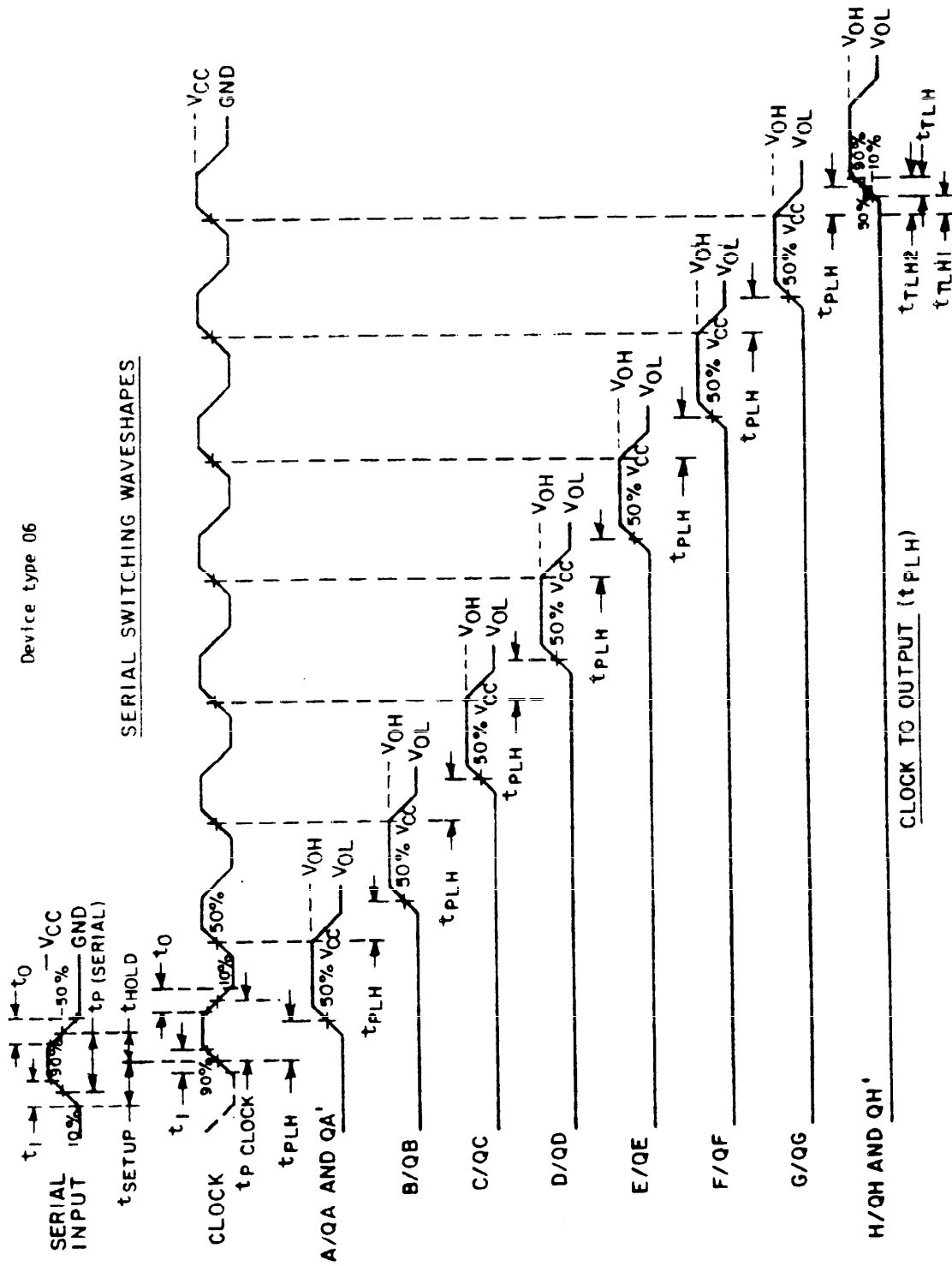


FIGURE 3. Switching test circuit and waveforms - Continued.

Device type 06

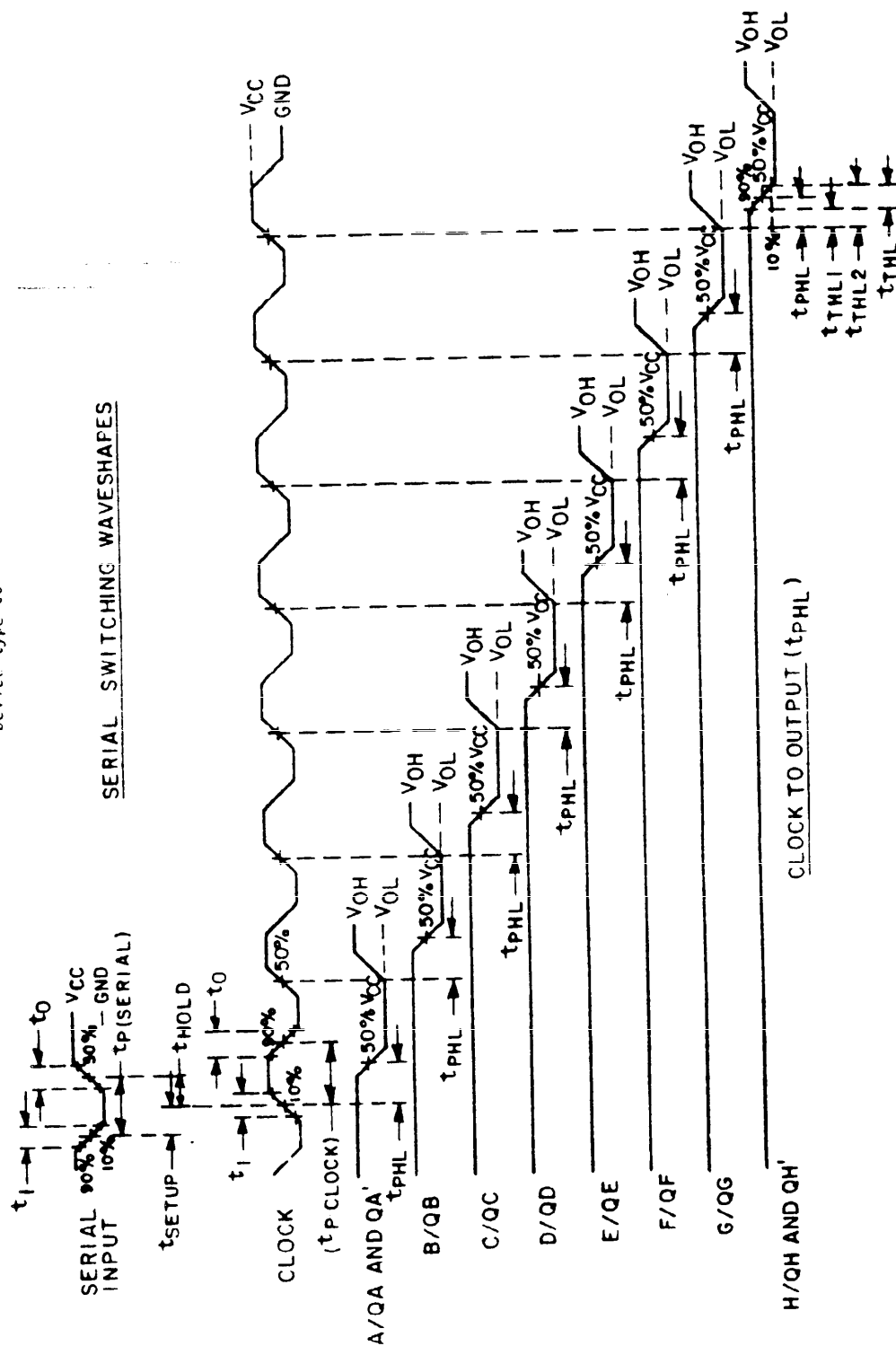
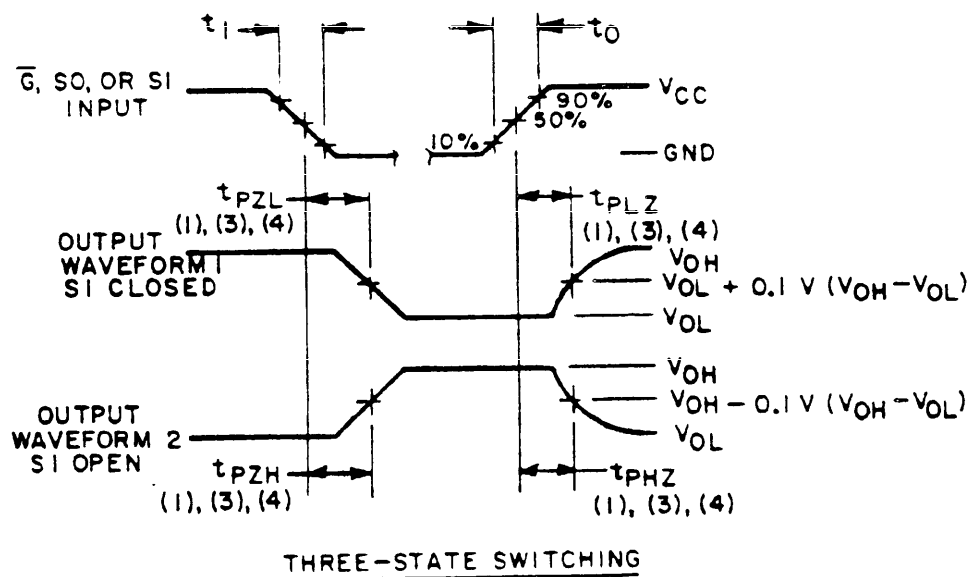
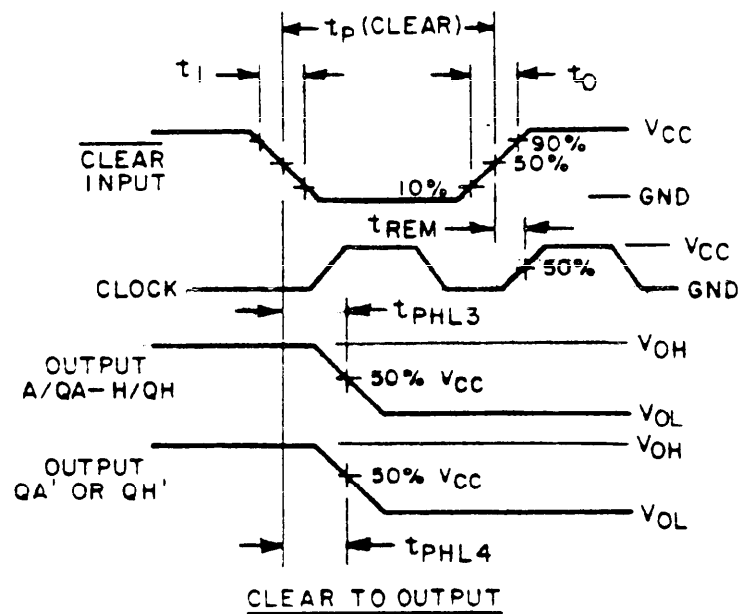
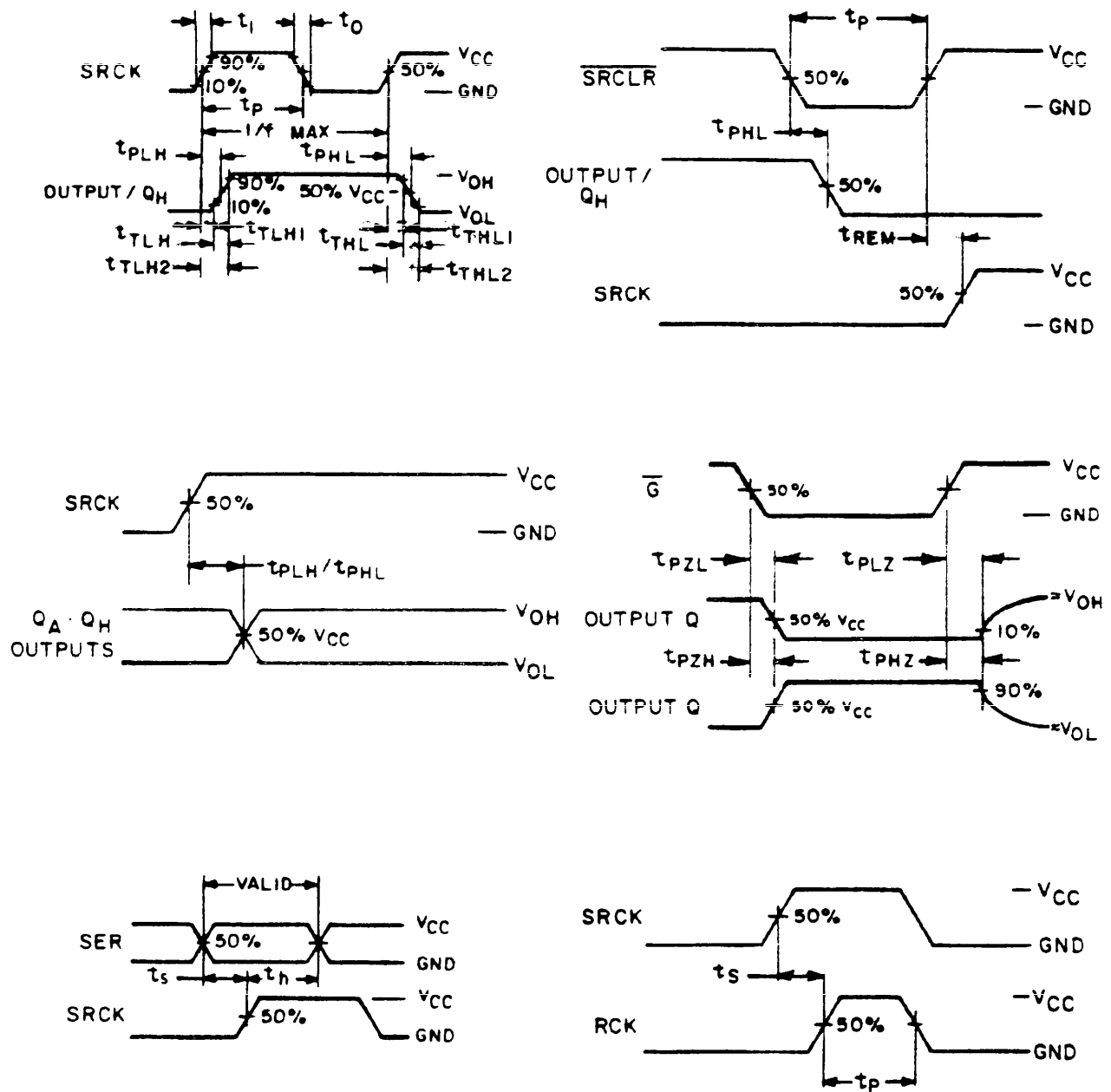


FIGURE 3. Switching test circuit and waveforms - Continued.

Device type 06

FIGURE 3. Switching test circuit and waveforms - Continued.

Device type 07

FIGURE 3. Switching test circuit and waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.1.1 Burn-in and life test circuits. Burn-in and life test circuits shall be constructed so that the devices are stressed at the maximum operating conditions stated 4.2b or 4.2c as applicable or equivalent as approved by the qualifying activity.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute lines 1 through 7 of table II herein.
- b. Static burn-in, test condition A method 1015 of MIL-STD-883.
 - (1) For static burn-in I, all inputs shall be connected to GND. Outputs may be open or connected to $V_{CC}/2$. Resistors R_1 are optional on both inputs and open outputs, and required on outputs connected to $V_{CC}/2 \pm 0.5$ V. $R_1 = 470$ to 47 k Ω .
 - (2) For static burn-in II, all inputs shall be connected through the R_1 resistors to V_{CC} . Outputs may be open or connected to required on outputs connected to $V_{CC}/2 \pm 0.5$ V. Resistors are optional on open outputs, and required on outputs connected to $V_{CC}/2 \pm 0.5$ V. $R_1 = 470$ to 47 k Ω .
 - (3) $V_{CC} = 6.0$ V ± 0.5 V.
- c. Dynamic burn-in, test condition D method 1015 of MIL-STD-883.
 - (1) Input resistors = 470Ω to 47 k Ω ± 20 percent.
 - (2) Output resistors = 1 k Ω for devices 01-05 and 670Ω for devices 06-07.
 - (3) $V_{CC} = 6.0$ V ± 0.5 V.
 - (4) $V_{CC}/2 = V_{CC}/2 \pm 0.5$ V.
 - (5) All clock inputs shall be connected through the resistors in parallel to a CP. All data and select (parallel 04, 05), (serial 02, 03), (serial 06) inputs shall be connected through the resistors in parallel to a CP/2. Outputs shall be connected to $V_{CC}/2$ through the resistors. Strobe (enable/disable), (06 and 07 pins 2, 3, and 19) input to ground; 01 tie pin 9 to V_{CC} , 02 tie pin 15 to ground, 04 tie pins 1, 2, 7, 9, and 10 to V_{CC} , 05 tie pins 1, 2, and 3 to V_{CC} and pin 9 to ground, 06 tie pins 1, 9, and 18 to V_{CC} , pins 2, 3, and 19 to ground.
 - (6) CP = 25 kHz to 1 MHz square wave; duty cycle = 50 ± 15 percent; $V_{IH} = 4.5$ V to V_{CC} , $V_{IL} = 0$ V ± 0.5 V; t_r , $t_f \leq 500$ ns.
- d. Interim and final electrical parameters shall be as specified in table II herein.
- e. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.1 Percent defective allowable (PDA).

- a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.
- b. Static burn-in I and II failures shall be cumulative for determining the PDA.
- c. The PDA for class B devices shall be in accordance with MIL-M-38510 for static burn-in. Dynamic burn-in is not required.
- d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table III, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510, and 4.3.1 herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D, inspections (see 4.4.1 through 4.4.5).

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. The option to categorize devices as ESD sensitive without performing the test, is not allowed. Only those device types that pass ESDS testing at 1,000 volts or greater shall be considered as conforming to the requirements of this specification. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be performed in accordance with table II herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_1 , C_C , and C_0 measurement) shall be measured only for initial qualification and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on 5 devices with no failures.
- d. Subgroups 9 and 11 shall be measured only for initial qualification and after process or design changes which may affect dynamic performance.
- e. Subgroups 7 and 8 tests sufficient to verify truth table, except three-state output conditions need not be verified.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

- a. Class S steady-state life (accelerated) shall be conducted using test condition D and the circuit described in 4.2c herein, or equivalent as approved by the qualifying activity.
- b. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IV herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table III herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) shall be conducted using test condition D and as specified in 4.5.2 herein using a circuit as described in 4.2c herein, or equivalent as approved by the qualifying activity.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

TABLE III. Delta limits at +25°C.

Parameter ^{1/}	Device types	
	All	
I _{CC} , I _{CCH} , I _{CCL}		±30 nA

^{1/} The above parameters shall be recorded before and after the required burn-in and life tests to determine deltas (Δ).

4.4.5 Group E inspection. Group E inspection shall be in accordance with table V of method 5005 of MIL-STD-883. End point electrical parameters shall be specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Burn-in and life test cool down procedures. When the burn-in and life tests are completed and prior to removal of bias voltages, the devices under test (DUT) shall be cooled to within +10°C of their power stable condition at room temperature; then, electrical parameter end-point measurements shall be performed.

4.5.3 Quiescent supply current (I_{CC} test). When performing quiescent supply current measurements (I_{CC}), the meter shall be placed so that all currents flow through the meter.

4.6 Data reporting. When specified in the purchase order or contract, a copy of the following data, as applicable, shall be supplied.

- a. Attributes data for all screening tests (see 4.2) and variables data for all static burn-in, dynamic burn-in, and steady-state life tests (see 3.5).
- b. A copy of each radiograph.
- c. The quality conformance inspection data (see 4.4).
- d. Parameter distribution data on parameters evaluated during burn-in (see 3.5).
- e. Final electrical parameters data (see 4.2c).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Acquisition requirements. The acquisition documents must specify the following:

- a. Title, number, and date of the specification.
- b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1).
- c. Complete PIN (see 6.7).
- d. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- e. Requirements for certificate of compliance, if applicable.
- f. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- g. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- h. Requirements for product assurance options.
- i. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the PIN. Unless otherwise specified, these requirements shall not apply to direct purchase by, or direct shipment to the Government.
- j. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

C_i	- - - - -	Input terminal-to-GND capacitance.
GND	- - - - -	Ground zero voltage potential.
ICC	- - - - -	Quiescent supply current.
T_C	- - - - -	Case operating temperature range.
VCC	- - - - -	Positive supply voltage.
C _{pd}	- - - - -	Power dissipation capacitance

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class S for National Aeronautics and Space Administration or class B for Department of Defense (see 1.2.2), lead finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	54HC164
02	54HC165
03	54HC166
04	54HC194
05	54HC195
06	54HC299
07	54HC595

6.6 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protective devices have been designed in the chip to minimize the effect of this static build up. However, the following handling practices are recommended:

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment and tools.
- c. Do not handle devices by the leads.
- d. Avoid use of plastic, rubber, or silk in MOS areas.
- e. Maintain relative humidity above 50 percent, if practical.

6.7 PIN. The PIN shall be in accordance with MIL-M-38510, and as specified herein.

CONCLUDING MATERIAL

Custodians:
 Army - ER
 Navy - EC
 Air Force - 17
 NASA - NA

Review activities:
 Army - AR, MI
 Air Force - 11, 19, 85, 99
 DLA - ES

User activities:
 Army - SM
 Navy - AS, CG, MC, OC, SH

Preparing activity:
 Air Force - 17

Agent:
 DLA - ES

(Project 5962-1129)