

INCH-POUND

MIL-M-38510/607A
29 JANUARY 1992
SUPERSEDING
MIL-M-38510/607
6 JULY 1988

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, CMOS SEMICUSTOM (GATE ARRAY) DEVICES, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, complimentary oxide insulated silicon gate semiconductor, semicustom (gate array) devices. Two product assurance classes (B and S) and a choice of case outlines and lead finishes are provided for each type, and are reflected in the complete Part or Identifying Number (PIN).

Customizations (personalizations) for each design, including circuit organization, electrical performance characteristics, and test conditions, shall be specified in an Altered Item Drawing (AID) (see 3.2 herein).

1.2 PIN. The PIN shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device types. The device types (total number of usable gates) and circuit organization shall be as identified in the specific AID and as follows:

<u>Device type</u>	<u>Circuit</u>
01	0 - 1,000 gate array
02	1,001 - 2,000 gate array
03	2,001 - 3,000 gate array
04	3,001 - 4,000 gate array
05	4,001 - 5,000 gate array
06	5,001 - 6,000 gate array
07	6,001 - 7,000 gate array
08	7,001 - 8,000 gate array
09	8,001 - 9,000 gate array
10	9,001 - 10,000 gate array
11	10,001 - 11,000 gate array
12	11,001 - 12,000 gate array
13	12,001 - 15,000 gate array
14	15,001 - 25,000 gate array
15	25,001 - 35,000 gate array
16	35,001 - 45,000 gate array
17	45,001 - 55,000 gate array
18	55,001 - 65,000 gate array
19	65,001 - 75,000 gate array
20	75,001 - 85,000 gate array

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Laboratory (RL/ERDS), Griffiss AFB, NY 13441-5700, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.2.3 Case outlines. The case outlines and letters shall be in accordance with MIL-M-38510, appendix C.

Outline letter	Case outline	Manufacturers (see table V)
M	P-8J (209-pin, square pin grid array) 1/	B
N	C-66 (84-terminal, leaded square chip carrier package with unformed leads)	B
T	P-8J (208-pin, square pin grid array)	B
U	P-AC (84-pin, square pin grid array)	A
X	C-7 (68-terminal, square chip carrier package)	C
Y	C-8 (84-terminal, square chip carrier)	D
Z	P-AG (180-pin, square chip carrier)	B
4	224-terminal, leaded chip carrier (see figure 1)	B
5	256-terminal, leaded chip carrier (see figure 1)	B
6	304-terminal, leaded chip carrier (see figure 1)	B

1.3 Absolute maximum ratings.

Supply voltage range	- - - - -	-0.3 V dc to +7.0 V dc
DC input, dc output voltage ranges (V_{IN} , V_{OUT})	- - - - -	-0.3 V dc to (V_{DD} +0.3 V dc)
Storage temperature range	- - - - -	-65°C to +150°C
Maximum junction temperature (T_J)	- - - - -	+175°C
Thermal resistance, junction-to-case (Θ_{JC}):		
4, 5, and 6	- - - - -	10°C/W
All others	- - - - -	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	- - - - -	4.5 V dc to 5.5 V dc
DC input voltage	- - - - -	0 V dc to V_{DD}
Case operating temperature range (T_C)	- - - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-976 - Certification Requirements for JAN Microcircuits.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

1/ The terminal E6 is used as a keying pin.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN NATIONAL STANDARDS INSTITUTE, INC. (ANSI)

ANSI Y14.5M-82 - Dimensioning and Tolerancing.

(Applications for copies should be addressed to American National Standards Institute, Inc. (ANSI), 1430 Broadway, New York, NY 10018.)

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 12 - Standard for Gate Array Benchmark Set.

JEDEC Standard No. 12-3 - CMOS Gate Array Macrocell Standard.

(Applications for copies should be addressed to the Electronic Industries Association, 2001 Eye Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations which prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained. The AID that forms a part of this specification shall not take precedence over the requirements of this specification. ^{1/}

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 AID requirements. The following items must be provided to the device manufacturer by the customer as part of an AID.

3.2.1 Terminal connections and pin assignments.

3.2.2 Package type (see 1.2.3).

3.2.3 Functional block diagram.

3.2.4 Functional description, terms, and symbols.

3.2.5 Logic diagram.

3.2.6 Pin function description.

3.2.7 Schematic circuits. Schematic circuits in terms of the JEDEC Standard No. 12-3, "CMOS Gate Array Macrocell Standard" or the manufacturer's "CMOS Gate Array Macrocell Library".

^{1/} An AID contains all essential information (design, test, etc.) regarding a particular customer personalization of a gate array microcircuit.

3.2.8 Fault grading. The manufacturing level logic test vectors shall be graded for fault coverage using a fault simulator. The resulting fault coverage shall be reported in the AID. For devices qualified on or after 1 January 1991, fault coverage shall be measured and reported in accordance with MIL-STD-883, test method 5012. For devices qualified prior to 1 January 1991, it is not a requirement that fault coverage be measured and reported in accordance with test method 5012; however, any differences between methods used for fault coverage and reporting, and test method 5012, shall be noted in the AID. For class S only, the fault coverage of 90 percent minimum shall be achieved.

3.2.9 Device electrical performance characteristics. Device electrical performance characteristics shall include dc parametric (see table I herein for minimum requirements), functional, and ac parameter. All electrical performance characteristics apply over the full recommended case operating temperature range and specified test load conditions. The total capacitive load shall be specified in all switching limits and shall be based on the defined load. When group E qualification or quality conformance inspection is required, postirradiation test parameters shall be specified in AID.

3.2.10 Timing diagram. Timing diagram shall show all critical interrelated inputs and outputs. Timing diagrams shall consist of one or more diagrams showing critical interrelationships between two or more signals. Timing requirements such as setup and hold times shall also be shown.

3.2.11 Burn-in circuit. The burn-in circuit shall be as described on figure 2 herein for the AID device. The actual values and conditions for burn-in shall be described in the AID.

3.2.12 Maximum power dissipation. Maximum power dissipation shall be in accordance with the application specific design.

3.2.13 Total dose bias circuit (see 4.4.5.1c).

3.3 Case outlines. Case outlines shall be as specified in MIL-M-38510, appendix C, and 1.2.3 herein.

3.4 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.5 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510.

3.6 Electrical performance characteristics. Each manufacturer shall submit to the qualifying activity a data sheet defining the gate array family being qualified. The data sheet shall contain all dc parametric, ac functional and parametric data, and any other data which is manufacturer-dependent but would be considered required by a design engineer. All devices, regardless of manufacturer, must meet the minimum dc parameter limits in table I. All electrical performance characteristics apply over the full recommended case operating temperature range. (The standard evaluation circuit (SEC) (see 4.3.2.2) electrical performance characteristics are as specified in the AID for each manufacturer's SEC.)

3.7 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups in table II herein. The electrical tests for each subgroup are described in the AID (for the user design) and in the AID for each manufacturer's SEC. The electrical test requirements shall, as a minimum, follow the requirements on figure 3 and table III herein.

3.8 Marking. Marking shall be in accordance with MIL-M-38510. The AID number shall be added to the marking by the manufacturer. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.8.1 Total dose radiation hardness identifier. The total dose radiation hardness identifier shall be in accordance with MIL-M-38510 and as specified herein.

3.9 Additional line certification requirements. In addition to the requirements of MIL-STD-976, the following documentation shall be provided to the qualifying activity for review and approval. The documentation will remain on file for internal Government use only.

- a. Design layout rules as a manufacturer's controlled document.

- b. A list of the macros in the manufacturer's macrocell library, macrocell performance data, and macrocell simulation verification data (see 4.3.2.3). The procedure(s) and supporting data that demonstrate correlation between process variations and macrocell performance and simulation shall be provided. The procedure(s) used by the manufacturer for change control and for adding new macrocells to the library shall be provided.
- c. Process control monitor design used by the manufacturer for qualification and wafer acceptance (see 4.3.2.1).
- d. SEC implementation in the form of an AID (see 4.3.2.2 for discussion of this circuit) used by the manufacturer for qualification and quality conformance inspection. (SEC design detail, test vectors, and all required information will be contained in the AID for each manufacturer's SEC.)
- e. JEDEC 12 gate array benchmark set (see appendix and 4.3.2.4) delay simulation data.
- f. A list of the software packages (including names and current version) used by the manufacturer in the gate array design process.
- g. Design rule check (DRC) and electrical rule check (ERC) software verification. The manufacturer's DRC and ERC software shall be run on a design which contains known rule violations; the output shall be presented to the qualifying activity and must show the violations were flagged.
- h. Layout versus schematic (LVS) checker. Manufacturer must demonstrate the effectiveness of the LVS software.
- i. Fault simulators, used for qualification. Documentation use in accordance with 3.2.8 herein.

3.10 Functional delay simulation. To be retained by manufacturer; simulation to be derived from each final application specific electrical design and layout (i.e., post-routed design). Simulation shall be done using actual delays as computed from the placement and layout of the device as it will be fabricated. Actual delays shall include the contribution associated with the delay through the gate, as well as the contribution due to actual metal capacitance and loading on the output(s). Using these actual delays, the application specific design shall insure that there are no timing violations remaining in the circuit. Such timing violations shall include, but not be limited to, setup, hold, critical delay path(s), and circuit race conditions due to variations in process, temperature, and supply voltage. The simulated circuit behavior at the two (fast and slow) worst case extremes of temperature, supply voltage and process shall be identical states at the specified strobe time (usually at the end of a typical clock cycle where all signals are stable). The functional delay simulation shall be approved by the customer before the design is released for production build.

3.11 Layout verification. The manufacturer shall retain the results of full, mask level DRC's, ERC's, and connectivity checks for each application specific design. Rule checking will encompass the rules set provided under 3.9a herein. The manufacturer will explain any rules not checked and all error reports produced by the checker. The LVS check will ensure that the layout matches exactly the logic schematic simulated by the application specific integrated circuit (ASIC) designer.

3.12 Power routing simulation. 2/ To be retained by the manufacturer; simulation to be derived from each final application specific electrical design and layout. The worst case simulation of power busses shall show that at no time shall the localized bus current density exceed specification for allowable current density of the power bus material as defined in MIL-M-38510. In addition, at no point in the power bus shall voltage levels exceed recommended IR drop values from the respective supply. Power routing simulation must be based upon actual placement of cells within the array. Such a simulation may be driven by Monte Carlo methods, or in conjunction with a digital event driven simulator using the selected set of test vectors.

2/ A manufacturer may use an alternate method for power routing simulation of specific gate array type (see 1.2.1) without accounting for specific personalizations of the array. Such an alternate would be a worst case simulation of each gate array device type (see 1.2.1) by populating all cell positions with the worst case power consumption cells (i.e., 100 percent utilization). Such a simulation must switch all transistors simultaneously at maximum rated frequency and operating voltage. The contribution to the current density from the output buffers should reflect a TTL load capacitance of 50 picofarads, as well as the TTL dc load current.

3.13 Procedure for updating certified software packages. Each manufacturer shall submit to the qualifying activity, for review, the procedure used for approval of updates and revisions of certified software packages (see 3.9f). This procedure shall outline the method and provide test descriptions regarding the process used to accept/reject updates and revisions to in-house or commercially supplied software packages. This requirement only applies to software packages used by the manufacturer in the gate array design process.

3.14 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 123 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.1.1 Wafer lot acceptance procedure. Each manufacturer shall submit to the qualifying activity for approval, a "Wafer Lot Acceptance Procedure". This procedure shall outline and provide limits regarding the process used to accept or reject a wafer lot. The procedure shall include:

- a. For class S product, the wafer lot acceptance requirements in method 5007 of MIL-STD-883 shall be met. For class B product, the physical measurements of wafer metallization, glassivation, and gold backing shall be in accordance with method 5007 of MIL-STD-883.
- b. Electrical measurements using the process monitor (PM). (NOTE: The PM may be dedicated drop-in or a set of structures in the kerf or scribe line.)
- c. Visual inspection to include:
 1. High magnification examination on a sample basis.
 2. Optical test structures to insure alignment, etc.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute lines 1 through 7 of table II herein.
- b. Burn-in, method 1015 of MIL-STD-883.
 1. Static tests (test condition A) using circuit shown on figure 2. Actual values and conditions for burn-in shall be specified in the AID. T_A shall be $+125^{\circ}\text{C}$ minimum. Test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table I of method 1015 for class B devices.
 2. Dynamic test (test condition D) using circuit shown on figure 2. Actual values and conditions for burn-in shall be specified in the AID. T_A shall be $+125^{\circ}\text{C}$ minimum. Test duration shall be in accordance with table I of method 1015.
- c. Interim and final electrical parameters shall be as specified in table II herein.
- d. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed or included in the final electrical parameter requirements.
- e. Constant acceleration shall be in accordance with test condition D, method 2001 of MIL-STD-883.
- f. For JAN class S only, an alternate procedure to the 100 percent non-destructive bond pull may be acceptable with qualifying activity approval. This procedure shall be part of the manufacturer's screening flow and must be available upon request.

4.2.1 Percent defective allowable (PDA).

- a. The PDA for static and dynamic burn-in for class S devices shall be 5 percent on subgroups 1 and 7 combined, and 3 percent on subgroup 7 alone. The PDA for the static burn-ins and the dynamic burn-in shall be based on the exact number of devices submitted to each separate burn-in.
- b. Static burn-in I and II failures shall be cumulative for determining the static burn-ins PDA.
- c. The PDA for class B devices shall be 5 percent on subgroup 1 for static burn-in. Dynamic burn-in is not required, but may be used as an alternate screen at manufacturer's option.
- d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits specified in table IV herein, or electrical parameter limits specified in table III, subgroup 1 (subgroups 1 and 7 for class S), are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection.

4.3.1 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510, and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5 herein). In addition, the five-phased qualification outlined below shall be performed through the use of the identified qualification vehicles.

4.3.2 Qualification phase and vehicles.

<u>Qualification phase</u>	<u>Qualification vehicles</u>
Control and stability	Process monitor (PM) die
Process reliability	Standard evaluation circuit (SEC)
Macrocell design and simulation	Macro test chip set
CAD routing and post routing simulation	JEDEC standard for gate array benchmark set
Design check software verification	Manufacturer test case

NOTE: Qualification of the macrocell design and simulation, and CAD and post routing simulation will be based on the manufacturer's ability to design, place and route, and manufacture devices where actual measured performance characteristics (i.e., propagation delays, rise and fall times, drive characterization, trigger levels etc.) are within simulated device performance limits (see 4.3.2.4).

4.3.2.1 Process control and stability. Process control and stability of dc parameters must be demonstrated through the use of the manufacturer's PM. The PM (either a dedicated drop-in or structures fabricated in the kerf) shall be designed so that the dc process parameters (ac parameters may be included as a manufacturer's option) may be measured in wafer form or packaged device form. The PM design must be submitted to the qualifying activity for approval prior to use for qualification and must contain, as a minimum, the following structures:

- a. N channel device (minimum geometry).
- b. P channel device (minimum geometry).
- c. N channel device (large device).
- d. P channel device (large device).
- e. Sheet resistance measurement structure.
- f. Metal step coverage structure. In-line Scanning Electron Microscope (SEM) monitor is an acceptable monitor as approved by the qualifying activity.
- g. Field threshold device(s).

- h. Intermetal oxide integrity structure.
- i. Contact chains (to be sufficient length to be representative of the contact resistance). The contact size must be the same as in the actual circuit.
 - 1. Metal to poly (where applicable).
 - 2. Metal 1 to metal 2 (where applicable), via resistance.
 - 3. Gated inverter chain(s) (for ac measurement; may be included as a manufacturer's option).
 - 4. Metal to diffusion (where applicable).

For qualification, PM's on a minimum of 3 different lots (minimum of 4 PM's per wafer) shall be measured to insure the establishment of a statistically valid data base on which a decision can be made as to whether the manufacturer's process is stable and under control. Non-JAN lots recently processed on the certified line can be used to satisfy this requirement with the qualifying activity's approval. (For production wafer lots, measurement of PM parameters will be required for wafer lot acceptance (see 4.1.1).)

4.3.2.2 Process reliability. The process reliability is to be qualified using the manufacturer's SEC. The SEC design shall be submitted to the qualifying activity for approval prior to use in the form of a manufacturer's AID, and as such shall contain the basic information as detailed in 3.2. It shall be fabricated with the same process that will produce any application specific gate array device under this detail specification. The SEC design shall be configured in such a manner so as to evaluate the reliability of the underlayer designs (diffusions, etc.) and evaluate worst case design rule conditions on the personalization layers. The design should utilize library macrocells to form oscillator rings and also include test structures which will detect metal-to-metal shorting or opening, and dielectric pinholes during reliability life testing. The SEC shall be implemented on the largest member (i.e., number device type with the largest number of gates and if applicable with the highest pin count package of the gate array family). Smaller gate count members of a manufacturer's gate array family in the highest pin count package or in smaller pin count packages may be qualified by extension (see 4.3.3).

The SEC will also be the main qualification vehicle for the electrical testing which follows (4.4.1, 4.4.2, 4.4.3, and 4.4.4). Test limits appear in the AID (see table I herein for minimum dc parameters) for each manufacturer's SEC. The electrical tests for each subgroup shall be described in table III. The SEC shall be suitable for static bias aging, as life testing will be performed on this device (see 4.4.3).

4.3.2.3 Macrocell design and simulation qualification. The macrocell design and simulation qualification shall be accomplished in a two step procedure consisting of parameter verification or simulation and functional verification.

A chip shall be designed to provide access to a set of macrocells to test performance characteristics. These macrocells are a subset of the JEDEC Standard No. 12-3, "CMOS Gate Array Macrocell Standard"; macrocell substitutions are allowable only if the manufacturer does not offer a particular macrocell, and such substitutions must be approved by the qualifying activity. The set of macrocells shall include:

<u>Macrocell (*)</u>	<u>Description</u>
JIV1	Inverter
JND4	4-input NAND
JA012	2-input AND into 3-input NOR
JLDR1	D latch with reset
JFJKR1	JK flip-flop with active low reset
JB1T1	TTL input buffer
JB1C1	CMOS input buffer
JB01	Output buffer
JB1B2	3-state I/O buffer with pull up

(*) JEDEC naming convention

The intent is to get a representative cross section of macrocell types (i.e., combinational, sequential, input, output). Chains shall be formed (when necessary to avoid rise and fall time measurement problems) and actual performance data over the full operating range shall be taken (a provision to extract for multiplexing and I/O buffer delay shall be included). Delay versus metal wire length and fanout for the above macrocells shall be determined. The actual performance data shall be submitted to the qualifying activity along with computer program simulation results. The actual performance data must be within the limits predicted by the simulation. If multipliers are used to extrapolate performance at the temperature extremes, such multipliers shall be verified as well.

In addition, for the above macrocells, a set of pins shall be provided on the test chip for observability. This will enable a verification of functionality of the macrocells. (NOTE: Inputs and outputs may be multiplexed.)

4.3.2.4 CAD routing and post routing simulation. A chip or set of chips incorporating JEDEC Standard No. 12, "Standard for Gate Array Benchmark Set" (see appendix herein) shall be used to qualify the manufacturer's ability to perform routing and to accurately predict post routing performance. The qualifying activity may approve the use of an equivalent test chip(s) to demonstrate routing and prediction of post routing performance. The manufacturer must submit to the qualifying activity:

- a. The actual measured performance data for each function in the benchmark over temperature and voltage.
- b. The computer simulation performance prediction. The two results will remain on file and the actual measured performance must fall between the two worst case (i.e., fast worst case $V_{CC} = 5.5$ V at -55°C and slow worst case $V_{CC} = 4.5$ V at $+125^{\circ}\text{C}$) simulation performance prediction limits.

4.3.2.5 Design check software verification. The manufacturer shall verify that the DRC, ERC, and LVS software is capable of performing the intended function. This shall be accomplished by running a design with known errors against the design check software and demonstrating that the errors were caught.

4.3.3 Microcircuit qualification extension. For qualification extension if a manufacturer part I qualifies the SEC (i.e., the highest gate count array) in the highest pin count package type, then lower gate count arrays in that package type that are manufactured identically (i.e., same line, same process) as the SEC may be part I qualified upon the approval of the qualifying activity.

- a. Lower gate count arrays in lower pin count packages that are manufactured identically (i.e., same line, same process) as the SEC may be part I qualified upon approval of the qualifying activity using another die provided the gate utilization is 60 percent or greater and by conducting group A electrical tests, unless otherwise approved by the qualifying activity.
- b. Lower pin count packages from the same package family, and same construction and assembly techniques, may be part I qualified without performing additional qualification testing upon approval by the qualifying activity. If required by the qualifying activity, package extension qualification testing will be conducted in accordance with MIL-M-38510.

TABLE I. DC electrical performance characteristics and postirradiation end-point electrical parameter limits. 1/ 2/

Test	Symbol		Conditions	Limits		Unit	
				Min	Max		
High level output voltage	VOH	TTL	IOH = -2 mA 3/		2.4	V	
				M, D, R, H	2.4		
		CMOS	IOH ≤ 1 μA		VDD -0.05		
				M, D, R, H	VDD -0.05		
Low level output voltage	VOL	TTL	IOL = 2.0 mA 3/		0.4	V	
				M, D, R, H	0.4		
		CMOS	IO ≤ 1 uA		0.05		
				M, D, R, H	0.05		
High level input voltage	VIH	TTL		4/ 2.0		V	
				M, D, R, H	2.2		
		CMOS			.7 VDD		
				M, D, R, H	.7 VDD		
Low level input voltage	VIL	TTL			0.8	V	
				M, D, R, H	0.8		
		CMOS			.3 VDD		
				M, D, R, H	.3 VDD		
Input capacitance	CIN		Freq = 1 MHz at 0 V		10	pF	
Output capacitance	COUT		Freq = 1 MHz at 0 V		20	pF	
Input current 5/	IIN		VIN= VDDor VSS	-1 6/	+1 7/	μA	
				M, D, R, H	-10		+10

See footnotes at end of table.

TABLE 1. DC electrical performance characteristics and postirradiation end-point electrical parameter limits - Continued. 1/ 2/

Test	Symbol	Conditions	Limits		Unit
			Min	Max	
Three-state output leakage current 5/	I _{OZ}	V _{OUI} = V _{DD} or V _{SS}	-10	+10	μ A
		M, D, R, H	-10	+10	

1/ This table comprises a core set of performance parameters; all products regardless of manufacturer, shall be within the specified limits.

2/ Limits apply for: $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$, $V_{DD} = 5\text{ V} \pm 10\%$.

3/ Measure voltage levels using the maximum load current specified in the AID for each output.

4/ Radiation hardened technology may have a V_{IHP} pre-irradiation minimum limit of 2.2 V.

5/ This test applies only to non pull up or pull down devices.

6/ This limit shall be $-10\text{ }\mu\text{A}$ at -55°C .

7/ This limit shall be $+10\text{ }\mu\text{A}$ at -55°C .

TABLE 1B. Single event phenomena (SEP) test limits. 1/ 2/

Device type	Temperature ($\pm 10^{\circ}\text{C}$)	Memory pattern	V _{DD} = 4.5 V Effective LET no upsets (MeV/(mg/cm ²)) ²	Bias for latchup test V _{DD} = 5.5 V no latchup LET

1/ This blank table will be filled when a qualified vendor exists.

2/ For SEP test conditions see 4.4.5.2 herein.

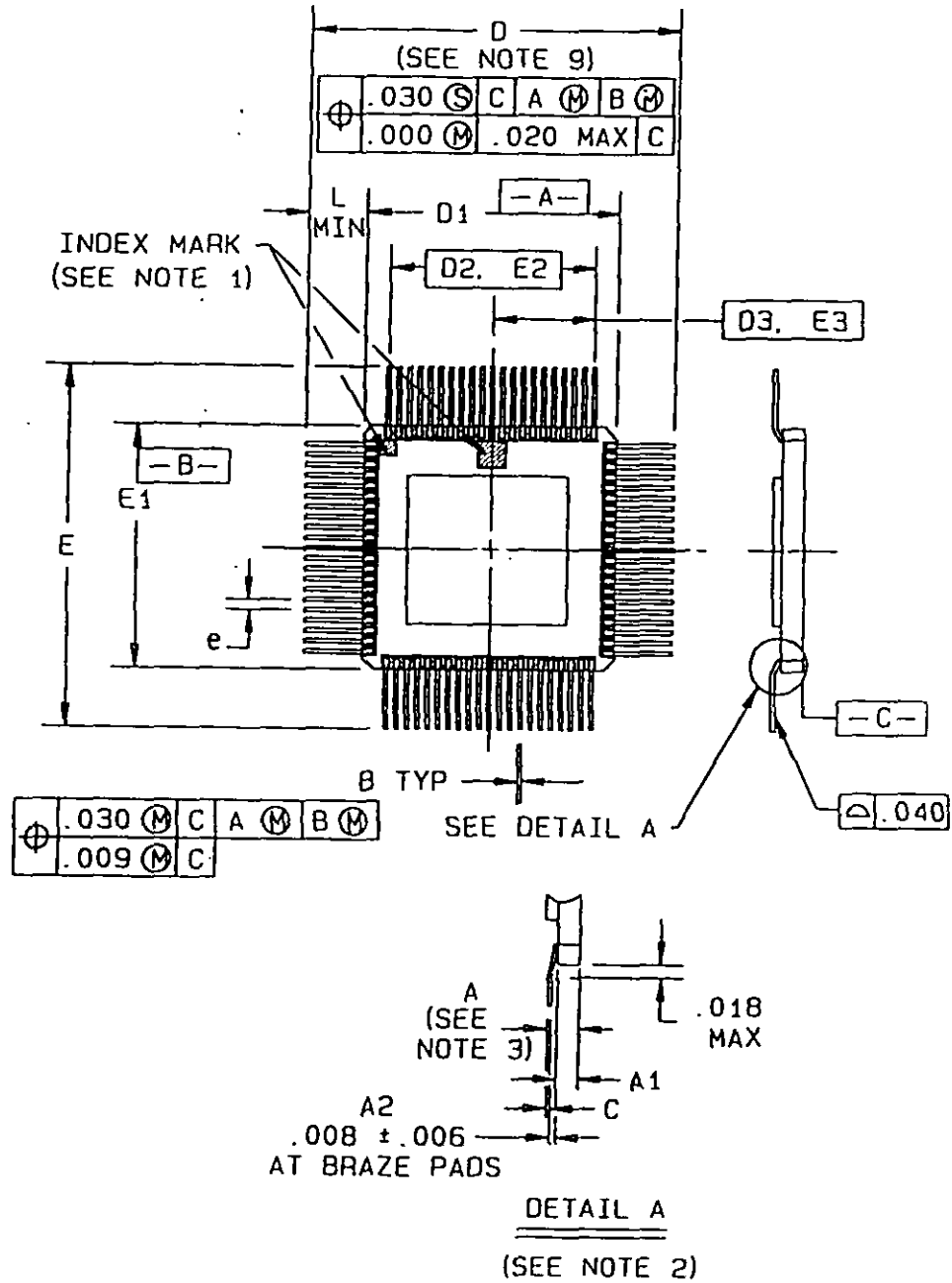


FIGURE 1. Case outlines.

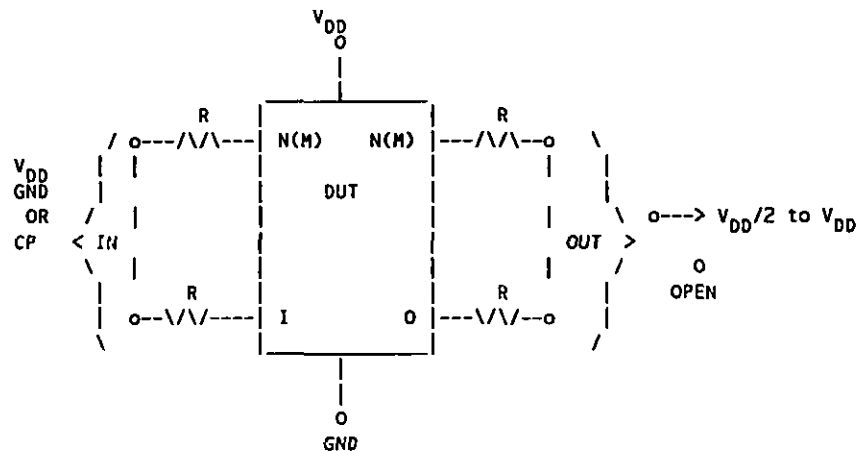
Symbol	Case 4				Case 5				Case 6			
	Min	Nom	Max	Notes	Min	Nom	Max	Notes	Min	Nom	Max	Notes
A	---	---	.130	3	---	---	.130	3	---	---	.130	3
A1	---	---	.105		---	---	.105		---	---	.105	
B	.006	.008	.012		.006	.008	.012		.006	.008	.012	
C	.005	.007	.010		.005	.007	.010		.005	.007	.010	
D, E			2.870				2.870				2.870	
D1, E1	1.515	1.525	1.535	5	1.445	1.460	1.475	5	1.635	1.650	1.665	
D2, E2	1.375 BSC				1.260 BSC				1.500 BSC			
D3, E3	.6875 BSC				.630 BSC				.750 BSC			
e	.025 BSC				.020 BSC				.020 BSC			
L	.380	---	---	6	.420	---	---	6	.455	---	---	6
N	224			7	256				304			
ND	56			8	64				76			

FIGURE 1. Case outlines - Continued.

NOTES:

1. An index mark shall be located within the shaded area shown.
2. Generic lead attach dogleg depiction. May be flat lead configuration.
3. Includes lead attach dogleg height and lid height, whichever is greater.
4. Corner chamfers or notches are optional, but any index corner shall be in accordance with JEDEC Pub. 95 leadless chip carrier indexing.
5. *Dimension D1: Exclusive of package anomalies (ceramic particles, etc.). Such anomalies shall not exceed .010 inch.*
6. *Dimension L: The distance between the body of package and the package lead protection mechanism (tie bars, carriers, etc.).*
7. *Dimension N: Number of terminals.*
8. *Dimension ND: Number of terminals per package edge.*
9. Regardless of the virtual length, the .020 limit ensure an accurate, square trim for subsequent lead forming tool registration.
10. Controlling dimension: Inch.
11. Dimensioning is in accordance with ANSI Y14.5M - 1982.
12. Lead dimension must be within tabulated callouts before solder dip or tin plate.
13. All lead finish thicknesses must be in accordance with MIL-M-38510.
14. The increase in the B dimension, as a result of solder finishes, does not change the positional tolerance, .009, which is applied at MMC of .010. The total envelope that the leads must simultaneously reside in is unchanged and remains at .009 (.009 + .010 - .019).
15. The leads on this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars, carriers, etc.) are not shown on the drawing; however, when microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.

FIGURE 1. Case outlines ^L Continued.



NOTES:

1. For static burn-in I, all inputs shall be connected to GND. Outputs shall be open or connected to $V_{DD}/2$ to V_{DD} . Resistors are optional on outputs if open. Resistors are required on inputs and outputs connected to V_{DD} . $R = 680$ ohms to 47 kohms, actual resistor value shall reflect 2 mA minimum load conditions.
2. For static burn-in II, all inputs shall be connected through resistors to V_{DD} . Outputs shall be open or connected to $V_{DD}/2$ to V_{DD} . Resistors are optional on outputs if open. Resistors are required on inputs and on outputs connected to $V_{DD}/2$ to V_{DD} . $R = 680$ ohms to 47 kohms, actual resistor value shall reflect 2 mA minimum load conditions.
3. For dynamic burn-in, all inputs shall be connected through the resistors in parallel to a common V_{DD} , GND, or CP. Outputs shall be connected to $V_{DD}/2$ to V_{DD} through the resistors. Resistor values shall be selected to ensure a minimum current of 2.0 mA on the outputs, 680 ohms to 47 kohms for inputs.
4. CP = 100 kHz $\pm$ 50%; duty cycle = 50 $\pm$ 15%; $V_{IH} = 4.5$ V to V_{DD} ; $V_{IL} = 0 \pm 0.5$ V, transition time < 0.5 μ s.
5. $V_{DD} = 5.0$ minimum.
6. I = input, O = output, N (M) = highest numbered input (output).
7. In the case of multiple V_{DD} or V_{SS} pins, all connections shall be tied to the appropriate level.
8. Pin designations determined by customer's configuration.

FIGURE 2. Burn-in circuit (device specific).

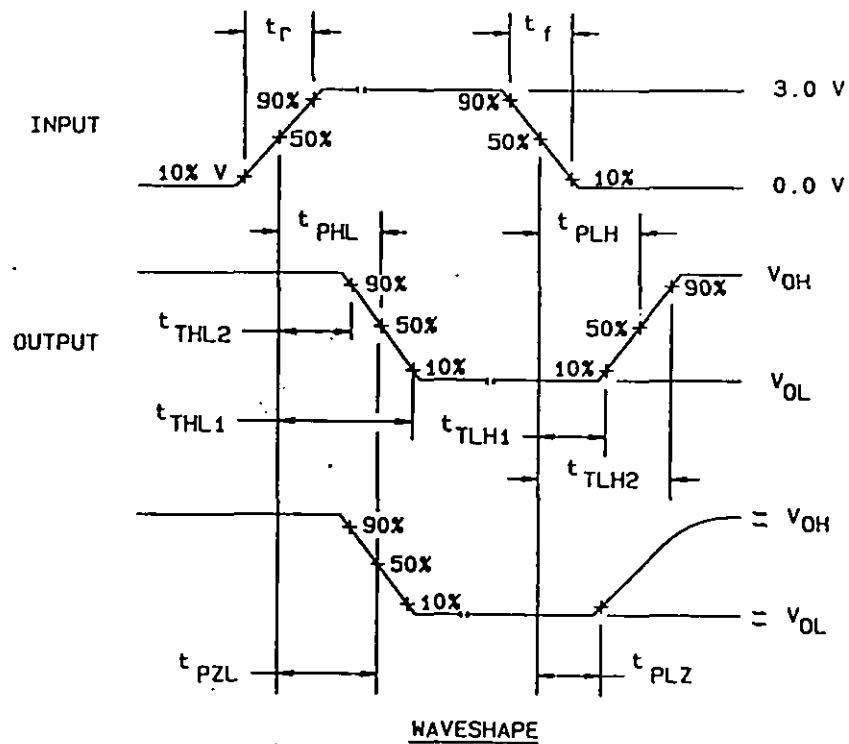
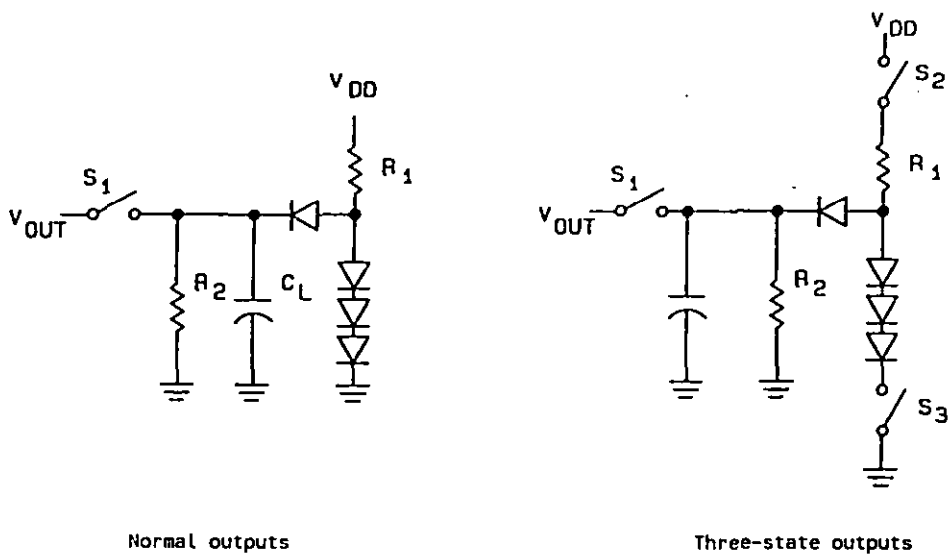


FIGURE 3. Switching time test circuit and waveforms.

NOTES:

1. C_L is determined by the specific automatic test equipment (ATE) being utilized, plus jig and probe capacitance. The total load shall be specified in AID and all switching test limit shall be based on the defined load.
2. Input pulse shall have the following characteristics:
 $t_r = t_f \leq \text{ns}$; PRR ≤ 1 MHz duty cycle = 50%
3. All used inputs are tied either to V_{DD} or GND
4. $t_{THL1} - t_{THL2} = t_{THL}$; $t_{TLH2} - t_{TLH1} = t_{TLH}$.
5. S1 is closed during function test and all ac tests, except output enable tests.
6. S1 and S3 are closed while S2 is open for t_{PZH} test.
 S1 and S2 are closed while S3 is open for t_{PZL} test.
7. $R2 = 1 \text{ kohm}$ for three-state output.
 $R2$ is determined by I_{OH} at $V_{OH} \pm 2.4 \text{ V}$ for non three-state outputs.
8. $R1$ is determined by $I_{OH}(\text{min})$ with $V_{DD} - .05 \text{ V}$ minus the current to ground through $R2$.
9. Switching tests shall be performed utilizing load circuits shown, or the equivalent.
10. Functional input test conditions shall be in accordance with MIL-STD-883, method 5004.

FIGURE 3. Switching time test circuit and waveforms - Continued.

TABLE II. Electrical test requirements.

Line no.	MIL-STD-883 test requirements	Subgroups	
		Class S devices	Class B devices
1	Interim electrical parameters (method 5004)	1, 7	1
2	Static burn-in I (method 1015)	Required	Not required
3	Same as line 1	1/ Plus delta (Δ) limit 1, 7	---
4	Static burn-in II (method 1015)	Required	Required
5	Same as line 1	1/ 2/ Plus (Δ) limit 1*,7*	1/ 2/ 3/ Plus (Δ) limit 1*
6	Dynamic burn-in (method 1015)	Required	Not required
7	Same as line 1	1/ 2/ Plus (Δ) limit 1*,7*	1*
8	Final electrical test parameters (method 5004)	2/ 1*,2,3,7*, 8,9,10,11	2/ 3/ 1*,2,3,7,8, 9,10,11
9	Group A test requirements (method 5005)	4/ 1,2,3,4,7, 8,9,10,11	4/ 1,2,3,4,7,8, 9,10,11
10	Group B end-point electrical parameters (method 5005)	1/ 5/ 1,2,3,7,8, 9,10,11 Plus (Δ) limit	1
11	Group C end-point electrical parameters (method 5005)	N/A	1/ 1, 2 Plus (Δ) limit
12	Group D end-point electrical parameters (method 5005)	1, 2, 3	1, 2
13	Group E end-point electrical parameters (method 5005)	1, 7, 9	1, 7, 9

1/ (Δ) indicates a delta limit shall be required per table IV and the delta values shall be computed with reference to the previous interim electrical parameters.

2/ (*) POA applies (see 4.2.1).

3/ The device manufacturer may, at his option, either complete the required electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete the required electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).

4/ Capacitance testing (see 4.4.1d).

5/ Electrostatic discharge sensitivity and latch-up tests require subgroup 1 only.

TABLE III. Group A inspection for all device types.

subgroups	Test	Symbol	Test no.	MIL-STD-883 method	Conditions	Measured terminal	Limits
1 T _C = +25°C 1/	Input clamp voltage, positive	V _{IC} , pos	1	---	V _{DD} = GND; 1 mA into terminal	All input terminals	Per manufacturer's data
	Input clamp voltage, negative	V _{IC} , neg	2	---	GND = V _{SS} ; -1 mA into terminal	All input terminals	Per manufacturer's data
	Output voltage high, TTL	V _{OH} , TTL	3	3006	V _{DD} = 4.5 V	All applicable output terminals	See table I
	Output voltage high, CMOS	V _{OH} , CMOS	4	3006	"	"	"
	Output voltage low, TTL	V _{OL} , TTL	5	3007	V _{DD} = 5.5 V	"	"
	Output voltage low, CMOS	V _{OL} , CMOS	6	3007	"	"	"
	Input current, high	I _{IH}	7	3010	V _{DD} = 5.5 V; input voltage = 5.5 V	All input terminals	"
	Input current, low	I _{IL}	8	3009	V _{DD} = 5.5 V; input voltage = V _{SS}	All input terminals	"
	Static supply current	I _{DDS}	9	3005	V _{DD} = 5.5 V	V _{DD} terminals	Per design

See footnotes at end of table.

TABLE III. Group A inspection for all device types - Continued.

Subgroups	Test	Symbol	Test no.	MIL-STD-883 method	Conditions	Measured terminal	Limits
2 1/ $T_C = +125^\circ\text{C}$	Same terminal conditions and limits as above, except $T_C = +125^\circ\text{C}$.						
3 1/ $T_C = -55^\circ\text{C}$	Same terminal conditions and limits as above, except $T_C = -55^\circ\text{C}$.						
4 1/ $T_C = +25^\circ\text{C}$	Input capacitance, negative	CIN	10	3012	$F = 1\text{ MHz}$	ALL input terminals	See table I
	Output capacitance high, TTL	COUT	11	3012	$F = 1\text{ MHz}$	ALL output terminals	See table I
7	Functional	---		3014	See figure 3 $V_{DD} = 4.5\text{ V}$	Design specific; according to AID	
8							
9 2/ $T_C = +25^\circ\text{C}$	AC switching	---		3003	See figure 3 $V_{DD} = 4.5\text{ V}$	Design specific; according to AID	
10 2/ $T_C = +125^\circ\text{C}$	Same as subgroup 9, except $T_C = +125^\circ\text{C}$.						
11 2/ $T_C = -55^\circ\text{C}$	Same as subgroup 9, except $T_C = -55^\circ\text{C}$						

1/ Static tests shall be conducted as required by table II of this specification; limits and conditions appear in table I herein. Particular terminal(s) to be measured are design specific and must appear in the applicable AID.

2/ Switching tests, comprising subgroups 9, 10, and 11, shall be conducted as required by table II. The test vectors to accomplish the functional and switching verification are design specific, and must be included in the AID. The vector set must meet the criteria as outlined in 3.2.8. Limits appear in the AID.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I, method 5005 of MIL-STD-883 and as follows:

- a. Test requirements shall be as specified in table II herein and as follows.
- b. The vehicles to be used for the group A inspection are as follows:
 1. Qualification - SEC.
 2. Quality conformance inspection - actual user device (via the AID).
- c. Subgroups 5 and 6 of table I, method 5005 of MIL-STD-883 shall be omitted.
- d. Subgroup 4 (CIN and COY measurements) shall be measured only for initial qualification and after process or design changes which may affect the value. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. One pin of each input/output driver (buffer) type shall be tested on each sample size. A minimum sample size of five devices with zero rejects shall be required.
- e. Switching and functional testing shall be performed using the circuit configuration shown on figure 3 herein or equivalent.

4.4.1.1 Alternate group A method. The alternate group A method may be used provided that:

- a. Inspection lot size is less than 500 devices.
- b. Final electrical test shall ensure that the electrical requirements of table II are met.
- c. All test software and procedures are under document control.

4.4.1.1.1 In-line verification testing.

- a. For each test setup (and operator for manual testing), production runs correlation unit to assure that the accuracy requirements of 4.5.2 in MIL-STD-883 are being met.
- b. Testing is performed using the verified setup.
- c. At the completion of testing utilizing, the verified setup (not to exceed eight hours and at the change of operators), a separate party (QA or QA designate) then verifies the production testing by:
 1. Checking visually to verify that the correct fixture, equipment, software, and procedure(s) were used.
 2. Actual testing of controlled known good device utilizing the fixtures, setups, software, and procedures that were used by production. Variables data for all required group A tests shall be read and recorded for the controlled unit. This data shall be maintained with the lot.
 3. The verifying party shall stamp or sign the lot traveller to attest that the above data meets the test requirements and that all of the above items were performed and were found to be acceptable.
 4. Failure of the verification test shall require, as a minimum, engineering to perform a detailed review of hardware, software, setup, and parts. If engineering locates the problem, a one time only 100 percent retest to all group A requirements for all devices that were under consideration for acceptance shall be required. If the engineering review does not locate the problem, the verification unit shall undergo failure analysis before retesting the lot.

- (a) If failure analysis locates the problem, the entire group of devices being considered for acceptance at the time of the failure may be retested for appropriate subgroup(s) acceptance one time only by repeating this group A method.
- (b) If the failure analysis does not specifically locate the problem, the lot may be considered for acceptance one time only by 100 percent retesting of all the devices of the group A requirements and by repeating this group A method.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II, method 5005 of MIL-STD-883. Electrical test requirements shall be as specified in table II herein, and as follows:

- a. The vehicles to be used for the group B inspection are as follows:
 - 1. Qualification - SEC.
 - 2. Quality conformance inspection - actual user device (via the AID).
- b. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 5 of group B inspection for class S and shall consist of tests specified in table IV herein.
- c. A latch-up test shall be performed on a special subgroup using an LTPD of 15. One of each input and output configuration (i.e., buffer) of the device under test (DUT) shall be subjected to a current pulse of ± 150 mA amplitude and 500 ms duration under the following conditions:
 - 1. $V_{DD} = +5.5$ V, $V_{SS} = GND$.
 - 2. $T_A = +125^\circ\text{C}$.

The selected pin will be subjected to the current pulse, while I_{DD} is monitored for latch-up. Untested inputs shall be tied to $\pm V_{DD}$. Untested outputs shall be open. The device shall pass all electrical tests (subgroup 1) after latch-up evaluations have been performed.

- d. Latch-up sensitivity and ESD tests shall be performed on a special subgroup for qualification and after input or output buffer design changes.
- e. The following sample plan shall be used in lieu of table II, method 5005 of MIL-STD-883 for class S, group B, subgroup 5 when the inspection lot size is less than 200 devices. A sample with LTPD of 10 shall be chosen and submitted to tests. The samples shall be selected proportionately from the sublots to meet the required LTPD sample size.

Steady-state life test, method 1005 of MIL-STD-883.

- 1. Use life-test condition A or D and the circuit configuration shown on figure 2. The life test circuit schematic shall be submitted to the qualifying activity for approval prior to use (for qualification only).
- 2. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- 3. $T_A = +125^\circ\text{C}$ minimum.
- f. When metal-glass die attach material is allowed, the die pull test (method 2027 of MIL-STD-883) may be performed in lieu of the die shear test (method 2019 of MIL-STD-883).

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III, method 5005 of MIL-STD-883 and as follows:

- a. Qualification and quality conformance inspection shall be performed on the manufacturer's SEC.
- b. End-point electrical parameters shall be as specified in table II with limits shown on the AID covering the manufacturer's SEC (see table I herein for minimum dc parameters).
- c. Steady-state life test, method 1005 of MIL-STD-883.
 1. Use life-test condition A or D using the SEC and the circuit configuration shown on figure 2. The life test circuit schematic shall be submitted to the qualifying activity for approval prior to use.
 2. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
 3. $T_A = +125^\circ\text{C}$ minimum.
- d. The following sampling plan shall be used in lieu of table III, method 5005 of MIL-STD-883 for all group C subgroups: A sample of 10 SEC devices shall be chosen and submitted to test with no failures allowed. If not more than 1 failure is found in the first sample of 10, a second sample of 10 SEC devices is permitted with no further failures allowed.
- e. End-point electrical parameters for class B, life test shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IV herein.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV, method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein. The SEC shall be used for group D inspection whenever practical; for smaller packages where the SEC cannot be used, another die may be used provided the gate utilization is 60 percent or greater, unless otherwise approved by the qualifying activity. Group D inspection shall be performed in accordance with MIL-M-38510, section 4.5, or as defined below:

- a. If more than one package type within a case outline family is qualified, then the group D inspection shall be rotated between the qualified package types. A different package type shall be tested every three months based on the inspection lot date code.
- b. If a package type is skipped in the rotation due to the absence of production, then the first lot of the skipped type shall receive group D inspection. The successful completion of this package type shall establish a new three-month period before the next package type in the rotation is selected for group D inspection.
- c. Failure of a group D subgroup shall discontinue coverage of all package types within the case outline family. Lot-by-lot inspection shall be initiated until three consecutive lots pass. The package type which failed the subgroup shall not be shipped until that package type has successfully passed the previously failed subgroup.
- d. Constant acceleration shall be performed using test condition D.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.8.1). RHA levels shall be in accordance with MIL-M-38510.

4.4.5.1 Total dose testing. The devices shall be subjected to RHA tests in accordance with MIL-STD-883, method 5005, table V. The devices shall be subjected to radiation hardness assurance tests as specified in MIL-M-38510 for the RHA level being tested.

- a. The vehicle to be used for the group E inspection are as follows:
 1. Qualification - SEC, or alternate qualification vehicle as approved by the qualifying activity. RHA tests shall be performed through each level or the RHA requirements.
 2. Quality conformance inspection - actual user device (via AID).

- b. Prior to and during total dose irradiation, each selected sample shall be assembled in its qualified package. RHA samples need not be tested at -55°C or $+125^{\circ}\text{C}$ prior to total dose irradiation.
- c. Prior to and during total dose irradiation, the devices shall be biased to the worst case conditions established during characterization of the devices.
- d. The samples shall pass the specified group A electrical parameters for subgroups specified in table II herein, and meet the post irradiation end-point electrical parameter limits as defined in table I and the AID at $T_A = +25^{\circ}\text{C}$, $\pm 5^{\circ}$ after exposure.
- e. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document or to a higher qualified level.

4.4.5.2 Single event phenomena (SEP). SEP testing shall be required on class S devices. SEP testing shall be performed on SEC or alternate SEP vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192-88 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ion/cm²/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The test temperature shall be $+25^{\circ}\text{C}$ and the maximum rated operating temperature $\pm 10^{\circ}\text{C}$.
- f. Bias conditions shall be $V_{DD} = 4.5$ V dc for the upset measurements and $V_{DD} = 5.5$ V dc for the latchup measurements.
- g. For SEP test limits see table IB herein.

4.4.5.3 When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

- a. RHA delta limits.
- b. RHA upset levels.
- c. Test conditions (SEP).
- d. Number of upsets (SEP).
- e. Number of transients.
- f. Occurrence of latchup.

4.5 Methods of inspection. Methods of inspection shall be specified as follows.

4.5.1 Voltage and current. All voltage values given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Burn-in and life test cool down procedures. When the burn-in and life tests are completed and prior to removal of bias voltages, the DUT shall be cooled to within 10°C of their power stable condition at room temperature; then, electrical parameter end-point measurements shall be performed.

TABLE IV. Burn-in and life test delta limits at +25°C.

Parameter 1/	Device types
	ALL
I _{DD}	±10% or 35 µA whichever is greater

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine deltas (Δ).

4.5.3 Quiescent supply current (I_{DD}test). When performing quiescent supply current measurements (I_{DD}), the meter shall be placed so that all currents flow through the meter.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. In addition, wherever practical, all devices shall be in contact with a conductive material which shorts all leads together to prevent electrostatic damage.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment), design applications, and logistic purposes.

6.2 Ordering data.

6.2.1 Acquisition requirements. Acquisition documents shall specify the following:

- a. Complete PIN (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis, including required test condition of method 5003 of MIL-STD-883, corrective action, and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable.
- h. Requirements for "JAN" marking.
- i. Requirements for AID provided to the manufacturer; see 3.2.
- j. Requirements for total dose radiation testing (see 3.8.1 and 4.4.5), if applicable.

6.3 Logistic support. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.5). Longer length leads and lead forming shall not affect the PIN.

6.4 Handling. MOS devices must be handled with certain precautions to avoid damage due to the discharge of accumulated static charge. These CMOS devices are fabricated with a silicon gate technology, including input protection, which reduces the susceptibility to damage; however, the following handling practices are recommended:

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment and tools.
- c. Handling of devices by the leads should be avoided.
- d. Devices should be stored in conductive foam or carriers.
- e. Avoid uses of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent, if practical.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

C_{IN}	-----	Input terminal-to-GND capacitance.
GND	-----	Ground zero voltage potential.
I_{DD}	-----	Quiescent supply current.
T_A	-----	Free air temperature.
V_{DD}	-----	Positive supply voltage.

6.6 Manufacturers' designations. Manufacturers of device types on this specification are designated as shown in table V herein. This does not imply qualification or certification, refer to QPL-38510 for information regarding qualified sources.

TABLE V. Manufacturers' designations.

A	B	C	D	E	F	G	H
Mostek/ Thompson	UTMC	GE	LSI	Motorola	TI	Siliconix	National

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Manufacturer specific generic-industry type</u>
01 through 20	See listed manufacturer, (6.6 and table V) data sheets

6.8 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

APPENDIX

GATE ARRAY BENCHMARK SET

10. SCOPE

10.1 Scope. This appendix contains benchmark description numbers from JEDEC Standard No. 12, "Standard for Gate Array Benchmark Set" as required by 4.3.2.4 CAD routing and post routing simulation herein.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. REQUIREMENTS

30.1 Benchmark number description.

1. 4-bit ALU, similar to 54S381
2. 16-bit ALU, similar to 54S381
3. 4-bit rotator
4. 16-bit rotator
5. 8-bit register
6. 8-bit up/down counter
7. 3- to 8- decoder, similar to 54S138
8. 9-bit parity generator, similar to 54S280

CONCLUDING MATERIAL

Custodians:

Air Force - 17
Navy - EC
Army - ER

Review activities:

Army - AR, MI
Navy - OS, SH, TD
Air Force - 19, 85, 99
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC

Preparing activity:

Air Force - 17

Agent:

DLA - ES

(Project 5962-1240)