

MILITARY SPECIFICATION
MICROCIRCUITS, DIGITAL, CMOS, STATIC SHIFT REGISTER,
MONOLITHIC SILICON, POSITIVE LOGIC

Reactivated after 21 Jan. 2005 and may be used for new and existing designs and acquisitions.

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS, logic microcircuits. Two product assurance classes and a choice of case outlines, lead finishes, and radiation hardness assurance (RHA) are provided and are reflected in the complete Part or Identifying Number (PIN). For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535 (see 6.3).

1.2 Part or identifying number (PIN). The PIN is in accordance with MIL-PRF-38535 and as specified herein.

1.2.1 Device types. The device types are as follows:

Device type	Circuit
01	Dual 4-stage/dual 5-stage static shift register
02	8-stage synchronous parallel or serial input/serial output static shift register
03	Dual 4-stage serial input/parallel output static shift register
04	8-stage asynchronous parallel input/serial output or synchronous serial input/serial output static shift register
05	64-stage static shift register
06	8-stage bidirectional parallel/serial input/output bus register
51	Dual 4-stage/dual 5-stage static shift register
52	8-stage synchronous parallel or serial input/serial output static shift register
53	Dual 4-stage serial input/parallel output static shift register
54	8-stage asynchronous parallel input/serial output or synchronous serial input/serial output static shift register
55	64-stage static shift register
56	8-stage bi-directional parallel/serial input/output bus register

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
A	GDFP5-F14 or CDFP6-F14	14	Flat pack
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or email CMOS@dscclia.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil>.

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J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
N	CDFP4-F16	16	Flat pack
T	CDFP3-F14	14	Flat pack
X <u>1/</u> <u>2/</u>	GDFP5-F14 or CDFP6-F14	14	Flat pack, except A dimension equals 0.100" (2.54 mm) max
Y <u>1/</u> <u>2/</u>	GDFP1-F14 or CDFP2-F14	14	Flat pack, except A dimension equals 0.100" (2.54 mm) max
Z <u>1/</u> <u>2/</u>	GDFP2-F16 or CDFP3-F16	16	Flat pack, except A dimension equals 0.100" (2.54 mm) max
U <u>1/</u> <u>2/</u>	GDFP2-F24 or CDFP3-F24	24	Flat pack, except A dimension equals 0.100" (2.54 mm) max

1.3 Absolute maximum ratings.

Supply voltage range ($V_{DD} - V_{SS}$):

Device types 01-06..... -0.5 V dc to +15.5 V dc

Device types 51-56..... -0.5 V dc to +18.0 V dc

Input current (each input) ± 10 mA

Input voltage range $(V_{SS} - 0.5 \text{ V}) \leq V_i \leq (V_{DD} + 0.5 \text{ V})$

Storage temperature range (T_{STG})..... -65° to +175°C

Maximum power dissipation (P_D) 200 mW

Lead temperature (soldering, 10 seconds) +300°C

Thermal resistance, junction to case (θ_{JC})..... See MIL-STD-1835

Junction temperature (T_J) 175°C

1.4 Recommended operating conditions.

Supply voltage range ($V_{DD} - V_{SS}$):

Device types 01-06..... 4.5 V dc to 12.5 V dc

Device types 51-56..... 4.5 V dc to 15.0 V dc

Input low voltage range (V_{IL}):

Device types 01-06..... 0.0 V to 0.85 V dc @ $V_{DD} = 5.0 \text{ V dc}$

Device types 01-06..... 0.0 V to 2.1 V dc @ $V_{DD} = 12.5 \text{ V dc}$

Device types 51-56..... $V_{OL} = 10\% V_{DD}$, $V_{OH} = 90\% V_{DD}$

Device types 51-56..... 0.0 V to 1.5 V dc @ $V_{DD} = 5.0 \text{ V dc}$

Device types 51-56..... 0.0 V to 2.0 V dc @ $V_{DD} = 10.0 \text{ V dc}$

Device types 51-56..... 0.0 V to 4.0 V dc @ $V_{DD} = 15.0 \text{ V dc}$

Input high voltage range (V_{IH}):

Device types 01-06..... 3.95 V to 5.0 V dc @ $V_{DD} = 5.0 \text{ V dc}$

Device types 01-06..... 10 V to 12.5 V dc @ $V_{DD} = 12.5 \text{ V dc}$

Device types 51-56..... $V_{OL} = 10\% V_{DD}$, $V_{OH} = 90\% V_{DD}$

Device types 51-56..... 3.5 V to 5.0 V dc @ $V_{DD} = 5.0 \text{ V dc}$

Device types 51-56..... 8.0 V to 10.0 V dc @ $V_{DD} = 10.0 \text{ V dc}$

Device types 51-56..... 11.0 V to 15.0 V dc @ $V_{DD} = 15.0 \text{ V dc}$

Load capacitance 50 pF maximum

Case operating temperature range (T_C) -55°C to +125°C

1/ As an exception to nickel plate or undercoating paragraph of MIL-PRF-38535, appendix A, for case outlines X, Y, Z, and U only, the leads of bottom brazed ceramic packages (i.e., configuration 2 of case outlines A, D, F, or K) may have electroless nickel undercoating which is 50 to 200 microinches (1.27 to 5.08 μm) thick provided the lead finish is hot solder dip (i.e., finish letter A) and provided that, after any lead forming, an additional hot solder dip coating is applied which extends from the outer tip of the lead to no more than 0.015 inch (0.38 mm) from the edge.

2/ For bottom or side brazed packages, case outlines X, Y, Z, and U only, the S_1 dimension may go to .000 inch (.00 mm) minimum.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein. Although eutectic die bonding is preferred, epoxy die bonding may be performed. However, the resin used shall be Dupont 5504 Conductive Silver Paste, or equivalent, which is cured at 200°C ±10°C for a minimum of 2 hours. The use of equivalent epoxies or cure cycles shall be approved by the qualifying activity. Equivalency shall be demonstrated in data submitted to the qualifying activity for verification.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Logic diagrams. The logic diagrams shall be as specified on figure 2.

3.3.3 Truth tables. The truth tables shall be as specified on figure 3.

3.3.4 Switching time test circuit and waveforms. The switching time test circuit and waveforms shall be as specified on figure 4.

3.3.5 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity or preparing activity upon request.

3.3.6 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.7.1 Radiation hardness assurance identifier. The radiation hardness assurance identifier shall be in accordance with MIL-PRF-38535 and 4.5.4 herein.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 40 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ^{1/} $V_{SS} = 0\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ Unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Positive clamping input to V_{DD}	$V_{IC(POS)}$	$T_C = 25^{\circ}\text{C}$, $V_{DD} = \text{GND}$, $V_{SS} = \text{Open}$, Output = Open, $I_I = 1\text{ mA}$	All		+1.5	V dc
Negative clamping input to V_{DD}	$V_{IC(NEG)}$	$T_C = 25^{\circ}\text{C}$, $V_{DD} = \text{Open}$, $V_{SS} = \text{GND}$, Output = Open, $I_I = -1\text{ mA}$	All		-6.0	V dc
Quiescent supply current	I_{SS}	Any combination of inputs	$V_{DD} = 15\text{ V dc}$	01	3.0	μA
				02, 03, 04, 06	5.0	
				05	20	
			$V_{DD} = 18\text{ V dc}$	51	3.0	
				52, 53, 54, 56	5.0	
				55	20.0	
High level output voltage, any output	V_{OH1}	$V_{DD} = 5\text{ V dc}$ See table III	$I_{OH} = -70\text{ }\mu\text{A}$	01	4.5	V
any output			$I_{OH} = -55\text{ }\mu\text{A}$	02, 03, 04		
Q output			$I_{OH} = -225\text{ }\mu\text{A}$	05		
$\overline{Q}$ output			$I_{OH} = -60\text{ }\mu\text{A}$	05		
Delayed clock output			$I_{OH} = -280\text{ }\mu\text{A}$	05		
any output			$I_{OH} = -35\text{ }\mu\text{A}$	06		
High level output voltage	V_{OH2}	$V_{DD} = 12.5\text{ V dc}$ See table III $I_{OH} = 0\text{ A}$	01, 02, 03, 04, 05, 06	11.25		V
High level output voltage	V_{OH3}	$V_{DD} = 15\text{ V dc}$ See table III $I_{OH} = 0\text{ A}$	51, 52, 53, 54, 55, 56	14.95		V
Low level output voltage, any output	V_{OL1}	$V_{DD} = 5\text{ V dc}$ See table III	$I_{OL} = 85\text{ }\mu\text{A}$	01, 02, 03, 04	0.50	V
Q output			$I_{OL} = 900\text{ }\mu\text{A}$	05		
$\overline{Q}$ output			$I_{OL} = 60\text{ }\mu\text{A}$	05		
Delayed clock output			$I_{OL} = 280\text{ }\mu\text{A}$	05		
any output			$I_{OL} = 70\text{ }\mu\text{A}$	06		
Low level output voltage	V_{OL2}	$V_{DD} = 12.5\text{ V dc}$ See table III $I_{OL} = 0\text{ A}$	01, 02, 03, 04, 05, 06		1.25	V
Low level output voltage	V_{OL3}	$V_{DD} = 15\text{ V dc}$ See table III $I_{OL} = 0\text{ A}$	51, 52, 53, 54, 55, 56		0.05	V
Output low (sink) current	I_{OL1}	$V_{DD} = 5\text{ V dc}$ $V_{OL} = 0.4\text{ V dc}$ $V_{IN} = V_{SS}$	51, 53, 52, 54, 55, 56	0.36		mA dc
	I_{OL2}	$V_{DD} = 15\text{ V dc}$ $V_{OL} = 1.5\text{ V dc}$ $V_{IN} = V_{SS}$		2.40		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> $V_{SS} = 0\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$ Unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Output high (source) current	I_{OH1}	$V_{DD} = 5\text{ V dc}$ $V_{OH} = 4.6\text{ V dc}$ $V_{IN} = V_{DD}$	51, 53 52, 54, 55, 56	-0.36		mA dc
	I_{OH2}	$V_{DD} = 15\text{ V dc}$ $V_{OH} = 13.5\text{ V dc}$ $V_{IN} = V_{DD}$		-2.4		
Input leakage current (high)	$I_{IH} \underline{2/}$	Measure inputs sequentially	$V_{DD} = 15\text{ V dc}$	01, 04, 05, 06, 02, 03	45 100	nA
			$V_{DD} = 18\text{ V dc}$	51, 52, 53, 55, 56 54	45 100	nA
			$V_{DD} = 15\text{ V dc}$	01, 04 05, 06 02, 03	-45 -100	nA
			$V_{DD} = 18\text{ V dc}$	51, 52, 53, 55, 56 54	-45 -100	nA
Input capacitance test	C_i	$V_{DD} = 0\text{ V dc}$, $f = 1\text{ MHz}$ $T_C = 25^{\circ}\text{C}$	01, 05		70	pF
			02, 03, 04, 06		12	
			56		7.5	
			51, 53 52, 54		12	
			55		70	
Propagation delay, high to low level (CLOCK to any output)	t_{PHL}	$V_{DD} = 5.0\text{ V dc}$	01	20	1200	ns
			51	20	560	
			06	13	1300	
			56	13	980	
(CLOCK or reset to output)			04	20	1465	
			54	20	490	
(Reset to output)			03	20	1465	
			53	20	490	
(CLOCK to Q output)			02	13	1465	
			52	13	450	
			03	20	1465	
			53	20	560	
			05	13	1590	
			55	13	840	
(CLOCK to $\overline{Q}$ output)			05	13	1980	
			55	13	840	
(CLOCK to delayed CLOCK output)			05	13	975	
			55	13	350	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

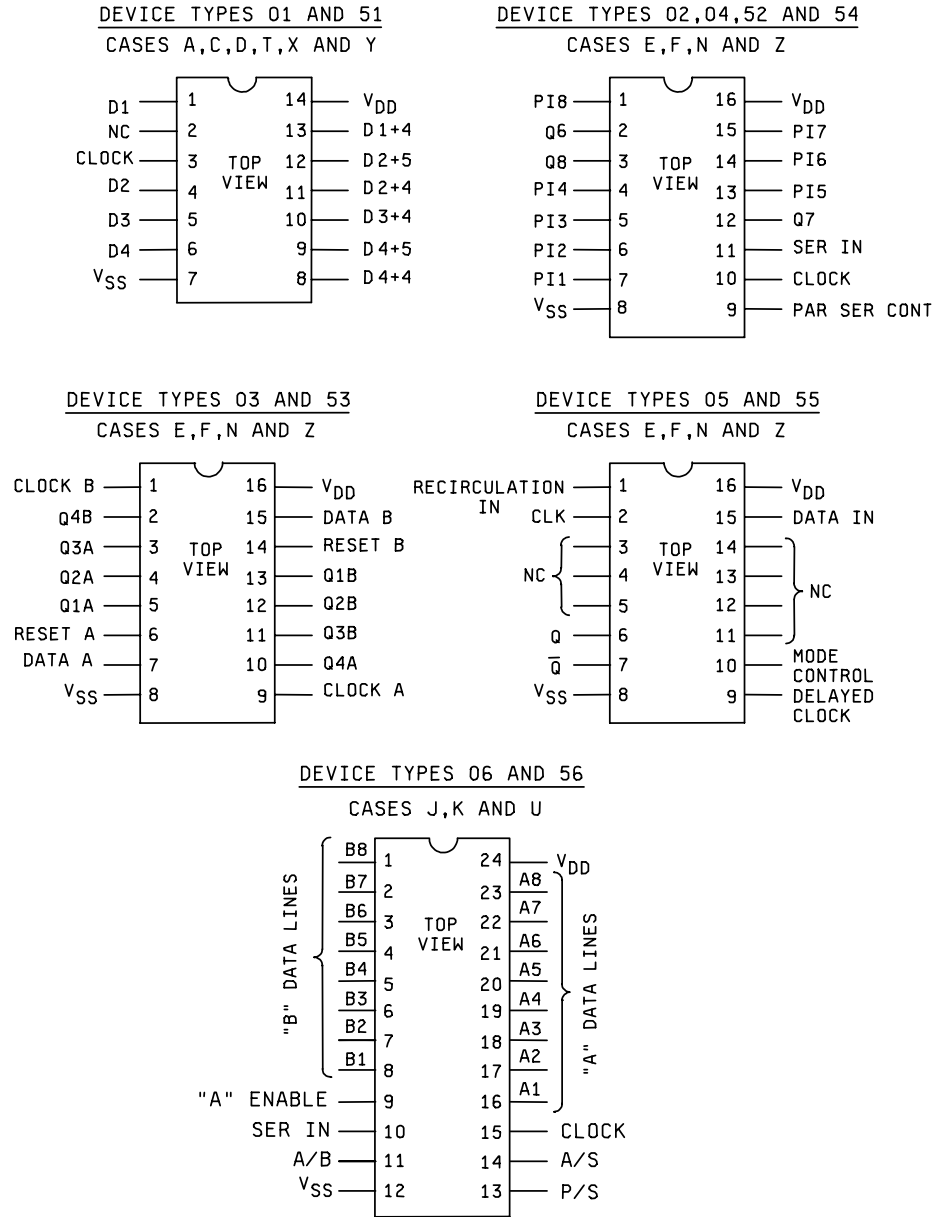
Test	Symbol	Conditions 1/ $V_{SS} = 0 \text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$ Unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Propagation delay, low to high level (CLOCK to any output)	t_{PLH}	$V_{DD} = 5.0 \text{ V dc}$	01	20	1200	ns
			51	20	560	
			06	13	1300	
			56	13	980	
(CLOCK or reset to output)			04	20	1465	
			54	20	490	
(CLOCK to Q output)			02	13	1465	
			52	13	450	
			03	20	1465	
			53	20	560	
			05	13	1590	
			55	13	840	
(CLOCK to $\overline{Q}$ output)			05	13	1980	
			55	13	840	
(CLOCK to delayed CLOCK output)			05	13	975	
			55	13	350	
Transition time, high to low level (Any output)	t_{THL}	$V_{DD} = 5.0 \text{ V dc}$	01	13	1140	ns
			51	13	200	
			02	10	975	
			52,56	10	280	
			03	13	975	
			53,54	13	280	
			04	13	1050	
			06	10	1300	
(Q output)			05	10	435	
			55	10	280	
($\overline{Q}$ output)			05	10	2100	
			55	10	280	
(Delayed CLOCK output)			05	10	525	
			55	10	200	
Transition time, low to high level (Any output)	t_{TLH}	$V_{DD} = 5.0 \text{ V dc}$	01	13	1140	ns
			51	13	200	
			02	10	1350	
			52,56	10	280	
			03	13	1465	
			53,54	13	280	
			04	13	1350	
			06	10	2300	
(Q output)			05	10	510	
			55	10	280	
($\overline{Q}$ output)			05	10	2100	
			55	10	280	
(Delayed CLOCK output)			05	10	525	
			55	10	200	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> $V_{SS} = 0 \text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$ Unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Maximum CLOCK frequency	f_{CL}	$V_{DD} = 5.0 \text{ V dc}, C_L = 50 \text{ pF}$	01,02	700		kHz
			03,04	700		
			05	550		
			06	525		
			51	1.4		MHz
			52	1.2		
			53	1.5		
			54	1.0		
			55	800		kHz
			56	750		
Setup time	t_{SETUP}	$V_{DD} = 5.0 \text{ V}, C_L = 50 \text{ pF}$ $T_C = 25^{\circ}\text{C}$	01,51	115		ns
			53	150		
			02,03,04	500		
			52,54	180		
			05	680		
			55	300		
			06	650		
			56	240		
			01,04,06	330		
			02,03,05	400		
Minimum CLOCK pulse width	t_p	$V_{DD} = 5.0 \text{ V}, C_L = 50 \text{ pF}$ $T_C = 25^{\circ}\text{C}$	51,54	200		ns
			52	180		
			53,56	250		
			55	300		
			03,05	400		
Minimum reset pulse width	$t_{p(RS)}$		06,56	480		
Minimum high level AE, P/S, A/S pulse width	t_{PH}					

1/ Complete terminal conditions shall be as specified in table III.2/ Input current at one input node.



NC = No connection

FIGURE 1. Terminal connections.

DEVICE TYPES 01 AND 51

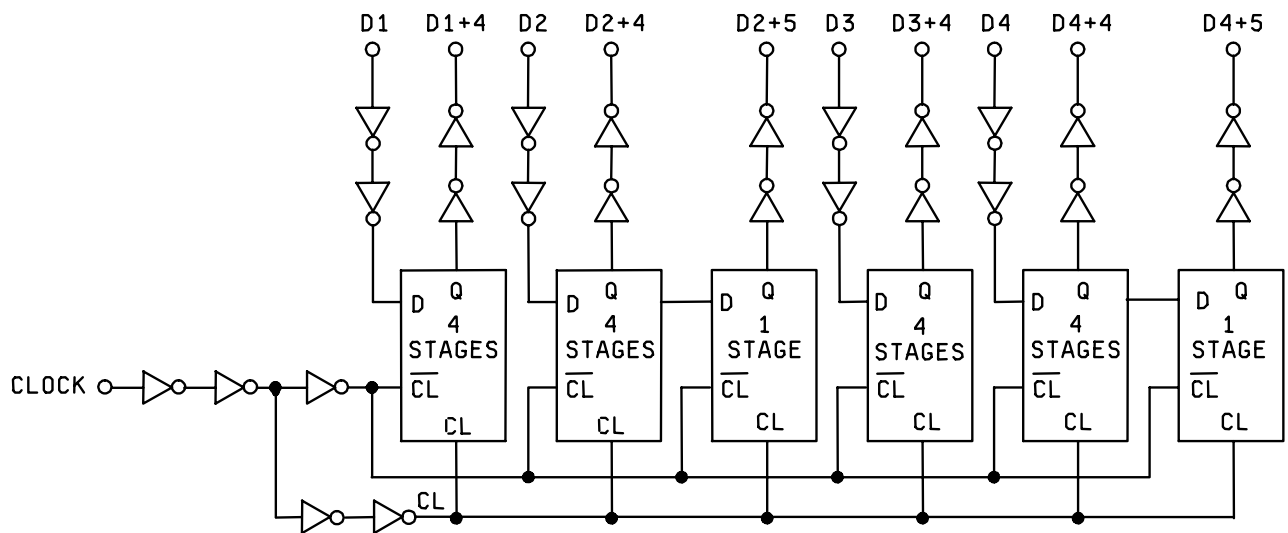
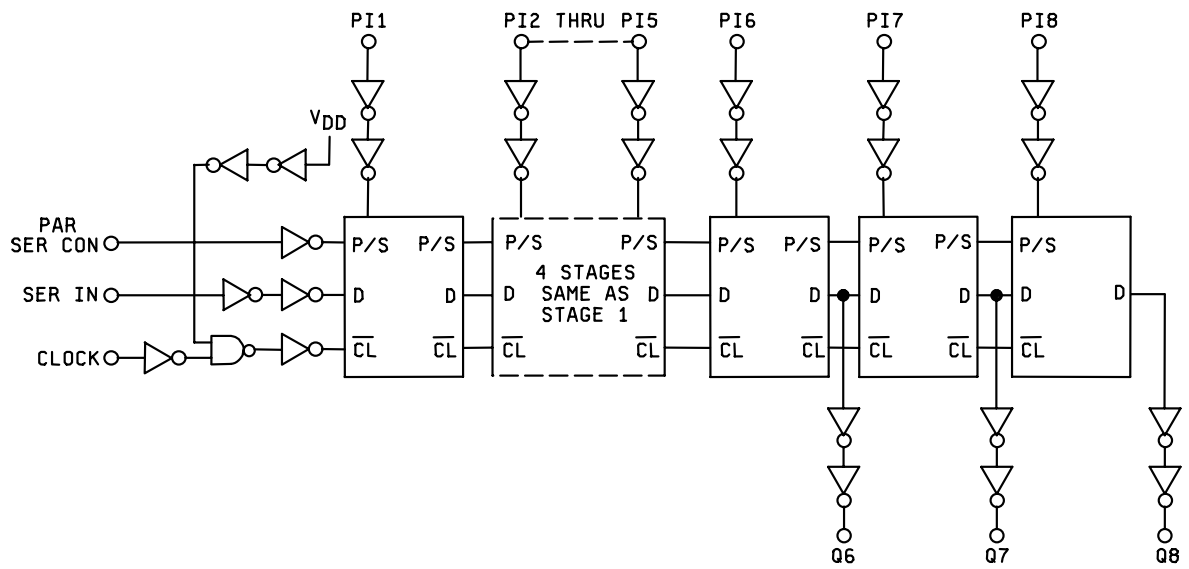


FIGURE 2. Logic diagrams.

DEVICE TYPES 02 AND 52FIGURE 2. Logic diagrams – Continued.

DEVICE TYPES 03 AND 53

(1/2 SHOWN)

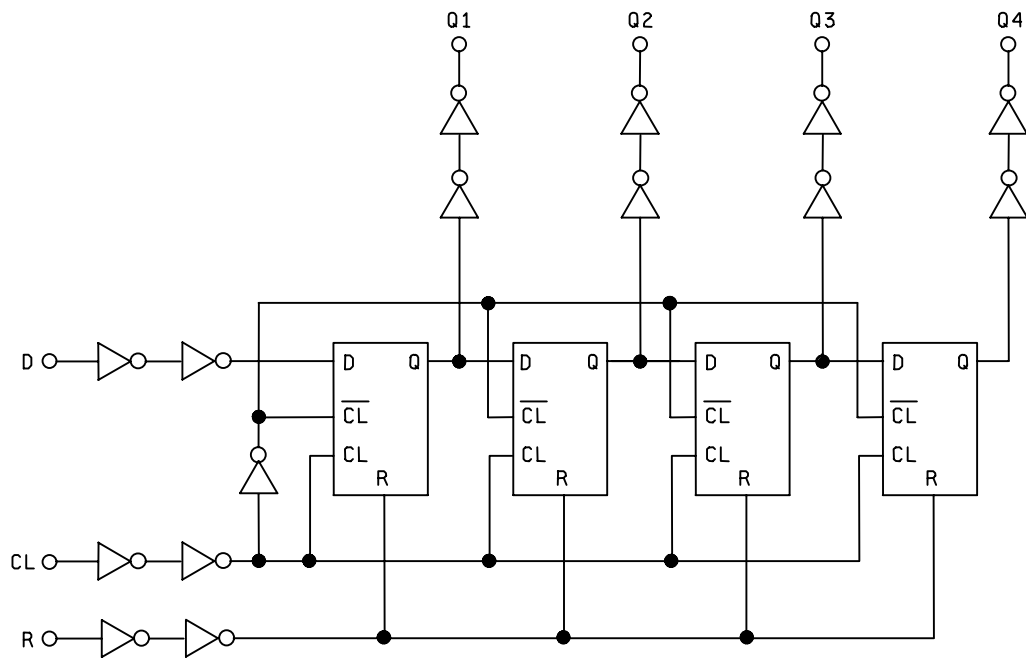
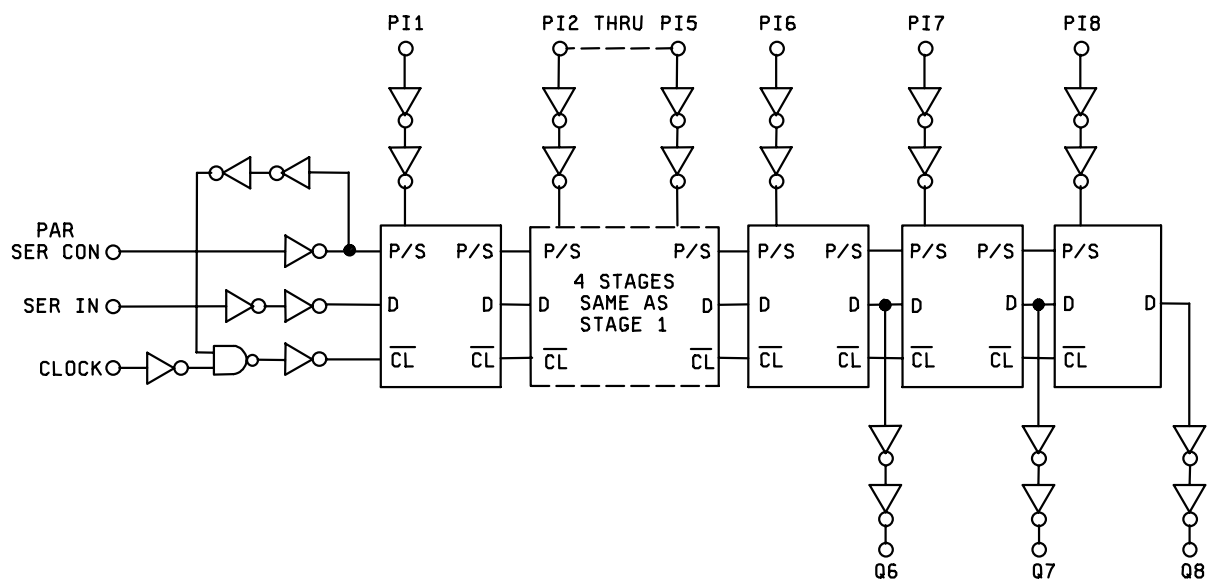


FIGURE 2. Logic diagrams - Continued.

DEVICE TYPES 04 AND 54FIGURE 2. Logic diagrams - Continued.

DEVICE TYPES 05 AND 55

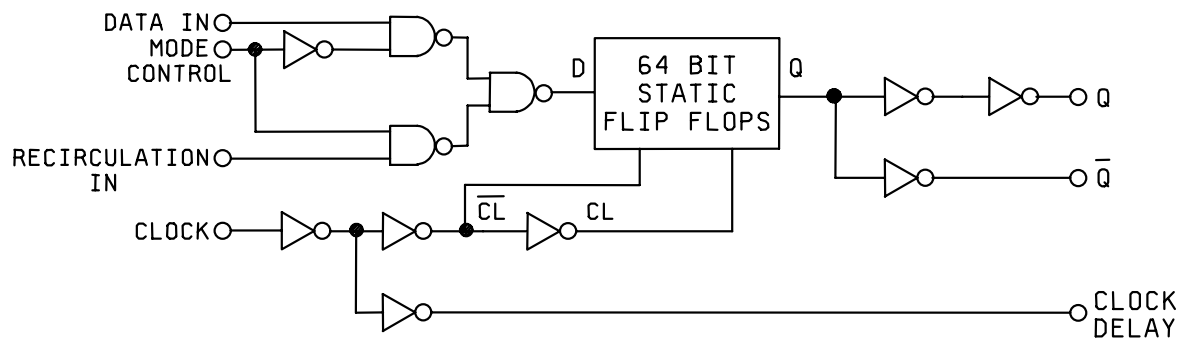


FIGURE 2. Logic diagrams - Continued.

DEVICE TYPES 06 AND 56

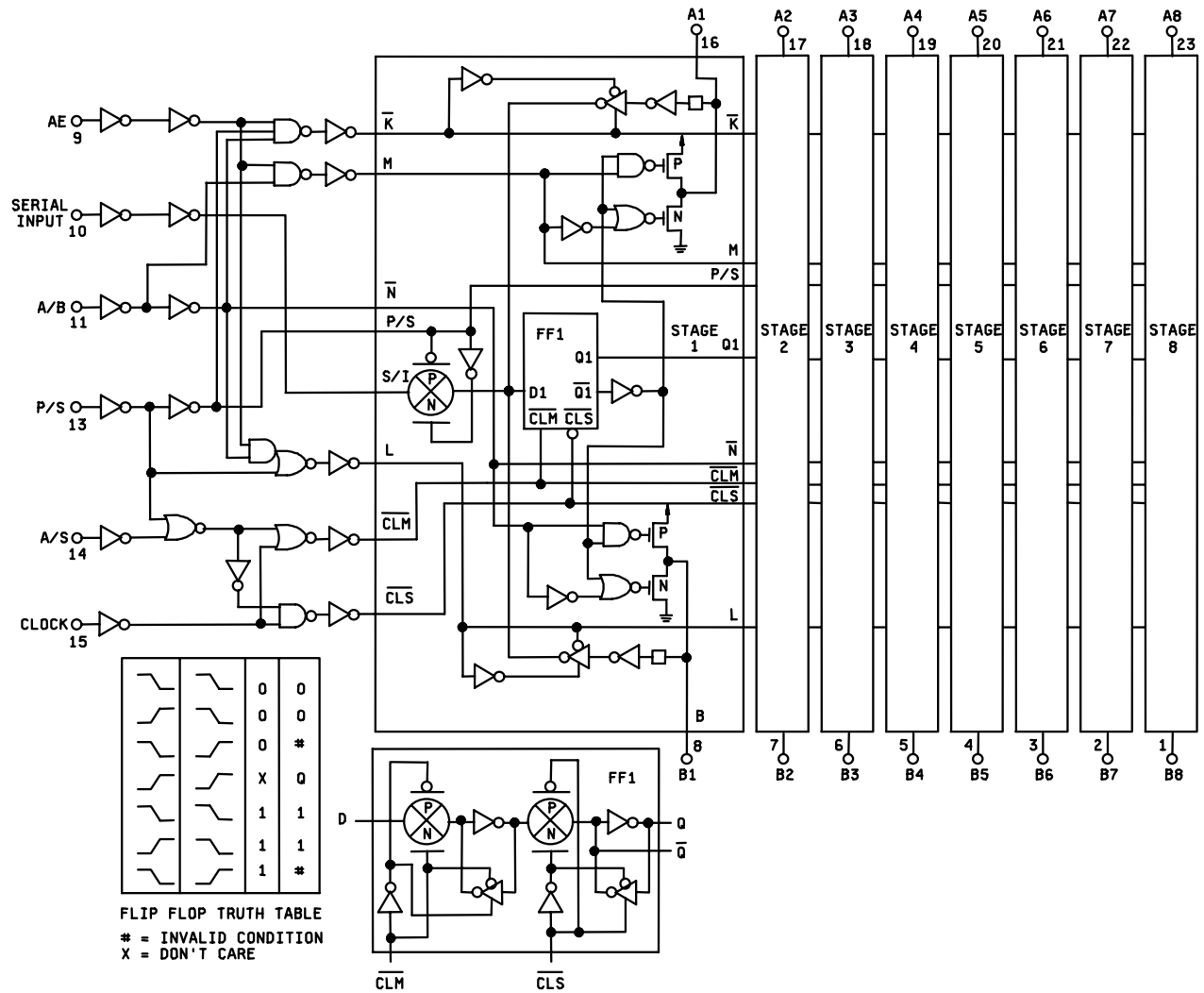


FIGURE 2. Logic diagrams - Continued.

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Device types 01 and 51

Inputs		Output
D	CL (level change)	D+1
0	↓	0
1	↓	1
X	↑	NC

Positive Logic 0 $\approx V_{SS}$.

Positive Logic 1 $\approx V_{DD}$.

NC = No change.

↓ = Clock transition from high to low.

↑ = Clock transition from low to high.

X = Don't care.

Device types 02 and 52

Inputs					Output	
CL (level change)	Serial IN	PAR/SER control	PI-1	PI-n	Q1 (internal)	Qn
↑	X	1	0	0	0	0
↑	X	1	1	0	1	0
↑	X	1	0	1	0	1
↑	X	1	1	1	1	1
↑	0	0	X	X	0	Qn-1
↑	1	0	X	X	1	Qn-1
↓	X	X	X	X	Q1	Qn

Positive Logic 0 $\approx V_{SS}$.

Positive Logic 1 $\approx V_{DD}$.

↓ = Clock transition from high to low.

↑ = Clock transition from low to high.

X = Don't care.

Device types 03 and 53

Inputs			Output	
CL (level change)	D	R	Q1	Qn
↑	0	0	0	Qn-1
↑	1	0	1	Qn-1
↓	X	0	Q1	Qn
X	X	1	0	0

Positive Logic 0 $\approx V_{SS}$.

Positive Logic 1 $\approx V_{DD}$.

↓ = Clock transition from high to low.

↑ = Clock transition from low to high.

X = Don't care.

FIGURE 3. Truth tables.

Device types 04 and 54

CL (level change)	Inputs				Output	
	Serial input	Parallel/serial control	PI-1	PI-n	Q1 (internal)	Qn
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
↑	0	0	X	X	0	Qn-1
↑	1	0	X	X	1	Qn-1
↓	X	0	X	X	Q1	Qn

Positive logic 0 $\approx V_{SS}$.Positive logic 1 $\approx V_{DD}$.

↓ = Clock transition from high to low.

↑ = Clock transition from low to high.

X = Don't care.

Device types 05 and 55

INPUT CONTROL CIRCUIT TRUTH TABLE

DATA	RECIRC.	MODE	BIT INTO STAGE 1
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

TYPICAL STAGE TRUTH TABLE

D	CL (level change)	D+1
0	↑	0
1	↑	1
X	↓	NC

Device types 06 and 56

"A" Enable	P/S	A/B	A/S	Operation *
L	L	L	X	Serial mode; synch. serial data input, "A" parallel data outputs disabled
L	L	H	X	Serial mode; synch. serial data input, "B" parallel data output
L	H	L	L	Parallel mode; "B" synch. parallel data inputs, "A" parallel data outputs disabled
L	H	L	H	Parallel mode; "B" asynch. parallel data inputs, "A" parallel data outputs disabled
L	H	H	L	Parallel mode; "A" parallel data inputs disabled, "B" parallel data outputs, synch. data recirculation
L	H	H	H	Parallel mode; "A" parallel data inputs disabled, "B" parallel data outputs, asynch. data recirculation
H	L	L	X	Serial mode; synch. serial data input, "A" parallel data output
H	L	H	X	Serial mode; synch. serial data input, "B" parallel data output
H	H	L	L	Parallel mode; "B" synch. parallel data input, "A" parallel data output
H	H	L	H	Parallel mode; "B" asynch. parallel data input, "A" parallel data output
H	H	H	L	Parallel mode; "A" synch. parallel data input, "B" parallel data output
H	H	H	H	Parallel mode; "A" asynch. parallel data input, "B" parallel data output

* Outputs change at positive transition of clock in the serial mode and when the A/S/ control input is "low" in the parallel mode.

Positive logic 0 $\approx V_{SS}$.Positive logic 1 $\approx V_{DD}$.

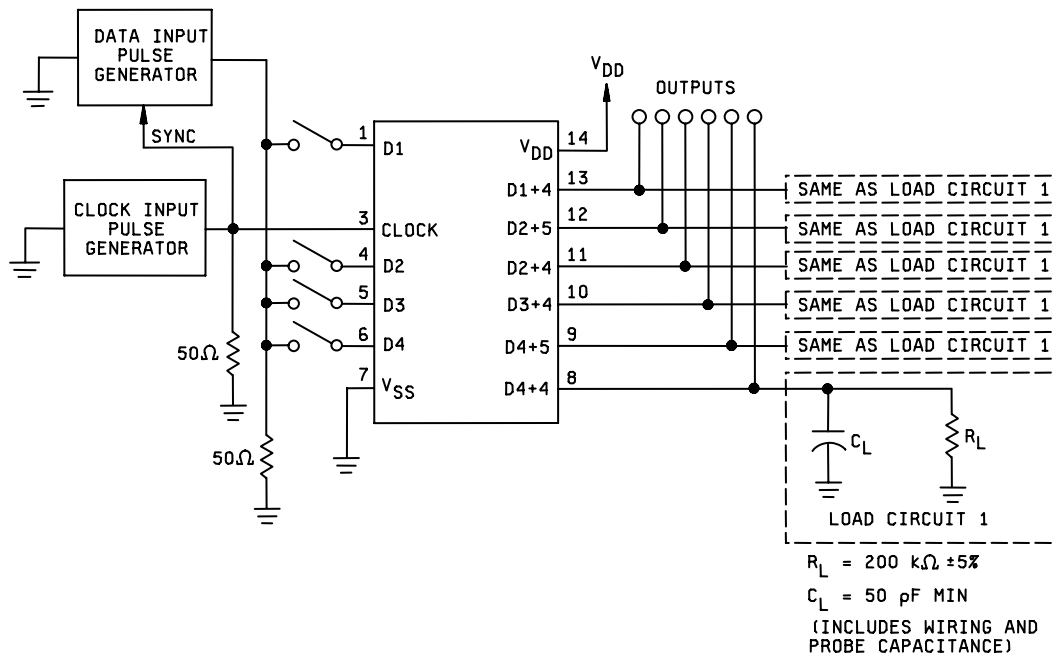
NC = No change.

↓ = Clock transition from high to low.

↑ = Clock transition from low to high.

X = Don't care.

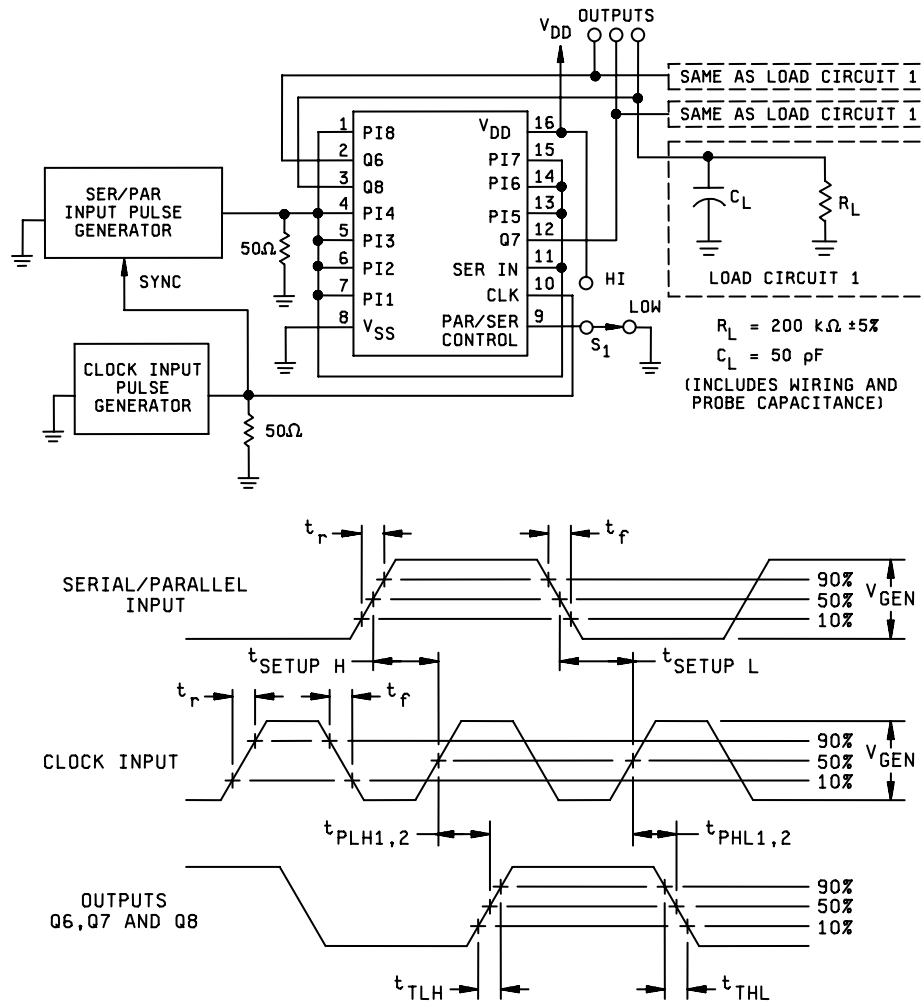
FIGURE 3. Truth tables – Continued.



NOTES:

1. The pulse generators have the following characteristics: $V_{\text{GEN}} = V_{\text{DD}} \pm 1$ percent, t_r and $t_f \leq 20$ ns, duty cycle = 50 percent, $Z_{\text{OUT}} = 50\Omega$.
2. $t_{\text{SETUP H}} = t_{\text{SETUP L}} = 80$ ns at $T_A = 25^\circ\text{C}$ and -55°C ; $t_{\text{SETUP H}} = t_{\text{SETUP L}} = 115$ ns at $T_A = 125^\circ\text{C}$.
3. Requirements for MAX clock frequency (f_{CL}) are established by setting the parameter to the limits given in table III and observing proper output state changes.
4. Initially, apply clock input pulses with data inputs low and set all outputs low.

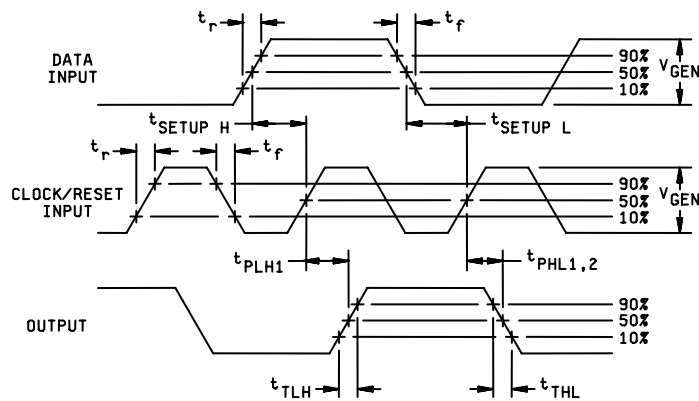
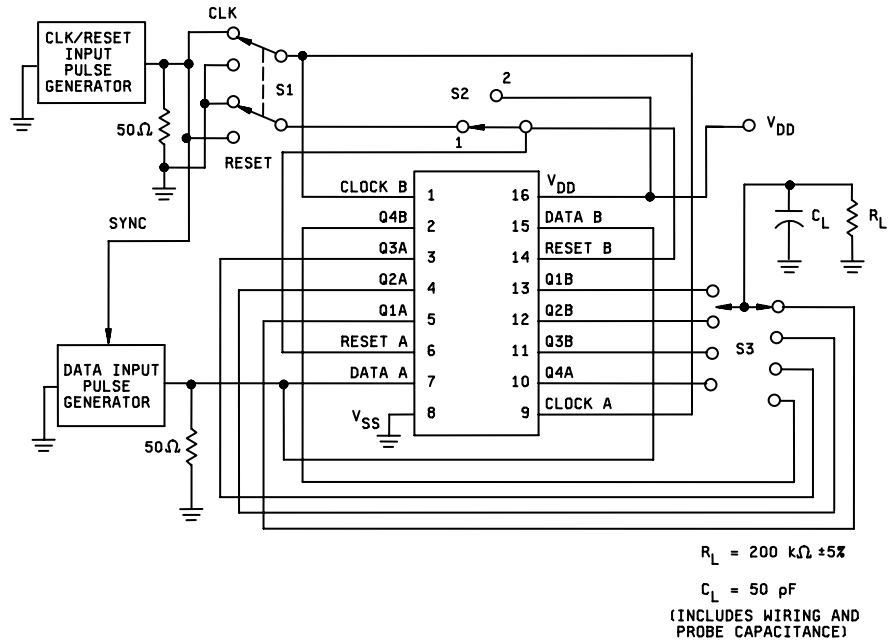
FIGURE 4. Switching time test circuit and waveforms.



NOTES:

1. The pulse generators have the following characteristics: $V_{GEN} = V_{DD} \pm 1 \text{ percent}$, t_r and $t_f \leq 20 \text{ ns}$, duty cycle = 50 percent, $Z_{OUT} = 50\Omega$.
2. When measuring t_{PHL1} and t_{PLH1} , set parallel serial control switch S1 to "LOW". Initially, apply clock pulse with serial/parallel inputs at 0 V to set outputs low.
3. When measuring t_{PHL2} , t_{PLH2} , t_{THL} , and t_{TLH} , set parallel serial control switch S1 to "HI". Initially, apply clock pulses with serial/parallel inputs at 0 V to set outputs low.
4. $t_{SETUPH} = t_{SETUPL} = 350 \text{ ns}$ at $T_A = 25^\circ\text{C}$ and -55°C ; $t_{SETUPH} = t_{SETUPL} = 500 \text{ ns}$ at $T_A = 125^\circ\text{C}$. For device type 02, $t_{SETUPH} = t_{SETUPL} = 130 \text{ ns}$ at $T_A = 25^\circ\text{C}$ and -55°C ; $t_{SETUPH} = t_{SETUPL} = 180 \text{ ns}$ at $T_A = 125^\circ\text{C}$.
5. Requirements for MAX clock frequency (f_{CL}) are established by setting the parameter to the limits given in table III and observing proper output state changes.

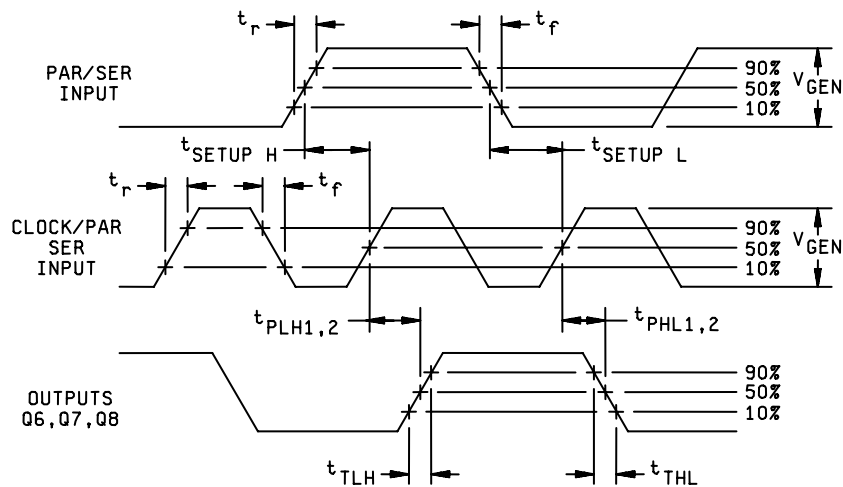
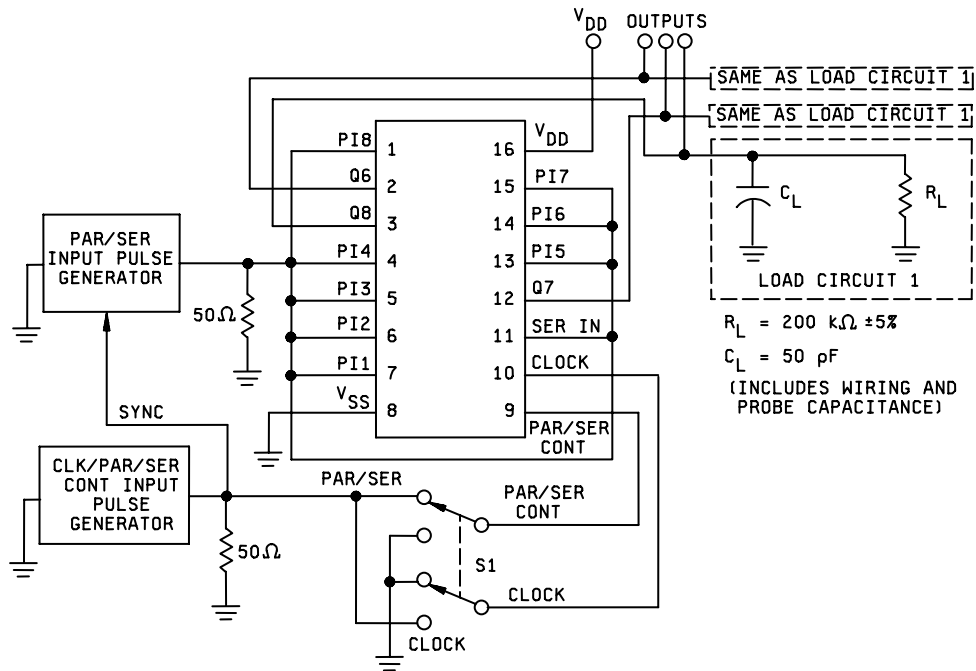
FIGURE 4. Switching time test circuit and waveforms – Continued.



NOTES:

1. The pulse generators have the following characteristics: $V_{GEN} = V_{DD} \pm 1$ percent, t_r and $t_f \leq 20$ ns, duty cycle = 50 percent, $Z_{OUT} = 50 \Omega$.
2. When measuring t_{PHL1} , t_{PLH1} , t_{THL} , and t_{TLH} , set switch S1 to clock position. Momentarily set switch S2 to position 2 to set outputs low and return to position 1.
3. When measuring t_{PHL2} set switch S2 to reset position. Momentarily set switch S2 to position 2 to set outputs low and return to position 1.
4. $t_{SETUPH} = t_{SETUPL} = 350$ ns at $T_A = 25^\circ\text{C}$ and -55°C ; $t_{SETUPH} = t_{SETUPL} = 500$ ns at $T_A = 125^\circ\text{C}$. For device types 03 and 53, $t_{SETUPH} = t_{SETUPL} = 108$ ns at $T_A = 25^\circ\text{C}$ and -55°C ; 150 ns at $T_A = 125^\circ\text{C}$.
5. For f_{CL} , set switch S1 to clock. Requirements for MAX clock frequency (f_{CL}) are established by setting the parameter to the limits given in table III and observing proper output state changes.

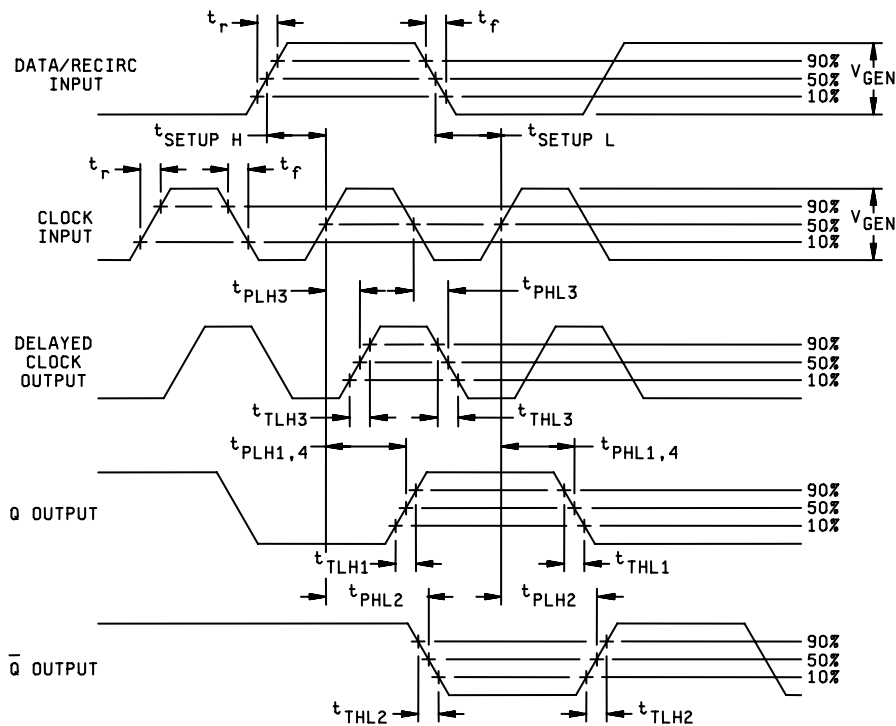
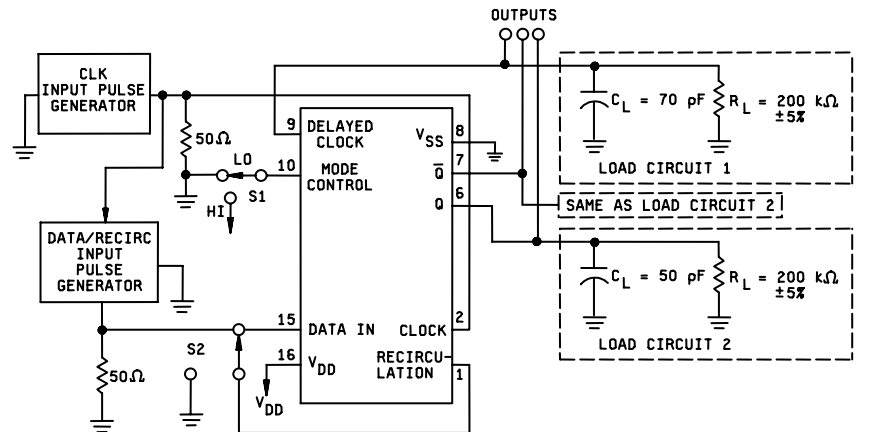
FIGURE 4. Switching time test circuit and waveforms – Continued.



NOTES:

1. The pulse generators have the following characteristics: $V_{GEN} = V_{DD} \pm 1$ percent, t_r and $t_f \leq 20$ ns, duty cycle = 50 percent, $Z_{OUT} = 50\Omega$.
2. When measuring t_{PHL1} and t_{PLH1} , set switch S1 to parallel/serial position.
3. When measuring t_{PHL2} , t_{PLH2} , t_{THL} , and t_{TLH} , set switch S1 to clock position.
4. $t_{SETUPH} = t_{SETUPL} = 350$ ns at $T_A = 25^\circ\text{C}$ and -55°C ; $t_{SETUPH} = t_{SETUPL} = 500$ ns at $T_A = 125^\circ\text{C}$. For device types 04 and 54, $t_{SETUPH} = t_{SETUPL} = 130$ ns at $T_A = 25^\circ\text{C}$ and -55°C ; 180 ns at $T_A = 125^\circ\text{C}$.
5. For f_{CL} , set switch S1 to clock. Requirements for MAX clock frequency (f_{CL}) are established by setting the parameter to the limits given in table III and observing proper output state changes.

FIGURE 4. Switching time test circuit and waveforms – Continued.

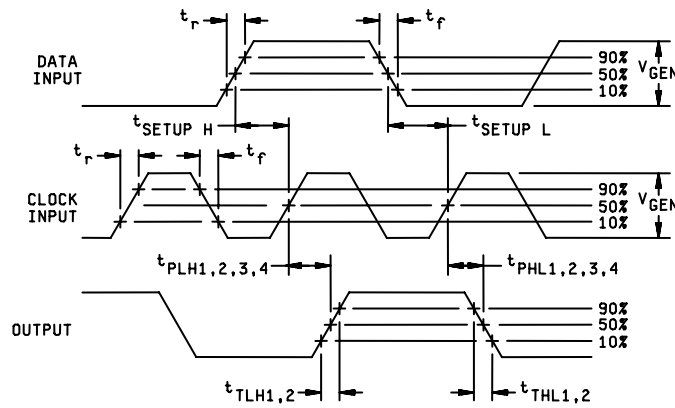
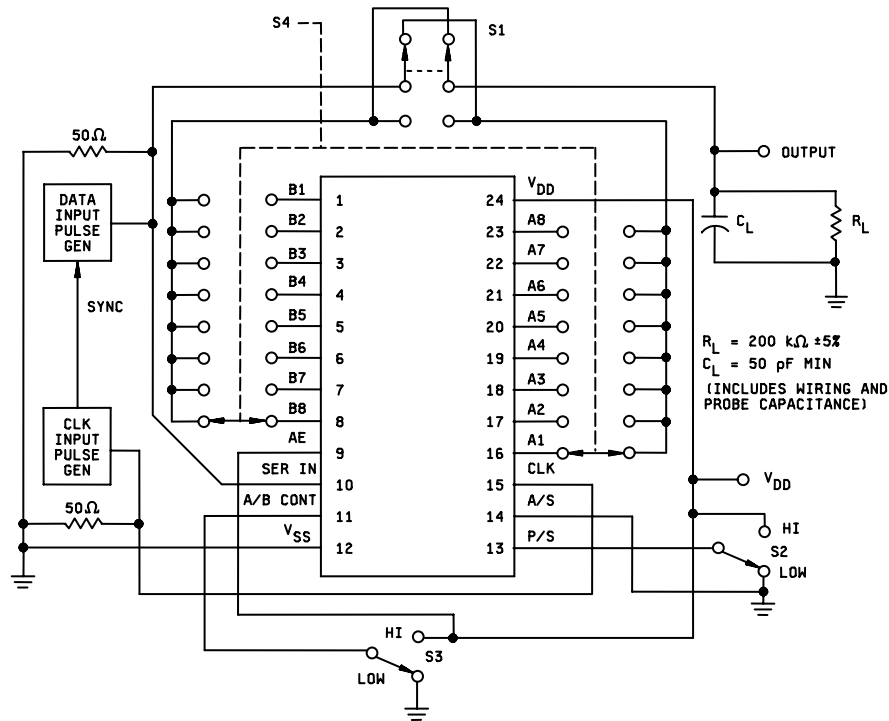


NOTES:

1. The pulse generators have the following characteristics: $V_{GEN} = V_{DD} \pm 1$ percent, t_r and $t_f \leq 20$ ns, duty cycle = 50 percent, $Z_{OUT} = 50\Omega$.
2. When measuring t_{PHL1} , t_{PHL2} , t_{PHL3} , t_{PLH1} , t_{PLH2} , t_{PLH3} , t_{THL1} , t_{THL2} , t_{THL3} , t_{TLH1} , t_{TLH2} , and t_{TLH3} , set switch S1 to low position.
3. When measuring t_{PHL4} and t_{PLH4} , set switch S2 to high position.
4. $t_{SETUPH} = t_{SETUPL} = 400$ ns at $T_A = 25^\circ\text{C}$ and -55°C ; $t_{SETUPH} = t_{SETUPL} = 680$ ns at $T_A = 125^\circ\text{C}$. For device types 05 and 55, $t_{SETUPH} = t_{SETUPL} = 215$ ns at $T_A = 25^\circ\text{C}$ and -55°C ; 300 ns at $T_A = 125^\circ\text{C}$.
5. For f_{CL} , set switch S1 to low position. Requirements for MAX clock frequency (f_{CL}) are established by setting the parameter to the limits given in table III and observing proper output state changes.

FIGURE 4. Switching time test circuit and waveforms – Continued.

Device types 06 and 56



NOTES:

1. The pulse generators have the following characteristics: $V_{GEN} = V_{DD} \pm 1$ percent, t_r and $t_f \leq 20$ ns, duty cycle = 50 percent, $Z_{OUT} = 50\Omega$.
2. When measuring t_{PHL1} , t_{PLH1} , t_{THL1} , and t_{TLH1} , set switch S2 and S3 to high position.
3. When measuring t_{PHL2} , t_{PLH2} , t_{THL2} , and t_{TLH2} , set switch S2 to high position and S3 to low position.
4. When measuring t_{PHL3} and t_{PLH3} , set switch S2 to low position and S3 to high position.
5. When measuring t_{PHL4} and t_{PLH4} , set switch S2 to low position and S3 to low position.
6. $t_{SETH} = t_{SETL} = 500$ ns at $T_A = 25^\circ\text{C}$ and -55°C ; $t_{SETH} = t_{SETL} = 650$ ns at $T_A = 125^\circ\text{C}$. For device types 06 and 56, $t_{SETH} = t_{SETL} = 172$ ns at $T_A = 25^\circ\text{C}$ and -55°C ; 240 ns at $T_A = 125^\circ\text{C}$.
7. For f_{CL} , set switch S2 to low position and S3 to low position and then high position. Requirements for MAX clock frequency (f_{CL}) are established by setting the parameter to the limits given in table III and observing proper output state changes.

FIGURE 4. Switching time test circuit and waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and conformance inspection. The following additional criteria shall apply:

- a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Delete the sequence specified as interim (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of table IA of MIL-PRF-38535 and substitute lines 1 through 7 of table II herein.
- c. Burn-in (method 1015 of MIL-STD-883).
 - (1) Unless otherwise specified in the manufacturers QM plan for static tests (test condition A), ambient temperature (T_A) shall be +125°C minimum. Test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table I of method 1015 for class B devices.
 - i. For static burn-in I, all inputs shall be connected to 0.0 V.
 - ii. For static burn-in II, all inputs shall be connected to V_{DD} .
 - iii. Except for V_{DD} and V_{SS} , the terminal shall be connected through resistors whose value is 2 k Ω to 47 k Ω . The actual measured value of the resistor selected shall not exceed $\pm 20\%$ of its branded value due to use, heat or age.
 - iv. Output may be open or connected to $V_{DD}/2$.
 - v. V_{DD} = 12.5 V minimum, 15 V maximum for device types 01 through 06.
 V_{DD} = 15 V minimum, 18 V maximum for device types 51 through 56.
 $V_{DD}/2$ = $V_{DD}/2 \pm 1.0$ V for all devices.
 V_{SS} = 0.0 V.
 - (2) Unless otherwise specified in the manufacturers QM plan for dynamic test (test condition D), ambient temperature shall be +125°C minimum. Test duration shall be in accordance with table I of method 1015.
 - i. Except for V_{DD} and V_{SS} , the terminals shall be connected through resistors whose value is 2 k Ω to 47 k Ω . The actual measured value of the resistor selected shall not exceed $\pm 20\%$ of its branded value due to use, heat or age.
 - ii. Input signal requirements: Square wave, 50% duty cycle; 25 kHz < PRR < 1 MHz; t_{TLH} and t_{THL} < 1 μ s. Voltage level: Minimum = $V_{SS} - 0.5$ V, +10% V_{DD} ; Maximum = $V_{DD} + 0.5$ V, -10% V_{DD} .
 - iii. V_{DD} = 12.5 V minimum, 15 V maximum for device types 01 through 06.
 V_{DD} = 15 V minimum, 18 V maximum for device types 51 through 56.
 $V_{DD}/2$ = $V_{DD}/2 \pm 1.0$ V.
 V_{SS} = 0.0 V.

- d. Interim and final electrical test parameters shall be as specified in table II.
- e. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.
- f. When device types 01 through 06 are qualified by extension (see 4.3.1), they shall be screened in accordance with the requirements for corresponding device types 51 through 56.

TABLE II. Electrical test requirements.

Line no.	MIL-PRF-38535 test requirements	Class S device <u>1/</u>			Class B device <u>1/</u>		
		Ref. par.	Table III Subgroups <u>2/</u>	Table IV delta limits <u>3/</u>	Ref. par.	Table III subgroups <u>2/</u>	Table IV delta limits <u>3/</u>
1	Interim electrical parameters		1			1	
2	Static burn-in I (method 1015)	4.2c 4.5.2					
3	Same as line 1		1	Δ			
4	Static burn-in II (method 1015)	4.2c 4.5.2			4.2c 4.5.2	<u>4/</u>	
5	Same as line 1	4.2e	1*	Δ	4.2e	1*	Δ
6	Dynamic burn-in (method 1015)	4.2c 4.5.2					
7	Same as line 1	4.2e	1*	Δ			
8	Final electrical parameters (method 5004)		1*, 2, 3, 7, 9			1*, 2, 3, 7, 9	
9	Group A test requirements (method 5005)	4.4.1	1, 2, 3, 4, 7, 8, 9, 10, 11		4.4.1	1, 2, 3, 4, 7, 8, 9, 10, 11	
10	Group B test when using method 5005 QCI option	4.4.2	1, 2, 3, 7, 8, 9, 10, 11	Δ			
11	Group C end-point electrical parameters (method 5005)				4.4.3	1, 2, 3	Δ
12	Group D end-point electrical parameters (method 5005)	4.4.4	1, 2, 3		4.4.4	1, 2, 3	

1/ Blank spaces indicate tests are not applicable.

2/ * indicates PDA applies to subgroup 1 (see 4.2.1).

3/ Δ indicates delta limits shall be required only on table III subgroup 1, where specified, and the delta values shall be computed with reference to the previous interim electrical parameters.

4/ The device manufacturer may at his option either perform delta measurements or within 24 hours after burn-in (or removal of bias) perform the final electrical parameter measurements.

4.2.1 Percent defective allowable (PDA).

- a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.
- b. Static burn-in I and II failure shall be cumulative for determining the PDA.
- c. The PDA for class B devices shall be in accordance with MIL-PRF-38535 for static burn-in. Dynamic burn-in is not required.
- d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table III, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualifying inspection, if a manufacturer qualifies to a 51-56 device type, which is manufactured identically to a 01-06 device type on this specification, then the 01-06 device type may be part I qualified by conducting only worst case group A electrical tests and any electrical tests specified as additional group C subgroups and submitting data in accordance with MIL-PRF-38535.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- a. Tests shall be performed in accordance with table II herein.
- b. Subgroups 5 and 6 shall be omitted.
- c. Subgroup 4 (C_i measurement) shall be measured only for initial qualification and after process or design changes that may affect input capacitance. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz.
- d. Subgroups 9 and 11 shall be measured only for initial qualification and after process or design changes which may affect dynamic performance.
- e. At the manufacturers option, test tapes may be programmed simultaneously for each identical section provided that each output is measured and each specified input combination is tested.
- f. When device types 01 through 06 are qualified by extension (see 4.3.1), these device types will be inspected (QCI) according to the requirements for device types 51 through 56, respectively.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IV herein.
- b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- c. When device types 01 through 06 are qualified by extension (see 4.3.1), these device types will be inspected (QCI) according to the requirements for device types 51 through 56, respectively.

TABLE III. Group A inspection for device type 01.

Symbol	MIL-STD-883 method	Cases A, C, D, T, X, Y	Terminal conditions and limits 1/														Measured Terminal	Test limits						Unit							
			Symbol	D1	NC	Clock	D2	D3	D4	V _{SS}	D4+4	D4+5	D3+4	D2+4	D2+5	D1+4		V _{DD}	Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C								
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13		14	Min	Max	Min	Max	Min		Max						
V _{IC} (pos)	1	2 3 4 5	1mA		1mA	1mA	1mA									GND	D1 Clock D2 D3 D4	1.5	"					V							
V _{IC} (neg)		6	7 8 9 10	-1mA		-1mA	-1mA	-1mA	GND								D1 Clock D2 D3 D4								-6	"					"
I _{SS} 2/			3005	11 12 13 14 15 16 17 18 19	GND 15.0V GND 15.0V GND 15.0V 15.0V 15.0V 15.0V GND	3	/" " " " GND 15.0V GND 15.0V GND	GND 15.0V GND 15.0V 15.0V 15.0V 15.0V 15.0V GND	GND 15.0V GND 15.0V 15.0V 15.0V 15.0V 15.0V GND	" " " " " " " " " "							15.0V " 														

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.

Symbol	MIL-STD-883 method	Cases A, C, D, T, X, Y	Terminal conditions and limits 1/														Measured Terminal	Test limits						Unit
			Symbol	D1	NC	Clock	D2	D3	D4	V _{SS}	D4+4	D4+5	D3+4	D2+4	D2+5	D1+4		V _{DD}	Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C	
		Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	Min	Max	Min	Max	
I _{IH1} 11/	3010	44	15.0V		15.0V	15.0V	15.0V	15.0V	GND							15.0V	All inputs together							nA
I _{IH2}		45	15.0V	GND	15.0V	GND	GND	GND	"							"	D1	5.0	"		"			"
		46	GND		GND	15.0V	GND	"	"						"	Clock		"		"			"	
		47	"		GND	GND	15.0V	"	"						"	D2	1.0	"	45	"			"	
		48	"		GND	GND	GND	15.0V	"	"					"	D3		"	"	"			"	
I _{IL1} 11/	3009	50	GND		GND	GND	GND	GND							15.0V	All inputs together							nA	
I _{IL2}		51	"		"	"	"	"	"						"	D1	-5.0	"		"			"	
		52	"		"	"	"	"	"						"	Clock		"		"			"	
		53	"		"	"	"	"	"						"	D2	-1.0	"	-45	"			"	
		54	"	"	"	"	"	"	"						"	D3		"	"	"			"	
		55	"		"	"	"	"	"						"	D4		"	"	"			"	
																	Subgroup 4 T _C = 25°C							
																	Min	Max						
C _i	3012	56	12/		12/	12/			GND							GND	D1							pF
		57							"							"	Clock		70					"
		58				12/			"							"	D2		12					"
		59				12/			"							"	D3		12					"
		60						12/	"							"	D4		12					"
																	Subgroup 7 T _C = 25°C		Subgroup 8					
																	T _C = 25°C		T _C = 125°C		T _C = -55°C			
																	Min	Max	Min	Max	Min	Max		
Truth table test	3014 13/	61	GND	14	/	GND	GND	GND	GND							5.0V	None	See 15/, 16/						
		62	5.0V		"	5.0V	5.0V	5.0V	"	"				"	None									
		63	GND		"	GND	GND	GND	"	"	L		L		"	None								
		64	"		"	"	"	"	"	"			L		"	None								
		65	"		GND	"	"	"	"	"	"			"		All								
		66	"		GND	"	"	"	"	"	"			"		outputs								
		67	"		GND	"	"	"	"	"	"			"		"								
		68	5.0V		5.0V	5.0V	5.0V	5.0V	"	"	"			"		"								
		69	"		"	"	"	"	"	"	"			"		"								
		70	"		"	"	"	"	"	"	"			"		"								
		71	"		"	"	"	"	"	"	"			"		"								
		72	"		GND	"	"	"	"	"	H	L	H		L	"								
		73	"		5.0V	"	"	"	"	"	H	L	H	L	L	"								
		74	"		GND	"	"	"	"	"	L	L	L	L	H	"								
		75	"		5.0V	"	"	"	"	"	L	H	L	L	H	"								
		76	"		GND	"	"	"	"	"	L	L	L	L	L	"								

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 – Continued.

Symbol	MIL-STD-883 method	Cases A, C, D, T, X, Y	Terminal conditions and limits 1/														Measured Terminal	Test limits						Unit
		Symbol	D1	NC	Clock	D2	D3	D4	V _{SS}	D4+4	D4+5	D3+4	D2+4	D2+5	D1+4	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C		
		Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	Min	Max	Min	Max	
t _{PHL}	3003 Fig. 4	77						IN	GND	OUT						5.0V	Clock to D4+4	20	800	30	1200	20	800	ns
		78		IN	"			IN	"		OUT					"	Clock to D4+5	"	"	"	"	"	"	"
		79			"		IN		"			OUT				"	Clock to D4+4	"	"	"	"	"	"	"
		80			"	IN			"			OUT				"	Clock to D3+4	"	"	"	"	"	"	"
		81			"	IN			"				OUT			"	Clock to D2+4	"	"	"	"	"	"	"
		82	IN		"				"						OUT	"	Clock to D2+5	"	"	"	"	"	"	"
																Clock to D1+4	"	"	"	"	"	"	"	
t _{PLH}	3003 Fig. 4	83						IN	GND	OUT						5.0V	Clock to D4+4	20	650	30	975	20	650	ns
		84		IN	"			IN	"		OUT					"	Clock to D4+4	"	"	"	"	"	"	"
		85			"		IN		"			OUT				"	Clock to D4+5	"	"	"	"	"	"	"
		86			"	IN			"				OUT			"	Clock to D3+4	"	"	"	"	"	"	"
		87			"	IN			"					OUT		"	Clock to D2+4	"	"	"	"	"	"	"
		88	IN		"				"						OUT	"	Clock to D2+5	"	"	"	"	"	"	"
																Clock to D1+4	"	"	"	"	"	"	"	
t _{THL}	3004 Fig. 4	89			"			IN	"	OUT						"	D4+4	13	760	18	1140	13	760	"
		90			"			IN	"		OUT					"	D4+5	"	"	"	"	"	"	"
		91			"		IN		"			OUT				"	D3+4	"	"	"	"	"	"	"
		92			"	IN			"				OUT			"	D2+4	"	"	"	"	"	"	"
		93			"	IN			"					OUT		"	D2+5	"	"	"	"	"	"	"
		94	IN		"				"						OUT	"	D1+4	"	"	"	"	"	"	"
t _{TLH}	3004 Fig. 4	95			"			IN	"	OUT						"	D4+4	"	"	"	"	"	"	"
		96			"			IN	"		OUT					"	D4+5	"	"	"	"	"	"	"
		97		"	"		IN		"			OUT				"	D3+4	"	"	"	"	"	"	"
		98			"	IN			"				OUT			"	D2+4	"	"	"	"	"	"	"
		99			"	IN			"					OUT		"	D2+5	"	"	"	"	"	"	"
		100	IN		"				"						OUT	"	D1+4	"	"	"	"	"	"	"
f _{CL} (max) 17/	101	102			"			IN	"	OUT						"	Clock							μs
		103			"			IN	"		OUT					"								"
		104		"	"	IN			"			OUT				"		1.0		1.4		1.0		"
		105			"	IN			"				OUT			"								"
		106	IN		"				"						OUT	"								"

See footnotes on next page.

TABLE III. Group A inspection for device type 01 – Continued.

- 1/ Terminals not designated may be “HIGH” level logic, “LOW” level logic, or open except as follows:
 $I_{C(POS)}$ tests; the V_{SS} terminal shall be open.
 $I_{C(NEG)}$ tests; the V_{DD} terminal shall be open.
 V_{SS} tests; the output terminals shall be open.
- 2/ Test numbers 11 through 19 shall be run in sequence. See 4.5.3.
- 3/ Apply single clock pulse; $V_{IN} = 0\text{ V}$ to V_{DD} .
- 4/ $V_{IH1} = 3.8\text{ V}$ at 25°C , 3.6 V at 125°C , 3.95 V at -55°C .
- 5/ Apply clock pulse; $V_{IN} = 0\text{ V}$ to V_{DD} until proper output state is achieved.
- 6/ $I_{OH} = -100\text{ }\mu\text{A}$ at 25°C , $-70\text{ }\mu\text{A}$ at 125°C , $-125\text{ }\mu\text{A}$ at -55°C .
- 7/ $V_{IH2} = 9.5\text{ V}$ at 25°C , 9.25 V at 125°C , 9.75 V at -55°C .
- 8/ $V_{IL1} = 1.1\text{ V}$ at 25°C , 0.85 V at 125°C , 1.35 V at -55°C .
- 9/ $I_{OL} = 125\text{ }\mu\text{A}$ at 25°C , $85\text{ }\mu\text{A}$ at 125°C , $155\text{ }\mu\text{A}$ at -55°C .
- 10/ $V_{IL2} = 2.8\text{ V}$ at 25°C , 2.55 V at 125°C , 3.05 V at -55°C .
- 11/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together.
- 12/ See 4.4.1c.
- 13/ Test numbers 61 through 76 shall be run in sequence.
- 14/ Apply single clock pulse; $V_{IN} = 0\text{ V}$ to V_{DD} .
- 15/ The output voltage limits for each temperature are “H” = $V_{DD} - 0.5\text{ V}$ min. and “L” = $V_{SS} + 0.5\text{ V}$ max.
- 16/ The functional tests shall be performed at V_{IH} and $V_{DD} \leq 5.0\text{ V}$ and $\geq 15\text{ V}$.
- 17/ The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.

TABLE III. Group A inspection for device type 02.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S Control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C		
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Min	Max	Min	Max	Min	Max	
V _{IC} (POS)	1	2 3 4 5 6 7 8 9 10 11	1mA			1mA	1mA	1mA	1mA		1mA		1mA		1mA		GND	PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial In PI5 PI6 PI7	1.5	"					V	
V _{IC} (NEG)	12	13 14 15 16 17 18 19 20 21 22	-1mA			-1mA	-1mA	-1mA	-1mA	GND	-1mA		-1mA		-1mA		PI8	PI4 PI3 PI2 PI1 P/S control Clock Serial In PI5 PI6 PI7	-6	"					"	
I _{SS} 2/	3005	23 24 25 26 27 28 29 30 31 32	GND GND GND 15.0V " " " " " GND			GND GND GND 15.0V " " " " " GND	15.0V 15.0V 15.0V GND " " " " " 15.0V	GND GND GND 15.0V " " " " " GND	15.0V 15.0V 15.0V GND " " " " " 15.0V	"	15.0V " " " " " GND " " " "	15.0V GND GND 15.0V GND 15.0V GND 15.0V	GND GND GND 15.0V GND 15.0V GND 15.0V	15.0V	15.0V 15.0V GND 15.0V GND 15.0V GND 15.0V	GND GND GND 15.0V GND 15.0V GND 15.0V	15.0V	15.0V	None " " " V _{SS} None V _{SS} None None V _{SS}	-0.5	"	-5.0	"			μA
V _{OH1}	3006	33 34 35	V _{IH1 3/} V _{IH1 3/} V _{IH1 3/}	I _{OH 4/}		V _{IH1 3/} V _{IH1 3/} V _{IH1 3/}	V _{IH1 3/} V _{IH1 3/} V _{IH1 3/}	V _{IH1 3/} V _{IH1 3/} V _{IH1 3/}	V _{IH1 3/} V _{IH1 3/} V _{IH1 3/}	"	V _{IH1 3/} V _{IH1 3/} V _{IH1 3/}	5/	V _{IH1 3/} V _{IH1 3/} V _{IH1 3/}	I _{OH 4/}	V _{IH1 3/} V _{IH1 3/} V _{IH1 3/}	V _{IH1 3/} V _{IH1 3/} V _{IH1 3/}	V _{IH1 3/} V _{IH1 3/} V _{IH1 3/}	5.0V 5.0V 5.0V	Q6 Q7 Q8	4.5 4.5 4.5		4.5 4.5 4.5		4.5 4.5 4.5	V	
V _{OH2}		36 37 38	V _{IH2 6/} V _{IH2 6/} V _{IH2 6/}			V _{IH2 6/} V _{IH2 6/} V _{IH2 6/}	V _{IH2 6/} V _{IH2 6/} V _{IH2 6/}	V _{IH2 6/} V _{IH2 6/} V _{IH2 6/}	V _{IH2 6/} V _{IH2 6/} V _{IH2 6/}	"	V _{IH2 6/} V _{IH2 6/} V _{IH2 6/}	"	V _{IH2 6/} V _{IH2 6/} V _{IH2 6/}	V	V _{IH2 6/} V _{IH2 6/} V _{IH2 6/}	V _{IH2 6/} V _{IH2 6/} V _{IH2 6/}	V _{IH2 6/} V _{IH2 6/} V _{IH2 6/}	12.5V 12.5V 12.5V	Q6 Q7 Q8	11.25 11.25 11.25		11.25 11.25 11.25		11.25 11.25 11.25	"	
V _{OL1}		39 40 41	V _{IL1 8/} V _{IL1 8/} V _{IL1 8/}	I _{OL 7/}		V _{IL1 8/} V _{IL1 8/} V _{IL1 8/}	V _{IL1 8/} V _{IL1 8/} V _{IL1 8/}	V _{IL1 8/} V _{IL1 8/} V _{IL1 8/}	V _{IL1 8/} V _{IL1 8/} V _{IL1 8/}	"	V _{IH1 3/} V _{IH1 3/} V _{IH1 3/}	"	V _{IL1 8/} V _{IL1 8/} V _{IL1 8/}	I _{OL 7/}	V _{IL1 8/} V _{IL1 8/} V _{IL1 8/}	V _{IL1 8/} V _{IL1 8/} V _{IL1 8/}	V _{IL1 8/} V _{IL1 8/} V _{IL1 8/}	5.0V 5.0V 5.0V	Q6 Q7 Q8		0.5 0.5 0.5		0.5 0.5 0.5		0.5 0.5 0.5	"
V _{OL2}		42 43 44	V _{IL2 9/} V _{IL2 9/} V _{IL2 9/}			V _{IL2 9/} V _{IL2 9/} V _{IL2 9/}	V _{IL2 9/} V _{IL2 9/} V _{IL2 9/}	V _{IL2 9/} V _{IL2 9/} V _{IL2 9/}	"	V _{IH2 6/} V _{IH2 6/} V _{IH2 6/}	"	V _{IL2 9/} V _{IL2 9/} V _{IL2 9/}	V	V _{IL2 9/} V _{IL2 9/} V _{IL2 9/}	V _{IL2 9/} V _{IL2 9/} V _{IL2 9/}	V _{IL2 9/} V _{IL2 9/} V _{IL2 9/}	12.5V 12.5V 12.5V	Q6 Q7 Q8		1.25 1.25 1.25		1.25 1.25 1.25		1.25 1.25 1.25	"	

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit					
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S Control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C							
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min		Max				
I _{IH1} 10/	3010	45	15.0V			15.0V	15.0V	15.0V	15.0V	GND	15.0V	15.0V	15.0V		15.0V	15.0V	15.0V	15.0V	All inputs together							nA					
I _{IH2}		46	15.0V			GND	GND	GND	GND	"	GND	GND	GND		"	GND	GND	"	PI8	1100					"						
		47	"			15.0V	GND	GND	GND	"	"	"	"		"	"	"	"	PI4	"					"						
		48	"			GND	15.0V	GND	"	"	"	"	"	GND	"	"	"	"	PI3	100	"	100	"		"						
		49	"			"	GND	15.0V	"	"	"	"	"	"	"	"	"	"	PI2	"					"						
		50	"			"	"	GND	15.0V	"	"	"	"	"	"	"	"	"	PI1	"					"						
		51	"			"	"	"	"	15.0V	GND	"	"	"	"	"	"	"	P/S control	"					"						
		52	"			"	"	"	"	"	GND	15.0V	"	"	"	"	"	"	Clock	"					"						
		53	"			"	"	"	"	"	"	GND	15.0V	GND	15.0V	"	"	"	Serial In	"					"						
		54	"			"	"	"	"	"	"	"	"	"	15.0V	GND	"	"	PI5	"					"						
		55	"			"	"	"	"	"	"	"	"	"	GND	15.0V	GND	"	PI6	"					"						
		56	"			"	"	"	"	"	"	"	"	"	GND	GND	15.0V	"	PI7	"					"						
I _{IL1} 10/	3009	57	GND			GND	GND	GND	GND	GND	GND	GND		GND	GND	GND	15.0V	All inputs together							nA						
I _{IL2}		58	"			"	"	"	"	"	"	"	"		"	"	"	"	PI8	-1100					"						
		59	"			"	"	"	"	"	"	"	"		"	"	"	"	PI4	"					"						
		60	"			"	"	"	"	"	"	"	"		"	"	"	"	PI3	-100	"	-100	"		"						
		61	"			"	"	"	"	"	"	"	"	"	"	"	"	"	PI2	"					"						
		62	"			"	"	"	"	"	"	"	"	"	"	"	"	"	PI1	"					"						
		63	"			"	"	"	"	"	"	"	"	"	"	"	"	"	P/S control	"					"						
		64	"			"	"	"	"	"	"	"	"	"	"	"	"	"	Clock	"					"						
		65	"			"	"	"	"	"	"	"	"	"	"	"	"	"	Serial In	"					"						
		66	"			"	"	"	"	"	"	"	"	"	"	"	"	"	PI5	"					"						
		67	"			"	"	"	"	"	"	"	"	"	"	"	"	"	PI6	"					"						
		68	"			"	"	"	"	"	"	"	"	"	"	"	"	"	PI7	"					"						
																		Subgroup 4 T _C = 25°C													
																		Min	Max												
C _i	3012	69	11/			11/				GND							GND	PI8	12					pF							
		70							"								"	PI4													
		71							"								"	PI3													
		72					11/			"							"	PI2													
		73								"							"	PI1													
		74								"		11/					"	P/S control													
		75								"							"	Clock													
		76								"							"	Serial In													
		77								"							"	PI5													
		78								"							"	PI6													
		79								"							"	PI7													

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N, Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S Control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 7 T _C = 25°C		Subgroup 8 T _C = 125°C T _C = 125°C				
		Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Min	Max	Min	Max	Min	Max		
Truth table test <u>12/</u>	3014	80	5.0V			5.0V	5.0V	5.0V	5.0V	GND	5.0V	5.0V	GND		5.0V	5.0V	5.0V	5.0V	None None All outputs	See <u>13/</u> and <u>14/</u>						
		81	5.0V			5.0V	5.0V	5.0V	5.0V	"	5.0V	GND	"	H	5.0V	5.0V	5.0V	"								
		82	5.0V	H	H	5.0V	5.0V	5.0V	5.0V	"	5.0V	5.0V	"	"	5.0V	5.0V	5.0V	"								
		83	GND	"	"	GND	GND	GND	GND	"	GND	5.0V	"	"	GND	GND	GND	"								
		84	"	"	"	"	"	"	"	"	"	GND	"	"	"	"	"	"								
		85	"	L	"	"	"	"	"	"	"	5.0V	"	"	"	"	"	"								
		86	"	"	"	"	"	"	"	"	"	5.0V	5.0V	"	"	"	"	"								
		87	"	"	"	"	"	"	"	"	"	GND	5.0V	"	"	"	"	"								
		88	"	"	"	"	"	"	"	"	"	5.0V	"	"	"	"	"	"								
		89	"	"	"	"	"	"	"	"	"	GND	"	"	"	"	"	"								
		90	"	"	"	"	"	"	"	"	"	5.0V	"	"	"	"	"	"								
		91	"	"	"	"	"	"	"	"	"	GND	"	"	"	"	"	"								
		92	"	"	"	"	"	"	"	"	"	5.0V	"	"	"	"	"	"								
		93	"	"	"	"	"	"	"	"	"	GND	"	"	"	"	"	"								
		94	"	"	"	"	"	"	"	"	"	5.0V	"	"	"	"	"	"								
		95	"	"	"	"	"	"	"	"	"	GND	"	"	"	"	"	"								
		96	"	L	"	"	"	"	"	"	"	5.0V	"	"	"	"	"	"								
		97	"	L	"	"	"	"	"	"	"	GND	"	"	"	"	"	"								
		98	"	H	"	"	"	"	"	"	"	5.0V	"	L	"	"	"	"								
		99	"	"	"	"	"	"	"	"	"	GND	"	L	"	"	"	"								
		100	"	"	L	"	"	"	"	"	"	5.0V	"	H	"	"	"	"								
		101	"	"	L	"	"	"	"	"	"	GND	"	"	"	"	"	"								
		102	"	"	H	"	"	"	"	"	"	5.0V	"	"	"	"	"	"								
		103	"	"	H	"	"	"	"	"	"	5.0V	5.0V	GND	"	"	"	"								
		104	"	"	H	"	"	"	"	"	"	5.0V	GND	"	"	"	"	"								
		105	"	L	L	"	"	"	"	"	"	5.0V	5.0V	"	L	"	"	"								
		106	5.0V	L	L	5.0V	5.0V	5.0V	5.0V	"	GND	GND	"	L	5.0V	5.0V	5.0V	"								

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																														
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S Control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 7		Subgroup 8																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																		
																				T _C = 25°C		T _C = 125°C		T _C = -55°C																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
																				Min	Max	Min	Max	Min	Max																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
Truth table test 12/	3014	107	5.0V	L	L	5.0V	5.0V	5.0V	5.0V	GND	GND	5.0V	GND	L	5.0V	5.0V	5.0V	5.0V	All outputs																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																					

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z Test no.	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S Control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C		
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Min	Max	Min	Max	Min	Max	
t _{PHL1}	3003 Fig. 4	128	IN	OUT		IN	IN	IN	IN	GND	GND	IN	IN		IN	IN	IN	5.0V	Clock to Q6	13	975	18	1465	13	975	ns
		129	"			"	"	"	"	"	"	"	"	OUT	"	"	"	"	Clock to Q7	"	"	"	"	"	"	"
		130	"		OUT	"	"	"	"	"	"	"	"		"	"	"	"	Clock to Q8	"	"	"	"	"	"	"
t _{PLH1}		131	"	OUT		"	"	"	"	"	"	"	"		"	"	"	"	Clock to Q6	"	"	"	"	"	"	"
		132	"			"	"	"	"	"	"	"	"	OUT	"	"	"	"	Clock to Q7	"	"	"	"	"	"	"
		133	"		OUT	"	"	"	"	"	"	"	"		"	"	"	"	Clock to Q8	"	"	"	"	"	"	"
t _{PHL2}		134	"	OUT		"	"	"	"	"	5.0V	"	"		"	"	"	"	Clock to Q6	"	"	"	"	"	"	"
		135	"			"	"	"	"	"	"	"	"	OUT	"	"	"	"	Clock to Q7	"	"	"	"	"	"	"
		136	"		OUT	"	"	"	"	"	"	"	"		"	"	"	"	Clock to Q8	"	"	"	"	"	"	"
t _{PLH2}		137	"	OUT		"	"	"	"	"	"	"	"		"	"	"	"	Clock to Q6	"	"	"	"	"	"	"
		138	"			"	"	"	"	"	"	"	"	OUT	"	"	"	"	Clock to Q7	"	"	"	"	"	"	"
		139	"		OUT	"	"	"	"	"	"	"	"		"	"	"	"	Clock to Q8	"	"	"	"	"	"	"
t _{THL}	3004 Fig. 4	140	"	OUT		"	"	"	"	"	"	"	"		"	"	"	"	Q6	10	650	14	975	10	650	"
		141	"			"	"	"	"	"	"	"	"	OUT	"	"	"	"	Q7	"	650	"	975	"	650	"
		142	"		OUT	"	"	"	"	"	"	"	"		"	"	"	"	Q8	"	650	"	975	"	650	"
t _{TLH}		143	"	OUT		"	"	"	"	"	"	"	"		"	"	"	"	Q6	"	900	"	1350	"	900	"
		144	"			"	"	"	"	"	"	"	"	OUT	"	"	"	"	Q7	"	900	"	1350	"	900	"
		145	"		OUT	"	"	"	"	"	"	"	"		"	"	"	"	Q8	"	900	"	1350	"	900	"
f _{CL} (max) 15/		147							"	GND	"	"	"				"	Clock							μs	
		148	OUT		OUT				"	GND	"	"	"	OUT			"	Clock	1.0	1.0	1.4	1.4	1.0	1.0	μs	

See footnotes on next page.

TABLE III. Group A inspection for device type 02 – Continued.

- 1/ Terminals not designated may be “HIGH” level logic, “LOW” level logic, or open except as follows:
 $I_{C(POS)}$ tests; the V_{SS} terminal shall be open.
 $I_{C(NEG)}$ tests; the V_{DD} terminal shall be open.
 V_{SS} tests; the output terminals shall be open.
- 2/ Test numbers 23 through 32 shall be run in sequence. See 4.5.3.
- 3/ $V_{IH1} = 3.8 \text{ V}$ at 25°C , 3.6 V at 125°C , 3.95 V at -55°C .
- 4/ $I_{OH} = -80 \mu\text{A}$ at 25°C , $-55 \mu\text{A}$ at 125°C , $-100 \mu\text{A}$ at -55°C .
- 5/ Apply clock pulse; $V_{IN} = 0 \text{ V}$ to V_{DD} until proper output state is achieved.
- 6/ $V_{IH2} = 9.5 \text{ V}$ at 25°C , 9.25 V at 125°C , 9.75 V at -55°C .
- 7/ $I_{OL} = 120 \mu\text{A}$ at 25°C , $85 \mu\text{A}$ at 125°C , $150 \mu\text{A}$ at -55°C .
- 8/ $V_{IL1} = 1.1 \text{ V}$ at 25°C , 0.85 V at 125°C , 1.35 V at -55°C .
- 9/ $V_{IL2} = 2.8 \text{ V}$ at 25°C , 2.55 V at 125°C , 3.05 V at -55°C .
- 10/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together.
- 11/ See 4.4.1c.
- 12/ Test numbers 80 through 127 shall be run in sequence.
- 13/ The output voltage limits for each temperature are “H” = $V_{DD} - 0.5 \text{ V min.}$ and “L” = $V_{SS} + 0.5 \text{ V max.}$
- 14/ The functional tests shall be performed at V_{IH} and $V_{DD} \leq 5.0 \text{ V}$ and $\geq 15 \text{ V}$.
- 15/ The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.

See footnotes at end of device type 03.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit		
			Clock B	Q4B	Q3A	Q2A	Q1A	Reset A	Data A	V _{SS}	Clock A	Q4A	Q3B	Q2B	Q1B	Reset B	Data B	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C				
		Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Min	Max	Min	Max	Min	Max			
V _{IC} (POS)	1	2 3 4 5 6	1mA					1mA	1mA		1mA						1mA	1mA	GND " " " " "	Clock A Data A Reset A Clock B Data B Reset B	1.5	" " " " "						V
V _{IC} (NEG)	7	8 9 10 11 12	-1mA					-1mA	-1mA	GND " " " "	-1mA						1mA	-1mA	Clock A Data A Reset A Clock B Data B Reset B	-6	" " " " "						"	
I _{SS} 2/	3005	13 14 15 16 17 18 19 20 21 22 23 24 25 26 27	GND 15.0V 15.0V GND 15.0V 15.0V GND 15.0V 15.0V GND 15.0V 15.0V GND 15.0V 15.0V					15.0V 15.0V GND " " " " " " " " " " " " " " "	15.0V 15.0V GND " " " " " " " " " " " " " "	" " " " " " " " " " " " " " "	GND 15.0V 15.0V GND 15.0V 15.0V GND 15.0V 15.0V GND 15.0V 15.0V GND 15.0V 15.0V						15.0V 15.0V GND 15.0V 15.0V GND 15.0V 15.0V GND 15.0V 15.0V GND 15.0V 15.0V	15.0V " " " " " " " " " " " " " "	V _{SS} None "<									

TABLE III. Group A inspection for device type 03 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit					
			Clock B	Q4B	Q3A	Q2A	Q1A	Reset A	Data A	V _{SS}	Clock A	Q4A	Q3B	Q2B	Q1B	Reset B	Data B	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C							
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min		Max				
V _{OL1}	3007	44	GND				I _{OL g/}	V _{IL1}	V _{IL1}	GND	3/					GND	GND	5.0V	Q1A	0.5		0.5		0.5		V					
		45																	Q2A												
		46			I _{OL}	I _{OL}													Q3A												
		47																	Q4A												
		48	3/					GND	GND		GND								Q1B												
		49																	Q2B												
		50																	Q3B												
V _{OL2}	3007	51		I _{OL}									I _{OL}	I _{OL}	I _{OL}				Q4B	1.25		1.25		1.25							
		52	GND					V _{IL2}	V _{IL2}		3/					GND	GND	12.5V	Q1A												
		53																	Q2A												
		54																	Q3A												
		55																	Q4A												
		56	3/					GND	GND		GND								Q1B												
		57																	Q2B												
I _{IH1} 10/ I _{IH2}	3010	58																	Q3B	600		100									
		59																	Q4B												
		60	15.0V					15.0V	15.0V	GND	15.0V					15.0V	15.0V	15.0V	All inputs together							100					nA
		61	GND					GND	GND		15.0V					GND	GND		Clock A												
		62	GND					GND	15.0V		GND								Data A												
		63	GND					15.0V	GND										Reset A												
		64	15.0V					GND											Clock B												
I _{IL1} 10/ I _{IL2}	3009	65	GND													15.0V	15.0V		Data B	-600		-100									
		66																	Reset B												
		67														GND	GND		All inputs together							-100					
		68																	Clock A												
		69																	Data A												
		70																	Reset A												
		71																	Clock B												
C _i	3012	72																	Data B	12			Unit								
		73																	Reset B												
		74																													
		75																													
		76																													
		77	11/					11/	11/	GND	11/								Clock A												
		78																	Data A												
C _i	3012	79																	Reset A	12			Unit								
		79																	Clock B												
C _i	3012	79																		Data B	12			Unit							
		79																		Reset B											

See footnotes at end of device type 03.

pF

TABLE III. Group A inspection for device type 03 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			Clock B	Q4B	Q3A	Q2A	Q1A	Reset A	Data A	V _{SS}	Clock A	Q4A	Q3B	Q2B	Q1B	Reset B	Data B	V _{DD}		Subgroup 7 T _C = 25°C		Subgroup 8				
																						T _C = 125°C		T _C = -55°C		
																						Min	Max	Min	Max	
Truth table test 12/	3014	80	5.0V	L	L	L	L	5.0V	5.0V	GND	5.0V	L	L	L	L	5.0V	5.0V	5.0V	All outputs	See 13/, 14/						
		81	5.0V	"	"	"	L	GND	"	"	5.0V	"	"	"	L	GND	"	"								
		82	GND	"	"	"	L	"	"	"	GND	"	"	"	L	"	"	"								
		83	5.0V	"	"	"	H	"	"	"	5.0V	"	"	"	H	"	"	"								
		84	5.0V	"	"	"	H	"	GND	"	5.0V	"	"	"	H	"	GND	"								
		85	GND	"	"	"	H	"	GND	"	GND	"	"	"	H	"	GND	"								
		86	5.0V	"	"	H	L	"	GND	"	5.0V	"	"	H	L	"	GND	"								
		87	5.0V	"	"	H	L	"	5.0V	"	5.0V	"	"	H	L	"	5.0V	"								
		88	GND	"	"	H	L	"	"	"	GND	"	"	H	L	"	"	"								
		89	5.0V	"	H	L	H	"	"	"	5.0V	"	H	L	H	"	"	"								
		90	GND	"	H	L	"	"	"	"	GND	"	H	L	"	"	"	"								
		91	5.0V	H	L	H	"	"	"	"	5.0V	H	L	H	"	"	"	"								
		92	GND	H	L	"	"	"	"	"	GND	H	L	"	"	"	"	"								
		93	5.0V	L	H	"	"	"	"	"	5.0V	L	H	"	"	"	"	"								
		94	GND	L	"	"	"	"	"	"	GND	L	"	"	"	"	"	"								
		95	5.0V	H	"	"	"	"	"	"	5.0V	H	"	"	"	"	"	"								
		96	GND	H	"	"	"	"	"	"	GND	H	"	"	"	"	"	"								
		97	GND	L	L	L	L	5.0V	"	"	GND	L	L	L	L	5.0V	"	"								
		98	5.0V	L	L	L	L	5.0V	"	"	5.0V	L	L	L	L	5.0V	"	"								
																			Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C			
																			Min	Max	Min	Max	Min	Max		
t _{PHL1}	3003 Fig. 4	99				OUT	GND	IN	GND	IN					GND		5.0V	Clock A to Q1A Clock A to Q2A Clock A to Q3A Clock A to Q4A Clock B to Q1B	20	975	30	1465	20	975	ns	
		100				OUT	"	"	"	"					"	"	"	"	"	"	"	"	"	"		
		101			OUT		"	"	"	"					"	"	"	"	"	"	"	"	"	"		
		102					"	"	"	"	OUT				"	"	"	"	"	"	"	"	"	"		
		103	IN				"	"	"					OUT	"	IN	"	"	"	"	"	"	"	"		
		104	IN					GND						OUT		GND	IN	5.0V	Clock B to Q2B Clock B to Q3B Clock B to Q4B	20	975	30	1465	20	975	ns
105	"					"	GND	"				OUT		"	"	"	"	"	"	"	"	"	"			
106	"	OUT				"	"	"						"	"	"	"	"	"	"	"	"	"			

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			Clock B	Q4B	Q3A	Q2A	Q1A	Reset A	Data A	V _{SS}	Clock A	Q4A	Q3B	Q2B	Q1B	Reset B	Data B	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C		
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Min	Max	Min	Max	Min	Max	
t _{PLH1}	3003 Fig. 4	107					OUT	GND	IN	GND	IN					GND		5.0V	Clock A to Q1A	20	975	30	1465	20	975	ns
		108				OUT		“	“	“	“					“		“	Clock A to Q2A	“	“	“	“	“	“	“
		109			OUT			“	“	“	“					“		“	Clock A to Q3A	“	“	“	“	“	“	“
		110						“	“	“	“	OUT				“		“	Clock A to Q4A	“	“	“	“	“	“	“
		111	IN					“		“				OUT		“	IN	“	Clock A to Q4A	“	“	“	“	“	“	“
		112	“					“		“				OUT		“	“	“	Clock B to Q1B	“	“	“	“	“	“	“
		113	“					“		“			OUT			“	“	“	Clock B to Q2B	“	“	“	“	“	“	“
		114	“	OUT				“		“						“	“	“	Clock B to Q3B	“	“	“	“	“	“	“
																	Clock B to Q4B	“	“	“	“	“	“	“		
t _{PHL2}	3003 Fig. 4	115	GND				OUT	IN			GND								Reset to Q1A	“	“	“	“	“	“	“
		116	“			OUT		“	“	“	“					“		“	Reset to Q2A	“	“	“	“	“	“	“
		117	“		OUT			“	“	“	“					“		“	Reset to Q3A	“	“	“	“	“	“	“
		118	“					“	“	“	“	OUT				“		“	Reset to Q4A	“	“	“	“	“	“	“
		119	“					“	“	“	“			OUT		IN	“	“	Reset to Q1B	“	“	“	“	“	“	“
		120	“					“	“	“	“			OUT		“	“	“	Reset to Q2B	“	“	“	“	“	“	“
		121	“					“	“	“	“		OUT			“	“	“	Reset to Q3B	“	“	“	“	“	“	“
		122	“	OUT				“	“	“	“					“	“	“	Reset to Q4B	“	“	“	“	“	“	“
t _{THL}	3004 Fig. 4	123					OUT	GND	IN	“	IN					GND		“	Q1A	13	650	18	975	13	650	“
		124						“	“	“	“					“		“	Q2A	“	“	“	“	“	“	“
		125			OUT			“	“	“	“					“		“	Q3A	“	“	“	“	“	“	“
		126						“	“	“	“	OUT				“		“	Q4A	“	“	“	“	“	“	“
		127	IN					“	“	“	“			OUT		“	IN	“	Q1B	“	“	“	“	“	“	“
		128	“					“	“	“	“			OUT		“	“	“	Q2B	“	“	“	“	“	“	“
		129	“					“	“	“	“		OUT			“	“	“	Q3B	“	“	“	“	“	“	“
		130	“	OUT				“	“	“	“					“	“	“	Q4B	“	“	“	“	“	“	“
t _{TLH}	3004 Fig. 4	131					OUT	“	IN	“	IN					“		“	Q1A	“	975	“	1465	“	975	“
		132				OUT		“	“	“	“					“		“	Q2A	“	“	“	“	“	“	“
		133			OUT			“	“	“	“					“		“	Q3A	“	“	“	“	“	“	“
		134						“	“	“	“	OUT				“		“	Q4A	“	“	“	“	“	“	“
		135	IN					“	“	“	“			OUT		“	IN	“	Q1B	“	“	“	“	“	“	“
		136	“					“	“	“	“			OUT		“	“	“	Q2B	“	“	“	“	“	“	“
		137	“					“	“	“	“		OUT			“	“	“	Q3B	“	“	“	“	“	“	“
		138	“	OUT				“	“	“	“					“	“	“	Q4B	“	“	“	“	“	“	“

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			Clock B	Q4B	Q3A	Q2A	Q1A	Reset A	Data A	V _{SS}	Clock A	Q4A	Q3B	Q2B	Q1B	Reset B	Data B	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C		
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min	
f _{CL} (max) <u>15/</u>	139	140				OUT	GND	IN	GND	IN					GND		5.0V	Clock A							μs	
141				OUT															1.0			1.4		1.0		
142											OUT															
143		IN												OUT					Clock B							
144																	IN									
145														OUT	OUT											
146		OUT										OUT														

1/ Terminals not designated may be "HIGH" level logic, "LOW" level logic, or open except as follows:

IC(POS) tests; the V_{SS} terminal shall be open.

IC(NEG) tests; the V_{DD} terminal shall be open.

V_{SS} tests; the output terminals shall be open.

2/ Test numbers 13 through 27 shall be run in sequence. See 4.5.3.

3/ Apply clock pulse; V_{IN} = 0 V to V_{DD} until proper output state is achieved.

4/ I_{OH} = -80 μA at 25°C, -55 μA at 125°C, -100 μA at -55°C.

5/ V_{IL1} = 1.1 V at 25°C, 0.85 V at 125°C, 1.35 V at -55°C.

6/ V_{IH1} = 3.8 V at 25°C, 3.6 V at 125°C, 3.95 V at -55°C.

7/ V_{IL2} = 2.8 V at 25°C, 2.55 V at 125°C, 3.05 V at -55°C.

8/ V_{IH2} = 9.5 V at 25°C, 9.25 V at 125°C, 9.75 V at -55°C.

9/ I_{OL} = 120 μA at 25°C, 85 μA at 125°C, 150 μA at -55°C.

10/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together.

11/ See 4.4.1c.

12/ Test numbers 80 through 98 shall be run in sequence.

13/ The output voltage limits for each temperature are "H" = V_{DD} -0.5 V min. and "L" = V_{SS} +0.5 V max.

14/ The functional tests shall be performed at V_{IH} and V_{DD} ≤ 5.0 V and ≥ 15 V.

15/ The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.

TABLE III. Group A inspection for device type 04.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C		
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Min	Max	Min	Max	Min	Max	
V _{IC} (POS)	1	2 3 4 5 6 7 8 9 10 11	1mA			1mA	1mA	1mA	1mA		1mA	1mA					GND	PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial IN PI5 PI6 PI7	1.5	"					V	
V _{IC} (NEG)	12	13 14 15 16 17 18 19 20 21 22	-1mA			-1mA	-1mA	-1mA	-1mA	GND							PI8	PI4 PI3 PI2 PI1 P/S control Clock Serial IN PI5 PI6 PI7	-6	"					"	
I _{SS} 2/	3005	23 24 25 26 27 28 29	GND 15.0V 15.0V 15.0V GND GND GND			GND 15.0V 15.0V 15.0V GND GND GND	15.0V GND 15.0V 15.0V 15.0V 15.0V 15.0V	GND 15.0V 15.0V 15.0V 15.0V 15.0V 15.0V	15.0V GND 15.0V 15.0V 15.0V 15.0V 15.0V	" " " " " " "	15.0V 15.0V 15.0V 15.0V 15.0V 15.0V 15.0V	GND GND 15.0V 15.0V 15.0V 15.0V 15.0V	15.0V 15.0V 15.0V 15.0V 15.0V 15.0V 15.0V	GND GND GND GND GND GND GND	15.0V 15.0V 15.0V 15.0V 15.0V 15.0V 15.0V	GND 15.0V 15.0V 15.0V 15.0V 15.0V 15.0V	15.0V 15.0V 15.0V 15.0V 15.0V 15.0V 15.0V	V _{SS} V _{SS} None V _{SS} None V _{SS} V _{SS}	-0.5	"	-5.0	"	"	"	μA	
V _{OH1}	3006	30 31 32	V _{IH1} 3/ V _{IH1} 3/ V _{IH1} 3/	I _{OH} 4/		V _{IH1} V _{IH1} V _{IH1}	V _{IH1} V _{IH1} V _{IH1}	V _{IH1} V _{IH1} V _{IH1}	V _{IH1} V _{IH1} V _{IH1}	" " "	V _{IH1} V _{IH1} V _{IH1}	5/ " "	V _{IH1} V _{IH1} V _{IH1}	I _{OH}	V _{IH1} V _{IH1} V _{IH1}	V _{IH1} V _{IH1} V _{IH1}	V _{IH1} V _{IH1} V _{IH1}	5.0V 5.0V 5.0V	Q6 Q7 Q8	4.5 4.5 4.5		4.5 4.5 4.5	4.5 4.5 4.5	4.5 4.5 4.5	"	
V _{OH2}		33 34 35	V _{IH2} 6/ V _{IH2} 6/ V _{IH2} 6/			V _{IH2} V _{IH2} V _{IH2}	V _{IH2} V _{IH2} V _{IH2}	V _{IH2} V _{IH2} V _{IH2}	V _{IH2} V _{IH2} V _{IH2}	" " "	V _{IH2} V _{IH2} V _{IH2}	" " "	V _{IH2} V _{IH2} V _{IH2}	V _{IH2} V _{IH2} V _{IH2}	V _{IH2} V _{IH2} V _{IH2}	V _{IH2} V _{IH2} V _{IH2}	V _{IH2} V _{IH2} V _{IH2}	12.5V 12.5V 12.5V	Q6 Q7 Q8	11.25 11.25 11.25	4.5 4.5 4.5	11.25 11.25 11.25	11.25 11.25 11.25	V		
V _{OL1}		36 37 38	V _{IL1} 7/ V _{IL1} 7/ V _{IL1} 7/	I _{OL} 8/		V _{IL1} V _{IL1} V _{IL1}	V _{IL1} V _{IL1} V _{IL1}	V _{IL1} V _{IL1} V _{IL1}	V _{IL1} V _{IL1} V _{IL1}	" " "	V _{IL1} V _{IL1} V _{IL1}	" " "	V _{IL1} V _{IL1} V _{IL1}	I _{OL}	V _{IL1} V _{IL1} V _{IL1}	V _{IL1} V _{IL1} V _{IL1}	V _{IL1} V _{IL1} V _{IL1}	5.0V 5.0V 5.0V	Q6 Q7 Q8		0.5 0.5 0.5	0.5 0.5 0.5	0.5 0.5 0.5	0.5 0.5 0.5	"	
V _{OL2}		39 40 41	V _{IL2} 9/ V _{IL2} 9/ V _{IL2} 9/			V _{IL2} V _{IL2} V _{IL2}	V _{IL2} V _{IL2} V _{IL2}	V _{IL2} V _{IL2} V _{IL2}	V _{IL2} V _{IL2} V _{IL2}	" " "	V _{IL2} V _{IL2} V _{IL2}	" " "	V _{IL2} V _{IL2} V _{IL2}	V _{IL2} V _{IL2} V _{IL2}	V _{IL2} V _{IL2} V _{IL2}	V _{IL2} V _{IL2} V _{IL2}	12.5V 12.5V 12.5V	Q6 Q7 Q8	1.25 1.25 1.25	1.25 1.25 1.25	1.25 1.25 1.25	1.25 1.25 1.25	1.25 1.25 1.25	"		
I _{IH1} 10/	3010	42	15.0V			15.0V	15.0V	15.0V	15.0V	"	15.0V	15.0V	15.0V	V	15.0V	15.0V	15.0V	15.0V	All inputs together		11.0				nA	

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit							
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C									
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min		Max						
I _{IH2}	3010	43	15.0V			GND	GND	GND	GND	GND	GND	GND	GND			GND	GND	15.0V	PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial IN PI5 PI6 PI7	1.0	45					nA							
		44	GND			15.0V	GND	GND	GND																								
		45				GND	15.0V	GND	GND																								
		46					GND	15.0V	GND																								
		47						GND	GND	15.0V																							
		48							GND			15.0V																					
		49										GND	15.0V																				
		50											GND	15.0V																			
		51												GND	15.0V																		
		52													GND		15.0V																
		53														GND	15.0V	15.0V															
I _{IL1} 10/	3010	54	GND			GND	GND	GND	GND	GND	GND	GND			GND	GND	15.0V	All inputs together		-11.0						nA							
I _{IL2}		55																	PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial IN PI5 PI6 PI7	-1.0	-45												
		56																															
		57																															
		58																															
		59																															
		60																															
		61																															
		62																															
		63																															
		64																															
65																																	
																		Subgroup 4 T _C = 25°C															
																		Min	Max														
C _i	3012	66	11/			11/	11/	11/	11/	GND							GND	PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial IN PI5 PI6 PI7	12														
67																																	
68																																	
69																																	
70																																	
71																																	
72																																	
73																																	
74																																	
75																																	
76																																	

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																	Measured terminal	Test limits						Unit
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}	Subgroup 7		Subgroup 8						
																			T _C = 25°C		T _C = 125°C		T _C = -55°C				
																			Min		Max	Min	Max	Min	Max		
Truth table test <u>12/</u>	3014	77	GND	L	L	GND	GND	GND	GND	GND	5.0V	5.0V	GND	L	GND	GND	GND	5.0V	All outputs	See <u>13/</u> , <u>14/</u>							
		78	GND	"	"	GND	GND	GND	GND	"	GND	5.0V	GND	"	GND	GND	GND	"									
		79	5.0V	"	"	5.0V	5.0V	5.0V	GND	"	"	"	<u>15/</u>	5.0V	"	5.0V	5.0V	5.0V				"					
		80	"	"	"	5.0V	5.0V	GND	5.0V	"	"	"	"	"	"	"	"	"				"					
		81	"	"	"	5.0V	GND	5.0V	GND	"	"	"	5.0V	"	"	"	"	"				"					
		82	"	"	"	GND	5.0V	GND	"	"	"	"	"	"	"	"	"	"				"					
		83	"	"	"	5.0V	GND	"	"	"	"	"	"	"	GND	"	"	"				"					
		84	"	"	"	5.0V	"	"	"	"	"	"	GND	"	GND	"	"	"				"					
		85	"	H	"	GND	"	"	"	"	"	"	5.0V	"	5.0V	GND	"	"				"					
		86	"	H	"	"	"	"	"	"	"	"	GND	"	5.0V	GND	"	"				"					
		87	"	L	"	"	"	"	"	"	"	"	5.0V	"	H	GND	5.0V	GND				"					
		88	"	L	"	"	"	"	"	"	"	"	GND	"	H	"	5.0V	GND				"					
		89	GND	H	H	"	"	"	"	"	"	"	5.0V	"	"	"	GND	5.0V				"					
		90	5.0V	"	L	"	"	"	"	"	"	"	<u>15/</u>	"	H	"	"	GND				"					
		91	GND	"	H	"	"	"	"	"	"	"	<u>15/</u>	"	H	"	"	"				"					
		92	"	"	H	"	"	"	"	"	"	"	GND	"	H	"	"	"				"					
		93	"	L	L	"	"	"	"	"	"	5.0V	GND	"	L	"	"	"				"					
		94	"	"	"	"	"	"	"	"	"	GND	GND	GND	"	"	"	"				"					
		95	5.0V	"	"	5.0V	5.0V	5.0V	5.0V	"	"	"	5.0V	"	"	5.0V	5.0V	5.0V				"					
		96	"	"	"	"	"	"	"	"	"	"	<u>15/</u>	"	"	"	"	"				"					
		97	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"					
		98	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"					
		99	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"					
		100	"	"	"	"	"	"	"	"	"	"	GND	"	"	"	"	"				"					
		101	"	H	H	"	"	"	"	"	"	5.0V	GND	"	H	"	"	"				"					
		102	"	"	"	"	"	"	"	"	"	GND	GND	5.0V	"	"	"	"				"					
		103	GND	"	"	GND	GND	GND	"	"	"	GND	5.0V	5.0V	"	GND	GND	GND				"					
		104	GND	"	"	GND	GND	5.0V	"	"	"	GND	<u>15/</u>	5.0V	"	GND	GND	GND				"					

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z Test no.	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit	
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 7 T _C =25°C		Subgroup 8					
																				Min	Max	T _C =125°C		T _C =-55°C			
																						Min	Max	Min	Max		Min
Truth table test 12/	3014	105 106 107 108 109 110 111 112 113	GND " " " 5.0V " " "	H H H L " " " "	H H H L " " " "	GND 5.0V 5.0V GND GND 5.0V 5.0V GND GND	5.0V 5.0V 5.0V GND GND 5.0V GND GND	5.0V 5.0V 5.0V GND GND 5.0V GND GND	5.0V 5.0V 5.0V GND GND 5.0V GND GND	GND " " " " " " "	GND GND GND 15/ 15/ 15/ GND	15/ 15/ 15/ 5.0V " " " "	5.0V " " " " " " "	H H H L " " " "	GND GND 5.0V GND 5.0V 5.0V 5.0V 5.0V GND	GND " " " " 5.0V 5.0V 5.0V 5.0V	GND " " " " 5.0V 5.0V 5.0V 5.0V	5.0V " " " " " " " "	All outputs " " " " " " " " "	See 13/, 14/							
																				Subgroup 9 T _C =25°C		Subgroup 10 T _C =125°C		Subgroup 11 T _C =-55°C			
																				Min	Max	Min	Max	Min	Max		
t _{PHL1}	3003 Fig. 4	114	IN	OUT		GND	GND	GND	GND	GND	IN	GND			GND	IN	IN	5.0V	P/S control to Q6 P/S control to Q7 P/S control to Q8	20	975	30	1465	20	975	ns	
		115	"			"	"	"	"	"	"	"		OUT	"	"	"	"	"	"	"	"	"	"	"	"	
		116	"		OUT	"	"	"	"	"	"	"			"	"	"	"	"	"	"	"	"	"	"	"	
t _{PLH1}		117	"	OUT		"	"	"	"	"	"	"			"	"	"	"	"	P/S control to Q6 P/S control to Q7 P/S control to Q8	"	"	"	"	"	"	"
		118	"			"	"	"	"	"	"	"		OUT	"	"	"	"	"	"	"	"	"	"	"	"	
		119	"		OUT	"	"	"	"	"	"	"			"	"	"	"	"	"	"	"	"	"	"	"	
t _{PHL2}		120									"	GND	IN	IN				"	Clock to Q6 Clock to Q7 Clock to Q8	"	"	"	"	"	"	"	
		121									"	"	"	"	OUT				"	"	"	"	"	"	"	"	
		122	OUT		OUT						"	"	"	"					"	"	"	"	"	"	"	"	
t _{PLH2}		123									"	"	"	"				"	Clock to Q6 Clock to Q7 Clock to Q8	"	"	"	"	"	"	"	
		124									"	"	"	"	OUT				"	"	"	"	"	"	"	"	
		125	OUT		OUT						"	"	"	"					"	"	"	"	"	"	"	"	
t _{THL}	3004 Fig. 4	126								"	"	"	"				"	Q6 Q7 Q8	13	700	18	1050	13	700	"		
		127									"	"	"	OUT				"	"	700	"	1050	"	700	"		
		128	OUT		OUT						"	"	"					"	"	700	"	1050	"	700	"		
t _{TLH}		129								"	"	"	"				"	Q6 Q7 Q8	"	900	"	1350	"	900	"		
		130								"	"	"	"	OUT				"	"	900	"	1350	"	900	"		
		131	OUT		OUT					"	"	"	"					"	"	900	"	1350	"	900	"		
f _{CL} (max) 13/		133								"	"	"	"	OUT				"	Clock Clock Clock						μs		
	132	134	OUT		OUT					"	"	"	"					"		1.0	1.0	1.4	1.4	1.0	1.0	μs	

See footnotes on next page.

TABLE III. Group A inspection for device type 04 – Continued.

- 1/ Terminals not designated may be “HIGH” level logic, “LOW” level logic, or open except as follows:
 $I_{C(POS)}$ tests; the V_{SS} terminal shall be open.
 $I_{C(NEG)}$ tests; the V_{DD} terminal shall be open.
 V_{SS} tests; the output terminals shall be open.
- 2/ Test numbers 23 through 29 shall be run in sequence. See 4.5.3.
- 3/ $V_{IH1} = 3.8 \text{ V}$ at 25°C , 3.6 V at 125°C , 3.95 V at -55°C .
- 4/ $I_{OH} = -80 \mu\text{A}$ at 25°C , $-55 \mu\text{A}$ at 125°C , $-100 \mu\text{A}$ at -55°C .
- 5/ Apply clock pulse; $V_{IN} = 0 \text{ V}$ to V_{DD} until proper output state is achieved.
- 6/ $V_{IH2} = 9.5 \text{ V}$ at 25°C , 9.25 V at 125°C , 9.75 V at -55°C .
- 7/ $V_{IL1} = 1.1 \text{ V}$ at 25°C , 0.85 V at 125°C , 1.35 V at -55°C .
- 8/ $I_{OL} = 120 \mu\text{A}$ at 25°C , $85 \mu\text{A}$ at 125°C , $150 \mu\text{A}$ at -55°C .
- 9/ $V_{IL2} = 2.8 \text{ V}$ at 25°C , 2.55 V at 125°C , 3.05 V at -55°C .
- 10/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together.
- 11/ See 4.4.1c.
- 12/ Test numbers 77 through 113 shall be run in sequence.
- 13/ The output voltage limits for each temperature are “H” = $V_{DD} - 0.5 \text{ V min.}$ and “L” = $V_{SS} + 0.5 \text{ V max.}$
- 14/ The functional tests shall be performed at V_{IH} and $V_{DD} \leq 5.0 \text{ V}$ and $\geq 15 \text{ V}$.
- 15/ Apply clock pulse; $V_{IN} = 0 \text{ V dc}$ to V_{DD} .
- 16/ The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.

TABLE III. Group A inspection for device type 05 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			Recirc in	Clock	NC	NC	NC	Q	$\overline{Q}$	V _{SS}	Delayed clock	Mode cont.	NC	NC	NC	NC	Data in	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C		
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min	
I _{SS} 2/	3005	46	GND	3/						GND							GND	15.0V	None							μA
		47	"	"						"							15.0V	"	"							"
		48	"	"						"							GND	"	"	-2.0			-20			"
		49	"	"						"							15.0V	"	"							"
		50	"	"						"							GND	"	"							"
		51	"	"						"							15.0V	"	"							"
		52	"	"						"							GND	"	"							"
		53	"	"						"							15.0V	"	"							"
		54	"	"						"							GND	"	"							"
		55	"	"						"							15.0V	"	"							"
		56	"	"						"							GND	"	"							"
		57	"	"						"							15.0V	"	"							"
		58	"	"						"							GND	"	"							"
		59	"	"						"							15.0V	"	"							"
		60	GND	3/						GND							GND	15.0V	None							μA
		61	"	"						"							15.0V	"	"							"
		62	"	"						"							GND	"	"	-2.0			-20			"
		63	"	"						"							15.0V	"	"							"
		64	"	"						"							GND	"	"							"
		65	"	"						"							15.0V	"	"							"
		66	"	"						"							GND	"	"							"
		67	"	"						"							15.0V	"	"							"
		68	"	"						"							GND	"	"							"
		69	"	"						"							15.0V	"	"							"
		70	"	"						"							GND	"	"							"
		71	"	15.0V						"							15.0V	"	V _{SS}							"
		72	"	GND						"							GND	"	V _{SS}							"
		73	"	15.0V						"							15.0V	"	None							"
		74	15.0V	"						"							GND	"	V _{SS}							"
		75	15.0V	"						"							GND	"	V _{SS}							"
		76	GND	"						"			15.0V				15.0V	"	V _{SS}							"
V _{OH1}	3006	77	V _{IL1 4/}	5/				I _{OH1 8/}		"		V _{IL1}					V _{IH1 9/}	5.0V	Q	4.5					"	
		78	V _{IL1 4/}	5/				I _{OH2 7/}		"		V _{IL1}					V _{IL1}	5.0V	$\overline{Q}$	4.5			4.5		4.5	"
		79	V _{IL1 4/}	V _{IH1}						"	I _{OH3 8/}	V _{IL1}					V _{IH1}	5.0V	Delayed clock	4.5	4.5	4.5	4.5	4.5	4.5	V
V _{OH2}		80	V _{IL2 10/}	5/						"		V _{IL2}					V _{IH2 11/}	12.5V	Q	11.25					"	
		81	V _{IL2 10/}	5/						"		V _{IL2}					V _{IL2}	12.5V	$\overline{Q}$	11.25			11.25		11.25	"
		82	V _{IL2 10/}	V _{IH2}						"		V _{IL2}					V _{IH2}	12.5V	Delayed clock	11.25	11.25	11.25	11.25	11.25	11.25	"
V _{OL1}	3007	83	V _{IL1}	5/				I _{OL1 12/}		"		V _{IL1}					V _{IL1}	5.0V	Q						"	
		84	V _{IL1}	5/				I _{OL2 13/}		"		V _{IL1}					V _{IH1}	5.0V	$\overline{Q}$						"	
		85	V _{IL1}	V _{IL1}						"	I _{OL3 14/}	V _{IL1}					V _{IL1}	5.0V	Delayed clock	0.5	0.5	0.5	0.5	0.5	0.5	"
V _{OL2}		86	V _{IL2}	5/						"		V _{IL2}					V _{IL2}	12.5V	Q						"	
		87	V _{IL2}	5/						"		V _{IL2}					V _{IH2}	12.5V	$\overline{Q}$						"	
		88	V _{IL2}	V _{IL2}						"		V _{IL2}					V _{IL2}	12.5V	Delayed clock	1.25	1.25	1.25	1.25	1.25	1.25	"

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z Test no.	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			Recirc. in	Clock	NC	NC	NC	Q	$\overline{Q}$	V _{SS}	Delayed clock	Mode cont.	NC	NC	NC	NC	Data in	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C		
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Min	Max	Min	Max	Min	Max	
I _{IH1} 15/	3010	89	15.0V	15.0V						GND		15.0V					15.0V	15.0V	All inputs together							nA
I _{IH2}		90	15.0V	GND						"		GND					GND	"	Recirc. in	4.0	"		"			"
		91	GND	15.0V						"		15.0V					GND	"	Clock	"	"		"			"
		92	"	GND						"		GND					15.0V	"	Mode control	1.0	"	45	"			"
I _{IL1} 15/	3009	94	"	"						"		"				GND	"	All inputs together							"	
I _{IL2}		95	"	"						"		"					"	"	Recirc. in	-4.0	"		"			"
		96	"	"						"		"					"	"	Clock	"	"		"			"
		97	"	"						"		"					"	"	Mode control	-1.0	"	-45	"			"
		98	"	"						"		"					"	"	Data in							"
																				Subgroup 4 T _C = 25°C						
																				Min	Max					
C _i	3012	99	16/	16/						GND							GND	Recirc in							pF	
		100								"		16/					"	Clock	70						"	
		101								"							"	Mode control	12	12					"	
		102								"						16/	"	Data in	12	12					"	
																			Subgroup 7 T _C = 25°C		Subgroup 8					
																			T _C = 25°C		T _C = 125°C		T _C = -55°C			
																			Min	Max	Min	Max	Min	Max		
Truth table test 17/	3014	103	GND	5.0V						GND		GND					5.0V	5.0V	None	} See 18/, 19/, 20/						
		104	GND	GND						"		"					5.0V	"	"							
		105	GND	5.0V						"		"					5.0V	"	"							
		106	5.0V	GND						"		"					GND	"	"							
		107	5.0V	5.0V						"		"					GND	"	"							
		108	GND	GND						"		"					5.0V	"	"							
		109	"	5.0V						"		"					"	"	"							
		110	"	GND						"		5.0V					"	"	"							
		111	"	5.0V						"		"					"	"	"							
		112	5.0V	GND						"		"					GND	"	"							
		113	"	5.0V						"		"					GND	"	"							
		114	"	21/						"		GND					5.0V	"	"							
		115	"	5.0V					H	L	"	"	"				"	"	All outputs							
		116	"	GND					H	L	"	L	"				"	"	"							
		117	"	5.0V					L	H	"	H	"				"	"	"							
		118	"	GND					L	H	"	L	"				"	"	"							
		119	"	5.0V					H	L	"	L	"				"	"	"							
		120	"	GND					H	L	"	L	"				"	"	"							
		121	"	5.0V					L	H	"	H	"				"	"	"							
		122	"	GND					L	H	"	L	"				"	"	"							
		123	"	5.0V					H	L	"	H	"				"	"	"							

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			Recirc. in	Clock	NC	NC	NC	Q	$\overline{Q}$	V _{SS}	Delayed clock	Mode cont.	NC	NC	NC	NC	Data in	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C		
																				Min	Max	Min	Max	Min	Max	
t _{PHL1}	3003 Fig. 4	124	GND	IN				OUT		GND		GND					IN	5.0V	Clock to Q	13	1060	18	1590	13	1060	ns
t _{PHL2}		125	GND	"					OUT	"		GND					IN	"	Clock to Q	"	1320	"	1980	"	1320	"
t _{PHL3}		126	GND	"						"	OUT	GND						"	Clock to delayed clock	"	650	"	975	"	650	"
t _{PHL4}		127	IN	"					OUT		"		5.0V					"	Clock to Q	"	1060	"	1590	"	1060	"
t _{PLH1}		128	GND	"					OUT		"		GND				IN	"	Clock to Q	"	1060	"	1590	"	1060	"
t _{PLH2}		129	GND	"						OUT	"		GND				IN	"	Clock to Q	"	1320	"	1980	"	1320	"
t _{PLH3}		130	GND	"						"	OUT	GND						"	Clock to delayed clock	"	650	"	975	"	650	"
t _{PLH4}		131	IN	"					OUT		"		5.0V					"	Clock to Q	"	1060	"	1590	"	1060	"
t _{THL1}	3004 Fig. 4	132	GND	"				OUT		"		GND					IN	"	Q	10	290	14	435	10	290	"
t _{THL2}		133	GND	"					OUT	"		GND					IN	"	$\overline{Q}$	"	1400	"	2100	"	1400	"
t _{THL3}		134	GND	"						"	OUT	GND						"	Delayed clock	"	350	"	525	"	350	"
t _{TLH1}	3004 Fig. 4	135	GND	IN				OUT		"		GND					IN	5.0V	Q	10	340	14	510	10	340	ns
t _{TLH2}		136	GND	"					OUT	"		"					IN	"	$\overline{Q}$	"	1400	"	2100	"	1400	"
t _{TLH3}		137	GND	"						"	OUT	"						"	Delayed clock	"	350	"	525	"	350	"
f _{CL} (max) 22/	138	139		"				OUT		"	OUT	"					IN	"	Clock		"		"		"	μs
		140		"						"		"					IN	"	"	1.25	"		"		"	"
		141	IN	"						"		5.0V						"	"		1.8	"			"	"
		142	IN	"						"		5.0V						"	"						"	"

See footnotes on next page.

TABLE III. Group A inspection for device type 05 – Continued.

- 1/ Terminals not designated may be “HIGH” level logic, “LOW” level logic, or open except as follows:
 $I_{C(POS)}$ tests; the V_{SS} terminal shall be open.
 $I_{C(NEG)}$ tests; the V_{DD} terminal shall be open.
 V_{SS} tests; the output terminals shall be open.
- 2/ Test numbers 9 through 76 shall be run in sequence. See 4.5.3.
- 3/ Apply single clock pulse; $V_{IN} = 0$ V dc to V_{DD} .
- 4/ $V_{IL1} = 1.1$ V at 25°C, 0.85 V at 125°C, 1.35 V at -55°C.
- 5/ Apply clock pulse; $V_{IN} = 0$ V to V_{DD} until proper output state is achieved.
- 6/ $I_{OH1} = -320$ μ A at 25°C, -225 μ A at 125°C, -400 μ A at -55°C.
- 7/ $I_{OH2} = -90$ μ A at 25°C, -60 μ A at 125°C, -110 μ A at -55°C.
- 8/ $I_{OH3} = -400$ μ A at 25°C, -280 μ A at 125°C, -480 μ A at -55°C.
- 9/ $V_{IH1} = 3.8$ V at 25°C, 3.6 V at 125°C, 3.95 V at -55°C.
- 10/ $V_{IL2} = 2.8$ V at 25°C, 2.55 V at 125°C, 3.05 V at -55°C.
- 11/ $V_{IH2} = 9.5$ V at 25°C, 9.25 V at 125°C, 9.75 V at -55°C.
- 12/ $I_{OL1} = 1.3$ mA at 25°C, 0.5 mA at 125°C, 1.5 mA at -55°C.
- 13/ $I_{OL2} = 90$ μ A at 25°C, 60 μ A at 125°C, 110 μ A at -55°C.
- 14/ $I_{OL3} = 400$ μ A at 25°C, 280 μ A at 125°C, 480 μ A at -55°C.
- 15/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together.
- 16/ See 4.4.1c.
- 17/ Test numbers 103 through 123 shall be run in sequence.
- 18/ The output voltage limits for each temperature are “H” = $V_{DD} - 0.5$ V min. and “L” = $V_{SS} + 0.5$ V max.
- 19/ For all test conditions, delayed clock (CL_D) is clock delayed by two inverters.
- 20/ The functional tests shall be performed at V_{IH} and $V_{DD} \leq 5.0$ V and ≥ 15 V.
- 21/ Apply 59 clock pulses; $V_{IN} = 0$ V dc to V_{DD} .
- 22/ The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.

See footnotes at end of device type 06.

Symbol	MIL-STD-883 method	Cases J.K.U	Terminal conditions and limits 1/																								Measured terminal	Test limits						Unit	
			Symbol	B8	B7	B6	B5	B4	B3	B2	B1	AE	Serial In	A/B	V _{SS}	P/S	A/S	Clock	A1	A2	A3	A4	A5	A6	A7	A8		V _{DD}	Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C		
				Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22		23	24	Min	Max	Min	Max		Min
V _{IC} (POS)	2/		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	AE Ser in A/B P/S A/S Clock	1.5					V		
V _{IC} (NEG)			7	8	9	10	11	12			-1mA	-1mA	-1mA	GND													AE Ser in A/B P/S A/S Clock	-6							
I _{SS} 3/	3005		13	14	15	16	17	18	19	20	21	22	23	24	15.0V	15.0V	15.0V	GND	15.0V	GND	15.0V	GND	15.0V	GND	15.0V	GND	V _{SS} V _{SS} None V _{SS} V _{SS} None V _{SS} V _{SS} None V _{SS} V _{SS}	-1.0		-5.0			μA		
V _{OH1}	3006		24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	5.0V	5.0V	5.0V	5.0V	5.0V	5.0V	5.0V	B1 B2 B3 B4 B5 B6 B7 B8 A1 A2 A3 A4 A5 A6 A7 A8 A1	4.5	4.5	4.5		V			
V _{OH2}			41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	12.5V	12.5V	12.5V			12.5V	B1 B2 B3 B4 B5 B6 B7 B8 A1 A2 A3 A4 A5 A6 A7 A8 A1	11.25		11.25		11.25				

TABLE III. Group A inspection for device type 06 – Continued.

Symbol	MIL-STD-883 method	Cases J,K,U Symbol	Terminal conditions and limits 1/																								Measured terminal	Test limits						Unit
			B8	B7	B6	B5	B4	B3	B2	B1	AE	Serial In	A/B	V _{SS}	P/S	A/S	Clock	A1	A2	A3	A4	A5	A6	A7	A8	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C		
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23		24	Min	Max	Min	Max	Min	
V _{OL1}	3007	58								8/	8/	5.0V		5.0V	GND	5.0V	GND	5/	9/	9/	9/	9/				5.0V	B1						V	
		59																								B2								
		60																									B3	0.5		0.5				
		61																									B4							
		62																									B5							
		63																									B6							
		64	8/	8/	8/																						B7							
		65																									B8							
		66																									A1							
		67																									A2							
		68																									A3							
		69																									A4							
		70																									A5							
		71																									A6							
		72																									A7							
		73	9/	9/	9/																							A8						
		74											9/															A1						
V _{OL2}		75										12.5V		12.5V		12.5V			10/	10/	10/	10/				12.5V	B1							
		76																									B2							
		77																									B3	1.25		1.25				
		78																									B4							
		79																									B5							
		80																									B6							
		81																									B7							
		82																									B8							
		83																									A1							
		84																									A2							
		85																									A3							
		86																									A4							
		87																									A5							
		88																									A6							
		89																									A7							
		90	10/	10/	10/																							A8						
		91																									A1							
I _{BH1} 11/	3010	92									15.0V	15.0V	15.0V		15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	All HIGH level inputs together		14					nA	
		92A	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	GND	15.0V	GND		15.0V	15.0V	15.0V											12						
I _{BH2}		93	15.0V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	B8							
		94		15.0V																							B7							
		95	GND		15.0V																						B6	1.0		45				
		96				15.0V																					B5							
		97					15.0V																				B4							
		98						15.0V																			B3							
		99							15.0V																		B2							
		100								15.0V																	B1							
		101									15.0V																AE							
		102										15.0V															Ser. IN							
		103											15.0V														A/B							
		104												15.0V													P/S							
		105													15.0V												A/S							
		106														15.0V											Clock							
		107															15.0V										A1							
		108																15.0V									A2							
		109																	15.0V								A3							
110																		15.0V							A4									
111																			15.0V							A5								
112																				15.0V						A6								
113																					15.0V					A7								
114																						GND				A8								

See footnotes at end of device type 06.

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See 14/, 15/

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TABLE III. Group A inspection for device type 06 – Continued.

Symbol	MIL-STD-883 method	Cases J,K,U	Terminal conditions and limits 1/																								Measured terminal	Test limits						Unit					
			Symbol	B8	B7	B6	B5	B4	B3	B2	B1	AE	Serial In	A/B	V _{SS}	P/S	A/S	Clock	A1	A2	A3	A4	A5	A6	A7	A8		V _{DD}	Subgroup 7		Subgroup 8								
				Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22		23	24	T _C = 25°C		T _C = 125°C			T _C = -55°C				
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max						
Truth table test 13/	3014	164	GND	5.0V	GND	5.0V	GND	5.0V	GND	5.0V	5.0V	5.0V	GND	GND	GND	5.0V	GND	L	H	L	H	L	H	L	H	5.0V	All outputs	See 14/, 15/											
		165	GND	5.0V	GND	5.0V	GND	5.0V	GND	5.0V	"	"	"	"	"	"	"	H	L	L	H	L	H	L	L	"													
		166	GND	5.0V	GND	5.0V	GND	5.0V	GND	5.0V	"	"	"	"	"	"	"	H	L	L	H	L	H	L	L	"													
		167	5.0V	GND	5.0V	GND	5.0V	GND	5.0V	GND	"	"	"	"	"	"	"	H	L	L	H	L	H	L	L	"													
		168	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	L	H	L	H	L	H	L	L	"													
		169	"	"	"	"	"	"	"	"	"	"	"	"	GND	"	5.0V	L	H	L	H	L	H	L	L	"													
170	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	5.0V	H	L	L	L	H	L	L	L	"															
																								Subgroup 9		Subgroup 10		Subgroup 11											
																								T _C = 25°C		T _C = 125°C		T _C = -55°C											
t _{PHL1}	3003 Fig. 4	171							OUT	5.0V		"	GND	5.0V	GND	IN	IN								5.0V	Clock to B1	13	1100	18	1300	13	1000	ns						
		172								"	5.0V	"	"	"	"	"		IN		IN					"	Clock to B2	"	"	"	"	"	"	"						
		173								"	"	"	"	"	"	"	"								"	Clock to B3	"	"	"	"	"	"	"						
		174								"	"	"	"	"	"	"	"								"	Clock to B4	"	"	"	"	"	"	"						
		175								"	"	"	"	"	"	"	"								"	Clock to B5	"	"	"	"	"	"	"						
		176								"	"	"	"	"	"	"	"	"								"	Clock to B6	"	"	"	"	"	"	"					
		177								"	"	"	"	"	"	"	"	"								"	Clock to B7	"	"	"	"	"	"	"					
		178	OUT	OUT						OUT	"	"	"	"	"	"	"								IN	Clock to B8	"	"	"	"	"	"	"						
t _{PLH1}		179							OUT		"	"	"	"	"	"	IN		IN						"	Clock to B1	"	1300	"	1500	"	1200	"						
		180								"	"	"	"	"	"	"	"	IN		IN					"	Clock to B2	"	"	"	"	"	"	"						
		181								"	"	"	"	"	"	"	"	"							"	Clock to B3	"	"	"	"	"	"	"						
		182								"	"	"	"	"	"	"	"	"							"	Clock to B4	"	"	"	"	"	"	"						
		183								"	"	"	"	"	"	"	"	"							"	Clock to B5	"	"	"	"	"	"	"						
		184								"	"	"	"	"	"	"	"	"							"	Clock to B6	"	"	"	"	"	"	"						
		185								"	"	"	"	"	"	"	"	"							IN	Clock to B7	"	"	"	"	"	"	"						
		186	OUT	OUT						OUT	"	"	"	"	"	"	"	"							IN	Clock to B8	"	"	"	"	"	"	"						
t _{PHL2}		187							IN	"		"	"	"	"	"	OUT		OUT						"	Clock to A1	"	1100	"	1300	"	1000	"						
		188								"	GND	"	"	"	"	"	"	"							"	Clock to A2	"	"	"	"	"	"	"						
		189								"	"	"	"	"	"	"	"	"							"	Clock to A3	"	"	"	"	"	"	"						
		190								"	"	"	"	"	"	"	"	"							"	Clock to A4	"	"	"	"	"	"	"						
		191								"	"	"	"	"	"	"	"	"							"	Clock to A5	"	"	"	"	"	"	"						
		192								"	"	"	"	"	"	"	"	"							"	Clock to A6	"	"	"	"	"	"	"						
		193								"	"	"	"	"	"	"	"	"							"	Clock to A7	"	"	"	"	"	"	"						
		194	IN	IN						IN	"	"	"	"	"	"	"	"							OUT	Clock to A8	"	"	"	"	"	"	"						

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 – Continued.

Symbol	MIL-STD-883 method	Cases J,K,U Symbol	Terminal conditions and limits 1/																								Measured terminal	Test limits						Unit	
			B8	B7	B6	B5	B4	B3	B2	B1	AE	Serial In	A/B	V _{SS}	P/S	A/S	Clock	A1	A2	A3	A4	A5	A6	A7	A8	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C			
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23		24	Min	Max	Min	Max	Min		Max
t _{PLH2}	3003 Fig. 4	195								IN	5.0V			GND	5.0V	GND	IN	OUT									5.0V	Clock to A1	13	1300	18	1500	13	1200	ns
		196																	OUT									Clock to A2							
		197																											Clock to A3						
		198																											Clock to A4						
		199					IN														OUT								Clock to A5						
		200				IN																OUT							Clock to A6						
		201		IN																			OUT						Clock to A7						
		202	IN																					OUT				Clock to A8							
t _{PHL3}		203								OUT		IN	5.0V		GND													Clock to B1		1100		1300		1000	
		204																										Clock to B2							
		205								OUT																		Clock to B3							
		206																										Clock to B4							
		207					OUT																					Clock to B5							
		208				OUT																						Clock to B6							
		209																										Clock to B7							
		210	OUT																									Clock to B8							
t _{PLH3}		211								OUT																		Clock to B1		1300		1500		1200	
		212																										Clock to B2							
		213																										Clock to B3							
		214																										Clock to B4							
		215					OUT																					Clock to B5							
		216				OUT																						Clock to B6							
		217																										Clock to B7							
		218	OUT																									Clock to B8							
t _{PHL4}		219											GND					OUT	OUT									Clock to A1		1100		1300		1000	
		220																										Clock to A2							
		221																										Clock to A3							
		222																										Clock to A4							
		223																				OUT						Clock to A5							
		224																					OUT					Clock to A6							
		225																						OUT				Clock to A7							
		226																							OUT			Clock to A8							

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 – Continued.

Symbol	MIL-STD-883 method	Cases J,K,U Symbol	Terminal conditions and limits 1/																								Measured terminal	Test limits						Unit										
			B8	B7	B6	B5	B4	B3	B2	B1	AE	Serial In	A/B	V _{SS}	P/S	A/S	Clock	A1	A2	A3	A4	A5	A6	A7	A8	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C												
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23		24	Min	Max	Min	Max	Min		Max									
t _{PLH4}	3003 Fig. 4	227								5.0V	IN	GND	GND	GND	GND	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0V	Clock to A1 Clock to A2 Clock to A3 Clock to A4 Clock to A5 Clock to A6 Clock to A7 Clock to A8	13	1300	18	1500	13	1200	ns									
		228																																										
		229																																										
		230																																										
		231																																										
		232																																										
		233																																										
		234																																										
t _{THL1}	3004 Fig. 4	235							OUT				5.0V			IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	B1 B2 B3 B4 B5 B6 B7 B8	10	1100	14	1300	10	1000											
		236																																										
		237																																										
		238																																										
		239																																										
		240																																										
		241																																										
		242	OUT	OUT	OUT	OUT	OUT	OUT	OUT																									IN	IN	IN								
t _{TLH1}		243							OUT							IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	B1 B2 B3 B4 B5 B6 B7 B8		2000		2300		1800											
		244																																										
		245																																										
		246																																										
		247																																										
		248																																										
		249																																										
		250	OUT	OUT	OUT	OUT	OUT	OUT	OUT																										IN	IN	IN							
t _{THL2}		251							IN							OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	A1 A2 A3 A4 A5 A6 A7 A8		1100		1300		1000											
		252																																										
		253																																										
		254																																										
		255																																										
		256																																										
		257																																										
		258	IN	IN	IN	IN	IN	IN	IN																											OUT	OUT							
t _{TLH2}		259							IN							OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	A1 A2 A3 A4 A5 A6 A7 A8		2000		2300		1800											
		260																																										
		261																																										
		262																																										
		263																																										
		264																																										
		265																																										
		266	IN	IN	IN	IN	IN	IN	IN																											OUT	OUT							

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 – Continued.

Symbol	MIL-STD-883 method	Cases J,K,U Symbol	Terminal conditions and limits 1/																								Measured terminal	Test limits						Unit																																																																																										
			B8	B7	B6	B5	B4	B3	B2	B1	AE	Serial In	A/B	V _{SS}	P/S	A/S	Clock	A1	A2	A3	A4	A5	A6	A7	A8	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C																																																																																												
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23		24	Min	Max	Min	Max	Min		Max																																																																																									
f _{CL} (max) 16/		267	268 269 270 271 272 273 274 275 276 277 278 279 280 281 282	OUT	OUT	OUT	OUT	OUT	OUT	OUT	5.0V " " " " " " " " " " " " " " " "	IN " " " " " " " " " " " " " " "	GND " " " " " " " " " " " " " " "	GND " " " " " " " " " " " " " " "	GND " " " " " " " " " " " " " " "	GND " " " " " " " " " " " " " " "	IN " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " " " " " " " " " " " " "	OUT " " "

1/ Terminals not designated may be “HIGH” level logic, “LOW” level logic, or open except as follows:

IC(POS) tests; the V_{SS} terminal shall be open.

IC(NEG) tests; the V_{DD} terminal shall be open.

V_{SS} tests; the output terminals shall be open.

I_{HH} tests; the undesignated terminals shall be open.

2/ In device type 06, circuit C, all terminals except 12 and 24 are inputs connected to gate structures; therefore, the table III, V_{IC(POS)} and V_{IC(NEG)} tests shall be expanded to include testing terminals 1 through 8, and 16 through 23.

3/ Test numbers 13 through 23 shall be run in sequence. See 4.5.3.

4/ I_{OH} = -50 μA at 25°C, -35 μA at 125°C, -75 μA at -55°C.

5/ Apply clock pulse; V_{IN} = 0 V to V_{DD} until proper output state is achieved.

6/ V_{IH1} = 3.8 V at 25°C, 3.6 V at 125°C, 3.95 V at -55°C.

7/ V_{IH2} = 9.5 V at 25°C, 9.25 V at 125°C, 9.75 V at -55°C.

8/ I_{OL} = 100 μA at 25°C, 70 μA at 125°C, 124 μA at -55°C.

9/ V_{IL1} = 1.1 V at 25°C, 0.85 V at 125°C, 1.35 V at -55°C.

10/ V_{IL2} = 2.8 V at 25°C, 2.55 V at 125°C, 3.05 V at -55°C.

11/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together.

12/ See 4.4.1c.

13/ Test numbers 144 through 170 shall be run in sequence.

14/ The output voltage limits for each temperature are “H” = V_{DD} -0.5 V min. and “L” = V_{SS} +0.5 V max.

15/ The functional tests shall be performed at V_{IH} and V_{DD} ≤ 5.0 V and ≥ 15 V.

16/ The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.

TABLE III. Group A inspection for device type 51.

Symbol	MIL-STD-883 method	Cases A C,D,T,X,Y	Terminal conditions and limits 1/														Measured terminal	Test limits						Unit
		Symbol	D1	NC	Clock	D2	D3	D4	V _{SS}	D4+4	D4+5	D3+4	D2+4	D2+5	D1+4	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C		
		Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	Min	Max	Min	Max	
V _{IC} (POS)		2 3 4 5	1mA		1mA	1mA	1mA	1mA								GND	D1 Clock D2 D3 D4	1.5						V
V _{IC} (NEG)	1	7 8 9 10	-1mA		-1mA	-1mA	-1mA	-1mA	GND								D1 Clock D2 D3 D4	-6.0						
I _{SS} 2/	3005	11 12 13 14 15 16 17 18 19	GND 18.0V GND 18.0V GND 18.0V 18.0V 18.0V GND	3	⌋ ⌋ ⌋ ⌋ ⌋ ⌋ ⌋ ⌋ ⌋	GND 18.0V GND 18.0V GND 18.0V 18.0V 18.0V GND	GND 18.0V GND 18.0V GND 18.0V 18.0V 18.0V GND	GND 18.0V GND 18.0V GND 18.0V 18.0V 18.0V GND								18.0V	None ⌋ ⌋ ⌋ ⌋ V _{SS} V _{SS} None V _{SS}	-0.3		-3.0				μA
V _{OH3}	3006	20 21 22 23 24 25	15.0V ⌋ ⌋ ⌋ ⌋ ⌋	4	⌋ ⌋ ⌋ ⌋ ⌋ ⌋	15.0V ⌋ ⌋ ⌋ ⌋ ⌋	15.0V ⌋ ⌋ ⌋ ⌋ ⌋	15.0V ⌋ ⌋ ⌋ ⌋ ⌋								15.0V ⌋ ⌋ ⌋ ⌋ ⌋ ⌋ ⌋ ⌋	D4+4 D4+5 D3+4 D2+4 D2+5 D1+4	14.95 ⌋ ⌋ ⌋ ⌋ ⌋ ⌋		14.95 ⌋ ⌋ ⌋ ⌋ ⌋ ⌋	14.95 ⌋ ⌋ ⌋ ⌋ ⌋ ⌋		V	
V _{OL3}	3007	26 27 28 29 30 31	GND ⌋ ⌋ ⌋ ⌋ ⌋		⌋ ⌋ ⌋ ⌋ ⌋ ⌋	GND ⌋ ⌋ ⌋ ⌋ ⌋	GND ⌋ ⌋ ⌋ ⌋ ⌋	GND ⌋ ⌋ ⌋ ⌋ ⌋									D4+4 D4+5 D3+4 D2+4 D2+5 D1+4	0.05 ⌋ ⌋ ⌋ ⌋ ⌋ ⌋		0.05 ⌋ ⌋ ⌋ ⌋ ⌋ ⌋	0.05 ⌋ ⌋ ⌋ ⌋ ⌋ ⌋			
V _{IH1} 11/		32	5/		5/	5/	5/	5/	⌋	5/	5/	5/	5/	5/	5/	5/	All outputs	5/	5/	5/	5/	5/	5/	5/
V _{IH2} 11/		33	⌋		⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	
V _{IH3} 11/		34	⌋		⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	
V _{IL1} 11/		35	⌋		⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	
V _{IL2} 11/		36	⌋		⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	
V _{IL3} 11/		37	⌋		⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	⌋	
I _{OL1}	38	39 40 41 42 43	GND ⌋ ⌋ ⌋ ⌋	4	⌋ ⌋ ⌋ ⌋ ⌋	GND ⌋ ⌋ ⌋ ⌋	GND ⌋ ⌋ ⌋ ⌋	GND ⌋ ⌋ ⌋ ⌋	⌋ ⌋ ⌋ ⌋ ⌋	0.4V ⌋ ⌋ ⌋ ⌋	0.4V ⌋ ⌋ ⌋ ⌋	0.4V ⌋ ⌋ ⌋ ⌋	0.4V ⌋ ⌋ ⌋ ⌋	0.4V ⌋ ⌋ ⌋ ⌋	0.4V ⌋ ⌋ ⌋ ⌋	5.0V ⌋ ⌋ ⌋ ⌋	D4+4 D4+5 D3+4 D2+4 D2+5 D1+4	0.51 ⌋ ⌋ ⌋ ⌋ ⌋ ⌋		0.36 ⌋ ⌋ ⌋ ⌋ ⌋ ⌋	0.64 ⌋ ⌋ ⌋ ⌋ ⌋ ⌋		mA	
I _{OL2}	44	45 46 47 48 49	⌋ ⌋ ⌋ ⌋ ⌋	⌋	⌋ ⌋ ⌋ ⌋ ⌋	⌋ ⌋ ⌋ ⌋ ⌋	⌋ ⌋ ⌋ ⌋ ⌋	⌋ ⌋ ⌋ ⌋ ⌋	⌋ ⌋ ⌋ ⌋ ⌋	1.5V ⌋ ⌋ ⌋ ⌋	1.5V ⌋ ⌋ ⌋ ⌋	1.5V ⌋ ⌋ ⌋ ⌋	1.5V ⌋ ⌋ ⌋ ⌋	1.5V ⌋ ⌋ ⌋ ⌋	1.5V ⌋ ⌋ ⌋ ⌋	15.0V ⌋ ⌋ ⌋ ⌋	D4+4 D4+5 D3+4 D2+4 D2+5 D1+4	3.4 ⌋ ⌋ ⌋ ⌋ ⌋ ⌋		2.4 ⌋ ⌋ ⌋ ⌋ ⌋ ⌋	4.2 ⌋ ⌋ ⌋ ⌋ ⌋ ⌋			

See footnotes at end of device type 51.

TABLE III. Group A inspection for device type 51 - Continued.

Symbol	MIL-STD-883 method	Cases A C,D,T,X,Y	Terminal conditions and limits 1/														Measured terminal	Test limits						Unit				
		Symbol	D1	NC	Clock	D2	D3	D4	V _{SS}	D4+4	D4+5	D3+4	D2+4	D2+5	D1+4	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C						
		Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	Min	Max	Min	Max					
I _{OH1}		50	5.0V	4		5.0V	5.0V	5.0V	GND	4.6V	4.6V	4.6V	4.6V	4.6V	4.6V	5.0V	D4+4	-0.51	-0.35	-0.64	mA							
		51													D4+5													
		52													D3+4													
		53													D2+4													
		54													D2+5													
I _{OH2}		55												4.6V		D1+4												
		56	15.0V			15.0V	15.0V	15.0V		13.5V	13.5V	13.5V	13.5V	13.5V	15.0V	D4+4	-3.4	-2.4	-4.2									
		57													D4+5													
		58													D3+4													
		59													D2+4													
60													D2+5															
I _{IH1} 6/	3010	61													13.5V	D1+4												
		62	18.0V		18.0V	18.0V	18.0V	18.0V							18.0V	All inputs together		5.0			nA							
		63	18.0V	GND		GND	GND	GND									D1	1.0	45									
		64	GND			GND	GND							Clock														
		65				GND	GND							D2														
66			GND		GND							D3																
I _{IL1} 6/	3009	67	GND		GND	GND	GND	GND								All inputs together		-5.0										
		68																										
		69	GND	18.0V		18.0V	18.0V	18.0V									D1	-1.0	-45									
		70	18.0V			18.0V	18.0V							Clock														
		71				GND	18.0V	GND						D2														
72			18.0V		GND	18.0V	GND					D3																
I _{IL2}		73			18.0V	18.0V	18.0V	GND								D4												
																	Subgroup 4 T _C = 25°C											
																	Min	Max										
		C _i	3012	74						GND							GND	D1 Clock D2 D3 D4	12.0					pF				
				75																								
76																												
77																												
78																												
																	Subgroup 7 T _C = 25°C		Subgroup 8 T _C = 125°C T _C = -55°C									
																	Min	Max	Min	Max	Min	Max						
Truth table test 8/	3014	79	GND	3		GND	GND	GND	GND	L		L	L		L	5.0V	None None None All outputs	}										
		80	5.0V																									
		81	GND																									
		82																										
		83																										
		84																										
		85																										
		86	5.0V		5.0V	5.0V	5.0V																					
		87																										
		88																										
		89																										
		90																										
		91																										
		92																										
		93																										
94																												

See footnotes at end of device type 51.

TABLE III. Group A inspection for device type 51 – Continued.

Symbol	MIL-STD-883 method	Cases A C,D,T,X,Y	Terminal conditions and limits 1/														Measured terminal	Test limits						Unit
		Symbol	D1	NC	Clock	D2	D3	D4	V _{SS}	D4+4	D4+5	D3+4	D2+4	D2+5	D1+4	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C		
		Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	Min	Max	Min	Max	
t _{PHL}	3003 Fig. 4	95			IN			IN	GND	OUT						5.0V	Clock to D4+4	20	421	30	560	20	421	ns
		96			"			IN	IN	"		OUT				"	Clock to D4+5	"	"	"	"	"	"	"
		97			"				"	"						"	Clock to D3+4	"	"	"	"	"	"	"
		98			"		IN		"	"		OUT				"	Clock to D2+4	"	"	"	"	"	"	"
		99			"		IN		"	"				OUT		"	Clock to D2+5	"	"	"	"	"	"	"
		100	IN		"				"	"					OUT	"	Clock to D1+4	"	"	"	"	"	"	"
t _{PLH}		101			"			IN	"	OUT						"	Clock to D4+4	"	"	"	"	"	"	"
		102			"			IN	IN	"		OUT				"	Clock to D4+5	"	"	"	"	"	"	"
		103			"				"		OUT					"	Clock to D3+4	"	"	"	"	"	"	"
		104		"	"	IN		"	"		OUT					"	Clock to D2+4	"	"	"	"	"	"	"
		105			"	IN		"	"				OUT		"	Clock to D2+5	"	"	"	"	"	"	"	"
		106	IN		"			"	"					OUT	"	Clock to D1+4	"	"	"	"	"	"	"	"
t _{THL}	3004 Fig. 4	107			"			IN	IN	"	OUT					"	D4+4	13	150	18	200	13	150	"
		108			"				"	"		OUT				"	D4+5	"	"	"	"	"	"	"
		109			"			IN	"	"			OUT			"	D3+4	"	"	"	"	"	"	"
		110			"		IN		"	"				OUT		"	D2+4	"	"	"	"	"	"	"
		111			"		IN		"	"					OUT	"	D2+5	"	"	"	"	"	"	"
		112	IN		"				"	"					OUT	"	D1+4	"	"	"	"	"	"	"
t _{TLH}		113			"			IN	IN	"	OUT					"	D4+4	"	"	"	"	"	"	"
		114			"				"	"		OUT				"	D4+5	"	"	"	"	"	"	"
		115			"			IN	"	"			OUT			"	D3+4	"	"	"	"	"	"	"
		116		"	"		IN	"	"					OUT		"	D2+4	"	"	"	"	"	"	"
		117			"	IN		"	"						OUT	"	D2+5	"	"	"	"	"	"	"
		118	IN		"			"	"						OUT	"	D1+4	"	"	"	"	"	"	"
f _{CL} (max) 10/	119	120			"			IN	IN	"	OUT					"	Clock							μs
		121			"				"	"		OUT				"	"							"
		122		"	"		IN		"	"			OUT			"	"	.54		.714		.54		"
		123			"				"	"					OUT		"							"
		124	IN		"				"	"						OUT	"							"

See footnotes on next page.

TABLE III. Group A inspection for device type 51 – Continued.

- 1/ Terminals not designated may be “HIGH” level logic, “LOW” level logic, or open except as follows:
 $I_{C(pos)}$ tests; the V_{SS} terminal shall be open.
 $I_{C(neg)}$ tests; the V_{DD} terminal shall be open.
 V_{SS} tests; the output terminals shall be open.
- 2/ The I_{SS} test measurements shall be run in sequence.
- 3/ Apply single clock pulse; $V_{IN} = 0$ V to V_{DD} .
- 4/ Apply clock pulse; $V_{IN} = 0$ V dc to V_{DD} until proper output state is achieved.
- 5/ V_{IH} and V_{IL} tests are performed by repeating the truth table test (numbers 79 through 94) using the input and output conditions as follows:

Test	V_{DD}	Input levels		Output levels	
		H	L	H	L
V_{IL1} V_{IH1}	5.0V	3.5V	1.5V	Min 4.5V	Max 0.5V
V_{IL2} V_{IH2}	10.0V	7.0V	3.0V	9.0V	1.0V
V_{IL3} V_{IH3}	15.0V	11.0V	4.0V	13.5V	1.5V

- 6/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together.
- 7/ See 4.4.1c.
- 8/ The truth table test shall be performed in sequence.
- 9/ The truth table tests shall be performed at V_{IH} and $V_{DD} \leq 5$ V dc and ≥ 18 V dc.
 $L = V_{SS} + 0.5$ V maximum, and $H = V_{DD} - 0.50$ V dc minimum.
- 10/ The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.
- 11/ The device manufacturer may perform V_{IL}/V_{IH} tests as functional tests.

TABLE III. Group A inspection for device type 52.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C		
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min	
V _{IC} (pos)	1	2 3 4 5 6 7 8 9 10 11	1mA			1mA	1mA	1mA	1mA		1mA	1mA	1mA		1mA	1mA	1mA	GND	PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial In PI5 PI6 PI7	1.5						V
V _{IC} (neg)	12	13 14 15 16 17 18 19 20 21 22	-1mA			-1mA	-1mA	-1mA	-1mA	GND	-1mA	-1mA	-1mA		-1mA	-1mA	-1mA		PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial In PI5 PI6 PI7	-6						
I _{SS} 2/	3005	23 24 25 26 27 28 29 30 31 32	GND GND GND 18.0V " " " " " GND			GND GND GND 18.0V " " " " " GND	18.0V 18.0V 18.0V GND " " " " " 18.0V	GND GND GND 18.0V " " " " " GND	18.0V 18.0V 18.0V GND " " " " " 18.0V	" " " " " " " " " GND	18.0V " " " " " " " " " 18.0V	GND GND GND 18.0V " " " " " GND	18.0V GND 18.0V 18.0V " " " " " 18.0V	18.0V GND 18.0V 18.0V " " " " " 18.0V	18.0V GND 18.0V GND " " " " " 18.0V	18.0V GND 18.0V GND " " " " " 18.0V	18.0V GND 18.0V GND " " " " " 18.0V	18.0V GND 18.0V GND " " " " " 18.0V	18.0V None " " V _{SS} None V _{SS} None None V _{SS}	-0.5		-5.0				μA
V _{OH3}	3006	33 34 35	15.0V 15.0V 15.0V			15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	" " "	15.0V " "	3/ 3/ 3/	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V " "	Q6 Q7 Q8	14.95 14.95 14.95		14.95 14.95 14.95		14.95 14.95 14.95		V	
V _{OL3}	3007	36 37 38	GND GND GND			GND GND GND	GND GND GND	GND GND GND	GND GND GND	" " "	" " "	GND GND GND	GND GND GND	GND GND GND	GND GND GND	GND GND GND	" " "	Q6 Q7 Q8	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05		
V _{IH1} 12/		39	4/	4/	4/	4/	4/	4/	4/	"	4/	4/	4/	4/	4/	4/	4/	All outputs	4/	4/	4/	4/	4/	4/	4/	4/
V _{IH2} 12/		40	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
V _{IH3} 12/		41	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
V _{IL1} 12/		42	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
V _{IL2} 12/		43	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
V _{IL3} 12/		44	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
I _{OL1}		45 46 47	GND " "	0.4V " 0.4V		GND " "	GND " "	GND " "	GND " "	" " "	5.0V 5.0V 5.0V	3/ " "	GND " "	0.4V " "	GND " "	GND " "	GND " "	5.0V 5.0V 5.0V	Q6 Q7 Q8	0.51 0.51 0.51		0.36 0.36 0.36		0.64 0.64 0.64	mA	
I _{OL2}		48 49 50	" " "	1.5V " 1.5V		" " "	" " "	" " "	" " "	" " "	15.0V 15.0V 15.0V	" " "	" " "	1.5V " "	" " "	" " "	" " "	15.0V 15.0V 15.0V	Q6 Q7 Q8	3.4 3.4 3.4		2.4 2.4 2.4		4.2 4.2 4.2	"	

See footnotes at end of device type 52.

TABLE III. Group A inspection for device type 52 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit		
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C				
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Min	Max	Min	Max	Min	Max			
I _{OH1}		51 52 53	5.0V 5.0V 5.0V	4.6V		5.0V 5.0V 5.0V	5.0V 5.0V 5.0V	5.0V 5.0V 5.0V	5.0V 5.0V 5.0V	GND " "	5.0V 5.0V 5.0V	3/ " "	5.0V 5.0V 5.0V	4.6V	5.0V 5.0V 5.0V	5.0V 5.0V 5.0V	5.0V 5.0V 5.0V	5.0V 5.0V 5.0V	Q6 Q7 Q8	-0.51 -0.51 -0.51		-0.36 -0.36 -0.36		-0.64 -0.64 -0.64		mA " "		
I _{OH2}		54 55 56	15.0V 15.0V 15.0V	13.5V		15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	" " "	15.0V 15.0V 15.0V	" " "	15.0V 15.0V 15.0V	13.5V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	Q6 Q7 Q8	-3.4 -3.4 -3.4		-2.4 -2.4 -2.4		-4.2 -4.2 -4.2		" " "		
I _{IH1} 5/	3010	57	18.0V				18.0V	18.0V	18.0V	"	18.0V	18.0V 6/	18.0V		18.0V	18.0V	18.0V	18.0V	All inputs together		11					nA		
I _{IH2}		58 59 60 61 62 63 64 65 66 67 68	18.0V GND " " " " " " " " "			18.0V GND " " " " " " " "	GND GND GND GND GND GND GND GND GND GND GND	GND GND GND GND GND GND GND GND GND GND GND	GND " " " " " " " " " " "	" " " " " " " " " " "	GND " " " " " " " " " " "	GND " " " " " " " " " " "	GND " " " " " " " " " " "	" " " " " " " " " " "	GND " " " " " " " " " " "	GND " " " " " " " " " " "	GND " " " " " " " " " " "	GND " " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	P/S control Clock Serial In PI5 PI6 PI7	1	"	45	"	"	"	"
		69	"				"	"	"	"	"	"	"	"	"	"	"	"	"	All inputs together		-11				"		
		70 71 72 73 74 75 76 77 78 79 80	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " "	" " " " " " " " " "	" " " " " " " " " "	" " " " " " " " " "	" " " " " " " " " "	P/S control Clock Serial In PI5 PI6 PI7	-1	"	-45	"	"	"	"	
																				Subgroup 4 T _C = 25°C								
																				Min	Max							
		C _i	3012	81 82 83 84 85 86 87 88 89 90 91	Z/ " " " " " " " " " "	 " " " " " " " " " "	 " " " " " " " " " "	Z/ " " " " " " " " " "	Z/ " " " " " " " " " "	Z/ " " " " " " " " " "	GND " " " " " " " " " "	 " " " " " " " " "	Z/ " " " " " " " " "	Z/ " " " " " " " " "	 " " " " " " " " "	 " " " " " " " " "	Z/ " " " " " " " " "	Z/ " " " " " " " " "	GND " " " " " " " " "	PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial In PI5 PI6 PI7	 " " " " " " " " "	12 " " " " " " " "	 " " " " " " " "	 " " " " " " " "	 " " " " " " " "	 " " " " " " " "	pF " " " " " " " "	

See footnotes at end of device type 52.

TABLE III. Group A inspection for device type 52 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																							
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 7		Subgroup 8																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																											
																				T _C = 25°C		T _C = 125°C		T _C = -55°C																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
																				Min	Max	Min	Max	Min	Max																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																								
Truth table test	3014 8/	92	5.0V			5.0V	5.0V	5.0V	5.0V	GND	5.0V	5.0V	GND		5.0V	5.0V	5.0V	5.0V	None None All outputs	See 9/, 10/																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																													

See footnotes at end of device type 52.

TABLE III. Group A inspection for device type 52 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C		
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min	
t _{PHL1}	3003 Fig. 4	140 141 142	IN IN IN	OUT		IN IN IN	IN IN IN	IN IN IN	IN IN IN	GND GND GND	GND GND GND	IN IN IN	IN IN IN	OUT	IN IN IN	IN IN IN	IN IN IN	5.0V 5.0V 5.0V	Clock to Q6 Clock to Q7 Clock to Q8	13 " " " "	338 " " " "	18 " " " "	450 " " " "	13 " " " "	338 " " " "	ns ns ns
t _{PLH1}	3003 Fig. 4	143 144 145	IN " " " "	OUT		IN " " OUT	IN " " " "	IN " " " "	IN " " " "	GND " " " "	GND GND GND	IN " " " "	IN " " " "	OUT	IN " " " "	IN " " " "	IN " " " "	5.0V " " " "	Clock to Q6 Clock to Q7 Clock to Q8	13 " " " "	338 " " " "	18 " " " "	450 " " " "	13 " " " "	338 " " " "	ns " " " "
t _{PHL2}		146 147 148	" " " " " "	OUT		" " " " OUT	" " " " " "	" " " " " "	" " " " " "	" " " " " "	5.0V " " " "	" " " " " "	" " " " " "	OUT	" " " " " "	" " " " " "	" " " " " "	" " " " " "	Clock to Q6 Clock to Q7 Clock to Q8	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "
t _{PLH2}		149 150 151	" " " " " "	OUT		" " " " OUT	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	OUT	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	Clock to Q6 Clock to Q7 Clock to Q8	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "
t _{THL}	3004 Fig. 4	152 153 154	" " " " " "	OUT		" " " " OUT	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	OUT	" " " " " "	" " " " " "	" " " " " "	" " " " " "	Q6 Q7 Q8	10 " " " "	210 " " " "	14 " " " "	280 " " " "	10 " " " "	210 " " " "	" " " " " "
t _{TLH}		155 156 157	" " " " " "	OUT		" " " " OUT	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	OUT	" " " " " "	" " " " " "	" " " " " "	" " " " " "	Q6 Q7 Q8	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "	" " " " " "
f _{CL} (max) 11/		159 160		OUT		OUT					" " GND GND GND	" " " " " "	" " " " " "	OUT				" "	Clock Clock Clock		.625	" "	.833	" "	.625	" "

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- 1/ Terminals not designated may be "HIGH" level logic, "LOW" level logic, or open except as follows: V_{IC(pos)} tests; the V_{SS} terminal shall be open.
 IC(neg) tests; the V_{DD} terminal shall be open. I_{SS} test; the output terminal shall be open.
 2/ I_{SS} tests; the output terminals shall be performed in sequence.
 3/ Apply a single clock pulse; V_{IN} = 0 V dc to V_{DD}.
 4/ V_{IH} and V_{IL} tests are performed by repeating the truth table test (numbers 92 through 139) using the input and output conditions as follows:

Test	V _{DD}	Input		Output	
		H	L	H	L
V _{IH1} V _{IL1}	5.0V	3.5V	1.5V	4.5V min	0.5V max
V _{IH2} V _{IL2}	10.0V	7.0V	3.0V	9.0V min	1.0V max
V _{IH3} V _{IL3}	15.0V	11.0V	4.0V	13.5V min	1.5V max

- 5/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together.
 6/ Apply six (6) clock pulses, V_{IN} = 0 V dc to V_{DD}.
 7/ See 4.4.1c.
 8/ Truth table test shall be run in sequence.
 9/ The output voltage limits for each temperature are "H" = V_{DD} - 0.5 V min and "L" = V_{SS} + 0.5 V max.
 10/ The truth table tests shall be performed at V_{IH} and V_{DD} ≤ 5 V dc and ≥ 18 V dc.
 11/ The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.
 12/ The device manufacturer may perform V_{IL}/V_{IH} tests as functional tests.

TABLE III. Group A inspection for device type 53.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			Clock B	Q4B	Q3A	Q2A	Q1A	Reset A	Data A	V _{SS}	Clock A	Q4A	Q3B	Q2B	Q1B	Reset B	Data B	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C		
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min	
V _{IC} (pos)	1	2 3 4 5 6	1mA					1mA	1mA	1mA						1mA	1mA	GND	Clock A Data A Reset A Clock B Data B Reset B		1.5					V
V _{IC} (neg)	7	8 9 10 11 12	-1mA					-1mA	-1mA	GND	-1mA								Clock A Data A Reset A Clock B Data B Reset B		-6					
I _{SS} 2/	3005	13 14 15 16 17 18 19 20 21 22 23 24 25 26 27	GND 18.0V 18.0V GND 18.0V 18.0V GND GND GND 18.0V 18.0V 18.0V GND 18.0V 18.0V GND GND GND 18.0V					18.0V 18.0V GND	18.0V GND GND GND 18.0V 18.0V 18.0V GND 18.0V 18.0V GND GND GND 18.0V		GND 18.0V 18.0V GND 18.0V 18.0V GND 18.0V 18.0V GND 18.0V 18.0V					18.0V 18.0V GND	18.0V GND GND GND 18.0V 18.0V GND GND GND 18.0V	18.0V V _{SS} None	-0.5	-5.0					μA	
V _{OH3}	3006	28 29 30 31 32 33 34 35	GND GND GND 3/ GND					15.0V GND	3/ GND							GND 15.0V	15.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B	14.95	14.95	14.95			V		
V _{OL3}	3007	36 37 38 39 40 41 42 43	GND GND GND 3/ GND						3/ GND							GND		Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B	0.05	0.05	0.05					
V _{IH1}			4/	4/	4/	4/	4/	4/		4/	4/	4/	4/	4/	4/	4/	4/	All outputs	4/	4/	4/	4/	4/	4/	4/	
V _{IH2}		45																								
V _{IH3}		46																								
V _{IL1}	44	47																								
V _{IL2}		48																								
V _{IL3}		49																								

See footnotes at end of device type 53.

TABLE III. Group A inspection for device type 53 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit											
			Clock B	Q4B	Q3A	Q2A	Q1A	Reset A	Data A	V _{SS}	Clock A	Q4A	Q3B	Q2B	Q1B	Reset B	Data B	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C													
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min		Max										
I _{OL1}		50	GND	0.4V	0.4V	0.4V	GND	GND	GND	3/	0.4V	0.4V	0.4V	0.4V	GND	GND	5.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B	0.51	0.36	0.64		mA														
		51																																			
		52																																			
		53		3/	0.4V	0.4V	0.4V	GND	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V	GND	GND	5.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B																			
		54																																			
		55																																			
		56		0.4V	0.4V	0.4V	GND	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V	GND	GND	5.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B																			
57																																					
I _{OL2}		58	GND	1.5V	1.5V	1.5V				3/	1.5V	1.5V	1.5V	1.5V			15.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B	3.4	2.4	4.2																
		59																																			
		60																																			
		61		1.5V	1.5V	1.5V				3/	1.5V	1.5V	1.5V	1.5V			15.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B																			
		62																																			
		63																																			
		64		1.5V	1.5V	1.5V				3/	1.5V	1.5V	1.5V	1.5V			15.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B																			
65																																					
I _{OH1}		66	GND	4.6V	4.6V	4.6V		5.0V		3/	4.6V	4.6V	4.6V	4.6V			5.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B	-0.51	-0.36	-0.64																
		67																																			
		68																																			
		69		4.6V	4.6V	4.6V		GND		3/	4.6V	4.6V	4.6V	4.6V			5.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B																			
		70																																			
		71																																			
		72		4.6V	4.6V	4.6V				3/	4.6V	4.6V	4.6V	4.6V			5.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B																			
73																																					
I _{OH2}		74	GND	13.5V	13.5V	13.5V		15.0V		3/	13.5V	13.5V	13.5V	13.5V			15.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B	-3.4	-2.4	-4.2																
		75																																			
		76																																			
		77		13.5V	13.5V	13.5V				3/	13.5V	13.5V	13.5V	13.5V			15.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B																			
		78																																			
		79																																			
		80		13.5V	13.5V	13.5V				3/	13.5V	13.5V	13.5V	13.5V			15.0V	Q1A Q2A Q3A Q4A Q1B Q2B Q3B Q4B																			
81																																					
I _{IH1} 5/	3010	82	18.0V					18.0V	18.0V		18.0V					18.0V	18.0V	18.0V	All inputs together		6.0					nA											
I _{IH2}		83	GND					GND	GND		18.0V					GND	GND		Clock A Data A Reset A Clock B Data B Reset B	1.0	45																
		84	GND					18.0V	GND																												
		85	GND					GND																													
		86	18.0V																																		
		87	GND																																		
88															18.0V	GND																					
I _{IL1} 5/	3009	89													GND			All inputs together		-6.0																	
I _{IL2}		90																	Clock A Data A Reset A Clock B Data B Reset B	-1.0	-45																
		91																																			
		92																																			
		93																																			
		94																																			
95																																					

See footnotes at end of device type 53.

TABLE III. Group A inspection for device type 53 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			Clock B	Q4B	Q3A	Q2A	Q1A	Reset A	Data A	V _{SS}	Clock A	Q4A	Q3B	Q2B	Q1B	Reset B	Data B	V _{DD}		Subgroup 4 T _C = 25°C						
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Min	Max					
C _i	3012	96 97 98 99 100 101	<u>6</u> /					<u>6</u> /	<u>6</u> /	GND	<u>6</u> /							GND	Clock A Data A Reset A Clock B Data B Reset B	12	"					pF
																				Subgroup 7 T _C = 25°C		Subgroup 8 T _C = 125°C T _C = -55°C				Unit
																				Min	Max	Min	Max	Min	Max	
Truth table test <u>7</u> /	3014	102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120	5.0V 5.0V GND 5.0V 5.0V GND 5.0V 5.0V GND 5.0V GND 5.0V 5.0V GND 5.0V 5.0V GND 5.0V 5.0V	L "																						

See footnotes at end of device type 53.

TABLE III. Group A inspection for device type 53 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			Clock B	Q4B	Q3A	Q2A	Q1A	Reset A	Data A	V _{SS}	Clock A	Q4A	Q3B	Q2B	Q1B	Reset B	Data B	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C		
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min	
t _{PLH1}	3003 Fig. 4	129	IN				OUT	GND	IN	GND	IN					GND	IN	5.0V	Clock A to Q1A	20	421	30	560	20	421	ns
		130	"				OUT	"	"	"	"					"	"	"	Clock A to Q2A	"	"	"	"	"	"	"
		131	"			OUT		"	"	"	"					"	"	"	Clock A to Q3A	"	"	"	"	"	"	"
		132	"					"	"	"	"	OUT				"	"	"	Clock A to Q4A	"	"	"	"	"	"	"
		133	"					"	"	"	"	"			OUT	"	"	"	Clock B to Q1B	"	"	"	"	"	"	"
		134	"					"	"	"	"	"		OUT		"	"	"	Clock B to Q2B	"	"	"	"	"	"	"
		135	"					"	"	"	"	"			OUT	"	"	"	Clock B to Q3B	"	"	"	"	"	"	"
		136	"	OUT				"	"	"	"	"				"	"	"	Clock B to Q4B	"	"	"	"	"	"	"
t _{PHL2}	3003 Fig. 4	137	GND				OUT	IN	IN	GND	GND					IN	IN	5.0V	Reset A to Q1A	20	368	30	490	20	368	ns
		138	"				OUT	"	"	"	"					"	"	"	Reset A to Q2A	"	"	"	"	"	"	"
		139	"			OUT		"	"	"	"					"	"	"	Reset A to Q3A	"	"	"	"	"	"	"
		140	"					"	"	"	"	OUT				"	"	"	Reset A to Q4A	"	"	"	"	"	"	"
		141	"					"	"	"	"	"			OUT	"	"	"	Reset B to Q1B	"	"	"	"	"	"	"
		142	"					"	"	"	"	"		OUT		"	"	"	Reset B to Q2B	"	"	"	"	"	"	"
		143	"					"	"	"	"	"	OUT			"	"	"	Reset B to Q3B	"	"	"	"	"	"	"
		144	"	OUT				"	"	"	"	"				"	"	"	Reset B to Q4B	"	"	"	"	"	"	"
t _{THL}	3004 Fig. 4	145	IN				OUT	GND	"	"	IN					GND	"	"	Q1A	13	210	18	280	13	210	"
		146	"					"	"	"	"	"				"	"	"	Q2A	"	"	"	"	"	"	"
		147	"			OUT		"	"	"	"					"	"	"	Q3A	"	"	"	"	"	"	"
		148	"					"	"	"	"	OUT				"	"	"	Q4A	"	"	"	"	"	"	"
		149	"					"	"	"	"	"			OUT	"	"	"	Q1B	"	"	"	"	"	"	"
		150	"					"	"	"	"	"		OUT		"	"	"	Q2B	"	"	"	"	"	"	"
		151	"					"	"	"	"	"				"	"	"	Q3B	"	"	"	"	"	"	"
		152	"	OUT				"	"	"	"	"				"	"	"	Q4B	"	"	"	"	"	"	"
t _{TLH}		153	"				OUT	"	"	"	"					"	"	"	Q1A	"	"	"	"	"	"	"
		154	"				OUT	"	"	"	"	"				"	"	"	Q2A	"	"	"	"	"	"	"
		155	"			OUT		"	"	"	"	"	OUT			"	"	"	Q3A	"	"	"	"	"	"	"
		156	"					"	"	"	"	"			OUT	"	"	"	Q4A	"	"	"	"	"	"	"
		157	"					"	"	"	"	"				"	"	"	Q1B	"	"	"	"	"	"	"
		158	"					"	"	"	"	"		OUT		"	"	"	Q2B	"	"	"	"	"	"	"
		159	"					"	"	"	"	"	OUT			"	"	"	Q3B	"	"	"	"	"	"	"
		160	"	OUT				"	"	"	"	"				"	"	"	Q4B	"	"	"	"	"	"	"

See footnotes at end of device type 53.

TABLE III. Group A inspection for device type 53 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			Clock B	Q4B	Q3A	Q2A	Q1A	Reset A	Data A	V _{SS}	Clock A	Q4A	Q3B	Q2B	Q1B	Reset B	Data B	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C		
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min	
f _{CL} (max) 10/	161	162	IN				OUT	OUT	GND	IN	GND	IN				GND	IN	5.0v	Clock A		.5					μs
		163	"						"	"	"	"				"	"	"	"		"				"	"
		164	"			OUT			"	"	"	"				"	"	"	"		.667	"		.5	"	"
		165	"						"	"	"	"				"	"	"	"						"	"
		166	"						"	"	"	"				"	"	"	"						"	"
		167	"						"	"	"	"				"	"	"	"						"	"
		168	"						"	"	"	"				"	"	"	"						"	"
				OUT						"	"	"	"	OUT	OUT		"	"	"						"	"

1/ Terminals not designated may be "HIGH" level logic, "LOW" level logic, or open except as follows: V_{IC(pos)} tests; the V_{SS} terminal shall be open. V_{IC(neg)} tests; the V_{DD} terminal shall be open. I_{SS} test; the output terminal shall be open.

2/ I_{SS} test measurements shall be performed in sequence.

3/ Apply a clock pulse; V_{IN} = 0 V dc to V_{DD} until proper output state is achieved.

4/ V_{IH} and V_{IL} tests are performed by repeating the truth table tests (numbers 102 through 120) using the input conditions as follows:

Test	V _{DD}	Input		Output	
		H	L	H	L
V _{IH1} V _{IL1}	5.0V	3.5V	1.5V	4.5V min	0.5 max
V _{IH2} V _{IL2}	10.0V	7.0V	3.0V	9.0V min	1.0V max
V _{IH3} V _{IL3}	15.0V	11.0V	4.0V	13.5V min	1.5V max

5/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together.

6/ See 4.4.1c.

7/ Truth table test shall run in sequence.

8/ The truth table test shall be performed at V_{IH} and V_{DD} ≤ 5.0 V dc and ≥ 18.0 V dc.

9/ The output voltage limits for each temperature are "H" = V_{DD} - 0.5 V min and "L" = V_{SS} + 0.5 V max.

10/ The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.

See footnotes at end of device type 54.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																	Measured terminal	Test limits						Unit
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}	Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C				
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Min		Max	Min	Max	Min	Max		
V _{IC} (pos)	1	2 3 4 5 6 7 8 9 10 11	1mA			1mA	1mA	1mA	1mA		1mA	1mA			1mA	1mA		GND	PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial In PI5 PI6 PI7	1.5	"					V	
V _{IC} (neg)	12	13 14 15 16 17 18 19 20 21 22	-1mA			-1mA	-1mA	-1mA	-1mA	GND " " " " " " "	-1mA	-1mA			-1mA	-1mA		-1mA	PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial In PI5 PI6 PI7	-6	"					"	
I _{SS} 2/	3005	23 24 25 26 27 28 29	GND 18.0V 18.0V 18.0V GND GND GND			GND 18.0V 18.0V 18.0V GND GND GND	18.0V GND 18.0V 18.0V GND 18.0V 18.0V	GND 18.0V GND 18.0V GND 18.0V GND	18.0V GND 18.0V 18.0V GND 18.0V 18.0V	" " " " " " "	18.0V 18.0V 18.0V " 18.0V GND GND	GND GND 18.0V 18.0V 18.0V 18.0V 18.0V	18.0V	GND 18.0V GND 18.0V GND 18.0V GND	GND 18.0V GND 18.0V GND 18.0V GND	18.0V 18.0V 18.0V 18.0V 18.0V 18.0V 18.0V	18.0V	V _{SS} V _{SS} None V _{SS} None V _{SS} V _{SS}	-0.5	"	-5.0	"			μA		
V _{OH3}	3006	30 31 32	15.0V 15.0V 15.0V			15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	" " "	15.0V " "	15.0V 15.0V 15.0V	15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V	Q6 Q7 Q8	14.95 14.95 14.95		14.95 14.95 14.95		14.95 14.95 14.95		V		
V _{OL3}	3007	33 34 35	GND GND GND			GND GND GND	GND GND GND	GND GND GND	GND GND GND	" " "	" " "	GND GND GND	GND	GND GND GND	GND GND GND	GND GND GND	"	Q6 Q7 Q8	.05 .05 .05	.05	.05 .05 .05	.05	.05 .05 .05	.05	"		
V _{IH1}			4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	All outputs	4/	4/	4/	4/	4/	4/	4/		
V _{IH2}		37	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	4/	4/	4/	4/	4/	4/		
V _{IH3}		38	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
V _{IL1}	36	39	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
V _{IL2}		40	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
V _{IL3}		41	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
I _{OL1}		42 43 44	GND " "	0.4V " 0.4V		GND " "	GND " "	GND " "	GND " "	" " "	5.0V 5.0V 5.0V	3/ " "	GND " 0.4V	GND " "	GND " "	GND " "	5.0V 5.0V 5.0V	Q6 Q7 Q8	0.51 0.51 0.51		0.36 0.36 0.36		0.64 0.64 0.64		mA		
I _{OL2}		45 46 47	" " "	1.5V " 1.5V		" " "	" " "	" " "	" " "	" " "	15.0V 15.0V 15.0V	" " "	" " 1.5V	" " "	" " "	" " "	15.0V 15.0V 15.0V	Q6 Q7 Q8	3.4 3.4 3.4		2.4 2.4 2.4		4.2 4.2 4.2		"		
I _{OH1}		48 49 50	5.0V 5.0V 5.0V	4.6V " 4.6V		5.0V 5.0V 5.0V	5.0V 5.0V 5.0V	5.0V 5.0V 5.0V	5.0V 5.0V 5.0V	" " "	5.0V 5.0V 5.0V	" " "	5.0V 5.0V 5.0V	4.6V 5.0V 5.0V	5.0V 5.0V 5.0V	5.0V 5.0V 5.0V	5.0V	Q6 Q7 Q8	-0.51 -0.51 -0.51		-0.36 -0.36 -0.36		-0.64 -0.64 -0.64		"		

TABLE III. Group A inspection for device type 54 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit	
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C			
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min		Max
I _{OH2}		51 52 53	15.0V 15.0V 15.0V	13.5V		15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	GND " "	15.0V 15.0V 15.0V	3/ 3/ 3/	15.0V 15.0V 15.0V	13.5V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	15.0V 15.0V 15.0V	Q6 Q7 Q8	-3.4 -3.4 -3.4			-2.4 -2.4 -2.4		-4.2 -4.2 -4.2		mA mA mA	
I _{IH1} 5/ I _{IH2}	3010	54	18.0V			18.0V	18.0V	18.0V	18.0V	"	18.0V	18.0V	18.0V		18.0V	18.0V	18.0V	18.0V	All inputs together		1100					nA	
		55 56 57 58 59 60 61 62 63 64 65	18.0V GND GND GND GND GND GND GND GND GND GND		18.0V	GND 18.0V GND GND GND GND GND GND GND GND GND	GND GND GND GND GND GND GND GND GND GND GND	GND GND GND GND GND GND GND GND GND GND GND	GND GND GND GND GND GND GND GND GND GND GND	" " " " " " " " " " "	GND GND GND GND GND GND GND GND GND GND GND	GND GND GND GND GND GND GND GND GND GND GND	GND GND GND GND GND GND GND GND GND GND GND		GND GND GND GND GND GND GND GND GND GND GND	GND GND GND GND GND GND GND GND GND GND GND	GND GND GND GND GND GND GND GND GND GND GND	GND GND GND GND GND GND GND GND GND GND GND	PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial In PI5 PI6 PI7	100	"	100	"	"	"	"	
I _{IL1} 5/ I _{IL2}	3009	66	"			"	"	"	"	"	"	"	"		"	"	GND	"	All inputs together		-1100					"	
		67 68 69 70 71 72 73 74 75 76 77	" " " " " " " " " " "			" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "		" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " " "	" " " " " " " " " "	PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial In PI5 PI6 PI7	-100	"	-100	"	"	"	"
																			Subgroup 4 T _C =25°C								
																			Min	Max							
C _i	3012	78 79 80 81 82 83 84 85 86 87 88	6/ " " " " " " " " " "			6/ " " " " " " " " " "	6/ " " " " " " " " " "	6/ " " " " " " " " "	6/ " " " " " " " " "	GND " " " " " " " " "	6/ " " " " " " " " "	6/ " " " " " " " " "	6/ " " " " " " " " "		6/ " " " " " " " " "	6/ " " " " " " " " "	6/ " " " " " " " " "	GND " " " " " " " " "	PI8 PI4 PI3 PI2 PI1 P/S control Clock Serial In PI5 PI6 PI7	12	"	"	"	"	"	pF	

See footnotes at end of device type 54.

TABLE III. Group A inspection for device type 54 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit	
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 7		Subgroup 8					
																				T _C = 25°C		T _C = 125°C		T _C = -55°C			
																				Min	Max	Min	Max	Min	Max		
Truth table test 7/	3014	89	GND	L	L	GND	GND	GND	GND	GND	5.0V	5.0V	GND	L	GND	GND	GND	5.0V	All outputs	See 9/, 10/							
		90	GND	"	"	GND	GND	GND	GND	"	GND	5.0V	GND	"	GND	GND	"	"									
		91	5.0V	"	"	5.0V	5.0V	5.0V	GND	"	GND	8/	5.0V	"	5.0V	5.0V	"	"									
		92	5.0V	"	"	5.0V	5.0V	GND	5.0V	"	GND	8/	GND	"	5.0V	5.0V	5.0V	"			"						
		93	5.0V	"	"	5.0V	GND	5.0V	GND	"	GND	8/	5.0V	"	5.0V	5.0V	"	"									
		94	"	"	"	GND	5.0V	GND	"	"	"	8/	"	"	5.0V	"	"	"			"						
		95	"	"	"	5.0V	GND	"	"	"	"	8/	"	"	GND	"	"	"			"						
		96	"	"	"	5.0V	"	"	"	"	"	GND	"	"	GND	"	"	"			"						
		97	"	H	"	GND	"	"	"	"	"	5.0V	"	"	5.0V	GND	"	"			"						
		98	"	H	"	"	"	"	"	"	"	GND	"	"	5.0V	GND	"	"			"						
		99	"	L	"	"	"	"	"	"	"	5.0V	"	H	GND	5.0V	GND	"			"						
		100	"	L	"	"	"	"	"	"	"	GND	"	H	GND	5.0V	GND	"			"						
		101	GND	H	H	"	"	"	"	"	"	5.0V	"	L	"	GND	5.0V	"			"						
		102	5.0V	"	L	"	"	"	"	"	"	8/	"	H	"	"	GND	"			"						
		103	GND	"	H	"	"	"	"	"	"	8/	"	H	"	"	"	"			"						
		104	"	"	H	"	"	"	"	"	"	GND	"	H	"	"	"	"			"						
		105	"	L	L	"	"	"	"	"	5.0V	GND	"	L	"	"	"	"			"						
		106	"	"	"	"	"	"	"	"	GND	GND	GND	"	"	"	"	"			"						
		107	5.0V	"	"	5.0V	5.0V	5.0V	5.0V	"	"	5.0V	"	"	5.0V	5.0V	5.0V	"			"						
		108	"	"	"	"	"	"	"	"	"	8/	"	"	"	"	"	"			"						
		109	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			"						
		110	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			"						
		111	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			"						
		112	"	"	"	"	"	"	"	"	"	"	GND	"	"	"	"	"			"						
		113	"	H	H	"	"	"	"	"	"	5.0V	GND	"	H	"	"	"			"						
		114	"	"	"	"	"	"	"	"	"	GND	GND	5.0V	"	"	"	"			"						
		115	GND	"	"	GND	GND	GND	5.0V	"	"	"	5.0V	"	"	GND	GND	GND			"						
		116	"	"	"	GND	GND	GND	"	"	"	"	8/	"	"	"	"	"			"						
		117	"	"	"	GND	5.0V	"	"	"	"	"	"	"	"	"	"	"			"						
		118	"	"	"	5.0V	5.0V	"	"	"	"	"	"	"	"	"	"	"			"						
		119	"	"	"	5.0V	5.0V	"	"	"	"	"	"	"	"	5.0V	"	"			"						
		120	"	L	L	GND	GND	GND	GND	"	"	8/	5.0V	"	L	GND	"	"			"						
		121	"	"	"	GND	GND	"	"	"	"	GND	8/	"	"	GND	"	"			"						
		122	5.0V	"	"	5.0V	5.0V	"	"	"	"	"	"	"	"	5.0V	5.0V	5.0V			"						
		123	"	"	"	5.0V	GND	"	"	"	"	"	"	"	"	5.0V	"	"			"						
		124	"	"	"	GND	GND	"	"	"	"	"	"	"	"	5.0V	"	"			"						
		125	"	"	"	GND	GND	"	"	"	"	"	"	"	"	GND	"	"			"						
																				Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C			
t _{PHL1}	3003 Fig. 4	126		OUT		IN	IN	IN	IN	GND	IN	GND		OUT	IN	IN	IN	5.0V	P/S to Q6	20	368	30	490	20	368	ns	
		127								"	"	"						"	P/S to Q7	"	"	"	"	"	"	"	
		128	IN		OUT		IN	IN	IN	IN	"	"	"		OUT	IN	IN	IN	"	P/S to Q8	"	"	"	"	"	"	"
t _{PLH1}		129		OUT		IN	IN	IN	IN	"	"	"			OUT	IN	IN	IN	5.0V	P/S to Q6	"	"	"	"	"	"	"
		130								"	"	"						"	P/S to Q7	"	"	"	"	"	"	"	
		131	IN		OUT					"	"	"						"	P/S to Q8	"	"	"	"	"	"	"	
t _{PHL2}		132								"	GND	IN	IN					"	Clock to Q6	"	"	"	"	"	"	"	
		133								"	"	"	"					"	Clock to Q7	"	"	"	"	"	"	"	
		134	OUT		OUT					"	"	"	"		OUT				"	Clock to Q8	"	"	"	"	"	"	"
t _{PLH2}		135								"	"	"	"		OUT				"	Clock to Q6	"	"	"	"	"	"	"
		136							"	"	"	"						"	Clock to Q7	"	"	"	"	"	"	"	
		137	OUT		OUT				"	"	"	"						"	Clock to Q8	"	"	"	"	"	"	"	

See footnotes at end of device type 54.

TABLE III. Group A inspection for device type 54 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			PI8	Q6	Q8	PI4	PI3	PI2	PI1	V _{SS}	P/S control	Clock	Serial In	Q7	PI5	PI6	PI7	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C		
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min	
t _{THL}	3004 Fig. 4	138							GND	GND	IN	IN					5.0V	Q6	13	210	18	280	13	210	ns	
		139											OUT					Q7								
		140	OUT		OUT													Q8								
t _{TLH}		141											OUT					Q6								
		142																Q7								
		143	OUT		OUT													Q8								
f _{CL} (max)		145											OUT					Clock		.75					μs	
11/		146	OUT		OUT													Clock			1.0		.75		μs	

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- 1/ Terminals not designated may be "HIGH" level logic, "LOW" level logic, or open except as follows: V_{IC(pos)} tests; the V_{SS} terminal shall be open. I_{C(neg)} tests; the V_{DD} terminal shall be open. I_{SS} tests; the output terminals shall be open.
- 2/ The I_{SS} test measurements shall be performed in sequence.
- 3/ Apply clock pulse; V_{IN} = 0 V dc to V_{DD} until proper state is achieved.
- 4/ V_{IH} and V_{IL} tests are performed by repeating the truth table tests (numbers 89 through 125) using the input and output conditions as shown below:

Test	V _{DD}	Input		Output	
		H	L	H	L
V _{IH1}	5.0V	3.5V	1.5V	Min	Max
V _{IL1}				4.5V	0.5V
V _{IH2}	10.0V	7.0V	3.0V	9.0V	1.0V
V _{IL2}	15.0V	11.0V	4.0V	13.5V	1.5V
V _{IH3}					
V _{IL3}					

- 5/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together.
- 6/ See 4.4.1c.
- 7/ The truth table test shall be performed in sequence.
- 8/ Apply clock pulse, V_{IN} = 0 V dc to V_{DD}, t_p = 500 ns (min), t_{THL} = 10 ns ± 10%.
- 9/ The output voltage limits for each temperature are "H" = V_{DD} - 0.5 V min and "L" = V_{SS} + 0.5 V max.
- 10/ The truth table tests shall be performed at V_{IH} and V_{DD} ≤ 5 V dc and ≥ 18 V dc.
- 11/ The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.

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See footnotes at end of device type 55.

TABLE III. Group A inspection for device type 55 – Continued.

Symbol	MIL-STD-883 method	Cases E, F, N, Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit	
			Recir In	Clock	NC	NC	NC	Q	Q	V _{SS}	Delayed clock	Mode cont	NC	NC	NC	NC	Data In	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C			
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min		Max
I _{SS} 2/	3005	46	GND	3/						GND							GND	18.0V	None							μA	
		47															18.0V										
		48															GND										
		49										GND						18.0V			-2		-20				
		50																GND									
		51																18.0V									
		52																GND									
		53																18.0V									
		54																GND									
		55																18.0V									
		56																GND									
		57																18.0V									
		58																GND									
		59																18.0V									
		60																GND									
		61																18.0V									
		62																GND									
		63	GND	3/							GND							18.0V	18.0V	None							μA
		64																GND									
		65																18.0V									
		66										GND						GND			-2		-20				
		67																18.0V									
		68																GND									
		69																18.0V									
		70																GND									
		71																18.0V		V _{SS}							
		72																18.0V		V _{SS}							
		73																18.0V		None							
		74	18.0V															GND		V _{SS}							
		75	18.0V															GND		V _{SS}							
		76	GND										18.0V					18.0V		V _{SS}							
V _{OH3}	3006	77	GND	4/													15.0V	15.0V	Q	14.95							
		78	GND	4/													GND		Q								
		79	GND	15.0V													15.0V		Delayed clock			14.95		14.95		V	
V _{OL3}	3007	80	GND	4/													GND		Q								
		81	GND	4/													15.0V		Q								
		82	GND	GND													GND		Delayed clock	0.05		0.05		0.05			
V _{IH1}			5/	5/					5/	5/		5/	5/				5/	5/	All outputs	5/	5/	5/	5/	5/	5/		
V _{IH2}		84																									
V _{IH3}		85																									
V _{IL1}	83	86																									
V _{IL2}		87																									
V _{IL3}		88																									
I _{OL1}		89	GND	4/					0.4V								GND	5.0V	Q	0.51							
		90		4/													5.0V	Q	0.51			0.36	0.36	0.64			
		91		GND							0.4V						GND	5.0V	Delayed clock	0.51	0.36	0.36	0.64	0.64	mA		
I _{OL2}		92		4/					1.5V								GND	15.0V	Q	3.4		2.4	2.4	4.2			
		93		4/													15.0V	Q	3.4								
		94		GND							1.5V						GND	15.0V	Delayed clock	3.4	2.4	2.4	4.2	4.2			

See footnotes at end of device type 55.

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See 9/, 10/, 11/

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TABLE III. Group A inspection for device type 55 – Continued.

Symbol	MIL-STD-883 method	Cases E,F,N,Z	Terminal conditions and limits 1/																Measured terminal	Test limits						Unit
			Recir In	Clock	NC	NC	NC	Q	$\overline{Q}$	V _{SS}	Delayed clock	Mode cont	NC	NC	NC	NC	Data In	V _{DD}		Subgroup 9 T _C =25°C		Subgroup 10 T _C =125°C		Subgroup 11 T _C =-55°C		
			Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	Min	Max	Min	Max	Min	
t _{PHL1}	3003 Fig. 4	136	GND	IN				OUT		GND		GND					IN	5.0V	Clock to Q	13	632	18	840	13	632	ns
t _{PHL2}		137	GND	IN					OUT	GND		GND					IN	5.0V	Clock to $\overline{Q}$	"	632	"	840	"	632	ns
t _{PHL3}		138	GND	IN						GND	OUT	GND						5.0V	Clock to Delayed clock	"	263	"	350	"	263	ns
t _{PHL4}	3003 Fig. 4	139	IN	IN						GND		5.0V						5.0V	Clock to Q	13	632	18	840	13	632	ns
t _{PLH1}		140	GND	"				OUT		"		GND					IN	"	Clock to Q	"	"	"	"	"	"	"
t _{PLH2}		141	GND	"				OUT		OUT	"	GND					IN	"	Clock to $\overline{Q}$	"	"	"	"	"	"	"
t _{PLH3}		142	GND	"							"	OUT	GND					"	Clock to Delayed clock	"	263	"	350	"	263	"
t _{PLH4}		143	IN	"				OUT		"		5.0V						"	Clock to Q	"	632	"	840	"	632	"
t _{THL1}	3004 Fig. 4	144	GND	"				OUT		"		GND					IN	"	Q	10	210	14	280	10	210	"
t _{THL2}		145	"	"					OUT	"		"					IN	"	$\overline{Q}$	"	210	"	280	"	210	"
t _{THL3}		146	"	"						"	OUT	"						"	Delayed clock	"	150	"	200	"	150	"
t _{TLH1}		147	"	"				OUT		"		"					IN	"	Q	"	210	"	280	"	210	"
t _{TLH2}		148	"	"					OUT	"		"					IN	"	$\overline{Q}$	"	210	"	280	"	210	"
t _{TLH3}		149	"	"						"	OUT	"						"	Delayed clock	"	150	"	200	"	150	"
f _{CL} (max) 13/	150	151		"				OUT		"	OUT	"					IN	"	Clock						μs	
		152		"					OUT	"		"					IN	"	"	.94	"	1.25	"	.94	"	
		153	IN	"						"		5.0V					"	"	"		"				"	
		154	IN	"					OUT	"		5.0V					"	"	"		"				"	

See footnotes on next page.

TABLE III. Group A inspection for device type 55 – Continued.

- 1/ Terminals not designated may be “HIGH” level logic, “LOW” level logic, or open except as follows: $V_{IC(POS)}$ tests; the V_{SS} terminal shall be open. $V_{IC(NEG)}$ tests; the V_{DD} terminal shall be open. I_{SS} test, the output terminal shall be open.
- 2/ The I_{SS} tests shall be performed in sequence.
- 3/ Apply a single clock pulse; $V_{IN} = 0$ V dc to V_{DD} .
- 4/ Apply clock pulse: $V_{IN} = 0$ V dc to V_{DD} , until proper output state is achieved.
- 5/ V_{IH} and V_{IL} tests are performed by repeating the truth table tests (numbers 115 through 135) using the input and output conditions follows:

Test	V_{DD}	Input		Output	
		H	L	H	L
V_{IH1} V_{IL1}	5.0V	3.5V	1.5V	4.5V min	0.5V max
V_{IH2} V_{IL2}	10.0V	7.0V	3.0V	9.0V min	1.0V max
V_{IH3} V_{IL3}	15.0V	11.0V	4.0V	13.5V min	1.5V max

- 6/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at °C for each individual input or measure all inputs together.
- 7/ See 4.4.1c.
- 8/ Test numbers 115 through 135 shall be run in sequence.
- 9/ For all test conditions, delayed clock (C_{LD}) is clock delayed by two inverters.

- 10/ The output voltage limits for each temperature are “H” = $V_{DD} - 0.5$ V min and “L” = $V_{SS} + 0.5$ V max.
- 11/ The functional test shall be performed at V_{IH} and $V_{DD} \leq 5.0$ V dc and ≥ 18.0 V dc.
- 12/ Apply 59 clock pulses: $V_{IN} = 0$ V dc to V_{DD} , $t_p = 500$ ns (min) and $t_{TLH} = t_{THL} = 10$ ns $\pm 10\%$.
- 13/ The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.

TABLE III. Group A inspection for device type 56.

Symbol	MIL-STD-883 method	Cases J,K,U	Terminal conditions and limits 1/																								Measured terminal	Test limits						Unit							
		Symbol	B8	B7	B6	B5	B4	B3	B2	B1	AE	Serial In	A/B	V _{SS}	P/S	A/S	Clock	A1	A2	A3	A4	A5	A6	A7	A8	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C									
		Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		Min	Max	Min	Max	Min	max								
V _{IC} (POS)	2/	1								1mA	1mA	1mA														5.0V	AE	1.5					V								
		2																									Ser In												"		
		3																									A/B												"		
		4																									P/S												"		
		5																									A/S												"		
		6																									Clock												"		
V _{IC} (NEG)		7								-1mA	-1mA	-1mA	GND														AE	-6													
	8																									Ser In													"		
	9																									A/B													"		
	10																									P/S													"		
	11																									A/S													"		
	12																									Clock													"		
I _{SS} 3-	3005	13									18.0V	18.0V	18.0V		18.0V	18.0V	GND	GND	18.0V	GND	18.0V	GND	18.0V	GND	18.0V	18.0V	V _{SS}		-1.0		-5.0			μA							
	14										"	"	"	18.0V	18.0V	18.0V	18.0V	18.0V	GND	18.0V	GND	18.0V	GND	18.0V	GND	V _{SS}														"	
	15										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	None														"	
	16										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	V _{SS}														"	
	17										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	V _{SS}														"	
	18										GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	None														"	
	19										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	V _{SS}														"	
	20										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	V _{SS}														"	
	21										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	None														"	
	22	18.0V	GND	18.0V	GND	18.0V	GND	18.0V	GND	18.0V	18.0V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	V _{SS}														"	
	23	18.0V	GND	18.0V	GND	18.0V	GND	18.0V	GND	18.0V	18.0V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	V _{SS}							"								
V _{OH3}	3006	24									15.0V		15.0V		15.0V		4/									15.0V	B1	14.95		14.95		14.95	V								
	25										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B2								"						
	26										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B3								"							
	27										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B4								"						
	28										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B5								"						
	29										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B6								"						
	30										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B7								"						
	31										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B8								"						
	32										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A1								"						
	33										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A2								"						
	34										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A3								"						
	35										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A4								"						
	36										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A5								"						
	37										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A6								"						
	38										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A7								"						
	39										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A8								"						
	40										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A1								"						
V _{OL3}	3007	41									15.0V		15.0V		15.0V												B1	.05		.05		.05									
	42										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B2														"
	43										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B3														"
	44										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B4														"
	45										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B5														"
	46										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B6														"
	47										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B7														"
	48										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B8														"
	49										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A1														"
	50										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A2														"
	51										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A3														"
	52										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A4														"
	53										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A5														"
	54										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A6														"
	55										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A7														"
	56										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A8														"
	57										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A1														"

See footnotes at end of device type 56.

TABLE III. Group A inspection for device type 56 – Continued.

Symbol	MIL-STD-883 method	Cases J,K,U	Terminal conditions and limits 1/																								Measured terminal	Test limits						Unit			
		Symbol	B8	B7	B6	B5	B4	B3	B2	B1	AE	Serial In	A/B	V _{SS}	P/S	A/S	Clock	A1	A2	A3	A4	A5	A6	A7	A8	V _{DD}		Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C					
		Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		Min	Max	Min	Max	Min	max				
V _{IH1}		58	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	GND	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	All outputs	5/	5/	5/	5/	5/	5/	5/				
V _{IH1}		59	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/				
V _{IH3}		60	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/				
V _{IL1}		61	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/				
V _{IL2}		62	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/				
V _{IL3}		63	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/				
I _{OL1}	64	65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V	5.0V		5.0V	5.0V	GND	4/	GND	GND	GND	GND	GND	GND	GND	GND	5.0V	B1 B2 B3 B4 B5 B6 B7 B8 A1 A2 A3 A4 A5 A6 A7 A8 A1	0.51	0.36	0.64		mA						
I _{OL2}		81	82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97	1.5V	1.5V	1.5V	1.5V	1.5V	1.5V	1.5V	15.0V		15.0V	15.0V			GND	GND	GND	GND	GND	GND	GND	15.0V	B1 B2 B3 B4 B5 B6 B7 B8 A1 A2 A3 A4 A5 A6 A7 A8 A1	3.4	2.4	4.2									
I _{OH1}			98	99 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114	4.6V	4.6V	4.6V	4.6V	4.6V	4.6V	4.6V	5.0V		5.0V	5.0V			5.0V	5.0V	5.0V	5.0V	5.0V	5.0V	5.0V	5.0V	5.0V	B1 B2 B3 B4 B5 B6 B7 B8 A1 A2 A3 A4 A5 A6 A7 A8 A1	-51		-36							
																										</											

See footnotes at end of device type 56.

TABLE III. Group A inspection for device type 56 – Continued.

Symbol	MIL-STD-883 method	Cases J,K,U	Terminal conditions and limits 1/																								Measured terminal	Test limits						Unit						
			Symbol	B8	B7	B6	B5	B4	B3	B2	B1	AE	Serial In	A/B	V _{SS}	P/S	A/S	Clock	A1	A2	A3	A4	A5	A6	A7	A8		V _{DD}	Subgroup 1 T _C = 25°C		Subgroup 2 T _C = 125°C		Subgroup 3 T _C = -55°C							
				Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22		23	24	Min	Max	Min	Max		Min	max				
I _{OH2}			115									13.5V	15.0V		15.0V	GND	15.0V	GND	4/	15.0V	15.0V	15.0V	15.0V				15.0V	B1	-3.4		-2.4		-4.2	mA						
			116																										B2											
			117																										B3											
			118																										B4											
			119																										B5											
			120																										B6											
			121																										B7											
			122	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	13.5V	B8												
			123																										A1											
			124																										A2											
			125																										A3											
			126																										A4											
			127																										A5											
			128																										A6											
			129																										A7											
			130	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	15.0V	A8												
			131											15.0V			GND			13.5V							13.5V		A1											
I _{IH1} 6-/	3010		132								18.0V	18.0V	18.0V		18.0V	18.0V	18.0V	18.0V	18.0V	18.0V	18.0V	18.0V	18.0V	18.0V	18.0V	All HIGH level inputs together						nA								
			133	18.0V	18.0V	18.0V	18.0V	18.0V	18.0V	18.0V	18.0V	GND	18.0V	GND		18.0V	18.0V	18.0V										14	12											
I _{IH2}			134	18.0V	GND	GND	GND	GND	GND	GND	GND	GND	GND		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	18.0V	B8	1.0		45										
			135	GND	18.0V	GND	GND	GND	GND	GND	GND	GND	GND	GND													B7													
			136	GND	GND	18.0V	GND	GND	GND	GND	GND	GND	GND	GND													B6													
			137																								B5													
			138																								B4													
			139																								B3													
			140																								B2													
			141																								B1													
			142																								AE													
			143																								Serial In													
			144																								A/B													
			145																								P/S													
			146																								A/S													
			147																								Clock													
			148																															A1						
			149																															A2						
			150																															A3						
			151																															A4						
			152																															A5						
			153																															A6						
			154																															A7						
			155																															A8						
I _{IL1} 6-/	3009		156																						GND		All inputs together		-22											
																											B8		-1.0		-45									
I _{IL2}					157																							B7												
					158																													B6						
					159																													B5						
					160																													B4						
					161																													B3						
					162																													B2						
					163																													B1						
					164																													AE						
					165																													Serial In						
					166																													A/B						
					167																													P/S						
					168																																			

See footnotes at end of device type 56.

See footnotes at end of device type 56.

[illegible]

TABLE III. Group A inspection for device type 56 – Continued.

Symbol	MIL-STD-883 method	Cases J,K,U	Terminal conditions and limits 1/																								Measured terminal	Test limits						Unit
		Symbol	B8	B7	B6	B5	B4	B3	B2	B1	AE	Serial In	A/B	V _{SS}	P/S	A/S	Clock	A1	A2	A3	A4	A5	A6	A7	A8	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C		
		Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		Min	Max	Min	Max	Min	max	
t _{PHL1}	3003 Fig. 4	216			OUT	OUT				5.0V			GND	5.0V	GND	IN						IN		IN		5.0V	Clock to B5	13	737	18	980	13	737	ns
		217										5.0V												IN			Clock to B6							
		218	OUT	OUT																							Clock to B7							
		219																						IN	IN			Clock to B8						
t _{PLH1}		220						OUT	OUT								IN	IN	IN	IN						Clock to B1								
		221																									Clock to B2							
		222																									Clock to B3							
		223																									Clock to B4							
		224																									Clock to B5							
		225																									Clock to B6							
		226		OUT																				IN	IN			Clock to B7						
		227	OUT																					IN			Clock to B8							
t _{PHL2}		228						OUT	OUT								IN	IN	IN	IN							Clock to B1							
		229																									Clock to B2							
		230																									Clock to B3							
		231																									Clock to B4							
		232																									Clock to B5							
		233																									Clock to B6							
		234		OUT																				IN	IN			Clock to B7						
		235	OUT																					IN			Clock to B8							
t _{PLH2}		236						IN	IN								OUT	OUT	OUT	OUT							Clock to A1							
		237																									Clock to A2							
		238																									Clock to A3							
		239																									Clock to A4							
		240																									Clock to A5							
		241		IN		IN	IN																				Clock to A6							
		242																									Clock to A7							
		243	IN	IN																				OUT	OUT		Clock to A8							
t _{PHL3}	3003 Fig. 4	244						OUT	OUT	5.0V	IN	5.0V	GND	GND	GND	IN										5.0V	Clock to B1	13	737	18	980	13	737	ns
		245																									Clock to B2							
		246																									Clock to B3							
		247																									Clock to B4							
		248																									Clock to B5							
		249																									Clock to B6							
		250																									Clock to B7							
		251	OUT	OUT																							Clock to B8							
t _{PLH3}		252						OUT	OUT																		Clock to B1							
		253																									Clock to B2							
		254																									Clock to B3							
		255																																

See footnotes at end of device type 56.

TABLE III. Group A inspection for device type 56 – Continued.

Symbol	MIL-STD-883 method	Cases J,K,U	Terminal conditions and limits 1/																								Measured terminal	Test limits						Unit
		Symbol	B8	B7	B6	B5	B4	B3	B2	B1	AE	Serial In	A/B	V _{SS}	P/S	A/S	Clock	A1	A2	A3	A4	A5	A6	A7	A8	V _{DD}		Subgroup 9 T _C = 25°C		Subgroup 10 T _C = 125°C		Subgroup 11 T _C = -55°C		
		Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		Min	Max	Min	Max	Min	max	
t _{THL1}	3004 Fig. 4	276							OUT	5.0V				GND	5.0V	GND	IN	IN								5.0V	B1	10	210	14	280	10	210	ns
		277						OUT	OUT			5.0V							IN							B2								
		278																		IN							B3							
		279																				IN					B4							
		280				OUT																	IN				B5							
		281			OUT	OUT																		IN			B6							
		282		OUT	OUT																			IN	IN		B7							
		283	OUT																					IN			B8							
t _{TLH1}		284							OUT	OUT								IN									B1							
		285																	IN								B2							
		286																		IN							B3							
		287																			IN						B4							
		288				OUT			OUT													IN						B5						
		289			OUT	OUT																	IN					B6						
		290		OUT	OUT																			IN	IN			B7						
		291	OUT																					IN			B8							
t _{THL2}		292							IN	IN								OUT	OUT								A1							
		293																		OUT							A2							
		294							IN												OUT							A3						
		295																				OUT						A4						
		296																					OUT					A5						
		297				IN																		OUT				A6						
		298			IN	IN																			OUT			A7						
		299	IN	IN																					OUT	OUT		A8						
t _{TLH2}		300							IN	IN								OUT	OUT								A1							
		301																		OUT							A2							
		302																			OUT							A3						
		303																				OUT						A4						
		304				IN			IN														OUT					A5						
		305			IN	IN																		OUT				A6						
		306		IN	IN																				OUT			A7						
		307	IN																						OUT	OUT		A8						
f _{CL} (max) 10/	308	309									IN			GND			OUT	OUT									Clock						μs	
		310																	OUT															
		311																			OUT													
		312																				OUT												
		313																					OUT											
		314																						OUT										
		315																							OUT									
		316																								OUT								
		317																																
		318																																
		319																																
		320				OUT																												
		321			OUT	OUT																												
		322		OUT	OUT																													
		323	OUT																															

See footnotes on next page.

TABLE III. Group A inspection for device type 56 – Continued.

- 1/ Pins not designated may be "HIGH" level logic, "LOW" level logic, or open. Exceptions are as follows: $V_{IC(POS)}$ tests, the V_{SS} terminal shall be open; $V_{IC(NEG)}$ tests, the V_{DD} terminal shall be open; I_{SS} tests, the output terminals shall be open; I_{IH1} tests, the undesignated terminals shall be open.
- 2/ In device type 56, circuit B, all terminals except 12 and 14, are inputs connected to gate structures; therefore, the table III, $V_{IC(POS)}$ and $V_{IC(NEG)}$ tests shall be expanded to include testing terminals 1 through 8 and 16 through 23.
- 3/ The I_{SS} test measurements shall be performed in sequence.
- 4/ Apply clock pulse $V_{IN} = 0$ V dc to V_{DD} until proper output state is achieved.
- 5/ V_{IH} and V_{IL} tests are performed by repeating the truth table tests (numbers 185 through 211) using the input and output conditions as follows:

Test	V_{DD}	Input		Output	
		H	L	H	L
V_{IH1} V_{IL1}	5.0V	3.5V	1.5V	4.5V min	0.5V max
V_{IH2} V_{IL2}	10.0V	7.0V	3.0V	9.0V min	1.0V max
V_{IH3} V_{IL3}	15.0V	11.0V	4.0V	13.5V min	1.5V max

- 6/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for individual input or measure all inputs together.
- 7/ See 4.4.1c.
- 8/ The truth table tests shall be performed in sequence.
- 9/ The truth table test shall be performed at V_{IH} and $V_{DD} \leq 5$ V dc and ≥ 18 V dc. $L = V_{SS} + 0.50$ V dc maximum and $H = V_{DD} - 0.5$ V dc minimum.
- 10/ The maximum clock frequency (f_{CL}) requirements are considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.7 herein). RHA levels for device classes B and S shall be as specified in MIL-PRF-38535 and 4.5.4 herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Burn-in and life test cool down procedures. When the burn-in and life tests are completed and prior to removal of bias voltages, the devices under test (DUT) shall be cooled to a temperature of $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$; then, electrical parameter end-point measurements shall be performed.

TABLE IV. Delta limits at 25°C .

Parameter 1/	Device types					
	01	02	03	04	05	06
I_{SS}	$\pm 60 \text{ nA}$	$\pm 100 \text{ nA}$	$\pm 100 \text{ nA}$	$\pm 100 \text{ nA}$	$\pm 400 \text{ nA}$	$\pm 100 \text{ nA}$
V_{OL1}	$\pm 0.04 \text{ V}$	$\pm 0.04 \text{ V}$	$\pm 0.04 \text{ V}$	$\pm 0.04 \text{ V}$	$\pm 0.04 \text{ V}$	$\pm 0.04 \text{ V}$
V_{OH1}	$\pm 0.08 \text{ V}$	$\pm 0.08 \text{ V}$	$\pm 0.08 \text{ V}$	$\pm 0.08 \text{ V}$	$\pm 0.08 \text{ V}$	$\pm 0.08 \text{ V}$

Parameter 1/	Device types					
	51	52	53	54	55	56
I_{SS}	$\pm 60 \text{ nA}$	$\pm 100 \text{ nA}$	$\pm 100 \text{ nA}$	$\pm 100 \text{ nA}$	$\pm 400 \text{ nA}$	$\pm 100 \text{ nA}$
I_{OL1}	$\pm 15\%$	$\pm 15\%$	$\pm 15\%$	$\pm 15\%$	$\pm 15\%$	$\pm 15\%$
I_{OH1}	$\pm 15\%$	$\pm 15\%$	$\pm 15\%$	$\pm 15\%$	$\pm 15\%$	$\pm 15\%$

1/ Each of the above parameters shall be recorded before and after the required burn-in and life tests to determine delta (Δ).

4.5.3 Quiescent supply current (I_{SS} test). When performing quiescent supply current measurements (I_{SS}), the meter shall be placed so that all currents flow through the meter.

4.5.4 Radiation hardness assurance (RHA) testing. The RHA testing shall be performed in accordance with test procedures and sampling specified in MIL-PRF-38535 and herein.

- Before irradiation, selected samples shall be assembled in qualified packages and pass the governing electrical parameters (group A subgroup 1 at 25°C) and also be subjected to the threshold-voltage test in table VII in order to calculate the delta threshold (ΔV_T) after irradiation.
- The devices shall be subjected to a total radiation dose as specified in MIL-PRF-38535 for the radiation hardness assurance level being tested, and meet the end-point electrical parameters as defined in table V at 25°C , after exposure. The start and completion of the end-point electrical parameter measurements shall not exceed 2 hours following irradiation.
- Threshold-voltage test circuit conditions shall be as specified in table VII and on figure 5. In situ and remote testing, the tests shall be performed with the devices biased in accordance with table VI and the bias may be interrupted for up to 1 minute to remove devices to the remote bias fixture.
- After irradiation, the devices shall pass the truth table test as specified in subgroup 7 in table III or if subgroup 7 is not required, then an equivalent truth table test shall be performed.

TABLE V. Radiation hardened end-point electrical parameters at 25°C.

Parameter	Test limits (All device types)	V_{DD}	
		Device types	
		01-06	51-56
V_{TN}	0.3 V min	10 V	10 V
V_{TP}	2.8 V max	10 V	10 V
ΔV_T	1.4 V max	10 V	10 V
I_{SS}	100 x max limit	15 V	18 V
t_{PLH}	1.35 x max limit	5 V	5 V
t_{PHL}	1.35 x max limit	5 V	5 V

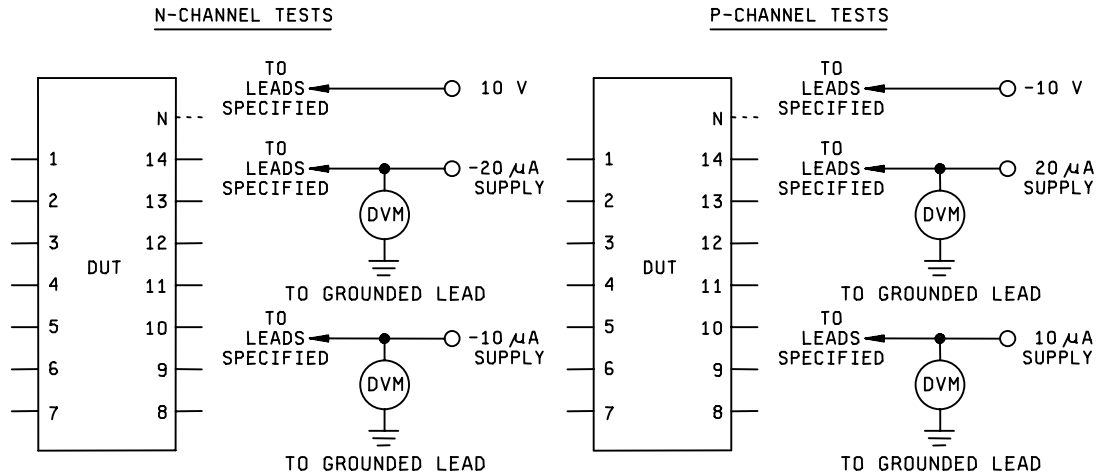
TABLE VI. Bias during exposure to radiation.

Device type	Pin connections ^{1/}		
	$V_{DD} = 10$ V dc (through a 30 k Ω to 60 k Ω resistor)	$V_{SS} = \text{GND}$	$V_{DD} = 10$ V dc
01, 51	1, 3, 4, 5, 6	7	14
02, 52	1, 4, 5, 6, 7, 9, 10, 11, 13, 14, 15	8	16
03, 53	1, 6, 7, 9, 14, 15	8	16
04, 54	1, 4, 5, 6, 7, 9, 10, 11, 13, 14, 15	8	16
05, 55	1, 2, 10, 15	8	16
06, 56	9, 10, 11, 13, 14, 15	12	24

^{1/} Pins not designated are open or tied to 10 V dc through a 30 k Ω to 60 k Ω resistor.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements are as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

FIGURE 5. Threshold-voltage test circuit.TABLE VII. Threshold-voltage test circuit conditions.

Device	GND	10 V	V _{TN} measured at		GND	-10 V	V _{TP} measured at	
			-20 μ A supply	-10 μ A supply			20 μ A supply	10 μ A supply
01, 51	3	14	1, 4, 5, 6, 7		3	1, 4, 5, 6, 7	14	
02, 52	10	16	1, 4, 5, 6, 7, 8, 9, 11, 13, 14, 15		10	1, 4, 5, 6, 7, 8, 9, 11, 13, 14, 15	16	
03, 53	1	16	6, 7, 8, 9, 14, 15		1	6, 7, 8, 9, 14, 15	16	
04, 54	10	16	1, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15		10	1, 4, 5, 6, 7, 8, 9, 11, 13, 14, 15	16	
05, 55	2	1, 10, 15, 16	8		2	1, 8, 10, 15	16	
06, 56	10	9, 11, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24		12	10	1, 2, 3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15		24

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of the specification.
- b. PIN and compliance identifier, if applicable (see 1.2).
- c. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirements for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- g. Requirements for product assurance and radiation hardness assurance options.
- h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- i. Requirements for "JAN" marking.
- j. Packaging requirements. (see 5.1)

6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractors parts lists.

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, P.O. Box 3990, Columbus, Ohio 43218-3990.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

C_I	Input terminal-to-GND capacitance.
GND	Ground zero voltage potential.
T_A	Free air temperature.
$V_{IC(pos)}$	Positive clamping input to V_{DD} .
$V_{IC(neg)}$	Negative clamping input to V_{SS} .
V_{DD}	Positive supply voltage.
V_{SS}	Negative supply voltage.
I_{SS}	Quiescent supply current.

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class S for National Aeronautics and Space Administration or class B for Department of Defense (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

6.7 Data reporting. When specified in the purchase order or contract, a copy of the following data, as applicable, will be supplied.

- a. Attributes data for all screening tests (see 4.2) and variables data for all static burn-in, dynamic burn-in, and steady-state life tests (see 3.6).
- b. A copy of each radiograph.
- c. The technology conformance inspection (TCI) data (see 4.4).
- d. Parameter distribution data on parameters evaluated during burn-in (see 3.6).
- e. Final electrical parameters data (see 4.2d).
- f. RHA delta limits.

6.8 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges, post irradiation performance or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type
01	4006A
02	4014A
03	4015A
04	4021A
05	4031A
06	4034A
51	4006B
52	4014B
53	4015B
54	4021B
55	4031B
56	4034B

6.9 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extent of the changes.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 11
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5962-2080)

Review activities:
 Army - MI, SM
 Navy - AS, CG, MC, SH, TD
 Air Force - 03, 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using ASSIST Online database at <http://assist.daps.dla.mil>.