

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, N-CHANNEL, SILICON GATE MONOLITHIC 16-BIT MICROPROCESSOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic N-channel, silicon gate microprocessor. Two product assurance classes and a choice of case outline/lead finish are provided for each type, and are reflected in the complete Part or Identifying Number (PIN).

1.2 PIN. The PIN shall be in accordance with MIL-M-38510.

1.2.1 Device types. The device types shall be as follows:

<u>Device type</u>	<u>Clock frequency</u>	<u>Circuit</u>
01	4 to 6.0 MHz	16-bit, fixed instruction microprocessor
02	4 to 8.0 MHz	16-bit, fixed instruction microprocessor
03	4 to 10.0 MHz	16-bit, fixed instruction microprocessor

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

<u>Letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
T	See figure 1, (68-pin, 1.080" x 1.080" x .345"), pin grid array
Y	D-13 (64-lead, 3.240" x .920" x .225"), dual-in-line package
Z	C-7 (68-terminal, .962" x .962" x .120"), leadless chip carrier package

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC} - GND) - - - - -	-0.3 V dc to +7.0 V dc
Voltage on any pin (referenced to ground) -	-0.3 V dc to +7.0 V dc
Storage temperature range - - - - -	-65°C to +150°C
Maximum power dissipation (P_D) at maximum clock frequency - - - - -	1.68 W
Lead temperature (soldering, 5 seconds) - -	+270°C
Maximum junction temperature (T_J) 1/ - - -	+150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case T - - - - -	15°C/W 2/
Cases Y and Z - - - - -	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage range - - - - -	4.75 V dc minimum to 5.25 V dc maximum
Minimum high level input voltage (V_{IH}):	
Logic inputs - - - - -	2.0 V dc
Maximum low level input voltage (V_{IL}):	
Logic inputs - - - - -	0.8 V dc
Frequency of operation:	
Device type 01 - - - - -	4.0 to 6.0 MHz
Device type 02 - - - - -	4.0 to 8.0 MHz
Device type 03 - - - - -	4.0 to 10.0 MHz
Case operating temperature range (T_C) - - -	-55°C to +110°C
Clock rise time (t_r) - - - - -	10 ns maximum
Clock fall time (t_f) - - - - -	10 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications, specification sheets, or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

- 1/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
- 2/ When a thermal resistance value is included in MIL-M-38510, appendix C, it shall supersede the value stated herein.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Functional block diagram and input and output signals. The functional block diagram and input and output signals shall be as specified on figure 3.

3.2.3 Register organization, terminal and pin definitions. Register organization and terminal and pin definitions shall be as specified in 6.5 (and figure 11) and 6.6 respectively.

3.2.4 Microprocessor instructions. Microprocessor instructions shall be as specified in table VI.

3.2.5 Case outlines. The case outlines shall be as specified in 1.2.3 and figure 1.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.7).

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and figures 5, 6, 7, and 8 and apply over the full recommended operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be as specified in table II. The electrical tests for each subgroup are described in tables III, IV, and V and figures 5, 6, 7, and 8.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 107 (see MIL-M-38510, appendix E).

3.8 Schematic circuits. Submission of schematic circuits to the qualifying activity is not required.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $T_C = -55^\circ\text{C}$ to $+110^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 5\%$ unless otherwise specified	Device type	Refer- ence number 1/	Limits		Unit
					Min	Max	
Low level output voltage A23-1, FCO-2, BG, E	V_{OL}	$I_{OL} = 3.2\text{ mA}$ $V_{CC} = 4.75\text{ V}$	A11			0.5	V
Low level output voltage HALT	V_{OL}	$V_{CC} = 4.75\text{ V}$ $I_{OL} = 1.6\text{ mA}$	A11			0.5	V
Low level output voltage AS, R/W, D15-0, UDS, LDS, VMA,	V_{OL}	$I_{OL} = 5.3\text{ mA}$ $V_{CC} = 4.75\text{ V}$	A11			0.5	V
Low level output voltage RESET	V_{OL}	$V_{CC} = 4.75\text{ V}$ $I_{OL} = 5.0\text{ mA}$	A11			0.5	V
High level output voltage	V_{OH}	$I_{OH} = -400\text{ }\mu\text{A}$	A11		2.4		V
High level input current (all inputs)	I_{IH}	$V_{IN} = 2.4\text{ V}$	A11			2.5	μA
Low level input current (all inputs)	I_{IL}	$V_{IN} = 0.0\text{ V}$	A11		-2.5		μA
High level input current HALT/RESET	I_{IH}	$V_{IN} = 2.4\text{ V}$	A11			20	μA
Low level input current HALT/RESET	I_{IL}	$V_{IN} = 0.4\text{ V}$	A11		-20		μA
Three-state output high leakage (all outputs)	I_{OHZ}	$V_{OUT} = 2.4\text{ V}$	A11			20	μA
Three-state output low leakage (all outputs)	I_{OLZ}	$V_{OUT} = 0.4\text{ V}$	A11		-20		μA
Supply current	I_{CC}	$V_{CC} = 5.25\text{ V}$	A11			320	mA
Input capacitance (all inputs)	C_I	$T_C = 25^\circ\text{C}$, $V_{CC} = \text{GND}$ $f = 1\text{ MHz}$	A11			20	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $T_C = -55^\circ\text{C}$ to $+110^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 5\%$ unless otherwise specified	Device type	Refer- ence number 1/	Limits		Unit
					Min	Max	
DIN to CLK low (t_{SET})	t_{DICL}	$V_{IH} = 2.4\text{ V}$ $V_{IL} = 0.8\text{ V}$ Freq = 4.0 MHz min $C_L = 130\text{ pF} \pm 10\%$ 3/	01 02 03	47	25 15 15		ns
DIN to CLK low (t_{HOLD}) 2/	t_{HDICL}		01 02 03	47	25 20 20		ns
$\overline{DTACK}$ to CLK low (t_{SET})	t_{SDTCL}		01 02 03	47	25 20 20		ns
$\overline{BR}$ to CLK low (t_{SET})	t_{SBRCL}		01 02 03	47	25 20 20		ns
$\overline{VPA}$ to CLK low (t_{SET})	$t_{SVPA CL}$		01 02 03	47	25 20 20		ns
$\overline{BERR}$ to CLK low (t_{SET})	t_{SPERCL}		01 02 03	47	25 20 20		ns
Clock period	t_{CYC}		01 02 03	1	167 125 100	250 250 250	ns
CLK width low	t_{CL}		01 02 03	2	75 55 45	125 125 125	ns
CLK width high	t_{CH}		01 02 03	3	75 55 45	125 125 125	ns
CLK high to FC valid	t_{CHFCV}		01 02 03	6A		80 70 60	ns
CLK high to $\overline{AS}$, $\overline{DS}$ low, max	t_{CHSLX}		01 02 03	9		60 60 55	ns
CLK high to $\overline{AS}$, $\overline{DS}$ low, min 4/	t_{CHSLN}		A11	10	0		ns
CLK low to $\overline{AS}$ high	t_{CLSH}		01 02 03	12		80 70 55	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $T_C = -55^\circ\text{C}$ to $+110^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 5\%$ unless otherwise specified	Device type	Refer- ence number 1/	Limits		Unit
					Min	Max	
CLK low to $\overline{DS}$ high	t_{CLSH}	$V_{IH} = 2.4\text{ V}$ $V_{IL} = 0.8\text{ V}$ $\text{Freq} = 4.0\text{ MHz min}$ $C_L = 130\text{ pF} \pm 10\%$ <u>3/</u>	01 02 03	12		80 70 55	ns
CLK high to R/W high, max	t_{CHRHX}		01 02 03	18		80 70 60	ns
CLK high to R/W high, min <u>4/</u>	t_{CHRHN}		A11	19	0		ns
CLK high to R/W low	t_{CHRL}		01 02 03	20		80 70 60	ns
CLK low to DOUT valid	t_{CLDO}		01 02 03	23		80 70 55	ns
CLK low to address valid	t_{CLAV}		01 02 03	6		80 70 60	ns
CLK high to $\overline{BG}$ low	t_{CHGL}		01 02 03	33		80 70 60	ns
CLK high to $\overline{BG}$ high	t_{CHGH}		01 02 03	34		80 70 60	ns
CLK low to $\overline{VMA}$ low	t_{CLVML}		01 02 03	40		80 70 70	ns
CLK low to E transition	t_{CLE}		01 02 03	41		85 70 55	ns
CLK high to address data three-state, max <u>4/</u>	t_{CHAZX}		01 02 03	7		100 80 70	ns
CLK high to address/FC invalid, min <u>4/</u>	t_{CHAZN}		A11	8	0		ns
CLK high to $\overline{AS}$, $\overline{DS}$, three-state <u>4/</u>	t_{CHSZ}		01 02 03	16		100 80 70	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $T_C = -55^\circ\text{C to } +110^\circ\text{C}$ $V_{CC} = 5.0\text{ V } \pm 5\%$ unless otherwise specified	Device type	Refer- ence number 1/	Limits		Unit
					Min	Max	
CLK high to R/W $\overline{VMA}$ three-state 4/ 5/	t_{CHZ}	$V_{IH} = 2.4\text{ V}$ $V_{IL} = 0.8\text{ V}$ Freq = 4.0 MHz min $C_L = 130\text{ pF } \pm 10\%$ 3/	01 02 03	24		100 80 70	ns
Address to $\overline{AS}$, $\overline{DS}$ (read) low/ $\overline{AS}$ write 4/	t_{AVSL}		01 02 03	11	35 30 20		ns
FC valid to $\overline{AS}$, $\overline{DS}$ (read) low/ $\overline{AS}$ write 4/	t_{FCVSL}		01 02 03	11A	70 60 50		ns
$\overline{AS}$, $\overline{DS}$, high to address/ FC invalid 4/	t_{SHAZ}		01 02 03	13	40 30 20		ns
$\overline{AS}$, $\overline{DS}$, width low (read) $\overline{AS}$ write 4/	t_{SL}		01 02 03	14	337 240 195		ns
$\overline{DS}$ width low (write) 4/	t_{DSL}		01 02 03	14A	170 115 95		ns
$\overline{AS}$, $\overline{DS}$ width high 4/	t_{SH}		01 02 03	15	180 150 105		ns
$\overline{AS}$ high to R/W high 4/	t_{SHRH}		01 02 03	17	50 40 20		ns
Address valid to R/W low 4/	t_{AVRL}		01 02 03	21	25 20 0		ns
R/W low to $\overline{DS}$ low (write) 4/	t_{RLSL}		01 02 03	22	140 80 50		ns
$\overline{DS}$ high to D_{OUT} invalid 4/	t_{SHDO}		01 02 03	25	40 30 20		ns
$\overline{AS}$, $\overline{DS}$ high to $\overline{DTACK}$ high 4/	t_{SHDAH}		01 02 03	28	0 0 0	325 245 190	ns
$\overline{DS}$ to data invalid (holdtime) 4/	t_{SHDI}		A11	29	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $T_C = -55^\circ\text{C}$ to $+110^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 5\%$ unless otherwise specified	Device type	Refer- ence number <u>1/</u>	Limits		Unit
					Min	Max	
$\overline{AS}$, $\overline{DS}$ high to $\overline{BERR}$ high <u>4/</u>	t_{SHBEH}	$V_{IH} = 2.4\text{ V}$ $V_{IL} = 0.8\text{ V}$ Freq = 4.0 MHz min $C_L = 130\text{ pF} \pm 10\%$	A11	30	0		ns
$\overline{DTACK}$ low to data in (setup time) <u>4/</u>	t_{DALDI}	<u>3/</u>	01 02 03	31		120 90 65	ns
$\overline{HALT}$ and $\overline{RESET}$ input transition time <u>4/</u>	t_{RHRF}		A11	32	0	200	ns
$\overline{BR}$ low to $\overline{BG}$ low <u>4/</u>	t_{BRLGL}		01 02 03	35	1.5	3.5 +100 ns	CLKS
$\overline{BR}$ high to $\overline{BG}$ high <u>1/ 4/</u>	t_{BRHGH}		01 02 03	36	1.5	3.0 +100 ns	CLKS
$\overline{BGACK}$ low to $\overline{BG}$ high <u>4/</u>	t_{GALGH}		01 02 03	37	1.5	3.0 +100 ns	CLKS
$\overline{BG}$ low to bus three-state w/ $\overline{AS}$ high <u>4/</u>	t_{GLZ}		01 02 03	38		100 80 70	ns
$\overline{BG}$ width high <u>4/</u>	t_{GH}		A11	39	1.5		CLKS
E output rise and fall time <u>4/</u>	t_{ERF}		A11	42		25	ns
$\overline{VMA}$ low to E high <u>4/</u>	t_{VMLEH}		01 02 03	43	240 200 150		ns
$\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high <u>4/</u>	t_{SHVPH}		01 02 03	44	0 0 0	160 120 90	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $T_C = -55^\circ\text{C}$ to $+110^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 5\%$ unless otherwise specified	Device type	Refer- ence number 1/	Limits		Unit
					Min	Max	
E low to address $\overline{VWA}/FC$ invalid 4/	t_{ELAI}	$V_{IH} = 2.4\text{ V}$ $V_{IL} = 0.8\text{ V}$ Freq = 4.0 MHz min $C_L = 130\text{ pF} \pm 10\%$	01 02 03	45	35 30 10		ns
$\overline{BGACK}$ width 4/	t_{BGL}	3/	A11	46	1.5		CLKS
$\overline{BERR}$ low to $\overline{DTACK}$ low 4/	t_{BELDAL}		01 02 03	48	25 20 20		ns
E low to $\overline{AS}$, $\overline{DS}$ invalid 4/	t_{ELSI}		01 02 03	49	-80 -70 -55	+80 +70 +55	ns
E width high 4/	t_{EH}		01 02 03	50	600 450 350		ns
E width low 4/	t_{EL}		01 02 03	51	900 700 550		ns
E extended rise time 4/	t_{CIEHX}		A11	52	80		ns
Data hold from clock high 4/	t_{CHDO}		A11	53	0		ns
Data hold from E low (write) 4/	t_{ELDOZ}		01 02 03	54	35 30 20		ns
$R/\overline{W}$ to data bus impedance change 4/	t_{RLDO}		01 02 03	55	35 30 20		ns
HALT/ ~~RESET~~ pulse width 4/ 6/	t_{HRPW}		A11	56	10		clk. per.

1/ The reference number refers to the position where the parameter being tested appears on figures 5, 6, 7 and 8.

2/ Not tested, user information only.

3/ Figures 5, 6, 7 and 8 represent the electrical performance characteristics associated with the ac limits shown in table I.

4/ Tested initially and at process or design changes.

5/ Combined with t_{CHSZ} (16), control bus specification.

6/ After V_{CC} has been applied for 100 ms.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	2,8(+110°C),10	2,8(+110°C),10
Final electrical test parameters (method 5004)	*1,*2,3, 8(+110°C),10,11	*1,*2,3 8(+110°C),10,11
Group A test requirements (method 5005)	2,**4,8(+110°C), 10,11	2,**4,8(+110°C), 10,11
Group C end-point electrical parameters (method 5005)	2,4,8(+110°C),10	2,8(+110°C),10
Group D end-point electrical parameters (method 5005)	2,4,8(+110°C),10	2,8(+110°C),10
Additional electrical tests for group C inspection	None	None

* PDA may apply to subgroup 1 or subgroup 2 with approval of qualifying activity (see 4.2c).

** Subgroup 4 shall be performed once upon qualification or device redesign which effects input capacitance. Select 5 samples at random and measure inputs of D3, BERR, DTACK, IPLD, and BR of each sample.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, as applicable, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) $T_A = +125^\circ\text{C}$ minimum.

(2) Test condition D or E using the burn-in circuit and timing waveforms as specified on figure 4.

b. Constant acceleration in accordance with test condition D of method 2001 of MIL-STD-883.

c. Percent defective allowable (PDA) - The PDA shall be in accordance with MIL-M-38510.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3.1 Qualification extention. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies a device type, then the slower device types of the same type (see MIL-M-38510, 3.1.3.21) may be part I qualified, upon request of the manufacturer, without additional testing.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and acceptance values as follows:

- a. Tests shall be as specified in table II.
- b. Subgroups 3, 5, 6, 7, and 9 of table I of method 5005 of MIL-STD-883 shall be omitted.

<u>Subgroups</u>	<u>Minimum sample (accept number)</u>
4	(See table II)
1, 2	32(0)
10, 11	22(0)
Subgroup 8 is encompassed in subgroups 10 and 11.	

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and acceptance values shown in table II of method 5005 of MIL-STD-883.

- a. A special subgroup shall be added using a minimum sample size of 15 with zero failures for class B. This subgroup shall consist of a high-voltage test of the input protection circuits, V_{ZAP} (see 4.5.2). This subgroup shall be done for initial design qualification and process or design changes which may affect input protection circuit sensitivity.
- b. Subgroup 3 (solderability) shall be omitted for devices in package Z. At the option of the manufacturer, the following alternate test method for subgroup 3 (solderability) shall be bath temperature = $+245^{\circ}\text{C} \pm 5^{\circ}\text{C}$ dwell times 5 seconds ± 5 seconds, R or RMA flux and steam aged for 1 hour for devices in Z package only.

4.4.3 Groups C and D inspections. Groups C and D inspections shall consist of the test subgroups and acceptance values shown in tables III and IV of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II.
- b. Steady-state life test (method 1005 of MIL-STD-883).
 - (1) Use life test condition D using the circuit and timing as shown on figure 4.
 - (2) $T_A = +125^{\circ}\text{C}$.

4.4.4 Constant acceleration. The constant acceleration tests of groups C and D shall be performed using test condition D.

4.4.5 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

TABLE III. Group A inspection for device types 01, 02, and 03. Terminal conditions (pins not designated are open)

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
				A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	VCC	A21	A22
1																		5.25 V		
2	$I_{CC} \downarrow$	3005	1															5.25 V		
	$V_{OL} \downarrow$	3007	2															4.75 V		
			3																	
			4																	
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			57																	
			58																	
			59																	
	$V_{OH} \downarrow$	3006	53																	
			54																	
			55																	
			56																	
			57																	
			58																	
			59																	

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	52	53	54	55	56	57	58	59	60	61	62	63	64	Measured terminal	Test limit		Unit
				A23	GND	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5		Min	Max	
1																		See table IIIA		
2	$I_{CC} \downarrow$	3005	1		GND												V _{CC}			mA
	$V_{OL} \downarrow$	3007	2		"												D4	0.5		V
			3		"												D3			
			4		"												D2			
			5		"												D1			
			6		"												D0			
			7		"		5.3 mA										D15			
			8		"			5.3 mA									D14			
			9		"												D13			
			10		"												D12			
			11		"												D11			
			12		"			5.3 mA									D10			
			13		"				5.3 mA								D9			
			14		"												D8			
			15		"												D7			
			16		"												D6			
			17		"												D5			
			18		"												A1			
			19		"												A2			
			20		"												A3			
			21		"												A4			
			22		"												A5			
			23		"												A6			
			24		"												A7			
			25		"												A8			
			26		"												A9			
			27		"												A10			
			28		"												A11			
			29		"												A12			
			30		"												A13			
			31		"												A14			
			32		"												A15			
			33		"												A16			
			34		"												A17			
			35		"												A18			
			36		"												A19			
			37		"												A20			
			38		"												A21			
			39		"												A22			
			40	3.2 mA	"												A23			
			41		"												FC2			
			42		"												FC1			
			43		"												FC0			
			44		"												AS			
			45		"												UDS			
			46		"												LDS			
			47		"												R/W			
			48		"												BG			
			49		"												VWA			
			50		"												E			
			51		"												HALT			
			52		"												RESET			
	$V_{OH} \downarrow$	3006	53		"												D4	2.4		V
			54		"												D3			
			55		"												D2			
			56		"												D1			
			57		"												D0			
			58		"	-400 μ A											D15			
			59		"		-400 μ A										D14			

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
				D4	D3	D2	D1	D0	X5	UDS	UDS	R/W	DTACK	BG	BGACK	BR	VCC	CLK	GND	HALT
$T_C = +110^\circ\text{C}$	VOH 1/	3006	60										2.4 V		2.4 V	2.4 V	4.75 V	2/	GND	0.8 V
			61										"		"	"	"	"	"	"
			62										"		"	"	"	"	"	"
			63										"		"	"	"	"	"	"
			64										"		"	"	"	"	"	"
			65										"		"	"	"	"	"	"
			66										"		"	"	"	"	"	"
			67										"		"	"	"	"	"	"
			68										"		"	"	"	"	"	"
			69										"		"	"	"	"	"	"
			70										"		"	"	"	"	"	"
			71										"		"	"	"	"	"	"
			72										"		"	"	"	"	"	"
			73										"		"	"	"	"	"	"
			74										"		"	"	"	"	"	"
			75										"		"	"	"	"	"	"
			76										"		"	"	"	"	"	"
			77										"		"	"	"	"	"	"
			78										"		"	"	"	"	"	"
			79										"		"	"	"	"	"	"
			80										"		"	"	"	"	"	"
			81										"		"	"	"	"	"	"
			82										"		"	"	"	"	"	"
			83										"		"	"	"	"	"	"
			84										"		"	"	"	"	"	"
			85										"		"	"	"	"	"	"
			86										"		"	"	"	"	"	"
			87										"		"	"	"	"	"	"
			88										"		"	"	"	"	"	"
			89										"		"	"	"	"	"	"
			90										"		"	"	"	"	"	"
			91										"		"	"	"	"	"	"
			92										"		"	"	"	"	"	"
			93										"		"	"	"	"	"	"
			94										"		"	"	"	"	"	"
			95										"		"	"	"	"	"	"
			96										"		"	"	"	"	"	"
			97										"		"	"	"	"	"	"
			98										"		"	"	"	"	"	"
			99										"		"	"	"	"	"	"
			100										"		"	"	"	"	"	"
			101										"		"	"	"	"	"	"
	I _{IH}	3010	102														5.25 V			
			103														2.4 V			
			104														2.4 V			
			105																	
			106																	
			107																	
			108																	
			109																	
			110																	
			111																	2.4 V
	I _{IL}	3009	112																	
			113																	
			114																	
			115																	
			116																	
			117																	
			118																	
			119																	
			120																	
			121																	0.4 V

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
				RST	WMA	E	VPA	BERR	IPL2	IPL1	IPL0	FC2	FC1	FC0	A1	A2	A3	A4	A5	A6
2 $T_C = +110^\circ\text{C}$	$V_{OH} \downarrow$	3006	60	0.8 V			2.4 V	2.4 V	2.4 V	2.4 V	2.4 V									
			61	"			"	"	"	"	"									
			62	"			"	"	"	"	"									
			63	"			"	"	"	"	"									
			64	"			"	"	"	"	"									
			65	"			"	"	"	"	"									
			66	"			"	"	"	"	"									
			67	"			"	"	"	"	"									
			68	"			"	"	"	"	"									
			69	"			"	"	"	"	"									
			70	"			"	"	"	"	"									
			71	"			"	"	"	"	"									
			72	"			"	"	"	"	"									
			73	"			"	"	"	"	"									
			74	"			"	"	"	"	"									
			75	"			"	"	"	"	"									
			76	"			"	"	"	"	"									
			77	"			"	"	"	"	"									
			78	"			"	"	"	"	"									
			79	"			"	"	"	"	"									
			80	"			"	"	"	"	"									
			81	"			"	"	"	"	"									
			82	"			"	"	"	"	"									
			83	"			"	"	"	"	"									
			84	"			"	"	"	"	"									
			85	"			"	"	"	"	"									
			86	"			"	"	"	"	"									
			87	"			"	"	"	"	"									
			88	"			"	"	"	"	"									
			89	"			"	"	"	"	"									
			90	"			"	"	"	"	"									
			91	"			"	"	"	"	"									
			92	"			"	"	"	"	"									
			93	"			"	"	"	"	"									
			94	"			"	"	"	"	"									
			95	"			"	"	"	"	"									
			96	"			"	"	"	"	"									
			97	"			"	"	"	"	"									
			98	"			"	"	"	"	"									
			99	"			"	"	"	"	"									
			100	"			"	"	"	"	"									
			101	"			"	"	"	"	"									
11H		3010	102																	
			103																	
			104																	
			105																	
			106																	
			107																	
			108																	
			109																	
			110																	
			111	2.4 V			2.4 V		2.4 V	2.4 V	2.4 V									
11L		3009	112																	
			113																	
			114																	
			115																	
			116																	
			117																	
			118																	
			119																	
			120																	
			121	0.4 V																

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroups	Symbol	MIL-STD-883 method	Test no.	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
$T_C = +110^\circ C$	$V_{OH} \frac{1}{2}$	3006	60																	
			61																	
			62																	
			63																	
			64																	
			65																	
			66																	
			67																	
			68																	
			69																	
			70																	
			71																	
			72																	
			73																	
			74																	
			75	-400 μA														14.75 V		
			76	-400 μA																
			77	-400 μA																
			78	-400 μA																
			79	-400 μA																
			80	-400 μA																
			81	-400 μA																
			82	-400 μA																
			83	-400 μA																
			84	-400 μA																
			85	-400 μA																
			86	-400 μA																
			87	-400 μA																
			88	-400 μA																
			89	-400 μA																
			90	-400 μA																
			91	-400 μA																
			92	-400 μA																
			93	-400 μA																
			94	-400 μA																
			95	-400 μA																
			96	-400 μA																
			97	-400 μA																
			98	-400 μA																
			99	-400 μA																
			100	-400 μA																
			101	-400 μA																
I_{IH}	3010		102																	
			103																	
			104																	
			105																	
			106																	
			107																	
			108																	
			109																	
			110																	
			111																	
			112															5.25 V		
I_{IL}	3009		113																	
			114																	
			115																	
			116																	
			117																	
			118																	
			119																	
			120																	
			121																	
			122																	

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	52	53	54	55	56	57	58	59	60	61	62	63	64	Measured terminal	Test limit		Unit
																		Min	Max	
2 $T_C = +110^\circ C$	$V_{OH} \underline{1/}$	3006	60		GND												D13	2.4		V
			61		"			-400 μA									D12			"
			62		"			-400 μA									D11			"
			63		"			-400 μA									D10			"
			64		"			-400 μA									D9			"
			65		"			-400 μA									D8			"
			66		"			-400 μA									D7			"
			67		"			-400 μA									D6			"
			68		"			-400 μA									D5			"
			69		"			-400 μA									A1			"
			70		"			-400 μA									A2			"
			71		"			-400 μA									A3			"
			72		"			-400 μA									A4			"
			73		"			-400 μA									A5			"
			74		"			-400 μA									A6			"
			75		"			-400 μA									A7			"
			76		"			-400 μA									A8			"
			77		"			-400 μA									A9			"
			78		"			-400 μA									A10			"
			79		"			-400 μA									A11			"
			80		"			-400 μA									A12			"
			81		"			-400 μA									A13			"
			82		"			-400 μA									A14			"
			83		"			-400 μA									A15			"
			84		"			-400 μA									A16			"
			85		"			-400 μA									A17			"
			86		"			-400 μA									A18			"
			87		"			-400 μA									A19			"
			88		"			-400 μA									A20			"
			89		"			-400 μA									A21			"
			90		"			-400 μA									A22			"
			91		"			-400 μA									A23			"
			92		"			-400 μA									FC2			"
			93		"			-400 μA									FC1			"
			94		"			-400 μA									FC0			"
			95		"			-400 μA									AS			"
			96		"			-400 μA									UDS			"
			97		"			-400 μA									LDS			"
			98		"			-400 μA									R/W			"
			99		"			-400 μA									BG			"
			100		"			-400 μA									VMA			"
			101		"			-400 μA									E			"
I_{IH}		3010	102		"												BERR	2.5		μA
			103		"												BEACK			"
			104		"												BR			"
			105		"												DTACK			"
			106		"												IPL2			"
			107		"												IPL1			"
			108		"												IPL0			"
			109		"												VPI			"
			110		"												HALT	20.0		"
			111		"												RESET	20.0		"
I_{IL}		3009	112		"												BERR	-2.5		"
			113		"												BEACK			"
			114		"												BR			"
			115		"												DTACK			"
			116		"												IPL2			"
			117		"												IPL1			"
			118		"												IPL0			"
			119		"												VPI			"
			120		"												HALT	-20.0		"
			121		"												RESET	-20.0		"

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
				D4	D3	D2	D1	D0	AS	UDS	LDS	R/W	DTACK	BG	BGACK	BR	VCC	CLK	GND	HALT
$T_C = +110^\circ C$	IOHZ 3/		122	2.4 V	2.4 V								2.4 V		2.4 V	2.4 V	5.25 V	2/	GND	0.8 V
			123																	
			124																	
			125																	
			126																	
			127																	
			128																	
			129																	
			130																	
			131																	
			132																	
			133																	
			134																	
			135																	
			136																	
			137																	
			138																	
			139																	
			140																	
			141																	
			142																	
			143																	
			144																	
			145																	
			146																	
			147																	
			148																	
			149																	
			150																	
			151																	
			152																	
			153																	
			154																	
			155																	
			156																	
			157																	
			158																	
			159																	
			160																	
			161																	
			162																	
			163																	
			164																	
			165																	
			166																	
			167																	
			168	0.4 V	0.4 V	0.4 V	0.4 V													
			169																	
			170																	
			171																	
			172																	
			173																	
			174																	
			175																	
			176																	
			177																	
			178																	
			179																	
			180																	
			181																	
			182																	
			183																	
			184																	
			185																	
			186																	
			187																	
			188																	
			189																	
			168	0.4 V	0.4 V	0.4 V	0.4 V													
			169																	
			170																	
			171																	
			172																	
			173																	
			174																	
			175																	
			176																	
			177																	
			178																	
			179																	
			180																	
			181																	
			182																	
			183																	
			184																	
			185																	
			186																	
			187																	
			188																	
			189																	

See footnote at end of table

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
2 $T_C = +110^\circ\text{C}$	10HZ 3/		122	0.8 V			2.4 V	2.4 V	2.4 V	2.4 V	2.4 V									
			123	"			"	"	"	"	"									
			124	"			"	"	"	"	"									
			125	"			"	"	"	"	"									
			126	"			"	"	"	"	"									
			127	"			"	"	"	"	"									
			128	"			"	"	"	"	"									
			129	"			"	"	"	"	"									
			130	"			"	"	"	"	"									
			131	"			"	"	"	"	"									
			132	"			"	"	"	"	"									
			133	"			"	"	"	"	"									
			134	"			"	"	"	"	"									
			135	"			"	"	"	"	"									
			136	"			"	"	"	"	"									
			137	"			"	"	"	"	"									
			138	"			"	"	"	"	"									
			139	"			"	"	"	"	"									
			140	"			"	"	"	"	"									
			141	"			"	"	"	"	"									
			142	"			"	"	"	"	"									
			143	"			"	"	"	"	"									
			144	"			"	"	"	"	"									
			145	"			"	"	"	"	"									
			146	"			"	"	"	"	"									
			147	"			"	"	"	"	"									
			148	"			"	"	"	"	"									
			149	"			"	"	"	"	"									
			150	"			"	"	"	"	"									
			151	"			"	"	"	"	"									
			152	"			"	"	"	"	"									
			153	"			"	"	"	"	"									
			154	"			"	"	"	"	"									
			155	"			"	"	"	"	"									
			156	"			"	"	"	"	"									
			157	"			"	"	"	"	"									
			158	"			"	"	"	"	"									
			159	"			"	"	"	"	"									
			160	"			"	"	"	"	"									
			161	"			"	"	"	"	"									
			162	"			"	"	"	"	"									
			163	"			"	"	"	"	"									
			164	"			"	"	"	"	"									
			165	"			"	"	"	"	"									
			166	"			"	"	"	"	"									
			167	"			"	"	"	"	"									
	10LZ 3/		168	"			"	"	"	"	"									
			169	"			"	"	"	"	"									
			170	"			"	"	"	"	"									
			171	"			"	"	"	"	"									
			172	"			"	"	"	"	"									
			173	"			"	"	"	"	"									
			174	"			"	"	"	"	"									
			175	"			"	"	"	"	"									
			176	"			"	"	"	"	"									
			177	"			"	"	"	"	"									
			178	"			"	"	"	"	"									
			179	"			"	"	"	"	"									
			180	"			"	"	"	"	"									
			181	"			"	"	"	"	"									
			182	"			"	"	"	"	"									
			183	"			"	"	"	"	"									
			184	"			"	"	"	"	"									
			185	"			"	"	"	"	"									
			186	"			"	"	"	"	"									
			187	"			"	"	"	"	"									
			188	"			"	"	"	"	"									
			189	"			"	"	"	"	"									

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
2 $T_C = +110^\circ\text{C}$	$I_{OHZ} \ 3/$		122																	
			123																	
			124																	
			125																	
			126																	
			127																	
			128																	
			129																	
			130																	
			131																	
			132																	
			133																	
			134																	
			135																	
			136																	
			137																	
			138																	
			139																	
			140																	
			141																	
			142																	
			143																	
			144	2.4 V																
			145		2.4 V															
			146			2.4 V														
			147				2.4 V													
			148					2.4 V												
			149						2.4 V											
			150							2.4 V										
			151								2.4 V									
			152									2.4 V								
			153										2.4 V							
			154											2.4 V						
			155												2.4 V					
			156													2.4 V				
			157														2.4 V			
			158															2.4 V		
			159																2.4 V	
			160																	2.4 V
			161																	
			162																	
			163																	
			164																	
			165																	
			166																	
			167																	
	$I_{OLZ} \ 3/$		168																	
			169																	
			170																	
			171																	
			172																	
			173																	
			174																	
			175																	
			176																	
			177																	
			178																	
			179																	
			180																	
			181																	
			182																	
			183																	
			184																	
			185																	
			186																	
			187																	
			188																	
			189																	

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	52	53	54	55	56	57	58	59	60	61	62	63	64	Measured terminal	Test limit		Unit
																		Min	Max	
2 T _C = +110°C	I _{OHZ} 3/		122	A23	GND												D4		20.0	μA
			123		"												D3			
			124		"												D2			
			125		"												D1			
			126		"												D0			
			127		"		2.4 V										D15			
			128		"												D14			
			129		"												D13			
			130		"												D12			
			131		"												D11			
			132		"												D10			
			133		"												D9			
			134		"												D8			
			135		"												D7			
			136		"												D6			
			137		"												D5			
			138		"												A1			
			139		"												A2			
			140		"												A3			
			141		"												A4			
			142		"												A5			
			143		"												A6			
			144		"												A7			
			145		"												A8			
			146		"												A9			
			147		"												A10			
			148		"												A11			
			149		"												A12			
			150		"												A13			
			151		"												A14			
			152		"												A15			
			153		"												A16			
			154		"												A17			
			155		"												A18			
			156		"												A19			
			157		"												A20			
			158		"												A21			
			159		"												A22			
			160														A23			
			161		2.4 V												FC2			
			162														FC1			
			163														FC0			
			164														AS			
			165														UDS			
			166														LDS			
			167														R/W			
			168														D4	-20.0		
			169														D3			
			170														D2			
			171														D1			
			172														D0			
			173				0.4 V										D15			
			174														D14			
			175														D13			
			176														D12			
			177														D11			
			178														D10			
			179														D9			
			180														D8			
			181														D7			
			182														D6			
			183														D5			
			184														A1			
			185														A2			
			186														A3			
			187														A4			
			188														A5			
			189														A6			

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17			
				D4	D3	D2	D1	D0	KS	UDS	UDS	R/W	DTACK	BG	BGACK	BR	VCC	CLK	GND	HOLD			
2 $T_C = +110^\circ\text{C}$	I_{OLZ} 3/		190										2.4 V		2.4 V	2.4 V	5.25 V	2.4 V	GND	0.8 V			
			191																				
			192																				
			193																				
			194																				
			195																				
			196																				
			197																				
			198																				
			199																				
			200																				
			201																				
			202																				
			203																				
204																							
3			205																				
			206																				
			207																				
			208																				
			209																				
			210								0.4 V												
			211									0.4 V											
			212										0.4 V										
			213											0.4 V									
			Same tests, terminal conditions, and limits as for subgroup 2, except $T_C = -55^\circ\text{C}$, and $I_{CC} = 320\text{ mA}$.																				
			4	I_{OLZ} 3/ $T_C = +25^\circ\text{C}$																			
			5	Functional	3012																		
			6	Functional	3014																		
			7	Switching	See figure 9																		
8	Switching	See figure 9																					
9	Switching	See figure 9																					
10	Switching	See figure 9																					
11	Switching	See figure 9																					
Same tests, terminal conditions, and limits as for subgroup 10 except $T_C = -55^\circ\text{C}$.																							

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
				RST	VMA	E	VPA	BERR	IPL2	IPL1	IPL0	FC2	FC1	FC0	A1	A2	A3	A4	A5	A6
2 $T_C = +110^\circ\text{C}$	$I_{OLZ} \frac{3}{\text{I}}$		190	0.8 V			2.4 V	2.4 V	2.4 V	2.4 V	2.4 V									
			191	"			"	"	"	"	"									
			192	"			"	"	"	"	"									
			193	"			"	"	"	"	"									
			194	"			"	"	"	"	"									
			195	"			"	"	"	"	"									
			196	"			"	"	"	"	"									
			197	"			"	"	"	"	"									
			198	"			"	"	"	"	"									
			199	"			"	"	"	"	"									
			200	"			"	"	"	"	"									
			201	"			"	"	"	"	"									
			202	"			"	"	"	"	"									
			203	"			"	"	"	"	"									
3			204	"			"	"	"	"	"									
			205	"			"	"	"	"	"									
			206	"			"	"	"	"	"									
			207	"			"	"	"	"	"									
			208	"			"	"	"	"	"	0.4 V	0.4 V	0.4 V						
			209	"			"	"	"	"	"									
			210	"			"	"	"	"	"									
			211	"			"	"	"	"	"									
			212	"			"	"	"	"	"									
			213	"			"	"	"	"	"									
4 $T_C = +25^\circ\text{C}$	I_{CI}	3012																		
8 $T_C = +110^\circ\text{C}$	Functional	See figure 9																		
10 $T_C = +110^\circ\text{C}$	Switching	See figure 9																		
11 $T_C = -55^\circ\text{C}$	Switching	See figure 9																		

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
2 $T_C = +110^\circ\text{C}$	10LZ 3/		190	0.4 V														5.25 V		
			191	0.4 V																
			192		0.4 V															
			193				0.4 V													
			194					0.4 V												
			195						0.4 V											
			196							0.4 V										
			197								0.4 V									
			198									0.4 V								
			199										0.4 V							
			200											0.4 V						
			201												0.4 V					
			202													0.4 V				
			203														0.4 V			
			204															0.4 V		
3			205																	
			206																	
			207																	
			208																	
			209																	
			210																	
			211																	
			212																	
			213																	
4 $T_C = +25^\circ\text{C}$	C _I	3012																5.25 V		
8 $T_C = +110^\circ\text{C}$	Functional	3014 See figure 9																		
10 $T_C = +110^\circ\text{C}$	Switching	3003 See figure 9																		
11 $T_C = -55^\circ\text{C}$	Switching	3003 See figure 9																		

See footnotes at end of table.

TABLE III. Group A inspection for device types 01, 02, and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	52	53	54	55	56	57	58	59	60	61	62	63	64	Measured terminal	Test limit		Unit
				A23	GND	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5		Min	Max	
2 $T_C = +110^\circ\text{C}$	IOLZ 3/		190		GND												A7	-20.0		μA
			191		"												A8	"		"
			192		"												A9	"		"
			193		"												A10	"		"
			194		"												A11	"		"
			195		"												A12	"		"
			196		"												A13	"		"
			197		"												A14	"		"
			198		"												A15	"		"
			199		"												A16	"		"
			200		"												A17	"		"
			201		"												A18	"		"
			202		"												A19	"		"
			203		"												A20	"		"
			204		"												A21	"		"
			205		"												A22	"		"
			206	0.4 V	"												A23	"		"
			207		"												FC2	"		"
			208		"												FC1	"		"
			209		"												FC0	"		"
			210		"												KS	"		"
			211		"												UDS	"		"
			212		"												LDS	"		"
			213		"												R/W	"		"
3																	-	See table IIIA		
4 4/ $T_C = +25^\circ\text{C}$	C_1	3012															D3, BERR, DTACK, IPLOD, BR	20		pF
8 5/6/ $T_C = +110^\circ\text{C}$	Functional	3014 See figure 9															-	See table IIIA		
10 6/7/ $T_C = +110^\circ\text{C}$	Switching	3003 See figure 9															-	See table IIIA		
11 6/7/ $T_C = -55^\circ\text{C}$	Switching	3003 See figure 9															-	See table IIIA		

See footnotes at end of table.

TABLE IIIA. Group A inspection for device types 01, 02, and 03.

Test	Symbol	Figure number 8/	Reference number 9/	Subgroups 10 and 11 limits T _C = -55°C and +110°C						Unit
				Device type 01		Device type 02		Device type 03		
				Min	Max	Min	Max	Min	Max	
D _{IN} to CLK low (t _{SET})	t _{DICL}	5	47	25		20		10		ns
$\overline{DTACK}$ to CLK low (t _{SET})	t _{SDTCL}	5	47	25		20		20		ns
$\overline{BR}$ to CLK low (t _{SET})	t _{SBRCL}	5	47	25		20		20		ns
$\overline{BGACK}$ to CLK low (t _{SET})	t _{SBGCL}	5	47	25		20		20		ns
$\overline{VPA}$ to CLK low (t _{SET})	t _{SVPACL}	5	47	25		20		20		ns
$\overline{BERR}$ to CLK low (t _{SET})	t _{SPERCL}	5	47	25		20		20		ns
CLK width low	t _{CL}	5	2	75	125	55	125	45	125	ns
CLK width high	t _{CH}	5	3	75	125	55	125	45	125	ns
CLK high to FC valid	t _{CHFCV}	5	6A		80		70		60	ns
CLK high to $\overline{AS}$, $\overline{DS}$ low, max	t _{CHSLX}	5	9		70		60		55	ns
CLK low to $\overline{AS}$ high	t _{CLSH}	5	12		80		70		55	ns
CLK low to $\overline{DS}$ high	t _{CLSH}	5	12		80		70		55	ns
CLK high to R/ $\overline{W}$ high, max	t _{CHRHX}	5	18		80		70		60	ns
CLK high to R/ $\overline{W}$ low	t _{CHRL}	6	20		80		70		60	ns
CLK low to D _{OUT} valid	t _{CLDO}	6	23		80		70		55	ns
CLK low to address valid	t _{CLAV}	5	6		80		70		60	ns
CLK high to $\overline{BG}$ low	t _{CHGL}	7	33		80		70		70	ns

See footnotes at end of table.

TABLE IIIA. Group A inspection for device types 01, 02, and 03 - Continued.

Test	Symbol	Figure number 8/	Reference number 9/	Subgroups 10 and 11 limits T _C = -55°C and +110°C						Unit
				Device type 01		Device type 02		Device type 03		
				Min	Max	Min	Max	Min	Max	
CLK high to $\overline{BG}$ high	t _{CHGH}	7	34		80		70		60	ns
CLK low to $\overline{VMA}$ low	t _{CLVML}	8	40		80		70		70	ns
CLK low to E transition	t _{CLE}	8	41		85		70		55	ns

1/ At the manufacturer's option this test may be performed as a functional test.

2/ Dynamic clock as specified:



3/ All three-state measurements are to the following output levels.

$V_{OUT} = 0.4 \text{ V}$

$V_{OUT} = 2.4 \text{ V}$

Output loads circuit in accordance with figure 9.

4/ Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz and a signal amplitude of 50 mV rms.

5/ Subgroup 8 is encompassed in subgroups 10 and 11.

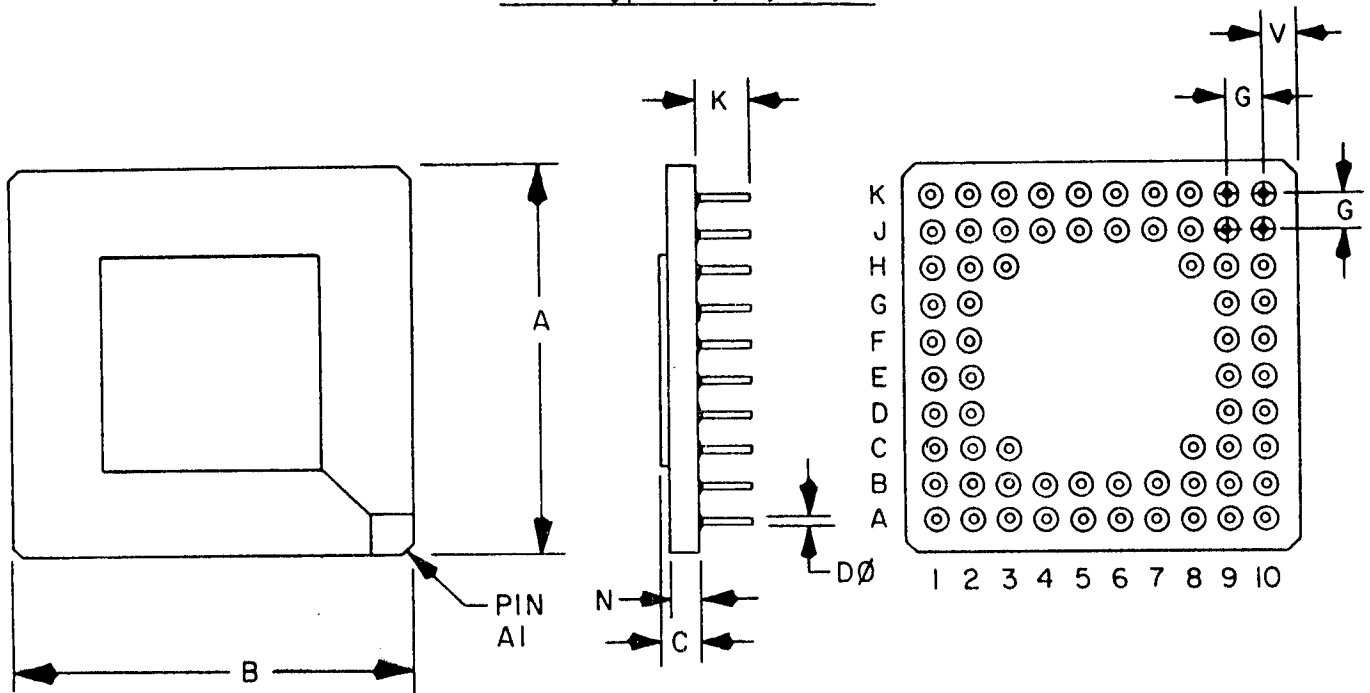
6/ For subgroups 8, 10, and 11 input and output voltage conditions appear in table IV.

7/ These tests are performed as a series of functional tests verifying the limits of table IIIA.

8/ Figures 5 through 8 represent the timing diagrams associated with subgroups 8, 10, and 11.

9/ The reference number refers to the position where the parameter being measured appears on figures 5, 6, 7, and 8.

Device types 01, 02, and 03



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	1.040	1.080	26.41	27.43
B	1.040	1.080	26.41	27.43
C	.083	.102	2.11	2.59
DØ	.017	.024	0.43	0.61
G	.100 BSC		2.54 BSC	
K	.140	.190	3.56	4.83
N	.072	.088	1.83	2.23
V	.070	.090	1.78	2.29

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Positional tolerance for leads (68 places):

⊕ ⌀ .005 (0.13 mm) (M)

4. Manufacturers option, chamfer .15 (3.8 mm) maximum at 45°, all edges.
5. There shall be a .20 inch (5.1 mm) minimum spacing between any two metallized areas on the surfaces of the packages.
6. Increase maximum limit of pin diameter (DØ) by .003 inch (0.08 mm) when lead finish "A" is applied.

FIGURE 1. Case outline T (68 terminal pin grid array).

Device types 01, 02, and 03

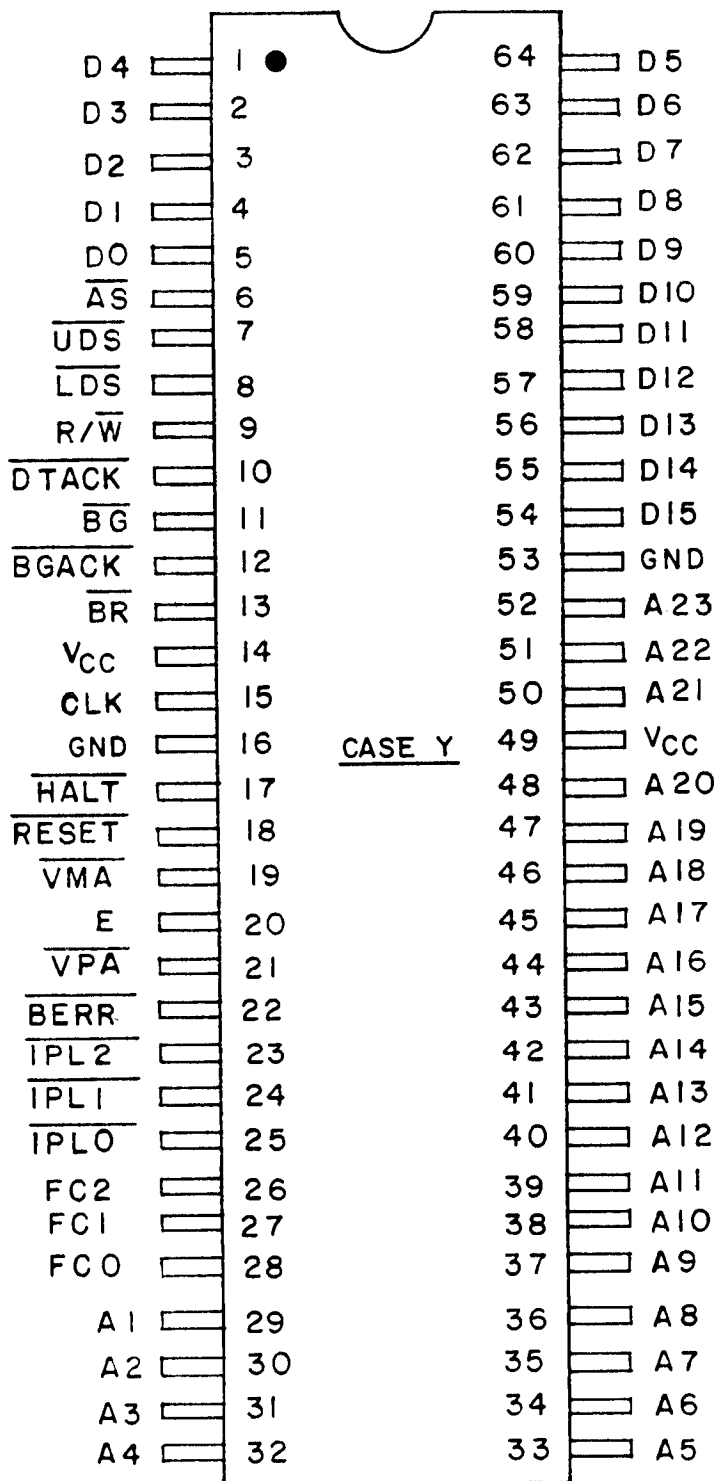
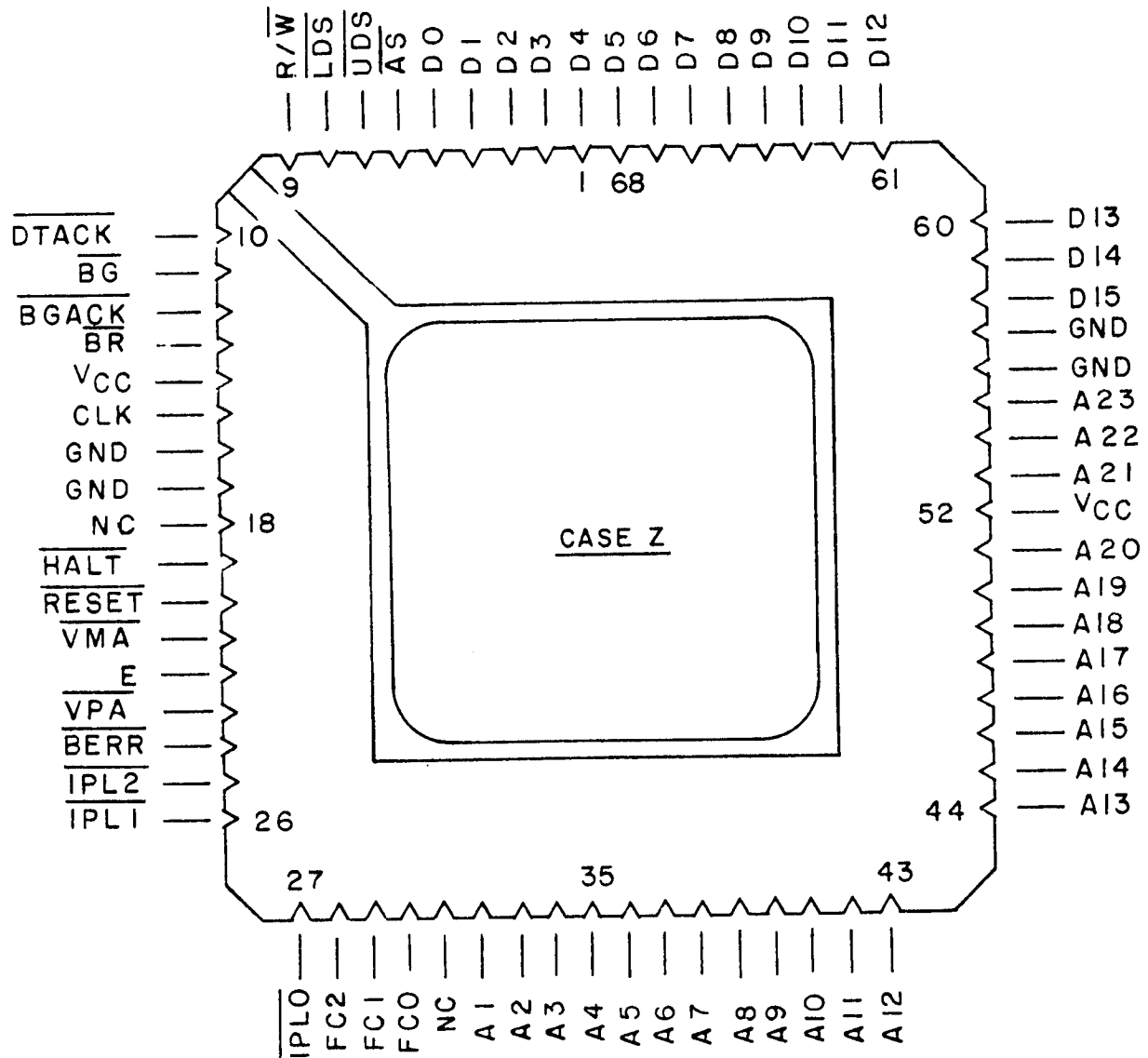
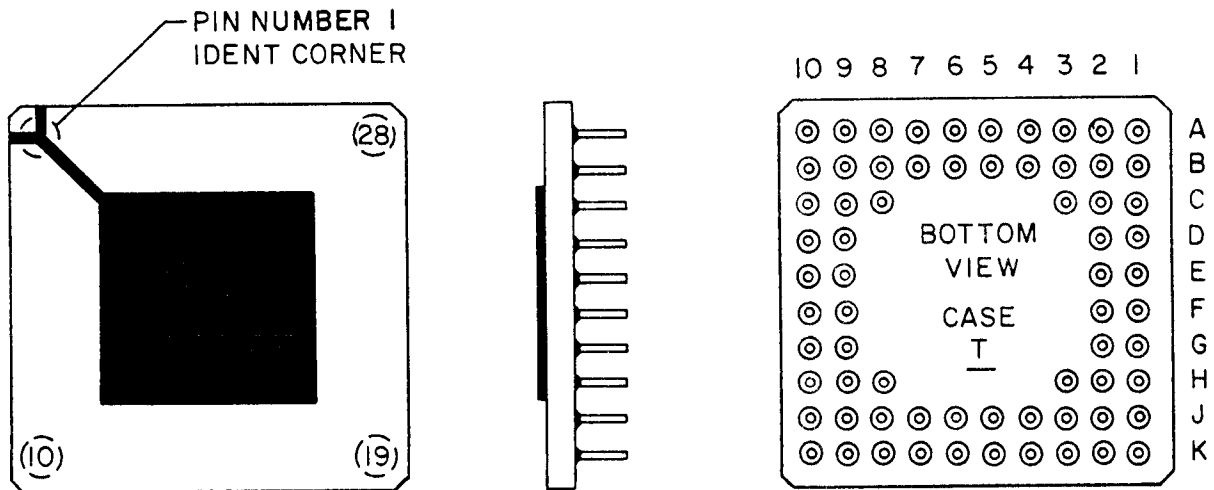


FIGURE 2. Terminal connections (top view).

Device types 01, 02, and 03FIGURE 2. Terminal connections (top view) - Continued.

Device types 01, 02, and 03



Pin number	Function	Pin number	Function	Pin number	Function	Pin number	Function
1A	Do not connect	9K	A9	3A	D1	9H	A12
1B	~~DTACK~~	10K	Do not connect	2A	~~AS~~	9G	A15
1C	~~BGACK~~	10J	A14	2B	~~LDS~~	9F	A18
1D	BR	10H	A16	2C	BG	9E	VCC
1E	CLK	10G	A17	2D	VCC	9D	GND
1F	~~HALT~~	10F	A19	2E	GND	9C	A23
1G	~~VMA~~	10E	A20	2F	~~RESET~~	9B	D14
1H	E	10D	A21	2G	~~VPA~~	8B	D11
1J	~~BERR~~	10C	A22	2H	~~IPL2~~	7B	D9
1K	Do not connect	10B	D15	2J	~~IPL0~~	6B	D6
2K	FC2	10A	D12	3J	FC1	5B	D3
3K	FC0	9A	D10	4J	Do not connect	9C	~~D0~~
4K	A1	8A	D8	5J	A2	3B	~~UDS~~
5K	A3	7A	D7	6J	A5	3C	R/W
6K	A4	6A	D5	7J	A8	3H	~~IPL1~~
7K	A6	5A	D4	8J	A10	8H	A13
7K	A7	4A	D2	9J	A11	8C	D13

FIGURE 2. Terminal connections - Continued.

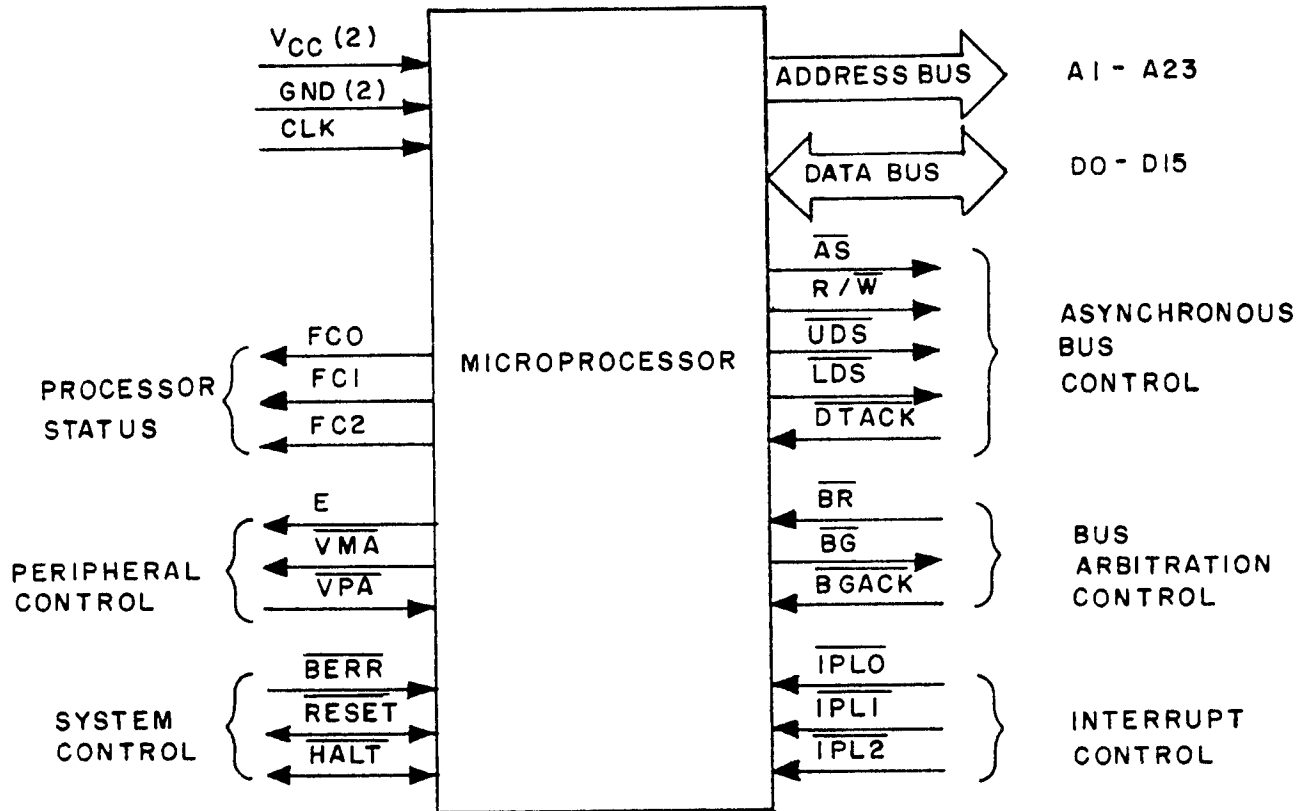
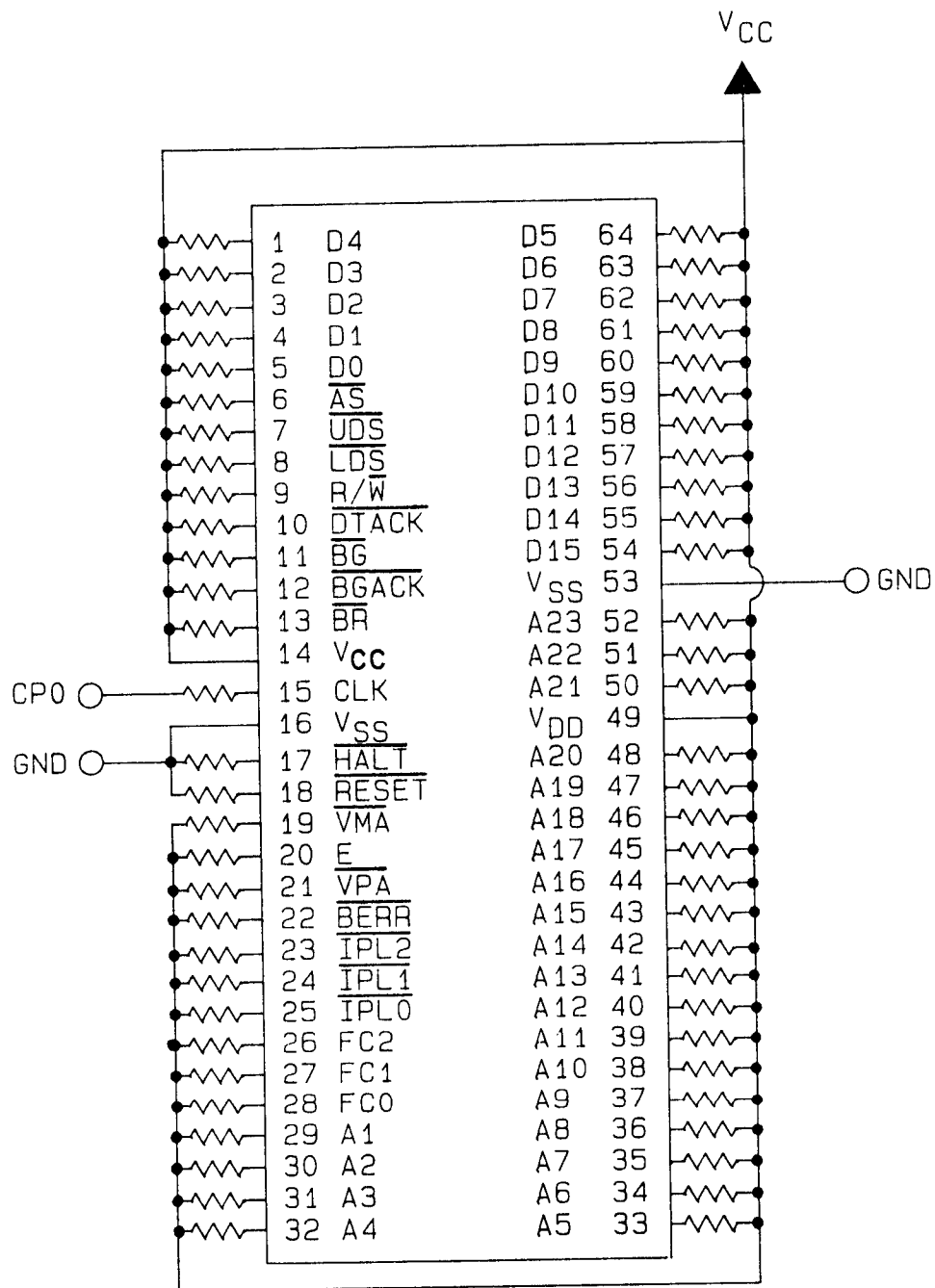


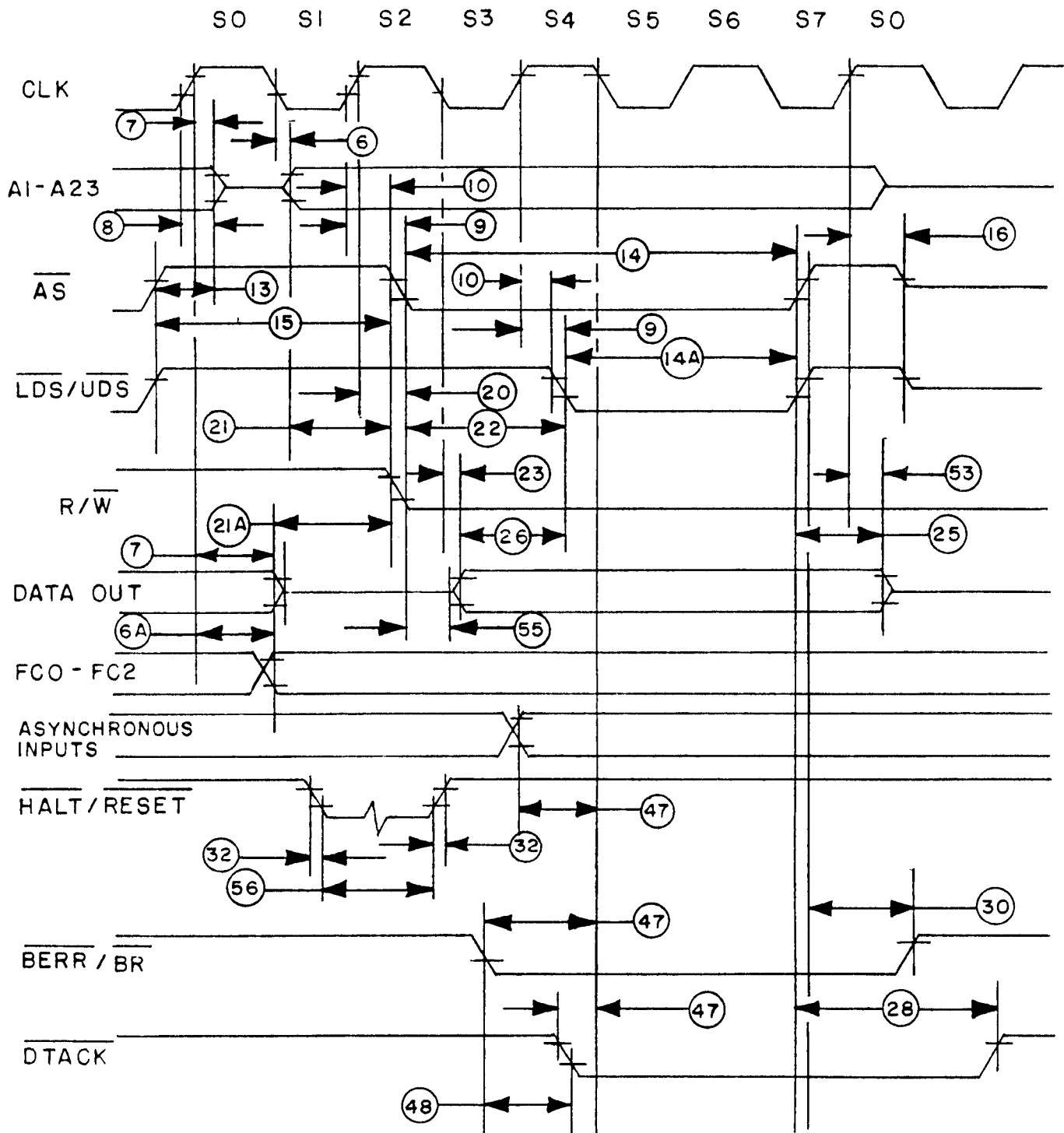
FIGURE 3. Functional block diagram and input and output signals.



NOTES:

1. $V_{CC} = 5.25$ to 5.5 V dc.
2. All resistors are 680Ω .
3. Clock pulse output = 200 kHz.

FIGURE 4. Burn-in circuit and timing waveforms.

FIGURE 6. Write cycle timing.

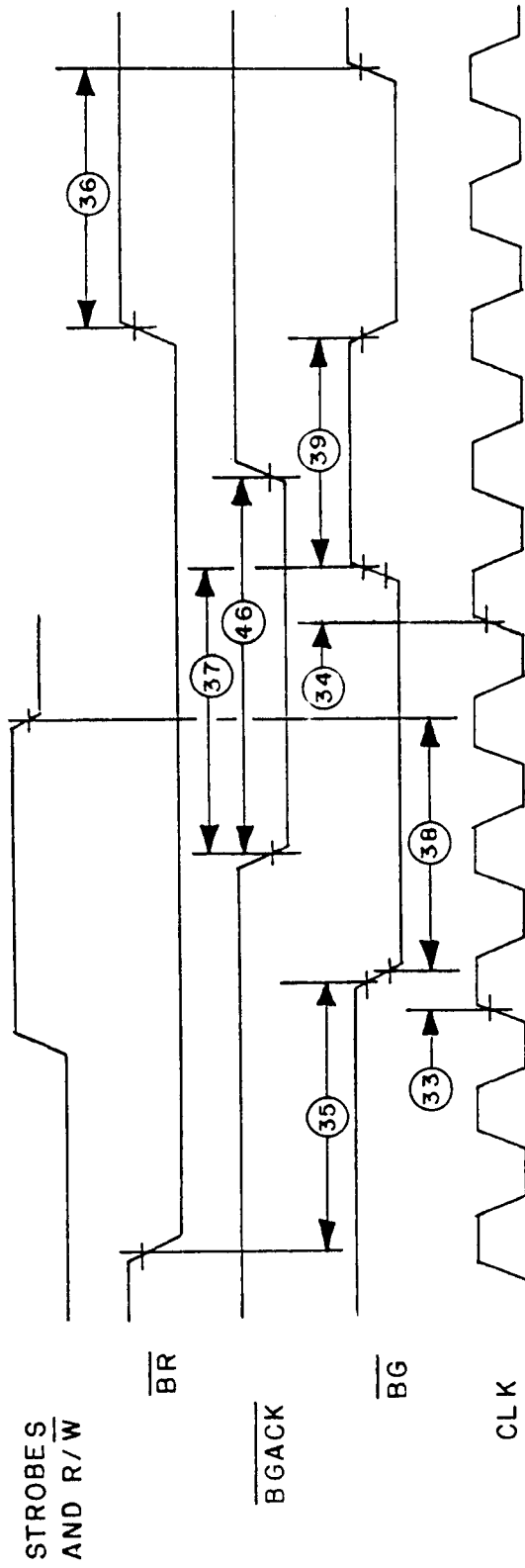


FIGURE 7. AC electrical waveforms - bus arbitration.

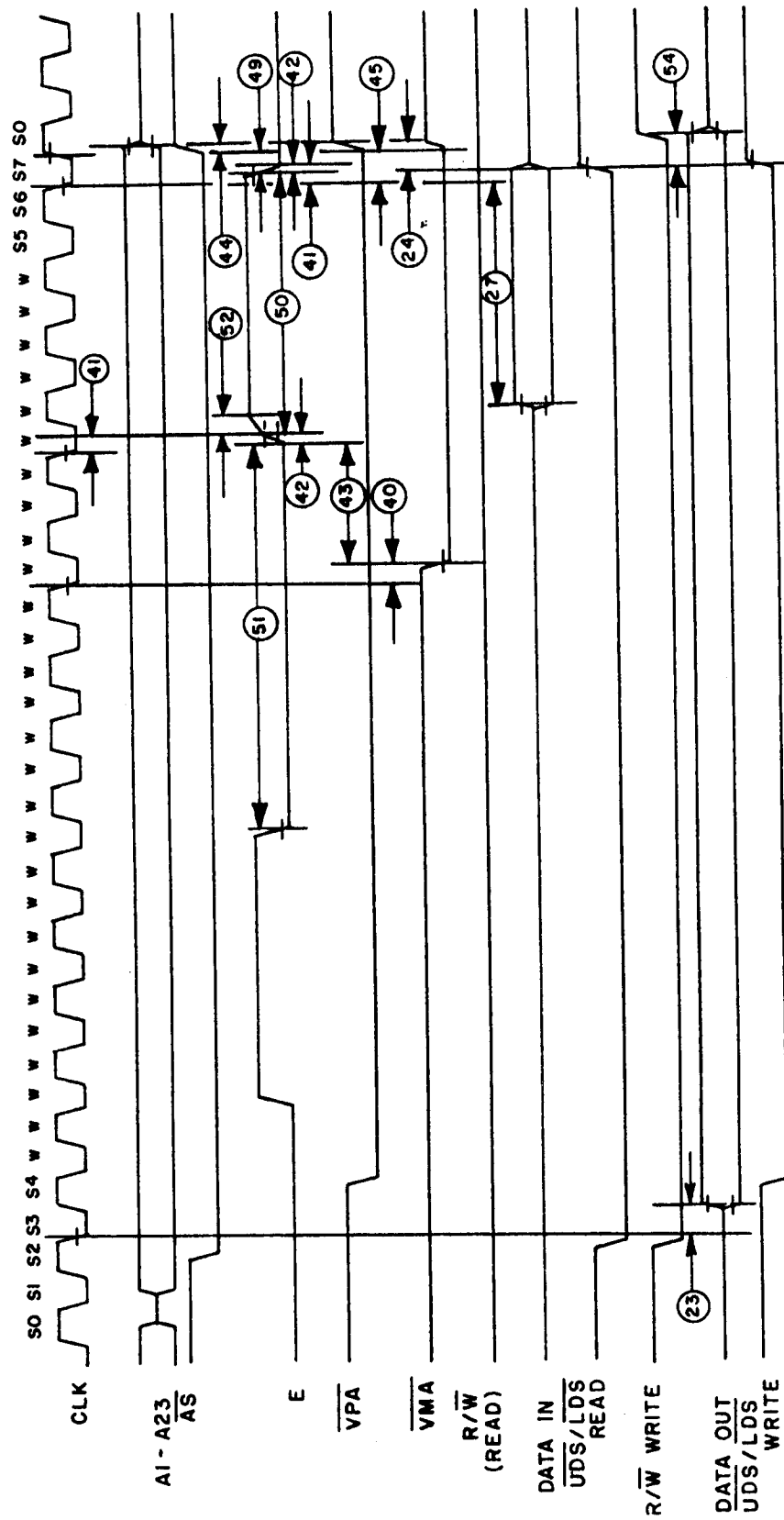
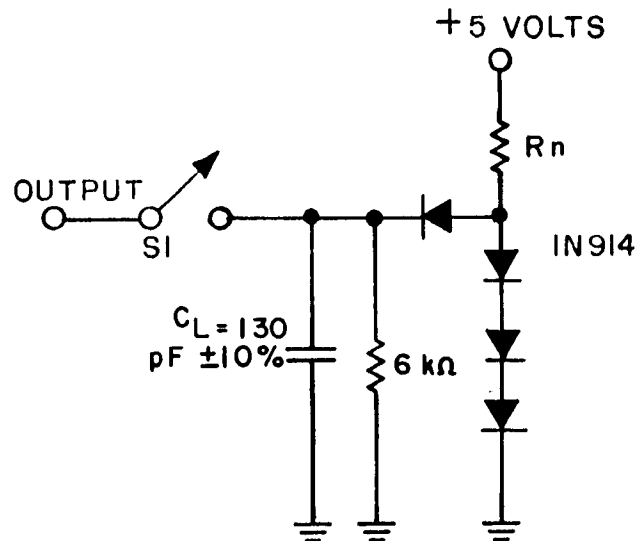


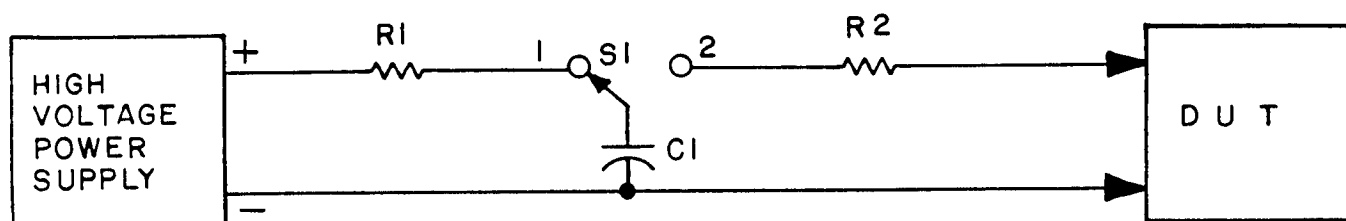
FIGURE 8. Enable/interface timing.



NOTES:

1. $R_n = 1.22 \text{ k}\Omega \pm 5\%$ for A1 through A23, $\overline{BG}$, E and FC0-2.
2. $R_n = 740\Omega \pm 5\%$ for all other outputs.
3. $C_L = 130 \text{ pF} \pm 10\%$.

FIGURE 9. Output load circuit for functional and ac testing.

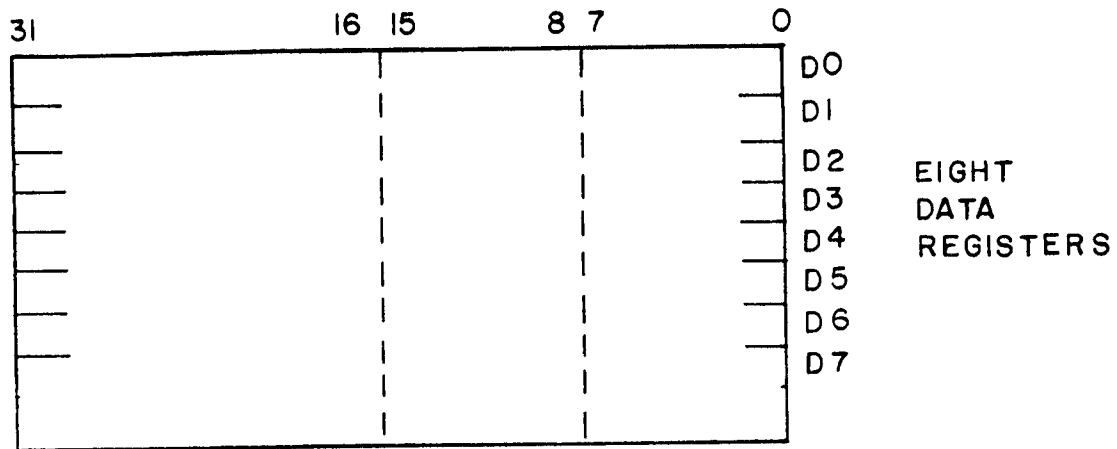


Modes for high voltage test		
Mode	+ Terminal	- Terminal
1	V _{CC}	Input
2	Input	GND
3	Input	Associated output
3	Associated output	Input

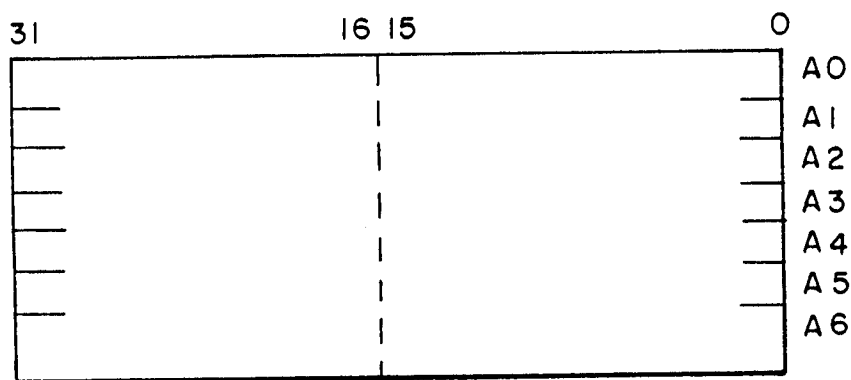
NOTES:

1. $V_{ZAP} = 400 \text{ V}$ minimum charge on C1.
2. $1 \text{ M}\Omega < R1 < 5 \text{ M}\Omega$.
3. $R2 = 1.5 \text{ k}\Omega \pm 5\%$.
4. $C1 = 100 \text{ pF} \pm 10\%$.
5. S1 = Hg-wetted "bounceless" relay.

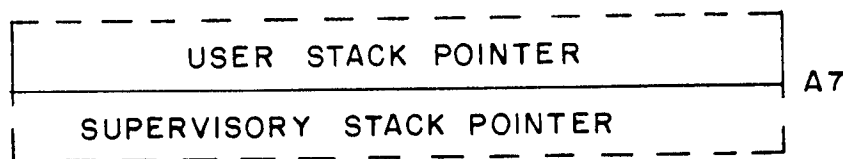
FIGURE 10. High voltage (V_{ZAP}) test circuit.



EIGHT
DATA
REGISTERS



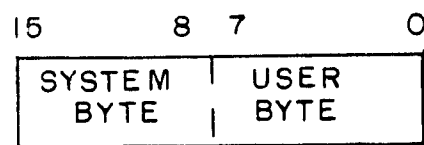
SEVEN
ADDRESS
REGISTERS



TWO STACK
POINTERS

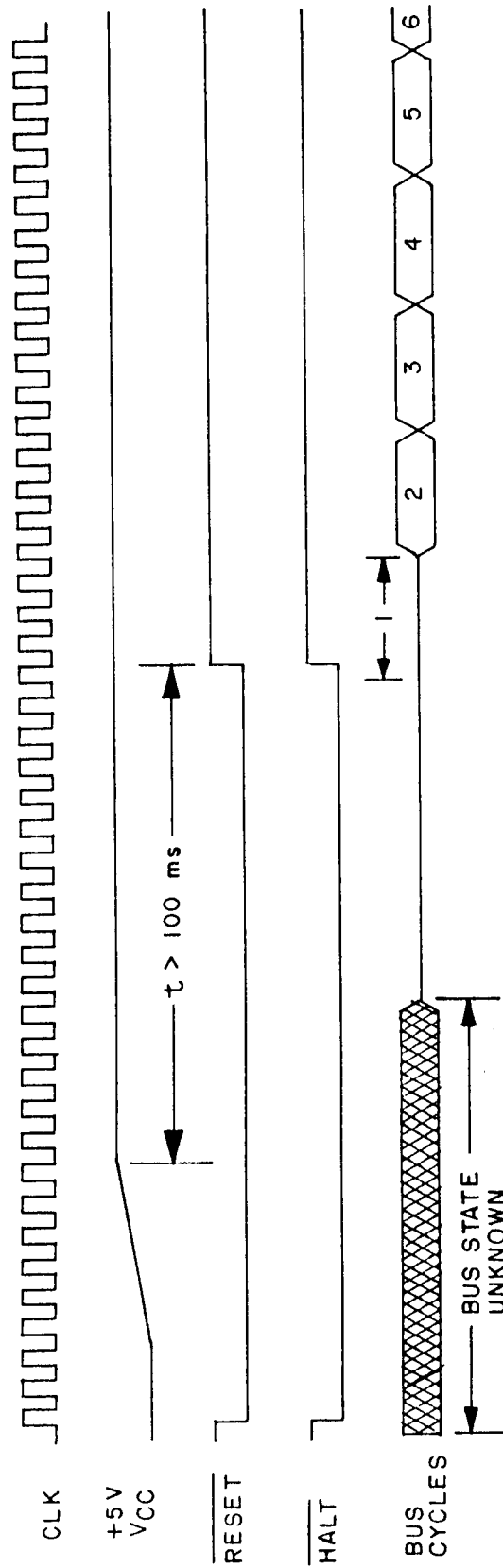


PROGRAM
COUNTER



STATUS
REGISTER

FIGURE 11. Register organization.



NOTES:

1. Internal start-up time.
2. SSP high read in here.
3. SSP low read in here.
4. PC high read in here.
5. PC low read in here.
6. First instruction fetched here. Data bus in read mode.

ALL CONTROL SIGNALS INACTIVE.

FIGURE 12. Reset operation timing diagram.

TABLE IV. Input voltage conditions for functional testing.

Symbol	Parameter	Unit
V _{CC}	5.25	V
GND	0	V
V _{IH}	2.4	V
V _{IL}	0.8	V
V _{OH}	≥1.4	V
V _{OL}	<1.4	V

TABLE VI. Instruction set.

Mnemonic	Description	Operation	Condition codes				
			X	N	Z	V	C
ABCD	Add decimal with extend	$(\text{Destination})_{10} + (\text{Source})_{10}$ Destination	*	U	*	U	*
ADD	Add binary	$(\text{Destination}) + (\text{Source})$ Destination	*	*	*	*	*
ADDA	Add address	$(\text{Destination}) + (\text{Source})$ Destination	-	-	-	-	-
ADDI	Add immediate	$(\text{Destination}) + \text{Immediate Data}$ Destination	*	*	*	*	*
ADDQ	Add quick	$(\text{Destination}) + \text{Immediate Data}$ Destination	*	*	*	*	*
ADDX	Add extended	$(\text{Destination}) + (\text{Source}) + X$ Destination	*	*	*	*	*
AND	And logical	$(\text{Destination}) \text{ } (\text{Source}) + X$ Destination	-	*	*	0	0
ANDI	And immediate	$(\text{Destination}) \text{ } \text{Immediate Data}$ Destination	-	*	*	0	0
ASL,ASR	Arithmetic shift	(Destination) Shifted by <count> Destination	*	*	*	*	*
BCC	Branch conditionally	If CC then PC + d PC	-	-	-	-	-
BCHG	Test a bit and change	$\sim(\text{<bit number>}) \text{ OF Destination}$ Z $\sim(\text{<bit number>}) \text{ OF Destination}$ <bit number> OF Destination	-	-	*	-	-
BCLR	Test a bit and clear	$\sim(\text{<bit number>}) \text{ OF Destination}$ Z 0 <bit number> OF Destination	-	-	*	-	-
BRA	Branch always	PC+d PC	-	-	-	-	-
BSET	Test a bit and set	$\sim(\text{<bit number>}) \text{ OF Destination}$ Z 1 <bit number> OF Destination	-	-	*	-	-
BSR	Branch to subroutine	PC SP0-; PC+d PC	-	-	-	-	-
BTST	Test a bit	$\sim(\text{<bit number>}) \text{ OF Destination}$ Z	-	-	*	-	-

* affected 0 cleared U defined
- unaffected 1 set

TABLE VI. Instruction set - Continued.

Mnemonic	Description	Operation	Condition codes				
			X	N	Z	V	C
CHK	Check register against bounds	If Dn <0 or Dn> (<ea>) then TRAP	-	*	U	U	U
CLR	Clear an operand	0 Destination	-	0	1	0	0
CMP	Compare	(Destination)-(Source)	-	*	*	*	*
CMPA	Compare address	(Destination)-(Source)	-	*	*	*	*
CMPI	Compare immediate	(Destination)-Immediate Data	-	*	*	*	*
CMPM	Compare memory	(Destination)-(Source)	-	*	*	*	*
DBCC	Test condition, decrement and branch	If ~CC then Dn-1 Dn; if Dn≠-1 then PC+d PC	-	-	-	-	-
DIVS	Signed divide	(Destination)/(Source) Destination	-	*	*	*	0
DIVU	Unsigned divide	(Destination)/(Source) Destination	-	*	*	*	0
EOR	Exclusive OR logical	(Destination)θ(Source) Destination	-	*	*	0	0
EORI	Exclusive OR immediate	(Destination) θ Immediate Data Destination	-	*	*	0	0
EXG	Exchange register	Rx Ry	-	-	-	-	-
EXT	Sign extend	(Destination)Sign-extended Destination	-	*	*	0	0
JMP	Jump	Destination PC	-	-	-	-	-
JSR	Jump to subroutine	PC~SPθ-;Destination PC	-	-	-	-	-
LEA	Load effective address	Destination An	-	-	-	-	-
LINK	Link and allocate	An SPθ-;SP An; SP+d SP	-	-	-	-	-

* affected 0 cleared U defined
 - unaffected 1 set

TABLE VI. Instruction set - Continued.

Mnemonic	Description	Operation	Condition codes					
			X	N	Z	V	C	
LSL,LSR	Logical shift	(Destination)Shifted by <count> Destination	*	*	*	0	*	
MOVE	Move data from source destination	(Source) Destination	-	*	*	0	0	
MOVE to CCR	Move to condition code	(Source) CCR	*	*	*	*	*	
MOVE to SR	Move to the status register	(Source) SR	*	*	*	*	*	
MOVE to SR	Move from the status register	SR Destination	-	-	-	-	-	
MOVE USP	Move user stack pointer	USP An; An USP	-	-	-	-	-	
MOVEA	Move address	(Source) Destination	-	-	-	-	-	
MOVEM	Move multiple registers	Registers Destination (Source) Registers	-	-	-	-	-	
MOVEP	Move peripheral data	(Source) Registers	-	-	-	-	-	
MOVEQ	Move quick	Immediate Data Destination	-	*	*	0	0	
MULS	Signed multiply	(Destination)*(Source) Destination	-	*	*	0	0	
MULU	Unsigned multiply	(Destination)*(Source) Destination	-	*	*	0	0	
NBCD	Negate decimal with extend	0-(Destination) ₁₀ -X Destination	*	U	*	U	*	
NEG	Negate	0-(Destination) Destination	*	*	*	*	*	
NEGX	Negate with extend	0-(Destination)-X Destination	*	*	*	*	*	
NOP	No operation	-	-	-	-	-	-	
NOT	Logical complement	~(Destination) Destination	-	*	*	0	0	

* affected 0 cleared U defined
 - unaffected 1 set

TABLE VI. Instruction set - Continued.

Mnemonic	Description	Operation	Condition codes					
			X	N	Z	V	C	
OR	Inclusive OR logical	(Destination)v(Source) Destination	-	*	*	0	0	
ORI	Inclusive OR immediate	(Destination)vImmediate Data Destination	-	*	*	0	0	
PEA	Push effective address	(Destination) SP@-	-	-	-	-	-	
RESET	Reset external devices	-	-	-	-	-	-	
ROL,ROR	Rotate (without extend)	(Destination) Rotated by <count> Destination	-	*	*	0	*	
ROXL,ROXR	Rotate (with extend)	(Destination) Rotated by <count> Destination	*	*	*	0	*	
RTE	Return from exception	SP@+ SR; SP@+ PC	*	*	*	*	*	
RTR	Return and restore condition codes	SP@+ CC; SP@+ PC	*	*	*	*	*	
RTS	Return from subroutine	SP@+ PC	-	-	-	-	-	
SBCD	Subtract decimal with extend	(Destination) ₁₀ -(Source) ₁₀ -X Destination	*	U	*	U	*	
SCC	Set according to condition	If CC then 1's Destination else 0's Destination	-	-	-	-	-	
STOP	Load status register and stop	Immediate Data SR; STOP	*	*	*	*	*	
SUB	Subtract binary	(Destination)-(Source) Destination	*	*	*	*	*	
SUBA	Subtract address	(Destination)-(Source) Destination	-	-	-	-	-	
SUBI	Subtract immediate	(Destination)-Immediate Data Destination	*	*	*	*	*	
SUBQ	Subtract quick	(Destination)-Immediate Data Destination	*	*	*	*	*	
SUBX	Subtract with extend	(Destination)-(Source)-X Destination	*	*	*	*	*	

* affected 0 cleared U defined
 - unaffected 1 set

TABLE VI. Instruction set - Continued.

Mnemonic	Description	Operation	Condition codes				
			X	N	Z	V	C
SWAP	Swap register halves	Register 31:16 Register 15:0	-	*	*	0	0
TAS	Test and set an operand	(Destination) Tested CC; 1 7 OF Destination	-	*	*	0	0
TRAP	Trap	PC SSP@-; SR SSP@-;(Vector) PC	-	-	-	-	-
TRAPV	Trap on overflow	If V then TRAP	-	-	-	-	-
TST	Trap an operand	(Destination) Tested CC	-	*	*	0	0
UNLK	Unlink	An SP; SP@+ An	-	-	-	-	-

= bit number
 * affected 0 cleared U defined
 - unaffected 1 set

4.5 Methods of inspection. Methods of inspection shall be specified as follows.

4.5.1 Voltage and current. All voltage values given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 High-voltage (V_{ZAP}) test of input protection circuits. One input terminal of the device under test (DUT) shall be subjected to a voltage pulse of 400 V from a 100 pF source in the following test sequence:

- a. Measure I_{IH} and I_{IL} at one input terminal of the device under tests at +25°C. These measurements shall be made in accordance with table III herein. The test limits for a single terminal measurement of I_{IH} and I_{IL} shall be as specified in table III.
- b. Apply the test voltage ($V_{ZAP} = 400$ V) to the same terminal selected for leakage current measurements. Apply V_{ZAP} in a 2-pulse sequence as follows and in accordance with the test circuit as shown on figure 10.
 - (1) Input (-) to GND.
 - (2) Input (+) to GND.
- c. Within 24 hours repeat the I_{IH} and I_{IL} measurements on the same terminal as performed above. At this time a DUT exhibiting leakage currents in excess of the specified limits is defective.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. In addition, all devices shall be in contact with a conductive material which shorts all leads together to prevent electrostatic damage.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Table V, test vectors. Table V, forms a part of this detail specification to the extent that is required by 3.5 herein. Table V is a software control program of the sequence of vectors needed for driving the devices represented in this detail specification as part of the inspection required by table II herein. Table V is generated only when a qualified source exists for this specification.

6.3 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.4 Ordering data. The contract or purchase order should specify the following:

- a. Complete PIN (see 1.2).
- b. Requirement for delivery of one copy of the data (see 4.4) pertinent to the device manufacturer, if applicable.
- c. Requirement for certificate of compliance, if applicable.
- d. Requirement for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirement for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- f. Requirement for product assurance options.
- g. Requirement for special carriers, lead lengths, or lead forming, if applicable.
- h. Requirement for "JAN" marking.

6.5 Register organization.

A block diagram of the register organization is shown on figure 11.

Data registers. Each data register is 32 bits wide. Byte operands occupy the low order 8 bits, word operands the low order 16 bits, and long operands the entire 32 bits. The least significant bit is addressed as bit zero; the most significant bit is addressed as bit 31. When a data register is used as either a source or destination operand, only the appropriate low order portion is changed; the remaining high order portion is neither used nor changed.

Address registers. Each address register and the stack pointer is 32 bits wide and holds a full 32 bit address. Address registers do not support byte sized operands. Therefore, when an address register is used as a source operand, either the low order word or the entire long word operand is used depending upon the operation size. When an address register is used as the destination operand, the entire register is affected regardless of the operation size. If the operation size is word, any other operands are sign extended to 32 bits before the operation is performed.

Stacks and queues.

In addition to supporting the array data structure with the index addressing mode, the microprocessor also supports stack and queue data structures with the address register indirect postincrement and predecrement addressing modes. A stack is a last-in-first-out (LIFO) list, a queue is a first-in-first-out (FIFO) list. When data is added to a stack or queue, it is "pushed" into the structure; when it is removed, it is "pulled" from the structure. The system stack is used implicitly by many instructions; user stacks and queues may be created and maintained through the addressing modes.

System stack. Address register seven (A7) is the system stack pointer (SP). The system stack pointer is either the supervisor stack pointer (SSP) or the user stack pointer (USP), depending on the state of the S-bit in the status register. If the S-bit indicates supervisor state, the SSP is the active system stack pointer and the USP cannot be referenced as an address register. If the S-bit indicates user state, the USP is the active system stack pointer and the SSP cannot be referenced. Each system stack fills from high memory to low memory.

The program counter is saved on the active system stack on subroutine calls, and restored from the active system stack on returns. On the other hand, both the program counter and the status register are saved on the supervisor stack during the processing of traps and interrupts. Thus, the correct execution of the supervisor state code is not dependent on the behavior of user code and user programs may use the user stack pointer arbitrarily.

In order to keep data on the system stack aligned properly, data entry on the stack is restricted so that data is always put in the stack on a word boundary. Thus, byte data is pushed on or pulled from the system stack in the high-order half of the word; the lower half is unchanged.

User stacks. User stacks can be implemented and maintained by employing the address register indirect with postincrement and predecrement addressing modes. Using the address register (one of A0 through A6), the user may implement stacks which are filled either from high memory to low memory, or vice versa. The important things to remember are:

- a. Using predecrement, the register is decremented before its contents are used as the pointer into the stack.
- b. Using postincrement, the register is incremented after its contents are used as the pointer into the stack.
- c. Byte data must be put on the stack in pairs when mixed with word or long data so that the stack will not get misaligned when the data is retrieved. Word and long accesses must be on word boundary (even) addresses.

6.6 Terminal and pin definition.

The input and output signals can be functionally organized into groups as shown on figure 3.

Address bus (A1 through A23). This 23-bit, unidirectional, three-state bus is capable of addressing 8 megawords of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are all set to a logic high.

Data bus (D0 through D15). This 16-bit, bidirectional, three-state bus is the general purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0 through D7.

Asynchronous bus control. Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

Address strobe ($\overline{AS}$). This signal indicates that there is a valid address on the address bus.

Read/write (R/W). This signal defines the data bus transfer as a read or write cycle. The R/W signal also works in conjunction with the upper and lower data strobes as explained in the following paragraph.

Data transfer acknowledge (DTACK). This input indicates that the data transfer is completed. When the processor recognizes DTACK during a read cycle, data is latched and the bus cycle terminated. When DTACK is recognized during a write cycle, the bus cycle is terminated.

Bus arbitration control. These three signals form a bus arbitration circuit to determine which device will be the bus master device.

Upper and lower data strobes (UDS, LDS). These signals control the data on the data bus as shown in table VII herein. When the R/W line is high, the processor will read from the data bus as indicated. When the R/W line is low, the processor will write to the data bus as shown.

TABLE VII. Data strobe control of data bus.

UDS	LDS	R/W	D8-D15	D0-D7
High	High	---	No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7	Valid data bits 0-7
Low	High	Low	Valid data bits 8-15	Valid data bits 8-15

Bus request (BR). This input is wire ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

Bus grant (BG). This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus grant acknowledge (BGACK). This input indicates that some other device has become the bus master. This signal cannot be asserted until the following four conditions are met:

- A bus grant has been received.
- Address strobe is inactive which indicates that the microprocessor is not using the bus.

- c. Data transfer acknowledge is inactive which indicates that either memory or the peripherals are not using the bus.
- d. Bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership.

Interrupt control (IPL0, IPL1, IPL2). These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. The least significant bit is contained in IPL0 and the most significant bit is contained in IPL2.

System control. The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

Bus error (BERR). This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

- a. Nonresponding devices.
- b. Interrupt vector number acquisition failure.
- c. Illegal access request as determined by a memory management unit.
- d. Other application dependent errors.

The bus error signal interacts with the halt signal to determine if exception processing should be performed or the current bus cycle should be retired.

Reset (RESET). This bidirectional signal line acts to reset (initiate a system initialization sequence) the processor in response to an external reset signal. An internally generated reset (result of a RESET instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external halt and reset signals applied at the same time (see figure 12 herein).

HALT (HALT). When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are put in their high impedance state.

When the processor has stopped executing instructions, such as in a double bus fault condition, the halt line is driven by the processor to indicate to external devices that the processor has stopped.

Peripheral control. These control signals are used to allow the interfacing of synchronous peripheral devices with the asynchronous processor. These signals are explained in the following paragraphs.

Enable (E). This signal is the standard enable signal common to all peripheral devices. The period for this output is 10 clock periods (6 clocks low; 4 clocks high).

Valid peripheral address (VPA). This input indicates that the device or region addressed is a family device and that data transfer should coincide with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt.

Valid memory address (VMA). This output is used to indicate to peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address (VPA) input which indicates that the peripheral is a family device.

Processor status (FC0, FC1, FC2). These function code outputs indicate the mode (user or supervisor) and the cycle type currently being executed as shown in table VIII. The information indicated by the function code outputs is valid whenever address strobe (AS) is active.

TABLE VIII. Function code outputs.

FC2	FC1	FC0	Cycle type
Low	Low	Low	(Undefined, reserved)
Low	Low	High	User data
Low	High	Low	User program
Low	High	High	(Undefined, reserved)
High	Low	Low	(Undefined, reserved)
High	Low	High	Supervisor data
High	High	Low	Supervisor program
High	High	High	Interrupt acknowledge

Clock (CLK). The clock input is a TTL compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input shall be a constant frequency.

6.7 Logistic support. Lead material and finish (see 3.3), are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish "C" (see 3.3). Longer length leads and lead forming shall not affect the PIN.

6.8 Handling. MOS microprocessors should be handled with certain precautions to avoid damage due to the discharge of accumulated static charge. These NMOS devices are fabricated with a silicon gate technology, including input protection, which reduces the susceptibility to damage; however, the following handling practices are recommended.

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment and tools.
- c. Handling of devices by the leads should be avoided.
- d. Devices should be stored in conductive carriers.
- e. Avoid uses of plastic, rubber, or silk in MOS areas.

6.9 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	68000-6
02	68000-8
03	68000-10

CONCLUDING MATERIAL

Custodians:

Air Force - 17
Navy - EC
Army - ER

Preparing activity:
Air Force - 17

Agent:
DLA - ES

Review activities:

Army - AR, MI
Navy - OS, SH
Air Force - 11, 19, 85, 99
DLA - ES

(Project 5962-1174)

User activities:

Army - SM
Navy - AS, CG, MC