

MILITARY SPECIFICATION
 MICROCIRCUITS, DIGITAL, N-CHANNEL, SILICON GATE
 MONOLITHIC 16-BIT MICROPROCESSOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic N-channel, silicon gate microprocessor. One product assurance class (B) and a choice of case outline/lead finish are provided for each type, and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. The device type shall be as follows:

<u>Device type</u>	<u>Clock frequency</u>	<u>Circuit</u>
01	4.0 MHz	16-bit, fixed instruction microprocessor
02	4.0 MHz	16-bit, fixed instruction microprocessor
03	6.0 MHz	16-bit, fixed instruction microprocessor
04	6.0 MHz	16-bit, fixed instruction microprocessor

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

<u>Letter</u>	<u>Case outline, (see MIL-M-38510, appendix C)</u>
Q	D-5 (40-lead, 9/16" x 2-1/16" dual-in-line package)
X	See figure 1 (48-lead, 9/16" x 2-7/16" dual-in-line package)
Y	C-5 (44-terminal SQ chip carrier, .650" x .650") Option A
Z	C-6 (52-terminal SQ chip carrier, .750" x .750") Option A

1.3 Absolute maximum ratings.

V _{CC} supply voltage range (referenced to GND) -	-0.3 V to +7 V
Voltage on any pin (referenced to ground)- - -	-0.3 V to +7 V
Storage temperature range- - - - -	-65°C to +150°C
Power dissipation per package (all device types) - - - - -	2.5 W
Maximum power dissipation per device (all device types)	
T _C = -55°C - - - - -	2.3 W
T _C = +125°C - - - - -	1.6 W
Lead temperature (soldering, 5 seconds)- - -	270°C
Maximum junction temperature (T _J)	
at T _C = 125°C - - - - -	150°C
Thermal resistance, junction to case (θ _{JC}) (Case Q) - - - - -	30°C/W

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RADC (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

Supply voltage - - - - -	4.5 V min to 5.5 V max
Minimum high-level input voltage (V_{IH})	
Logic inputs - - - - -	2.4 V
Clock input - - - - -	$V_{CC} - 0.4$ V
Reset - - - - -	2.4 V
Maximum low-level input voltage (V_{IL})	
Logic and reset inputs - - - - -	0.8 V
Clock input - - - - -	0.45 V
Frequency of operation	
Device types 01 and 02 - - - - -	0.5 to 4.0 MHz
Device types 03 and 04 - - - - -	0.5 to 6.0 MHz
Case operating temperature range - - - - -	-55°C to +125°C
Clock rise time (t_r)	
Device types 01 and 02 - - - - -	20 ns max
Device types 03 and 04 - - - - -	10 ns max
Clock fall time (t_f)	
Device types 01 and 02 - - - - -	20 ns max
Device types 03 and 04 - - - - -	10 ns max

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION**MILITARY**

MIL-M-38510 - Microcircuits, General Specification For

STANDARD**MILITARY**

MIL-STD-883 - Test Methods and Procedures for Microelectronics

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections and pin assignments. The terminal connections and pin assignments shall be as specified on figure 2.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.3 Functional description, terms, and symbols. The functional description, terms, and symbols shall be as specified in 6.5.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3, herein.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.6).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ($T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$; $V_{CC} = 5.0\text{ V} \pm 10\%$ unless otherwise specified)	Figure no. 4/	Reference no. 3/	Device types								Limits		Unit	
					-01		-02		-03		-04					
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		Min
Clock input low voltage	V_{IL1}															
Clock input high voltage	V_{IH1}													-0.3	0.45	V
Input low voltage	V_{IL2}													$V_{CC} - 0.4$	$V_{CC} + 0.3$	V
Input high voltage	V_{IH2}													-0.3	0.8	V
RESET input high voltage	V_{IH3}													2.4	$V_{CC} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 2.0\text{ mA}$; $V_{CC} = 5.5\text{ V}$												2.4	$V_{CC} + 0.3$	V
Output high voltage	V_{OH}	$I_{OH} = -250\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$												2.4	0.4	V
Power supply current	I_{CC}	$V_{CC} = 5.5\text{ V}$														mA
Input high current (input and bidirectional)	I_{IH}	$V_{CC} = 5.5\text{ V}$; $V_{IN} = 2.4\text{ V}$												-10	± 10	μA
Input low current (input and bidirectional)	I_{IL}	$V_{CC} = 5.5\text{ V}$; $V_{IN} = 0.4\text{ V}$												-10	± 10	μA
Tristate output high leakage current (in float)	I_{ZH}	$V_{CC} = 5.5\text{ V}$; $V_{IN} = 2.4\text{ V}$												-10	± 10	μA
Tristate output low leakage current (in float)	I_{ZL}	$V_{CC} = 5.5\text{ V}$; $V_{IN} = 0.4\text{ V}$												-10	± 10	μA
Input clock capacitance	C_{I1}														50	pF
Input capacitance	C_{I2}														10	pF
Input capacitance-bidirectional inputs	C_{I3}														25	pF
Output capacitance, all other outputs	C_O														15	pF
Maximum clock frequency	f_{MAX}	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $C_L = 130\text{ pF} \pm 10\%$			4.0		4.0		6.0		6.0					MHz
Clock cycle time	t_{cyc}	$-55^\circ\text{C} \leq T_C \leq +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 130\text{ pF} \pm 10\%$	5	1	250	2,000	250	2,000	165	2,000	165	2,000				ns
Clock width (high)	t_{pH1}			2	105	1,895	105	1,895	70	1,930	70	1,930				ns
Clock width (low)	t_{pL1}			3	105	1,895	105	1,895	70	1,930	70	1,930				ns
WEQ width (high)	t_{pH7}			19	210	5/	210	5/	135	5/	135	5/				ns
AS width (low)	t_{pL2}			29	85	5/	85	5/	55	5/	55	5/				ns
DS (read) width (low)	t_{pL3}			38	275	5/	275	5/	185	5/	185	5/				ns
DS (write) width (low)	t_{pL4}			40	185	5/	185	5/	110	5/	110	5/				ns
DS (I/O) width (low)	t_{pL5}			43	410	5/	410	5/	255	5/	255	5/				ns
NM1 width (low)	t_{pL6}			51	100		100		70		70					ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	Figure no. 4/	Reference no. 3/	Device types										Limits		Unit
					-01		-02		-03		-04		Min	Max	Min	Max	
Data in to clock $\uparrow$ setup	t _{SLH1} t _{SHL1}	-55°C $\leq$ T _C $\leq$ +125°C V _{CC} = 5.0 V $\pm$ 10% C _L = 130 pF $\pm$ 10%	6	12	Min	Max	Min	Max	Min	Max	Min	Max	20	20			ns
RESET to clock $\uparrow$ setup	t _{SLH2} t _{SHL2}	"	"	49	180		180		70		70						"
VT, NVT to clock $\uparrow$ setup	t _{SLH3} t _{SHL3}	"	"	53	110		110		50		50						"
SEG $\uparrow$ to clock $\uparrow$ setup $\overline{1/}$	t _{SLH4} t _{SHL4}	"	"	55	70				55								"
MI to clock $\uparrow$ setup	t _{SLH5} t _{SHL5}	"	"	57	180		180		140		140						"
STOP to clock $\uparrow$ setup	t _{SLH6} t _{SHL6}	"	"	60	140		140		100		100						"
WAIT to clock $\uparrow$ setup	t _{SLH7} t _{SHL7}	"	"	62	50		50		30		30						"
BUSRQ to clock $\uparrow$ setup	t _{SLH8} t _{SHL8}	"	"	64	90		90		80		80						"
NVT to clock $\uparrow$ setup	t _{SHL9}	"	"	52	140		140		70		70						"
Data in to $\overline{DS}$ $\uparrow$ hold	t _{HLZ1} t _{HHZ1}	"	"	15	0		0		0		0						"
RESET to clock $\uparrow$ hold	t _{HLH1} t _{HHL1}	"	"	50	0		0		0		0						"
VT, NVT to clock $\uparrow$ hold	t _{HLH2} t _{HHL2}	"	"	54	20		20		20		20						"
SEG $\uparrow$ to clock $\uparrow$ hold $\overline{1/}$	t _{HLH3} t _{HHL3}	"	"	56	0		0		0		0						"
MI to clock $\uparrow$ hold	t _{HLH4} t _{HHL4}	"	"	58	0		0		0		0						"
STOP to clock $\uparrow$ hold	t _{HLH5} t _{HHL5}	"	"	61	0		0		0		0						"
WAIT to clock $\uparrow$ hold	t _{HLH6} t _{HHL6}	"	"	63	10		10		10		10						"
BUSRQ to clock $\uparrow$ hold	t _{HLH7} t _{HHL7}	"	"	65	10		10		10		10						"
Clock $\uparrow$ to segment number valid $\overline{1/}$	t _{2/t_{PLH1}} t _{PHL1}	"	"	6			130				110						"
Clock $\uparrow$ to segment number not valid $\overline{1/}$	t _{2/t_{PLH2}} t _{PHL2}	"	"	7	20				10								"
Clock $\uparrow$ to address valid	t _{2/t_{PLH3}} t _{PHL3}	"	"	9			100		100		75						"

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ($T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$; $V_{CC} = 5.0 \text{ V} \pm 10\%$ unless otherwise specified)	Figure no. 4/	Reference no. 3/	Device types										Limits		Unit
					-01		-02		-03		-04		Max		Min	Max	
Address valid to data in required valid	t_{PLH4} t_{PHL4}	$C_L = 130 \text{ pF} \pm 10\%$	6	11	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	ns
$\overline{DS} \uparrow$ to address active	t_{PZL1} t_{PZH1}	"	"	13	80 $\overline{5/}$	455 $\overline{5/}$	80 $\overline{5/}$	455 $\overline{5/}$	40	5/	305	5/	40	5/			"
$\overline{MREQ} \uparrow$ to address not active	t_{PLZ1} t_{PHZ1}	"	"	20	70 $\overline{5/}$	70 $\overline{5/}$	35	5/	35	5/	35	5/	35	5/			"
$\overline{AS} \uparrow$ to address not active	t_{PLZ2} t_{PHZ2}	"	"	30	60 $\overline{5/}$	60 $\overline{5/}$	30	5/	30	5/	30	5/	30	5/			"
Clock $\uparrow$ to address float	t_{PLZ3} t_{PHZ3}	"	"	10		90		90	75	75							"
Clock $\uparrow$ to bus float	t_{PLZ4} t_{PHZ4}	"	"	8		90		90	75	75							"
$\overline{MREQ} \uparrow$ to data in required valid	t_{PLH5} t_{PHL5}	"	"	22	350 $\overline{5/}$	350 $\overline{5/}$	225	5/	225	5/	225	5/	225	5/			"
$\overline{AS} \uparrow$ to data in required valid	t_{PLH6} t_{PHL6}	"	"	27	340 $\overline{5/}$	340 $\overline{5/}$	215	5/	215	5/	215	5/	215	5/			"
$\overline{DS} \text{ (read)} \uparrow$ to data in required valid	t_{PLH7} t_{PHL7}	"	"	33	185 $\overline{5/}$	185 $\overline{5/}$	130	5/	130	5/	130	5/	130	5/			"
$\overline{DS} \text{ (input)} \uparrow$ to data in required valid	t_{PLH8} t_{PHL8}	"	"	41	320 $\overline{5/}$	320 $\overline{5/}$	200	5/	200	5/	200	5/	200	5/			"
$\overline{DS} \text{ (Ack)} \uparrow$ to data in required valid	t_{PLH9} t_{PHL9}	"	"	46	435 $\overline{5/}$	435 $\overline{5/}$	295	5/	295	5/	295	5/	295	5/			"
Clock $\uparrow$ to data out valid	t_{PLH10} t_{PHL10}	"	"	14		100		100	75	75							"
$\overline{DS} \uparrow$ to data out not valid	t_{PLH11} t_{PHL11}	"	"	35	75 $\overline{5/}$	75 $\overline{5/}$	45	5/	45	5/	45	5/	45	5/			"
Clock $\uparrow$ to status valid delay	t_{PLH12} t_{PHL12}	"	"	47		110		110	85	85							"
Clock $\uparrow$ to $\overline{RD}$ delay	t_{PLH13} t_{PHL13}	"	"	59		120		120	85	85							"
Data out valid to $\overline{DS} \uparrow$ delay	t_{PLH14}	"	"	16	295 $\overline{5/}$	295 $\overline{5/}$	195	5/	195	5/	195	5/	195	5/			"
Data out valid to $\overline{DS} \uparrow$ (write) delay	t_{PHL14}	"	"	21	55 $\overline{5/}$	55 $\overline{5/}$	35	5/	35	5/	35	5/	35	5/			"
Address float to $\overline{DS} \uparrow$ (read) delay	t_{PHL15}	"	"	31	0	0	0	0	0	0	0	0	0	0			"
$\overline{AS} \uparrow$ to $\overline{DS} \uparrow$ (read) delay	t_{PHL16}	"	"	32	70 $\overline{5/}$	70 $\overline{5/}$	35	5/	35	5/	35	5/	35	5/			"
Clock $\uparrow$ to $\overline{DS} \uparrow$ delay	t_{PHL28}	"	"	34		70		70	65	65							"
Address valid to $\overline{DS} \uparrow$ (read) delay	t_{PHL17}	"	"	36	180 $\overline{5/}$	180 $\overline{5/}$	110	5/	110	5/	110	5/	110	5/			"

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ($T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$; $V_{CC} = 5.0\text{ V} \pm 10\%$ unless otherwise specified)	Figure no. 4/	Reference no. 3/	Device types												Limits		Unit
					-01			-02			-03			-04					
					Min	Max		Min	Max		Min	Max		Min	Max		Min	Max	
Clock $\uparrow$ to $\overline{\text{DS}} \downarrow$ (read) delay	t_{PHL18} 2/	$C_L = 130\text{ pF} \pm 10\%$	6	37		120			120			85			85			ns	
Clock $\uparrow$ to $\overline{\text{DS}} \downarrow$ (write) delay	t_{PHL19}	"	"	39		95			95			80			80			"	
Clock to $\overline{\text{DS}}$ (I/O) delay	t_{PHL20}	"	"	42		120			120			100			100			"	
$\overline{\text{AS}} \downarrow$ to $\overline{\text{DS}} \downarrow$ (Ack) delay	t_{PHL21}	"	"	44	1,065 5/		1,065 5/		1,065 5/		690 5/	690 5/			690 5/			"	
Clock $\uparrow$ to $\overline{\text{DS}} \downarrow$ (Ack) delay	t_{PHL22}	"	"	45		120			120			85			85			"	
Clock $\uparrow$ to $\overline{\text{DS}} \downarrow$ (Ack) delay	t_{PHL22}	"	"	17	55 $\overline{5/}$		55 $\overline{5/}$		55 $\overline{5/}$		35 $\overline{5/}$	35 $\overline{5/}$			35 $\overline{5/}$			"	
Address valid to $\overline{\text{MREQ}} \downarrow$ delay	t_{PHL23}	"	"	18		80			80			70			70			"	
Clock $\uparrow$ to $\overline{\text{MREQ}} \downarrow$ delay	t_{PHL24}	"	"	23		80			80			60			60			"	
Clock $\uparrow$ to $\overline{\text{AS}} \downarrow$ delay	t_{PHL25}	"	"	24		80			80			60			60			"	
Address valid to $\overline{\text{AS}} \downarrow$ delay	t_{PLH29}	"	"	25	55 $\overline{5/}$		55 $\overline{5/}$		55 $\overline{5/}$		35 $\overline{5/}$	35 $\overline{5/}$			35 $\overline{5/}$			"	
Clock $\uparrow$ to $\overline{\text{AS}} \downarrow$ delay	t_{PLH30}	"	"	26		90			90			80			80			"	
$\overline{\text{DS}} \uparrow$ to $\overline{\text{AS}} \downarrow$ delay	t_{PHL26}	"	"	28	70 $\overline{5/}$		70 $\overline{5/}$		70 $\overline{5/}$		35 $\overline{5/}$	35 $\overline{5/}$			35 $\overline{5/}$			"	
Status valid to $\overline{\text{AS}} \downarrow$ delay	t_{PLH31}	"	"	48	60 $\overline{5/}$		60 $\overline{5/}$		60 $\overline{5/}$		30 $\overline{5/}$	30 $\overline{5/}$			30 $\overline{5/}$			"	
Clock $\uparrow$ to $\overline{\text{BUSAR}} \downarrow$ delay	t_{PLH27}	"	"	66		100			100			75			75			"	
Clock $\uparrow$ to $\overline{\text{BUSAR}} \downarrow$ delay	t_{PHL27}	"	"	67		100			100			75			75			"	

1/ These parameters apply to the -01 and -03 parts only.

2/ Propagation delays and pulse widths are specified with load of figure 5 attached to output pins.

3/ The reference number refers to the position where the parameter being tested appears on figure 6.

4/ Figure 6 represents the electrical performance characteristics associated with the ac limits shown in table 1.

5/ These reference number parameters are dependent upon clock high or clock low or clock cycle time. The limits provided are at maximum frequency. To determine the limits at other frequencies use the following equations (see next page).

5/ - Continued.

Reference	Symbol	Device types 01 and 02	Device types 03 and 04
11	tPLH4 tPHL4	2 t _{cyc} + t _{PWH1} - 150 ns	2 t _{cyc} + t _{PWH1} - 95 ns
13	tpZL1 tpZH1	t _{PWL1} - 25 ns	t _{PWL1} - 30 ns
16	tPLH14	t _{cyc} + t _{PWH1} - 60 ns	t _{cyc} + t _{PWL1} - 40 ns
17	tPHL23	t _{PWH1} - 50 ns	t _{PWH1} - 35 ns
19	tPWH7	t _{cyc} - 40 ns	t _{cyc} - 30 ns
20	tPLZ1 tPHZ1	t _{PWL1} - 35 ns	t _{PWL1} - 35 ns
21	tPHL14	t _{PWH1} - 50 ns	t _{PWH1} - 35 ns
22	tPLH5 tPHL5	2 t _{cyc} - 150 ns	2 t _{cyc} - 105 ns
25	tPLH29	t _{PWH1} - 50 ns	t _{PWH1} - 35 ns
27	tPLH6 tPHL6	2 t _{cyc} - 160 ns	2 t _{cyc} - 115 ns
28	tPHL26	t _{PWL1} - 35 ns	t _{PWL1} - 35 ns
29	tPWL2	t _{PWH1} - 20 ns	t _{PWH1} - 15 ns
30	tPLZ2 tPHZ2	t _{PWL1} - 45 ns	t _{PWL1} - 40 ns
32	tPHL16	t _{PWL1} - 35 ns	t _{PWL1} - 35 ns
33	tPLH7 tPHL7	t _{cyc} + t _{PWH1} - 170 ns	t _{cyc} + t _{PWH1} - 105 ns
35	tPLH11 tPHL11	t _{PWL1} - 30 ns	t _{PWL1} - 25 ns
36	tPHL17	t _{cyc} - 70 ns	t _{cyc} - 55 ns
38	tPWL3	t _{cyc} + t _{PWH1} - 80 ns	t _{cyc} + t _{PWH1} - 50 ns
40	tPWL4	t _{cyc} - 65 ns	t _{cyc} - 55 ns
41	tPLH8 tPHL8	2 t _{cyc} - 180 ns	2 t _{cyc} - 130 ns
43	tPWL5	2 t _{cyc} - 90 ns	2 t _{cyc} - 75 ns
44	tPHL21	4 t _{cyc} + t _{PWL1} - 40 ns	4 t _{cyc} + t _{PWL1} - 40 ns
46	tPLH9 tPHL9	2 t _{cyc} + t _{PWH1} - 170 ns	2 t _{cyc} + t _{PWL1} - 105 ns
48	tPLH31	t _{PWH1} - 55 ns	t _{PWH1} - 40 ns

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I and on figure 6, and unless otherwise specified, apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III, table V, and figure 6.

3.6 Microprocessor instructions. The microprocessor instructions shall be as specified in table VI.

3.7 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in a microcircuit group number 107 (see MIL-M-38510, appendix E).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirement	Subgroups (see table III) Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	1,7
Final electrical test parameters (method 5004)	*1,2,3,*7,8,**9 10,11
Group A test requirements (method 5005)	1,2,3,4,7,8,*9 10,11,12
Group C end-point electrical parameters (method 5005)	1,2,3,7,8
Group D end-point electrical parameters (method 5005)	1,2,3,7,8

*PDA applies to subgroups 1 and 7 (see 4.2c).

**Subgroup 9 is run concurrently with subgroup 7 with a combined LTPD of 5.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, as applicable, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
 - (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameters test prior to burn-in, is at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) is specified as 10 percent for class B devices based on failures from group A, subgroups 1 and 7 tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA.

If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroups 1 and 7 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for the lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

- d. Constant acceleration in accordance with test condition D of method 2001 of MIL-STD-883.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.3).

4.3.1 Qualification extension. For qualification inspection, if a manufacturer qualifies to a higher frequency device type which is designed and manufactured identically to a lower frequency device type on this specification, then the lower frequency device type may be part I qualified by conducting only group A electrical tests and electricals specified as additional group C subgroups in table II (when authorized by the qualifying activity) and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.3).

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in table I of method 5005 of MIL-STD-883 and as follows:

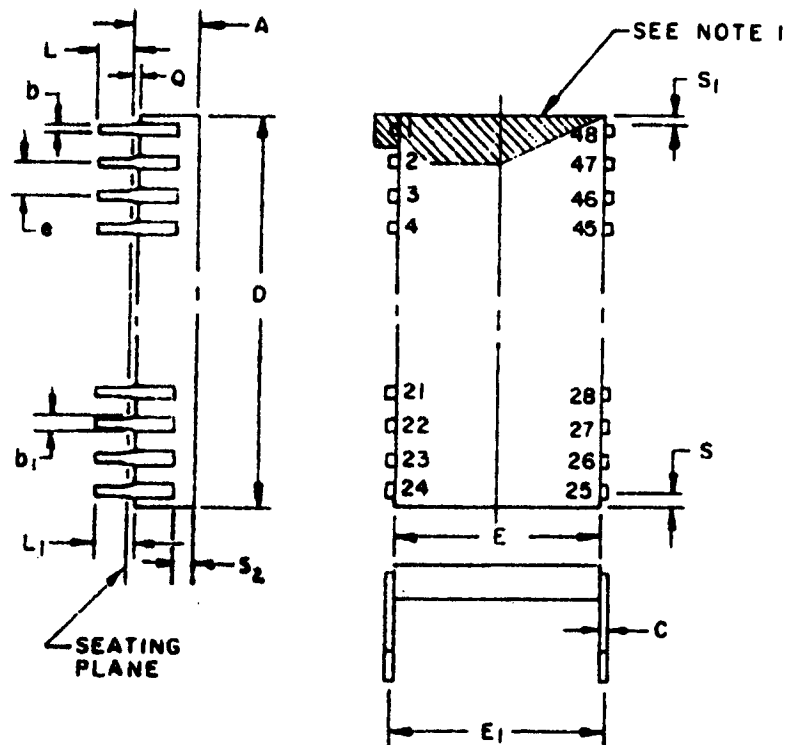
- a. Tests shall be as specified in table II, herein.
- b. Subgroup 4 (C_0 , C_{11} , C_{12} , and C_{13} measurements) shall be performed only for initial qualification and after process or design changes which may affect device capacitance. Tests 88-132 for device types 01 and 03 and tests 72-108 for device types 02 and 04 shall be performed on 5 devices. Test 10 additional devices with the exception that one test be chosen from the following test group and performed as representative of the test group. The representative tests that are chosen will be the worst case high measured values taken on the previous 5 units. The test groups are tests 98-113 for device types 01 and 03 and tests 81-96 for device types 02 and 04."
- c. Subgroup 12 shall be added to group A inspection requirements for class B devices using an LTPD of 10 and consist of the procedures, test conditions, and limits specified in table III. This subgroup shall be used for initial qualification only and variables data shall be submitted.
- d. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in table II of method 5005 of MIL-STD-883, and as follows: A special subgroup shall be added to the group B inspection requirements for class B. This subgroup shall consist of the test, conditions, and limits specified in 4.5.2. The LTPD for this subgroup shall be 15.

4.4.3 Groups C and D inspections. Groups C and D inspections shall consist of the test subgroups and LTPD values shown in tables III and IV of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II, herein.

TEXT CONTINUES ON PAGE 75.



NOTES:

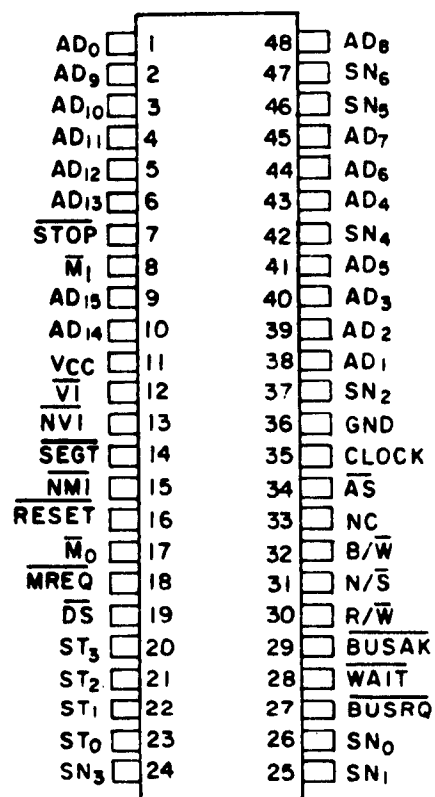
1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be .020 (.51 mm) for leads number 1, 24, 25, and 48 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within $\pm .010$ (.25 mm) of its exact longitudinal position relative to pins 1 and 48.
5. Applies to all four corners (leads number 1, 24, 25, and 48), and 40.5 shall apply.
6. Leads center when α is 0° . E_1 shall be measured at the centerline of the leads (see 40.4 of appendix C of MIL-M-38510).
7. All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
8. Forty six spaces.
9. The top edge of lead shall not extend above the brazed pad top surface.

FIGURE 1. Case outline X (48-lead, 9/16" x 2-7/16" dual-in-line package).

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	---	.225	---	5.72	
b	.014	.023	.36	.58	7
b ₁	.030	.070	.76	1.78	2,7
c	.008	.015	.20	.28	7
D	---	2.480	---	63.00	
E	.510	.620	12.95	15.75	
E ₁	.520	.620	13.21	15.75	6
e	.100 BSC		2.54 BSC		4,8
L	.120	.200	3.05	5.08	
L ₁	.150	---	3.81	---	
Q	.020	.060	.51	1.52	3
S	---	.098	---	2.49	5
S ₁	.005	---	.13	---	5
S ₂	.005	---	.13	---	9

FIGURE 1. Case outline X (48-lead, 9/16" x 2-7/16" dual-in-line package) - Continued.

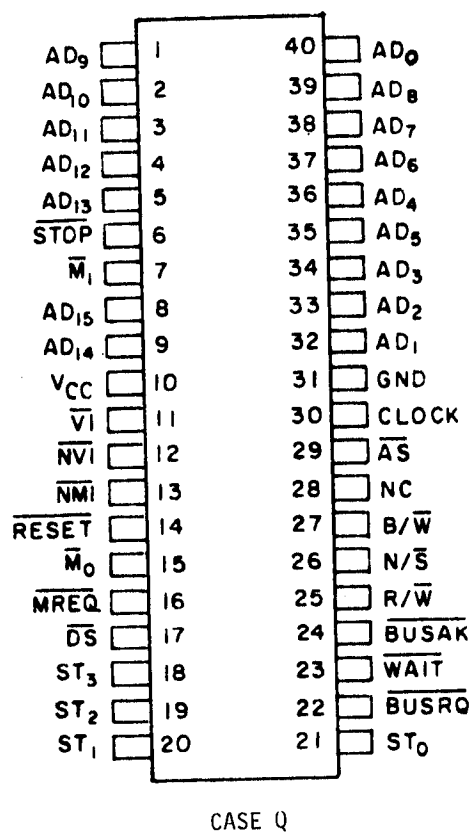
Device types 01 and 03

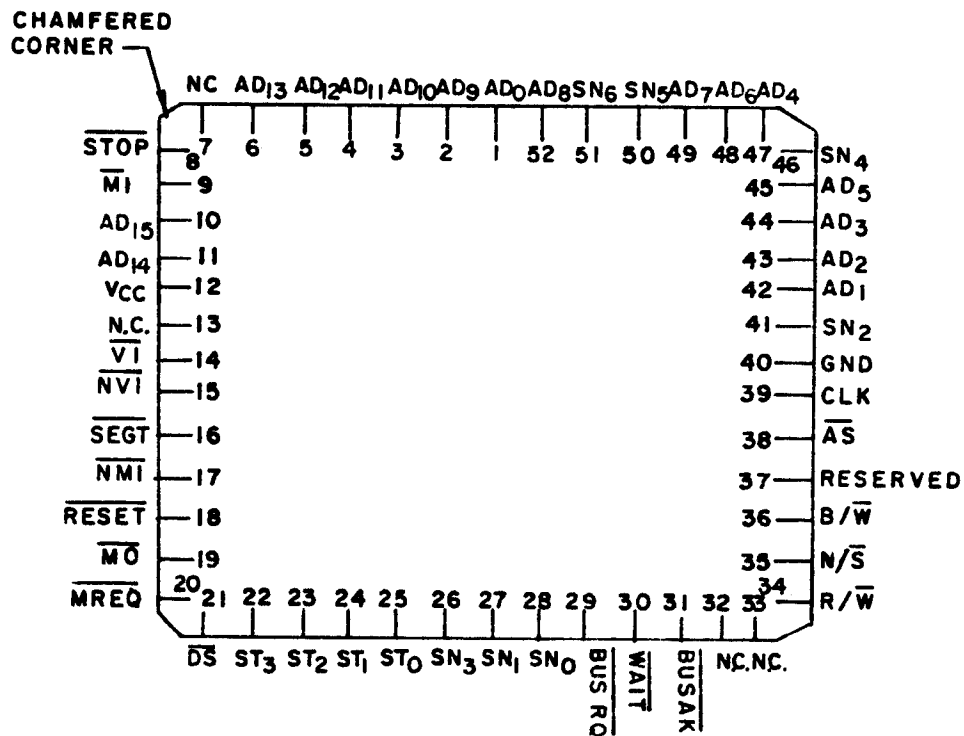


CASE X

FIGURE 2. Terminal connections and pin assignments.

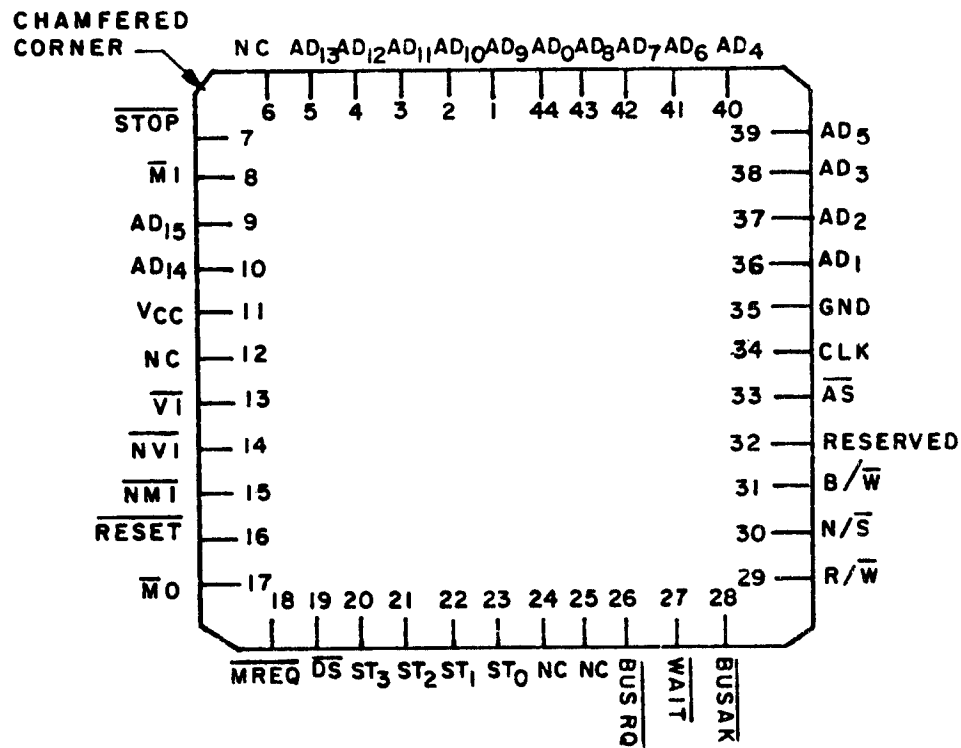
Device types 02 and 04

FIGURE 2. Terminal connections and pin assignments - Continued.



DEVICE TYPES 01 AND 03
N.C.=NO CONNECTION

FIGURE 2. Terminal connections (case outline Z, 52-terminal SQ chip carrier) - Continued.



DEVICE TYPES 02 AND 04
NC = NO CONNECTION

FIGURE 2. Terminal connections (case outline Y, 44-terminal SQ chip carrier) - Continued.

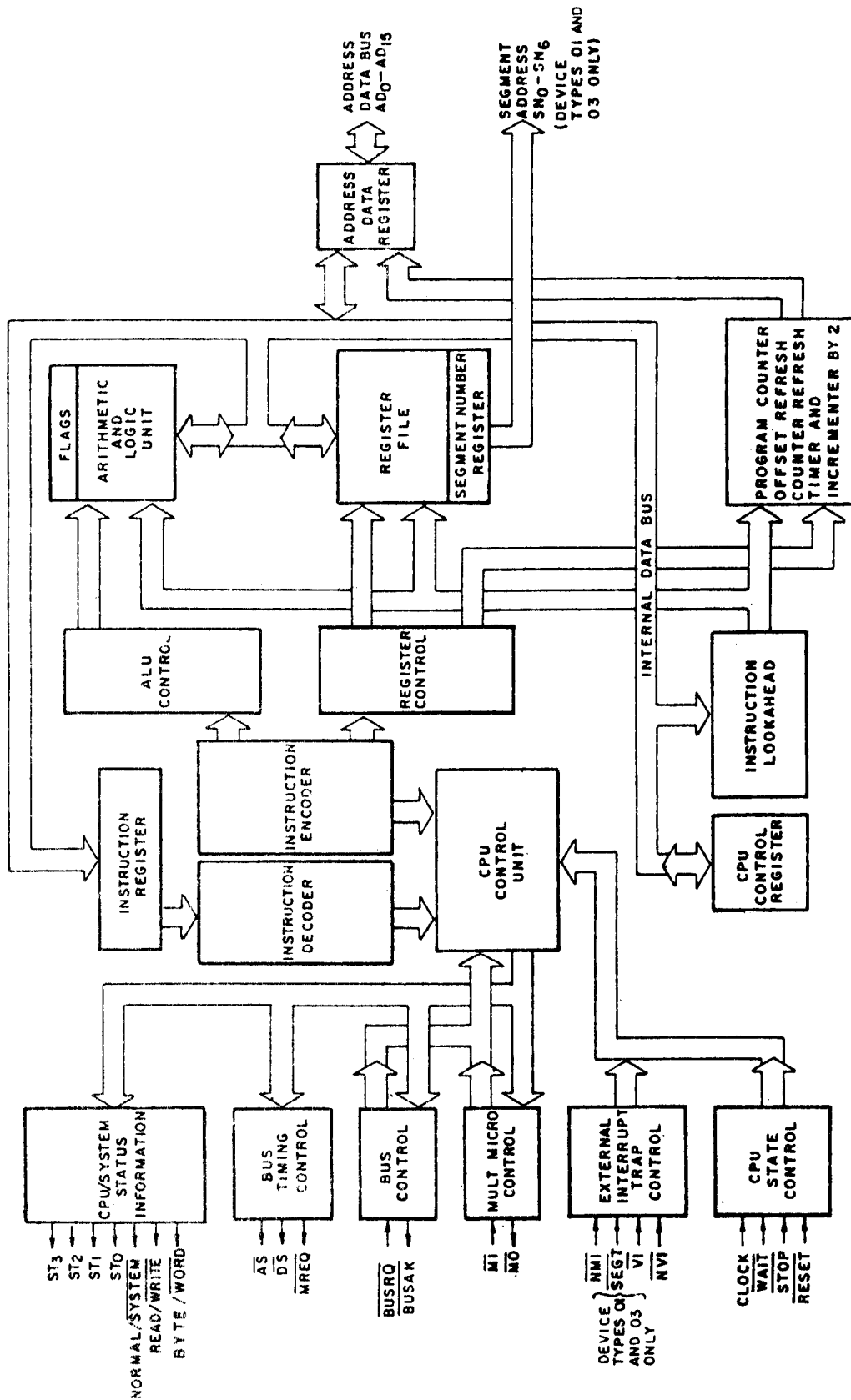
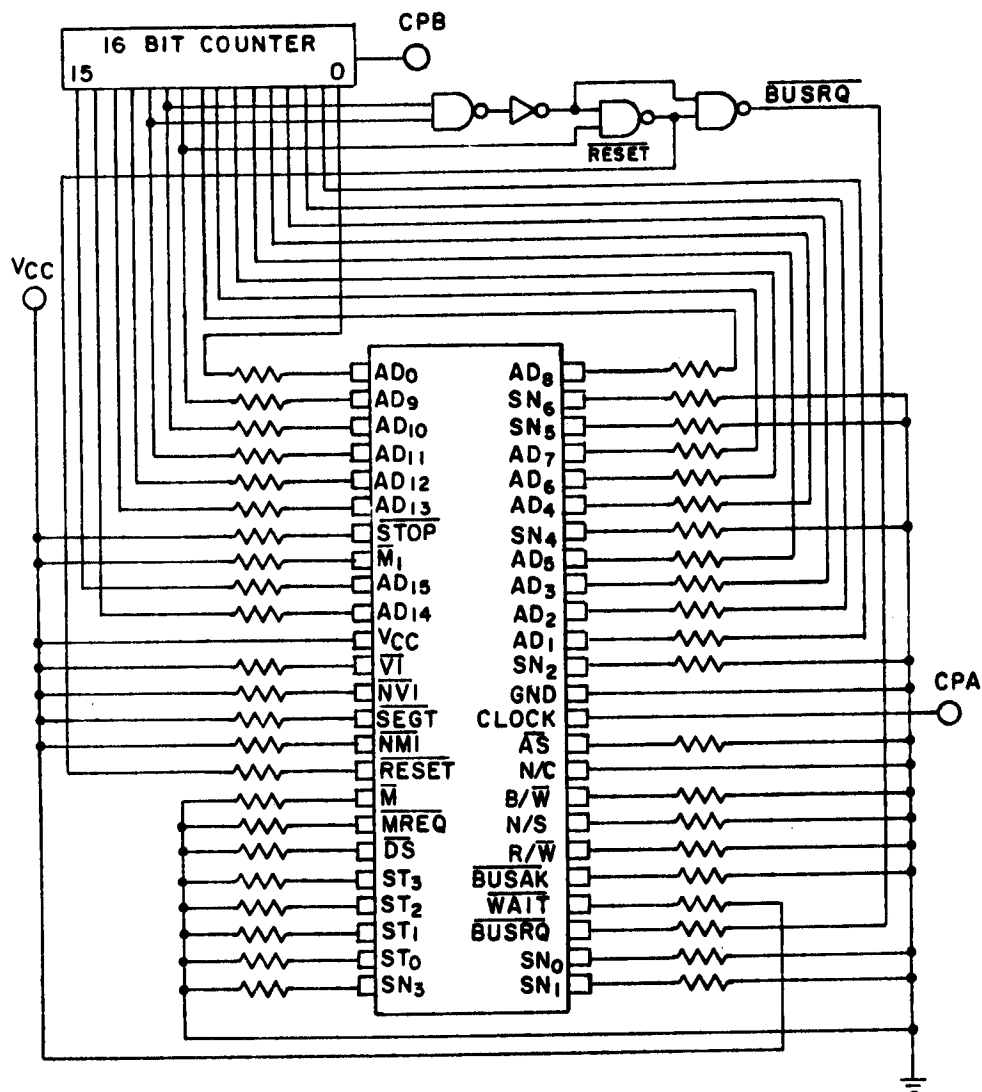


FIGURE 3. Functional block diagram.

Device types 01 and 03

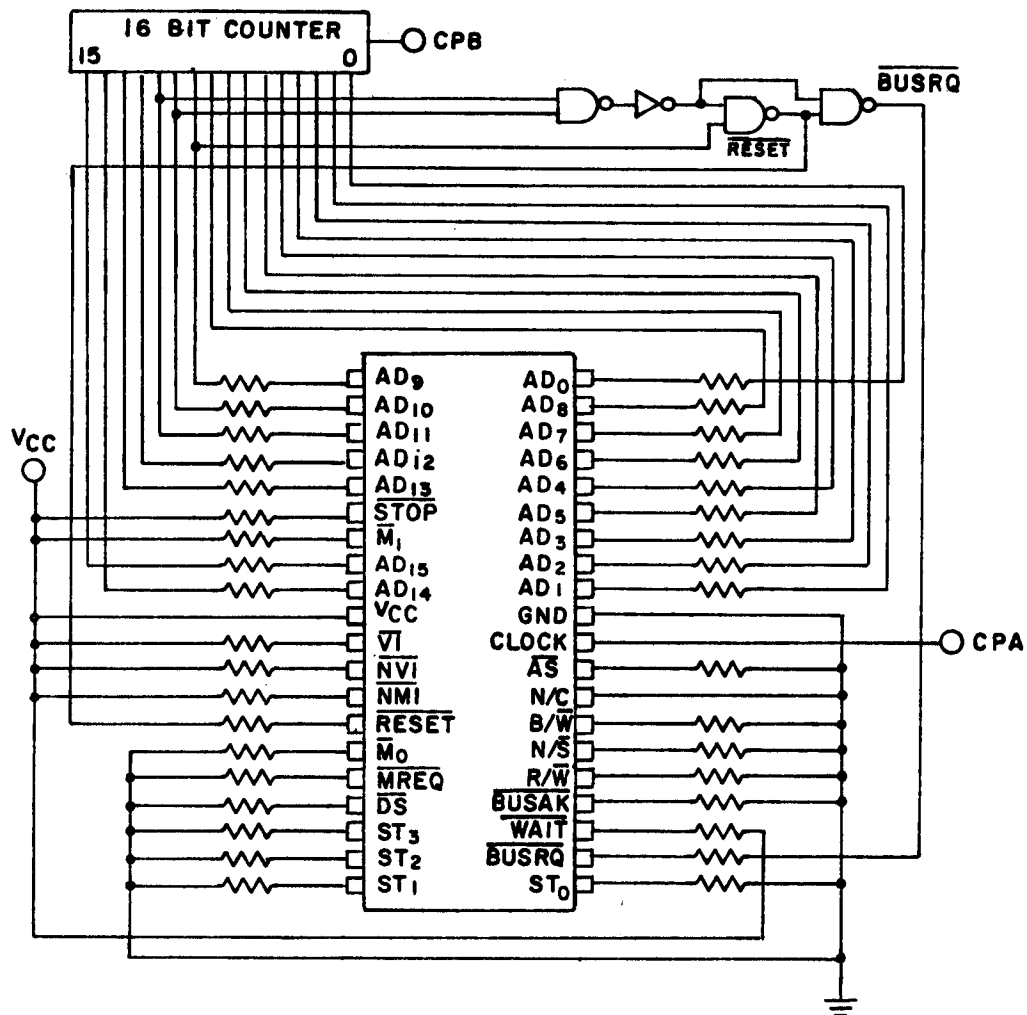


NOTES:

- NOTES:
1. CPA = 250 kHz $\pm 10\%$ square wave; 50% duty cycle.
 2. VCC shall be no less than 4.5 V at device terminal.
VCC shall be no more than 5.5 V at device terminal.
 3. VIL shall be no more than 0.5 V at device terminal.
VIH shall be no less than VCC - 0.4 V at device terminal.
 4. All resistors shall be 10 k Ω $\pm 10\%$ 1/4 W minimum.
 5. CPB = 0.1 Hz $\pm 10\%$ square wave; 50% duty cycle.

FIGURE 4. Dynamic burn-in and life test.

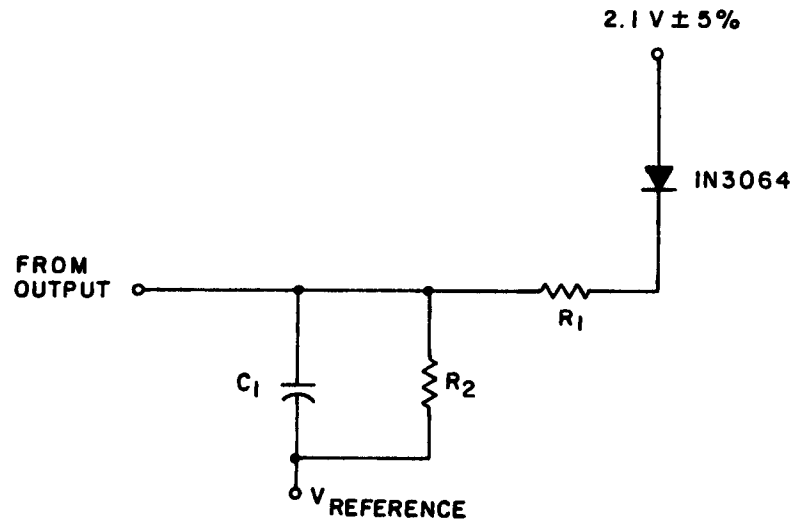
Device types 02 and 04



NOTES:

1. CPA = 250 kHz $\pm 10\%$ square wave; 50% duty cycle.
2. VCC shall be no less than 4.5 V at device terminal.
VCC shall be no more than 5.5 V at device terminal.
3. VIL shall be no more than 0.5 V at device terminal.
VIH shall be no less than VCC - 0.4 V at device terminal.
4. All resistors shall be 10 k Ω $\pm 10\%$ 1/4 W minimum.
5. CPB = 0.1 Hz $\pm 10\%$ square wave; 50% duty cycle.

FIGURE 4. Dynamic burn-in and life test - Continued.



NOTES:

1. $R_1 = 550\Omega \pm 5\%$.
2. $R_2 = 9.6\text{ k}\Omega \pm 5\%$.
3. $C_1 = 130\text{ pF} \pm 20\%$.
4. $V_{\text{REFERENCE}} = \text{GND}$ except for tests 145 and 146 for device types 01 and 03, and tests 121 and 122 for device types 02 and 04 during which $V_{\text{REFERENCE}} = -10\text{ V}$.
5. During tests 145 and 146 (device types 01 and 03) and tests 121 and 122 (device types 02 and 04) testing proceeds as follows:
 - a. Search actual V_{OH} and V_{OL} levels during output data drive time of DUT.
 - b. Set tester output comparators to:
 - V_{OH} (1 level) = Search value - 0.050 volts
 - V_{OL} (0 level) = Search value + 0.050 volts
 - c. Search with appropriate timing generator for data out not valid (tri-state).
 - d. Compare search value < limits -- force error if not true.

FIGURE 5. Output load circuit for functional and ac testing.

TABLE III. Group A inspection for device types 01 and 03.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883C Method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	I_{CC}	3005	1							2.4 V	2.4 V			5.5 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V								
$T_C = 25^\circ\text{C}$	I_{IH}		2	12.4 V																							
			3		2.4 V																						
			4																								
			5																								
			6																								
			7																								
			8																								
			9																								
			10																								
			11																								
			12																								
			13																								
			14																								
			15																								
			16																								
			17																								
	I_{ZH}		18																								
			19																								
			20																								
			21																								
			22																								
			23																								
			24																								
			25																								
			26																								
			27																								
			28																								
			29																								
			30																								
			31																								
			32																								
			33																								
			34																								
	I_{IL}		35																								
			36																								
			37																								
			38																								
			39																								
			40																								
			41																								
			42																								
			43																								
			44																								
			45	10.4 V																							
			46		10.4 V																						
			47			10.4 V																					
			48				10.4 V																				
			49					10.4 V																			
			50						10.4 V																		
			51							10.4 V																	
			52								10.4 V																
			53									10.4 V															
			54										10.4 V														
			55											10.4 V													
			56												10.4 V												
			57													10.4 V											
			58														10.4 V										
			59															10.4 V									
			60																10.4 V								

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (pins not designated are open)

Test no.	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	Measured terminal	Test Limits Min	Test Limits Max	Unit
1	SW1	SKO	BUSRQ	WATT	BUSRQ	WATT	N/S	B/W	MC	AS	CLK	GND	SH2	AD1	AD2	AD3	AD5	SH4	AD4	AD6	AD7	SH5	SH6	AD8	VCC	20	275	mA
2											5.1 V														AD0	20	210	mA
3																									AD9			
4																									AD10			
5																									AD11			
6																									AD12			
7																									AD13			
8																									AD14			
9																									AD15			
10																									AD1			
11																									AD2			
12																									AD3			
13																									AD5			
14																									AD6			
15																									AD7			
16																									AD8			
17																												
18																									ST3			
19																									ST2			
20																									ST1			
21																									SH0			
22																									SH3			
23																									SH1			
24	2.4 V																								SH2			
25		2.4 V																							SH4			
26																									SH5			
27																									SH6			
28																												
29																												
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See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 - Continued.

[illegible]

See footnotes at end of device types 01 and 03

See footnotes at end of device types 01 and 03.

[illegible]

TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (pins not designated are open)

Terminal conditions (pins not designated as I/O inputs)																												
Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
				AD	AP	AD10	AD11	AD12	AD13	STOP	MI	AD15	AD14	VCC	VT	WT	SEGT	MMI	RESET	MO	WREQ	DS	ST3	ST2	ST1	S10	SM3	
1 T _C = 25°C	V _{OH}		123	-250 μA	-250 μA	-250 μA	-250 μA	-250 μA	-250 μA	2.4 V	2.4 V	-250 μA	-250 μA	4.5 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V								
			124																									
			125																									
			126																									
			127																									
			128																									
			129																									
			130																									
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152																												
153																												
154																												
155																												
156																												
157																												
2	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = +125°C and I _{CC} = 220 mA.																											
3	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = -55°C and I _{CC} = 350 mA.																											
4 T _C = 25°C	C11		158	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	
			159																									
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TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (pins not designated are open)

Test no.	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	Measured terminal	Test Limits Min	Test Limits Max	Unit
123	SM1	SH0	BUSRQ	WAIT	BUSAK	N/A	N/S	B/F	NC	AS	CLK	CHD	SH2	AD1	AD2	AD3	AD5	SH4	AD4	AD6	AD7	SH5	SH6	AD8	AD0	2.4	V	
124			12.4 V								4.1 V	10.0 V													AD9			
125																									AD10			
126																									AD11			
127																									AD12			
128																									AD13			
129																									AD14			
130																									AD1			
131																									AD2			
132																									AD3			
133																									AD5			
134																									AD6			
135																									AD7			
136																									AD8			
137																									ST3			
138																									ST2			
139																									ST1			
140																									SH3			
141																									SH1			
142																									SH0			
143																									SH2			
144																									SH5			
145																									SH6			
146																									SH4			
147																									SH0			
148																									SH5			
149																									SH6			
150																									SH4			
151																									SH5			
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179																									SH6			
180																									SH4			
181																									SH5			
182																									SH6			
183																									SH4			

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883C Method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
				AD0	AD9	AD10	AD11	AD12	AD13	STOP	MI	AD15	AD14	VCC	VI	WVI	SEGT	WMI	RESET	MO	WREQ	DS	ST3	ST2	ST1	ST0	SW3	
4 T _C = 25°C	C ₀		184	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	
			185	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	
			186	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	
			187	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	
			188	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	
			189	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	
			190	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	
			191	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	
			192	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	
			193	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	
			194	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	
195	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V				
196	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V				
197	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V				
198	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V				
199	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V			
200	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V			
201	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V			
202	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V			
7	3/ 3A/ 3014																			2/ 10.0 V	2/ 10.0 V	2/ 10.0 V	2/ 10.0 V	2/ 10.0 V	2/ 10.0 V	2/ 10.0 V		
8	Same tests, terminal conditions, and limits as for subgroup 7, except T _C = +125°C and T _C = -55°C 3/ 3A/																											
9	3/ 3A/ 3/ 3A/ 3/ 3A/																			2/ 10.0 V	2/ 10.0 V	2/ 10.0 V	2/ 10.0 V	2/ 10.0 V	2/ 10.0 V	2/ 10.0 V		
10	3/ 3A/ 3/ 3A/ 3/ 3A/																											
11	3/ 3A/ 3/ 3A/ 3/ 3A/																											

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (pins not designated are open)

Test no.																										Measured terminal	Test Limits		Unit
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	Min		Max		
	SN1	SN0	BUSRQ	WAIT	BUSAK	IR/M	N/S	B/M	NC	AS	CLK	GND	SN2	AD1	AD2	AD3	AD5	SN4	AD4	AD6	AD7	SN5	SN6	AD8					
184	0.0 V	2/	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	SN0	15	pF		
185	0.0 V	0.0 V											0.0 V												SN1				
186	0.0 V												0.0 V												SN2				
187													0.0 V												SN3				
188																		2/							SN4				
189																		0.0 V				0.0 V	2/			SN5			
190																									SN6				
191																									ST0				
192																									ST1				
193																									ST2				
194																									ST3				
195																									BUSAK				
196																									R/M				
197																									N/S				
198																									R/M				
199																									R/M				
200																									R/M				
201																									R/M				
202																									R/M				

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T _C = 25°C and +125°C	Figure number 4/	Reference number 9/	-01		-03		Unit
				Min	Max	Min	Max	
	Symbol	Terminal						
203 <u>8/</u>	tpMH7	$\overline{MREQ}$	19	210		135		ns
204 <u>8/</u>	tpWL2	$\overline{AS}$	29	85		55		"
205 <u>8/</u>	tpWL3	$\overline{DS}$	38	275		185		"
206 <u>8/</u>	tpWL4	$\overline{DS}$	40	185		110		"
207 <u>8/</u>	tpWL5	$\overline{DS}$	43	410		255		"
208 <u>6/</u>	tpLH1 tpHL1	SN0 - SN6	6		130		110	"
209 <u>6/</u>	tpLH2 tpHL2	SN0 - SN6	7	20		10		"
210 <u>6/</u>	tpLH3 tpHL3	AD0 - AD15	9		100		75	"
211 <u>6/</u> <u>8/</u>	tpLH4 tpHL4	AD0 - AD15	11	455		305		"
212 <u>6/</u> <u>8/</u>	tpZL1 tpZH1	AD0 - AD15	13	80		40		"

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T _C = 25°C and +125°C	Figure number 4/ 9/	Reference number 9/	-01		-03		Unit
				Min	Max	Min	Max	
	Symbol	Terminal						
213 <u>6/</u> <u>8/</u>	t _{PLZ1} t _{PHZ1}	AD ₀ - AD ₁₅	6	20		35		ns
214 <u>6/</u> <u>8/</u>	t _{PLZ2} t _{PHZ2}	AD ₀ - AD ₁₅	"	30		60		"
215 <u>6/</u>	t _{PLZ3} t _{PHZ3}	AD ₀ - AD ₁₅	"	10	90		75	"
216	t _{PLZ4} t _{PHZ4}	AS, SN ₀ - SN ₆ , DS, B/W, AD ₀ - AD ₁₅ , R/W, N/S, MREQ, ST ₀ - ST ₃	"	8	90		75	"
217 <u>6/</u> <u>8/</u>	t _{PLH5} t _{PHL5}	AD ₀ - AD ₁₅	"	22	350		225	"
218 <u>6/</u> <u>8/</u>	t _{PLH6} t _{PHL6}	AD ₀ - AD ₁₅	"	27	340		215	"
219 <u>6/</u> <u>8/</u>	t _{PLH7} t _{PHL7}	AD ₀ - AD ₁₅	"	33	185		130	"
220 <u>6/</u> <u>8/</u>	t _{PLH8} t _{PHL8}	AD ₀ - AD ₁₅	"	41	320		200	"

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T _C = 25°C and +125°C	Symbol	Terminal	Figure number 4/	Reference number 9/	-01		-03		Unit
						Min	Max	Min	Max	
221 <u>6/</u> <u>8/</u>		t _{PLH9} t _{PHL9}	AD ₀ - AD ₁₅	6	46	435		295		ns
222 <u>6/</u>		t _{PLH10} t _{PHL10}	AD ₀ - AD ₁₅	"	14		100		75	"
223 <u>6/</u> <u>8/</u>		t _{PLH11} t _{PHL11}	AD ₀ - AD ₁₅	"	35	75		45		"
224		t _{PLH12} t _{PHL12}	R/ <u>M</u> , B/ <u>M</u> , ST ₀ - ST ₃ , N/ <u>S</u>	"	47		110		85	"
225		t _{PLH13} t _{PHL13}	<u>M</u> ₀	"	59		120		85	"
226 <u>8/</u>		t _{PLH14}	<u>D</u> _S	"	16	295		195		"
227 <u>8/</u>		t _{PHL14}	<u>D</u> _S	"	21	55		35		"
228		t _{PHL15}	<u>D</u> _S	"	31	0		0		"
229 <u>8/</u>		t _{PHL16}	<u>D</u> _S	"	32	70		35		"
230		t _{PLH28}	<u>D</u> _S	"	34		70		65	"

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 3/ - Continued.

Test number	10/ II/ Subgroup 12, $T_C = 25^\circ\text{C}$ and $+125^\circ\text{C}$	Symbol	Terminal	Figure number 4/	Reference number 9/	-01			-03			Unit
						Min	Max		Min	Max		
231 8/		t _{PHL17}	$\overline{DS}$	6	36	180			110			ns
232		t _{PHL18}	$\overline{DS}$	"	37		120			85		"
233		t _{PHL19}	$\overline{DS}$	"	39		95			80		"
234		t _{PHL20}	$\overline{DS}$	"	42		120			100		"
235 8/		t _{PHL21}	$\overline{DS}$	"	44	1,065			690			"
236		t _{PHL22}	$\overline{DS}$	"	45		120			85		"
237 8/		t _{PHL23}	$\overline{MREQ}$	"	17	55			35			"
238		t _{PHL24}	$\overline{MREQ}$	"	18		80			70		"
239		t _{PLH24}	$\overline{MREQ}$	"	23		80			60		"
240		t _{PHL25}	$\overline{AS}$	"	24		80			60		"
241 8/		t _{PLH29}	$\overline{AS}$	"	25	55			35			"

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T _C = 25°C and +125°C	Figure number 4/ <u> </u>	Reference number 9/ <u> </u>	-01		-03		Unit
				Min	Max	Min	Max	
	Symbol	Terminal						
242	t _{PLH30}	$\overline{AS}$	26		90		80	ns
243 <u>8/</u>	t _{PHL26}	$\overline{AS}$	28	70		35		"
244 <u>8/</u>	t _{PLH31}	$\overline{AS}$	48	60		30		"
245	t _{PLH27}	$\overline{BUSAK}$	66		100		75	"
246	t _{PHL27}	$\overline{BUSAK}$	67		100		75	"

- 1/ Apply input conditions and pulse CLK until ~~BUSAK~~ is low.
- 2/ The capacitance measurements shall be made between the indicated terminal and ground at a frequency of 1 MHz. The dc bias of the measuring instrument shall be less than ± 0.1 V. The ac signal amplitude shall be less than 50 mV rms.
- 3/ For subgroups 7, 8, 9, 10, 11, and 12 tests input conditions A, B, C, D, E, F, G, and H appear in table IV (see footnotes 7 and 10).
- 3A/ For subgroups 7, 8, 9, 10, and 11 tests output conditions A0, B0, C0, D0, E0, F0, G0, and H0 appear in table IV.
- 4/ Figure 6 represents the timing diagrams associated with subgroups 7, 8, 9, 10, 11, and 12.
- 5/ All subgroups 9, 10, and 11 tests are run concurrently with subgroups 7 and 8.
- 6/ Where propagation delay tests for subgroup 12 indicate a group of pins and where two or more propagation delays are specified for a test, only the reading for the pin with the worst case delay requires recording. In some cases this will be a minimum reading, while in others it will be a maximum as indicated in the table.
- 7/ For subgroup 12 input conditions A-D will each be individually used when making measurements for device type 01. Input conditions E-H will each be individually used for device type 03.
- 8/ These reference number parameters are dependent upon clock high or clock low or clock cycle time. The limits provided are at maximum frequency. To determine the limits at other frequencies use the equations in footnote 5 of table I herein.
- 9/ The reference number refers to the position where the parameter being measured appears on figure 6.
- 10/ Subgroup 12 tests are the only tests for which an ac data value is actually recorded. Subgroups 7, 8, 9, 10, and 11 are pass/fail tests and shall be checked by an automated tester controlled by the test software represented in table V using input and output conditions of table IV.
- 11/ Limits shown for subgroup 12 are from f_{MAX} input conditions A, B, E, and F of table IV. The limits for f_{MIN} input conditions C, D, G, and H are not shown.

TABLE III. Group A inspection for device types 02 and 04. Terminal conditions (pins not designated are open).

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				AD ₉	AD ₁₀	AD ₁₁	AD ₁₂	AD ₁₃	STOP	WT	AD ₁₅	AD ₁₄	V _{CC}	VT	WYT	WMT	RESET	WD	WREQ	DS	ST ₃	ST ₂	ST ₁
1	I _{CC}	3005	1						2.0 V	2.0 V			5.5 V	2.0 V	2.0 V	2.0 V	2.0 V						
T _C = 25°C	I _{TH} 1/		2	2.4 V	2.4 V	2.4 V	2.4 V																
			3																				
			4																				
			5																				
			6																				
			7																				
			8																				
			9																				
			10																				
			11																				
			12																				
			13																				
			14																				
			15																				
			16																				
			17																				
				I _{ZH}		18																	
			19																				
			20																				
			21																				
			22																				
			23																				
			24																				
			25																				
			26																				
			27																				
	I _{IH}		28						2.4 V	2.4 V													
			29						2.4 V	2.4 V													
			30											2.4 V	2.4 V								
			31																				
			32																				
			33																				
			34																				
			35																				
			36																				
	I _{IL}		37	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V															
			38																				
			39																				
			40																				
			41																				
			42																				
			43																				
			44																				
			45																				
			46																				
			47																				
			48																				
			49																				
			50																				
			51																				
			52																				

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04.
Terminal conditions (pins not designated are open).

Test no.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits		Unit
																						Min	Max	
1	ST ₀	BUSRQ	WATT	BUSAR	R/W	N/S	B/W	NC	AS	CLK	GND	AD ₁	AD ₂	AD ₃	AD ₅	AD ₄	AD ₆	AD ₇	AD ₈	AD ₀	VCC			mA
2										5.1 V	GND													
3												2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V				
4																								
5																								
6																								
7																								
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20																								
21	2.4 V																							
22																								
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25																								
26																								
27									2.4 V															
28																								
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49																								
50																								
51																								
52																								

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 - Continued.
Terminal conditions (pins not designated are open).

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1 $T_C = 25^\circ\text{C}$	I_{ZL}		53 54 55 56 57 58 59 60 61 62	AD ₉	AD ₁₀	AD ₁₁	AD ₁₂	AD ₁₃	STOP	NT	AD ₁₅	AD ₁₄	V_{CC}	VT	NVI	NMI	RESET	M $\bar{O}$	MREQ	DS	ST ₃	ST ₂	ST ₁
									2.4 V	2.4 V			5.5 V	2.4 V	2.4 V	2.4 V	2.4 V				0.4 V	0.4 V	0.4 V
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
	I_{IL}		63 64 65 66 67 68 69 70 71						0.4 V	0.4 V			"	"	"	"	"						
									2.4 V	0.4 V			"	"	"	"	"						
									"	2.4 V			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
									"	"			"	"	"	"	"						
	I_{OL}		72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99	2.0 mA	2.0 mA	2.0 mA	2.0 mA	2.0 mA					4.5 V										
	I_{OH}		100 101 102 103 104 105 106 107 108 109 110	-250 μA	-250 μA	-250 μA	-250 μA	-250 μA															

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 - Continued.
Terminal conditions (pins not designated are open).

Test no.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits		Unit
																						Min	Max	
	ST ₀	BUSRQ	WATT	BUSAK	R/W	N/S	B/W	NC	XS	CLK	GND	AD ₁	AD ₂	AD ₃	AD ₅	AD ₄	AD ₆	AD ₇	AD ₈	AD ₀				
53		0.8 V	2.4 V							5.1 V	GND										ST ₃	-10	10	μA
54		"	"							"	"										ST ₂	"	"	"
55		"	"							"	"										ST ₁	"	"	"
56	0.4 V	"	"							"	"										ST ₀	"	"	"
57		"	"							"	"										MREQ	"	"	"
58		"	"							"	"										R/W	"	"	"
59		"	"		0.4 V					"	"										N/S	"	"	"
60		"	"		0.4 V		0.4 V			"	"										B/W	"	"	"
61		"	"						0.4 V	"	"										DS	"	"	"
62		"	"							"	"										AS	"	"	"
63		"	"							"	"										STOP	"	"	"
64		"	"							"	"										PI	"	"	"
65		"	"							"	"										VI	"	"	"
66		"	"							"	"										NMI	"	"	"
67		"	"							"	"										NMI	"	"	"
68		"	"							"	"										RESET	"	"	"
69		"	0.4 V							"	"										WATT	"	"	"
70		"	2.4 V							0.4 V	"										CLK	"	"	"
71		0.4 V	2.4 V							5.1 V	"										BUSRQ	"	"	"
72		2.4 V	"							4.1 V	10.0 V										AD ₉			0.4 V
73		"	"							"	"										AD ₁₀			"
74		"	"							"	"										AD ₁₁			"
75		"	"							"	"										AD ₁₂			"
76		"	"							"	"										AD ₁₃			"
77		"	"							"	"										AD ₁₄			"
78		"	"							"	"										AD ₁₅			"
79		"	"							"	"	2.0 mA									AD ₁			"
80		"	"							"	"		2.0 mA								AD ₂			"
81		"	"							"	"			2.0 mA							AD ₃			"
82		"	"							"	"				2.0 mA						AD ₅			"
83		"	"							"	"					2.0 mA					AD ₄			"
84		"	"							"	"						2.0 mA				AD ₆			"
85		"	"							"	"							2.0 mA			AD ₇			"
86		"	"							"	"								2.0 mA		AD ₈			"
87		"	"							"	"									2.0 mA	AD ₀			"
88		"	"							"	"										ST ₃			"
89		"	"							"	"										ST ₂			"
90		"	"							"	"										ST ₁			"
91	2.0 mA	"	"							"	"										ST ₀			"
92		"	"							"	"										MREQ			"
93		"	"							"	"										R/W			"
94		"	"							"	"										N/S			"
95		"	"							"	"										B/W			"
96		"	"							"	"										DS			"
97		"	"							"	"										AS			"
98		"	"							"	"										MO			"
99		0.8 V	"	2.0 mA						"	"										BUSAK			"
100		"	"							"	"										AD ₉	2.4		"
101		"	"							"	"										AD ₁₀	"		"
102		"	"							"	"										AD ₁₁	"		"
103		"	"							"	"										AD ₁₂	"		"
104		"	"							"	"										AD ₁₃	"		"
105		"	"							"	"										AD ₁₄	"		"
106		"	"							"	"										AD ₁₅	"		"
107		"	"							"	"										AD ₁	"		"
108		"	"							"	"										AD ₂	"		"
109		"	"							"	"										AD ₃	"		"
110		"	"							"	"										AD ₅	"		"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04.
(terminal conditions (pins not designated are open).)

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
				AD9	AD10	AD11	AD12	AD13	STOP	M1	AD15	AD14	VCC	VT	NVI	NMT	RESET	M0	MREQ	DS	ST3	ST2	ST1	
1 TC = 25°C	VOH		111						2.4 V	2.4 V			4.5 V	2.4 V	2.4 V	2.4 V	2.4 V							
			112																					
			113																					
			114																					
			115																					
			116																					
			117																					
			118																					
			119																					
			120																					
	121																							
	122																							
	123																							
	124																							
	125																							
	126																							
	127																							
2				Same tests, terminal conditions, and limits as for subgroup 1, except TC = +125°C, and ICC = 220 mA.																				
3				Same tests, terminal conditions, and limits as for subgroup 1, except TC = -55°C, and ICC = 350 mA.																				
4 TC = 25°C	C11		128	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	
		C12	129	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			130	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			131	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			132	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			133	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			134	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			135	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			136	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			C13	137	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
138	"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
139	"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
140	"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
141	"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
142	"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
143	"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
144	"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
145	"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
146	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
147	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
148	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
149	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
150	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
151	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
152	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			
C0	153	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
	154	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
	155	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
	156	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
	157	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
	158	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
	159	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		
	160	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"								

See footnotes at end of device types 02 and 04.

TABLE III. Group A Inspector
Terminal condition
Ins not designated are open).
"r device types 02 and 04 - Continued.

[illegible]

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04.
Terminal conditions (pins not designated are open).

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				AD ₉	AD ₁₀	AD ₁₁	AD ₁₂	AD ₁₃	STOP	MT	AD ₁₅	AD ₁₄	V _{CC}	VT	WYT	WMT	RESET	MO	PREQ	DS	ST ₃	ST ₂	ST ₁
7	3/ 3A/ 4/ 5/	3014		See 6.2 and table VI.																			
8	3/ 3A/ 4/ 5/			Same tests, terminal conditions, and limits as for subgroup 7, except T _C = +125°C, and T _C = -55°C.																			
9	3/ 3A/ 4/ 5/																						
10	3/ 3A/ 4/ 5/			Repeat subgroup 9 at T _C = +125°C.																			
11	3/ 3A/ 4/ 5/			Repeat subgroup 9 at T _C = -55°C.																			

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 - Continued.
Terminal conditions (pins not designated are open).

Test no.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits		Unit
	ST ₀	BUSRQ	WATT	BUSAK	R/W	N/S	B/W	NC	AS	CLK	GND	AD ₁	AD ₂	AD ₃	AD ₅	AD ₄	AD ₆	AD ₇	AD ₈	AD ₀		Min	Max	

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 3/ - Continued.

Test number	10/ 11/ Subgroup 12, $T_C = 25^\circ\text{C}$ and $+125^\circ\text{C}$	Figure number 4/	Reference number 9/	-02		-04		Unit
				Min	Max	Min	Max	
	Symbol	Terminal						
165 <u>8/</u>	tpWH7	MREQ	19	210		135		ns
166 <u>8/</u>	tpWL2	AS	29	85		55		"
167 <u>8/</u>	tpWL3	DS	38	275		185		"
168 <u>8/</u>	tpWL4	DS	40	185		110		"
169 <u>8/</u>	tpWL5	DS	43	410		255		"
170 <u>6/</u>	tplH3 tPHL3	AD0 - AD15	9		100		75	"
171 <u>6/</u> <u>8/</u>	tplH4 tPHL4	AD0 - AD15	11	455		305		"
172 <u>6/</u> <u>8/</u>	tpZL1 tpZH1	AD0 - AD15	13	80		40		"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 3/ - Continued.

Test number	Symbol	Terminal	Figure number 4/	Reference number 9/	-02		-04		Unit
					Min	Max	Min	Max	
173 <u>6/</u> <u>8/</u>	tPLZ1 tPHZ1	AD0 - AD15	6	20	70		35		ns
174 <u>6/</u> <u>8/</u>	tPLZ2 tPHZ2	AD0 - AD15	"	30	60		30		"
175 <u>6/</u>	tPLZ3 tPHZ3	AD0 - AD15	"	10		90		75	"
176	tPLZ4 tPHZ4	AS, SNQ - SN6, DS, B/W, AD0 - AD15, R/W, N/S, MREQ, ST0 - ST3	"	8		90		75	"
177 <u>6/</u> <u>8/</u>	tPLH5 tPHL5	AD0 - AD15	"	22	350		225		"
178 <u>6/</u> <u>8/</u>	tPLH6 tPHL6	AD0 - AD15	"	27	340		215		"
179 <u>6/</u> <u>8/</u>	tPLH7 tPHL7	AD0 - AD15	"	33	185		130		"
180 <u>6/</u> <u>8/</u>	tPLH8 tPHL8	AD0 - AD15	"	41	320		200		"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 3/ - Continued.

Test number	^{10/} II/ Subgroup 12, T _C = 25°C and +125°C	Figure number 4/	Reference number 9/	-02		-04		Unit
				Min	Max	Min	Max	
181 <u>6/</u> <u>8/</u>	t _{PLH9} t _{PHL9}	6	46	435		295		ns
182 <u>6/</u>	t _{PLH10} t _{PHL10}	"	14		100		75	"
183 <u>6/</u> <u>8/</u>	t _{PLH11} t _{PHL11}	"	35	75		45		"
184	t _{PLH12} t _{PHL12}	"	47		110		85	"
185	t _{PLH13} t _{PHL13}	"	59		120		85	"
186 <u>8/</u>	t _{PLH14}	"	16	295		195		"
187 <u>8/</u>	t _{PHL14}	"	21	55		35		"
188	t _{PHL15}	"	31	0		0		"
189 <u>8/</u>	t _{PHL16}	"	32	70		35		"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T _C = 25° and +125°C	Figure number 4/	Reference number 9/	-02		-04		Unit
				Min	Max	Min	Max	
190	t _{PLH28}	6	34		70		65	ns
191 8/	t _{PHL17}	"	36	180		110		"
192	t _{PHL18}	"	37		120		85	"
193	t _{PHL19}	"	39		95		80	"
194	t _{PHL20}	"	42		120		100	"
195 8/	t _{PHL21}	"	44	1065		690		"
196	t _{PHL22}	"	45		120		85	"
197 8/	t _{PHL23}	"	17	55		35		"
198	t _{PHL24}	"	18		80		70	"
199	t _{PLH24}	"	23		80		60	"
200	t _{PHL25}	"	24		80		60	"
201 8/	t _{PLH29}	"	25	55		35		"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 3/ - Continued.

Test number	10/ II/ Subgroup 12, $T_C = 25^\circ$ and $+125^\circ C$	Figure number 4/ <u> </u>	Reference number 9/ <u> </u>	-02		-04		Unit
				Min	Max	Min	Max	
202	tPLH30	6	26		90		80	ns
203 <u>8/</u>	tPHL26	"	28	70		35		"
204 <u>8/</u>	tPLH31	"	48	60		30		"
205	tPLH27	"	66		100		75	"
206	tPHL27	"	67		100		75	"

See footnotes at end of device types 02 and 04.

- 1/ Apply input conditions and pulse CLK until BUSAK is low.
- 2/ The capacitance measurements shall be made between the indicated terminal and ground at a frequency of 1 MHz. The dc bias of the measuring instrument shall be less than ± 0.1 V. The ac signal amplitude shall be less than 50 mV rms.
- 3/ For subgroups 7, 8, 9, 10, 11 and 12 tests input conditions A, B, C, D, E, F, G and H appear in table IV (see footnotes 7 and 10).
- 3A/ For subgroups 7, 8, 9, 10, and 11 tests output conditions A0, B0, C0, D0, E0, F0, G0, and H0 appear in table IV.
- 4/ Figure 6 represents the timing diagrams associated with subgroups 7, 8, 9, 10, 11, and 12.
- 5/ All subgroups 9, 10, and 11 tests are run concurrently with subgroups 7 and 8.
- 6/ Where propagation delay tests for subgroup 12 indicate a group of pins and where two or more propagation delays are specified for a test, only the reading for the pin with the worst case delay requires recording. In some cases this will be a minimum reading, while for others it will be a maximum as indicated in the table.
- 7/ For subgroup 12 input conditions A-D will each be individually used when making measurements for device type 02. Input conditions E-H will each be individually used for device type 04.
- 8/ These reference number parameters are dependent upon clock high or clock low or clock cycle time. The limits provided are at maximum frequency. To determine the limits at other frequencies use the equations in footnote 5 of table I herein.
- 9/ The reference number refers to the position where the parameter being measured appears on figure 6.
- 10/ Subgroup 12 tests are the only test for which an ac data value is actually recorded. Subgroups 7, 8, 9, 10, and 11 are pass/fail tests and shall be checked by an automated tester controlled by the test software represented in table V using input and output conditions in table IV.
- 11/ Limits shown in subgroup 12 are from f_{MAX} input conditions A, B, E, and F of table IV. The limits for f_{MIN} input conditions C, D, G, and H are not shown.

TABLE IV. Input conditions for device types 01 and 02 functional tests.

Symbol	Reference 2/	Terminal(s)	A 5/	B 5/	C 5/	D 5/	Unit
V _{CC}		V _{CC}	5.5	4.5	4.5	4.5	V
V _{IH2}		Logic inputs	2.4	2.4	2.4	2.4	V
V _{IL2}		Logic inputs	0.8	0.8	0.8	0.8	V
V _{IH1}		CLK	5.1	4.1	4.1	4.1	V
V _{IL1}		CLK	0.45	0.45	0.45	0.45	V
t _{cyc}	1	CLK	250	250	2,000	2,000	ns
t _{PWH1} 4/	2	CLK	105		105		ns
t _{PWL1} 4/	3	CLK		105		105	ns
t _{PWL6}	51	<u>NMI</u>	100	100	100	100	ns
t _{SLH1} }	12	AD ₀ -AD ₁₅	50	50	50	50	ns
t _{SHL1} }							
t _{SLH2} }	49	<u>RESET</u>	180	180	180	180	ns
t _{SHL2} }							
t _{SLH3} }	53	<u>VT</u> , <u>NVT</u>	110	110	110	110	ns
t _{SHL3} }							
t _{SLH5} }	57	<u>MT</u>	180	180	180	180	ns
t _{SHL5} }							
t _{SLH6} }	60	<u>STOP</u>	140	140	140	140	ns
t _{SHL6} }							
t _{SLH7} }	62	<u>WAIT</u>	50	50	50	50	ns
t _{SHL7} }							
t _{SLH8} }	64	<u>BUSRQ</u>	90	90	90	90	ns
t _{SHL8} }							
t _{SLH9}	52	<u>NMI</u>	140	140	140	140	ns
t _{SLH4} }	3/ 55	<u>SEGT</u>	70	70	70	70	ns
t _{SHL4} }							
t _{HLH3} }	3/ 56	<u>SEGT</u>	0	0	0	0	ns
t _{HHL3} }							

See footnotes at end of device types 01 and 02.

TABLE IV. Input conditions for device types 01 and 02 functional tests - Continued.

Symbol	Reference <u>2/</u>	Terminal(s)	A <u>5/</u>	B <u>5/</u>	C <u>5/</u>	D <u>5/</u>	Unit <u>5/</u>
t_{HLZ1} t_{HHZ1}	15	AD ₀ -AD ₁₅	0	0	0	0	ns
t_{HLH1} t_{HHL1}	50	RESET	0	0	0	0	ns
t_{HLH2} t_{HHL2}	54	V _I , N _{VI}	20	20	20	20	ns
t_{HLH4} t_{HHL4}	58	MT	0	0	0	0	ns
t_{HLH5} t_{HHL5}	61	STOP	0	0	0	0	ns
t_{HLH6} t_{HHL6}	63	WAIT	10	10	10	10	ns
t_{HLH7} t_{HHL7}	65	BUSRQ	10	10	10	10	ns

See footnotes at end of device types 01 and 02.

TABLE IV. Output conditions for device types 01 and 02 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	A0 6/	B0 6/	C0 6/	D0 6/	Unit 6/
V _{OH}		Outputs	2.0	2.0	2.0	2.0	V
V _{OL}		Outputs	0.8	0.8	0.8	0.8	V
t _{PWL2} 1/	29	$\overline{AS}$	85	85			ns
t _{PWL3} 1/	38	$\overline{DS}$	275	275			ns
t _{PWL4} 1/	40	$\overline{DS}$	185	185			ns
t _{PWL5} 1/	43	$\overline{DS}$	410	410			ns
t _{PWH7} 1/	19	MREQ	210	210			ns
t _{PLH1} } 3/ t _{PHL1}	6	SN ₀ -SN ₆	130	130	130	130	ns
t _{PZL1} } 1/ t _{PZH1}	13	AD ₀ -AD ₁₅	80	80			ns
t _{PLZ1} } 1/ t _{PHZ1}	20	AD ₀ -AD ₁₅	70	70			ns
t _{PLH2} } 3/ t _{PHL2}	7	SN ₀ -SN ₆	20	20	20	20	ns
t _{PLZ2} } 1/ t _{PHZ2}	30	AD ₀ -AD ₁₅	60	60			ns
t _{PLH3} } t _{PHL3}	9	AD ₀ -AD ₁₅	100	100	100	100	ns
t _{PLZ3} } 1/ t _{PHZ3}	10	AD ₀ -AD ₁₅	90	90	90	90	ns
t _{PLH4} } 1/ t _{PHL4}	11	AD ₀ -AD ₁₅	455	455			ns
t _{PLZ4} } 1/ t _{PHZ4} } 3/	8	AD ₀ -AD ₁₅ , $\overline{AS}$, $\overline{DS}$, B/W, R/W, N/S, MREQ, ST ₀ -ST ₃ , SN ₀ -SN ₆	90	90	90	90	ns
t _{PLH5} } 1/ t _{PHL5}	22	AD ₀ -AD ₁₅	350	350			ns
t _{PLH6} } 1/ t _{PHL6}	27	AD ₀ -AD ₁₅	340	340			ns
t _{PLH7} } 1/ t _{PHL7}	33	AD ₀ -AD ₁₅	185	185			ns

See footnotes at end of device types 01 and 02.

TABLE IV. Output conditions for device types 01 and 02 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	A0 6/	B0 6/	C0 6/	D0 6/	Unit
tPLH8} 1/ tPHL8}	41	AD ₀ -AD ₁₅	320	320			ns
tPLH9} 1/ tPHL9}	46	AD ₀ -AD ₁₅	435	435			ns
tPLH10} tPHL10}	14	AD ₀ -AD ₁₅	100	100	100	100	ns
tPLH11} 1/ tPHL11}	35	AD ₀ - AD ₁₅	75	75			ns
tPLH12} tPHL12}	47	ST ⁰ -ST ₃	110	110	110	110	ns
tPLH13} tPHL13}	59	M0	120	120	120	120	ns
tPLH14 1/ tPHL14 1/	16 21	DS DS	295 55	295 55			ns ns
tPHL15	31	DS	0	0	0	0	ns
tPHL16 1/	32	DS	70	70			ns
tPHL17 1/	36	DS	180	180			ns
tPHL18	37	DS	120	120	120	120	ns
tPHL19	39	DS	95	95	95	95	ns
tPHL20	42	DS	120	120	120	120	ns
tPLH20	66	BUSAK	100	100	100	100	ns
tPHL21 1/	44	DS	1,065	1,065			ns
tPHL22	45	DS	120	120	120	120	ns
tPHL23 1/	17	MREQ	55	55			ns
tPHL24	18	MREQ	80	80	80	80	ns
tPLH24	23	MREQ	80	80	80	80	ns
tPHL25	24	AS	80	80	80	80	ns
tPLH28	34	DS	70	70	70	70	ns
tPLH29 1/	25	AS	55	55			ns

TABLE IV. Output conditions for device types 01 and 02 functional tests - Continued.

Symbol	Reference <u>2/</u>	Terminal(s)	A0 <u>6/</u>	B0 <u>6/</u>	C0 <u>6/</u>	D0 <u>6/</u>	Unit
t _{PLH30}	26	$\overline{AS}$	90	90	90	90	ns
t _{PHL26} <u>1/</u>	28	$\overline{AS}$	70	70			ns
t _{PHL27}	67	BUSAK	100	100	100	100	ns
t _{PLH31} <u>1/</u>	48	$\overline{AS}$	60	60			ns

1/ Limits for output conditions C and D are calculated using footnote 5 of table I herein. (These parameters are dependent upon the clock high, clock low or clock cycle time).

2/ The reference number refers to the position where the parameter being measured appears on figure 6.

3/ For device type 01 only.

4/ Clock input high or low or cycle times for device types 01 and 02 shall be 20 ns maximum.

5/ Input conditions A and B are at f_{MAX} , input conditions C and D are at f_{MIN} .

6/ Output conditions A0 and B0 are at f_{MAX} , output conditions C0 and D0 are at f_{MIN} .

TABLE IV. Input conditions for device types 03 and 04 functional tests.

Symbol	Reference 2/	Terminal(s)	E 5/	F 5/	G 5/	H 5/	Unit
V _{CC}		V _{CC}	5.5	4.5	4.5	4.5	V
V _{IH2}		Logic inputs	2.4	2.4	2.4	2.4	V
V _{IL2}		Logic inputs	0.8	0.8	0.8	0.8	V
V _{IH1}		CLK	5.1	4.1	4.1	4.1	V
V _{IL1}		CLK	0.45	0.45	0.45	0.45	V
t _{cyc}	1	CLK	165	165	2,000	2,000	ns
t _{PWH1} 4/	2	CLK	70		70		ns
t _{PWL1} 4/	3	CLK		70		70	ns
t _{PWL6}	51	NMI	70	70	70	70	ns
t _{SLH1} } t _{SHL1} }	12	AD ₀ -AD ₁₅	20	20	20	20	ns
t _{SLH2} } t _{SHL2} }	49	RESET	70	70	70	70	ns
t _{SLH3} } t _{SHL3} }	53	VI, NVI	50	50	50	50	ns
t _{SLH5} } t _{SHL5} }	57	MI	140	140	140	140	ns
t _{SLH6} } t _{SHL6} }	60	STOP	100	100	100	100	ns
t _{SLH7} } t _{SHL7} }	62	WAIT	30	30	30	30	ns
t _{SLH8} } t _{SHL8} }	64	BUSRQ	80	80	80	80	ns
t _{SLH9}	52	NMI	70	70	70	70	ns
t _{SLH4} } t _{SHL4} }	3/ 55	SEGT	55	55	55	55	ns
t _{HLH3} } t _{HHL3} }	3/ 56	SEGT	0	0	0	0	ns
t _{HLZ1} } t _{HHZ1} }	15	AD ₀ -AD ₁₅	0	0	0	0	ns

See footnotes at end of device types 03 and 04.

TABLE IV. Input conditions for device types 03 and 04 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	E 5/	F 5/	G 5/	H 5/	Unit
t _{HLH1}	50	RESET	0	0	0	0	ns
t _{HHL1}							
t _{HLH2}	54	VI, $\overline{\text{NVI}}$	20	20	20	20	ns
t _{HHL2}							
t _{HLH4}	58	MT	0	0	0	0	ns
t _{HHL4}							
t _{HLH5}	61	STOP	0	0	0	0	ns
t _{HHL5}							
t _{HLH6}	63	WAIT	10	10	10	10	ns
t _{HHL6}							
t _{HLH7}	65	BUSRQ	10	10	10	10	ns
t _{HHL7}							

See footnotes at end of device types 03 and 04.

TABLE IV. Output conditions for device types 03 and 04 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	E0 6/	F0 6/	G0 6/	H0 6/	Unit
V _{OH}		Outputs	2.0	2.0	2.0	2.0	V
V _{OL}		Outputs	0.8	0.8	0.8	0.8	V
t _{PWL2} 1/	29	$\overline{AS}$	55	55			ns
t _{PWL3} 1/	38	$\overline{DS}$	185	185			ns
t _{PWL4} 1/	40	$\overline{DS}$	110	110			ns
t _{PWL5} 1/	43	$\overline{DS}$	255	255			ns
t _{PWH7} 1/	19	$\overline{MREQ}$	135	135			ns
t _{PLH1} } 3/ t _{PHL1}	6	SN ₀ -SN ₆	110	110	110	110	ns
t _{PZL1} } 1/ t _{PZH1}	13	AD ₀ -AD ₁₅	40	40			ns
t _{PLZ1} } 1/ t _{PHZ1}	20	AD ₀ -AD ₁₅	35	35			ns
t _{PLH2} } 3/ t _{PHL2}	7	SN ₀ -SN ₆	10	10	10	10	ns
t _{PLZ2} } 1/ t _{PHZ2}	30	AD ₀ -AD ₁₅	30	30			ns
t _{PLH3} } t _{PHL3}	9	AD ₀ -AD ₁₅	75	75	75	75	ns
t _{PLZ3} } t _{PHZ3}	10	AD ₀ -AD ₁₅	75	75	75	75	ns
t _{PLH4} } 1/ t _{PHL4}	11	AD ₀ -AD ₁₅	305	305			ns
t _{PLZ4} } t _{PHZ4}	8	AD ₀ -AD ₁₅ , $\overline{AS}$, $\overline{DS}$, B/W, R/W, N/S, $\overline{MREQ}$, ST ₀ -ST ₃ , SN ₀ -SN ₆	75	75	75	75	ns
t _{PLH5} } 1/ t _{PHL5}	22	AD ₀ -AD ₁₅	225	225			ns
t _{PLH6} } 1/ t _{PHL6}	27	AD ₀ -AD ₁₅	215	215			ns

See footnotes at end of device types 03 and 04.

TABLE IV. Output conditions for device types 03 and 04 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	E0 6/	F0 6/	G0 6/	H0 6/	Unit
t _{PLH7} 1/	33	AD ₀ -AD ₁₅	130	130			ns
t _{PHL7}							
t _{PLH8} 1/	41	AD ₀ -AD ₁₅	200	200			ns
t _{PHL8}							
t _{PLH9} 1/	46	AD ₀ -AD ₁₅	295	295			ns
t _{PHL9}							
t _{PLH10}	14	AD ₀ -AD ₁₅	75	75	75	75	ns
t _{PHL10}							
t _{PLH11} 1/	35	AD ₀ -AD ₁₅	45	45			ns
t _{PHL11}							
t _{PLH12}	47	ST ₀ -ST ₃	85	85	85	85	ns
t _{PHL12}							
t _{PLH13}	59	M0	85	85	85	85	ns
t _{PHL13}							
t _{PLH14} 1/	16	DS	195	195			ns
t _{PHL14} 1/	21	DS	35	35			ns
t _{PHL15}	31	DS	0	0	0	0	ns
t _{PHL16} 1/	32	DS	35	35			ns
t _{PHL17} 1/	36	DS	110	110			ns
t _{PHL18}	37	DS	85	85	85	85	ns
t _{PHL19}	39	DS	80	80	80	80	ns
t _{PLH20}	66	BUSAK	75	75	75	75	ns
t _{PHL20}	42	DS	100	100	100	100	ns
t _{PHL21} 1/	44	DS	690	690			ns
t _{PHL22}	45	DS	85	85	85	85	ns
t _{PHL23} 1/	17	MREQ	35	35			ns
t _{PHL24}	18	MREQ	70	70	70	70	ns
t _{PLH24}	23	MREQ	60	60	60	60	ns

TABLE IV. Output conditions for device types 03 and 04 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	E0 6/	F0 6/	G0 6/	H0 6/	Unit
t _{PHL25}	24	$\overline{AS}$	60	60	60	60	ns
t _{PLH28}	34	$\overline{DS}$	65	65	65	65	ns
t _{PLH29} 1/	25	$\overline{AS}$	35	35			ns
t _{PLH30}	26	$\overline{AS}$	80	80	80	80	ns
t _{PHL26} 1/	28	$\overline{AS}$	35	35			ns
t _{PHL27}	67	$\overline{BUSAK}$	75	75	75	75	ns
t _{PLH31} 1/	48	$\overline{AS}$	30	30			ns

1/ Limits for output conditions G and H are calculated using footnote 5 of table I herein. (These parameters are dependent upon the clock high or clock low).

2/ The reference number refers to the position where the parameter being measured appears on figure 6.

3/ For device type 03 only.

4/ Clock input high or low or cycle times for device types 03 and 04 shall be 10 ns maximum

5/ Input conditions E and F are at f_{MAX} , input conditions G and H are at f_{MIN} .

6/ Output conditions E0 and F0 are at f_{MAX} , output conditions G0 and H0 are at f_{MIN} .

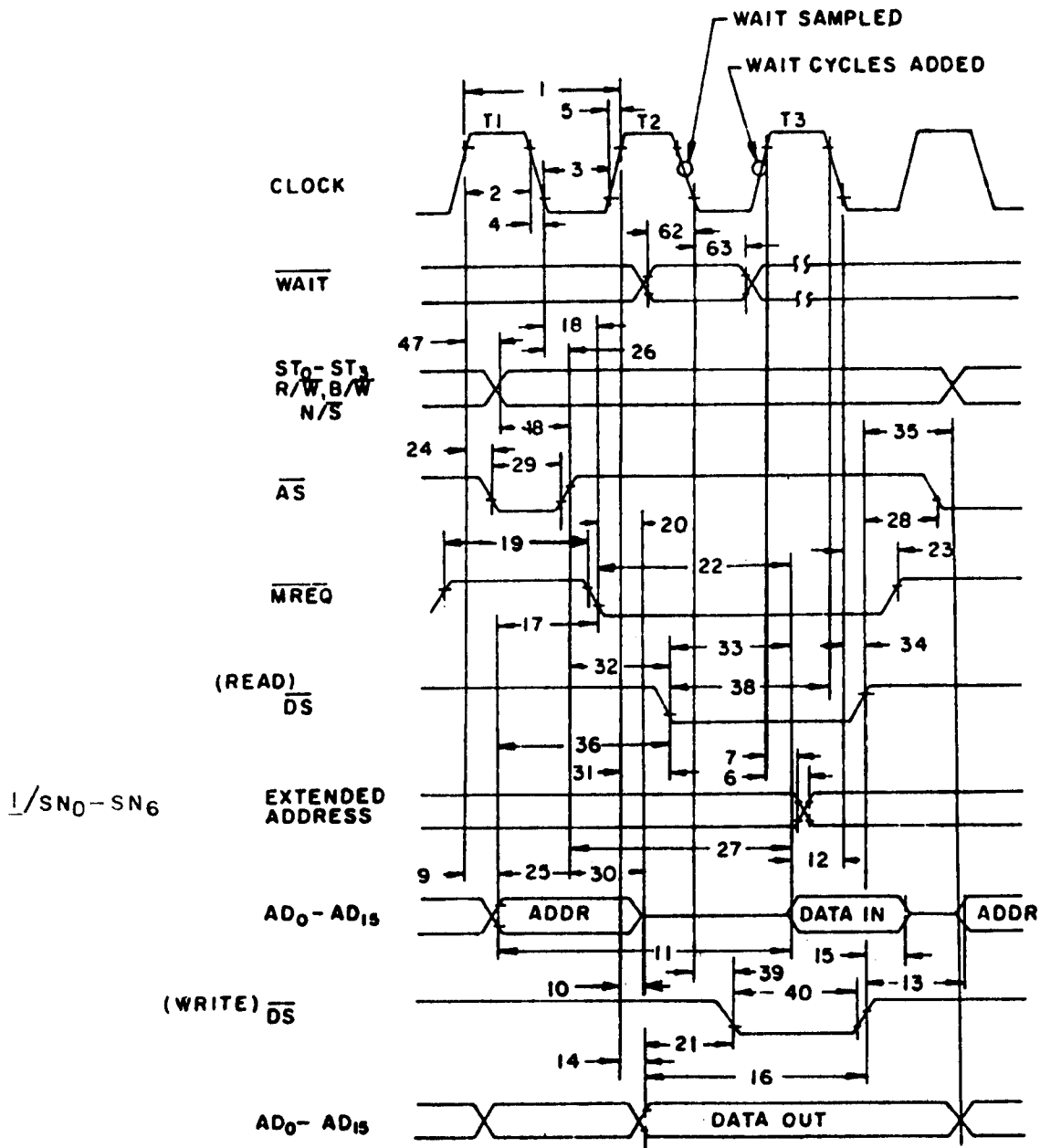
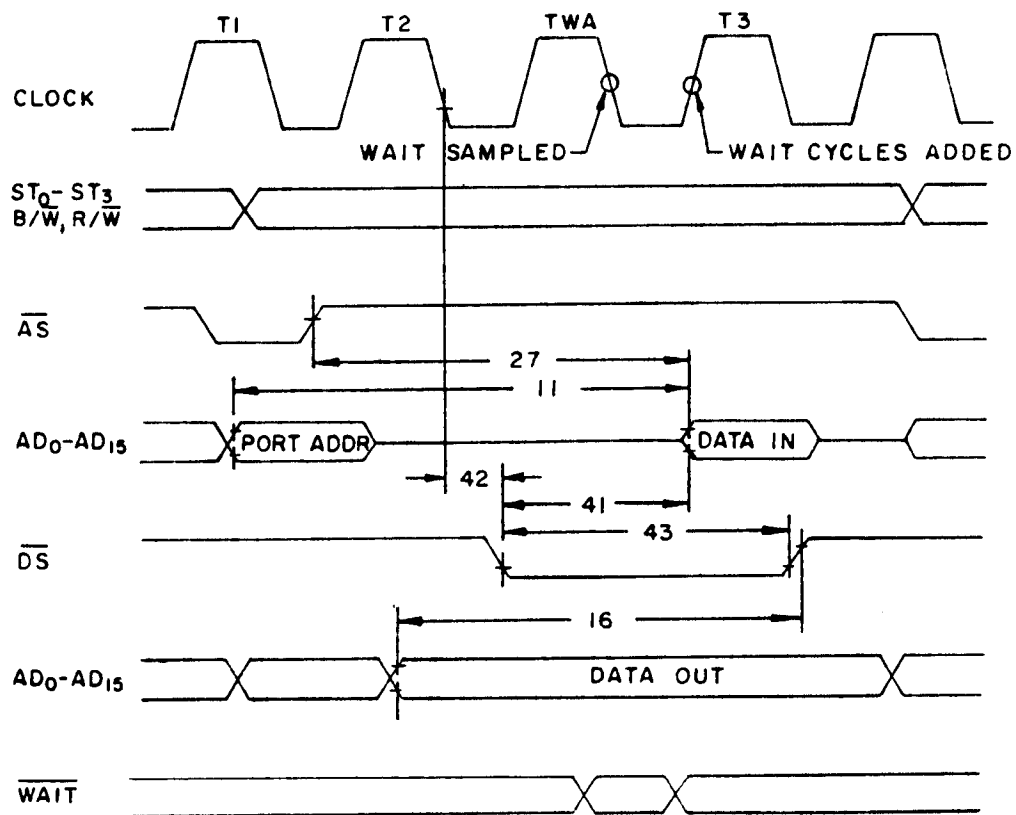


FIGURE 6. AC timing diagram (memory read/write timing).

1/ THESE SIGNALS APPLY TO DEVICE TYPES 01 AND 03 ONLY.

FIGURE 6. AC timing diagram (input/output timing) - Continued.

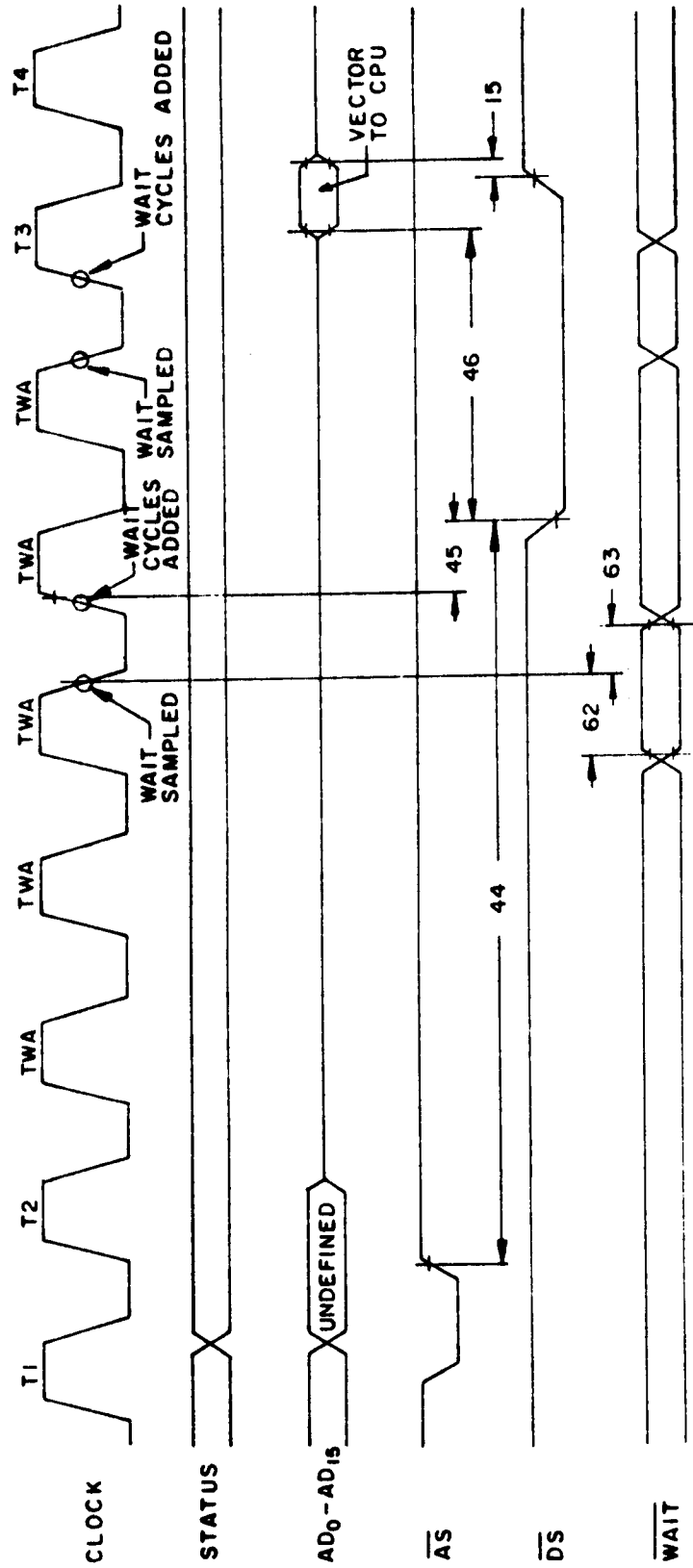
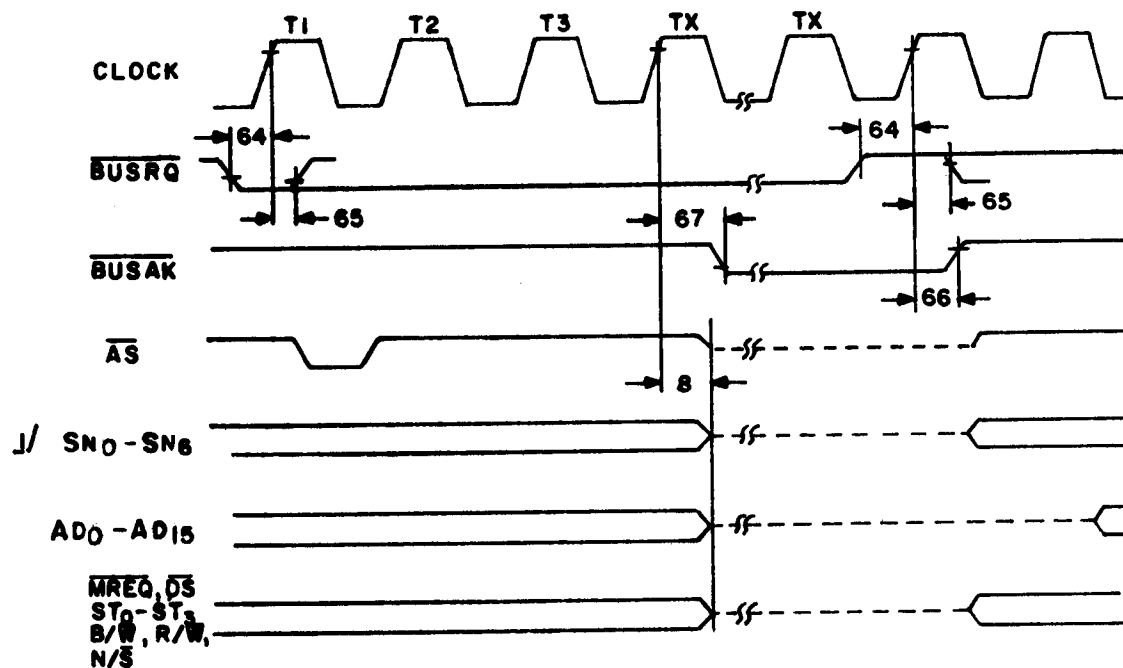
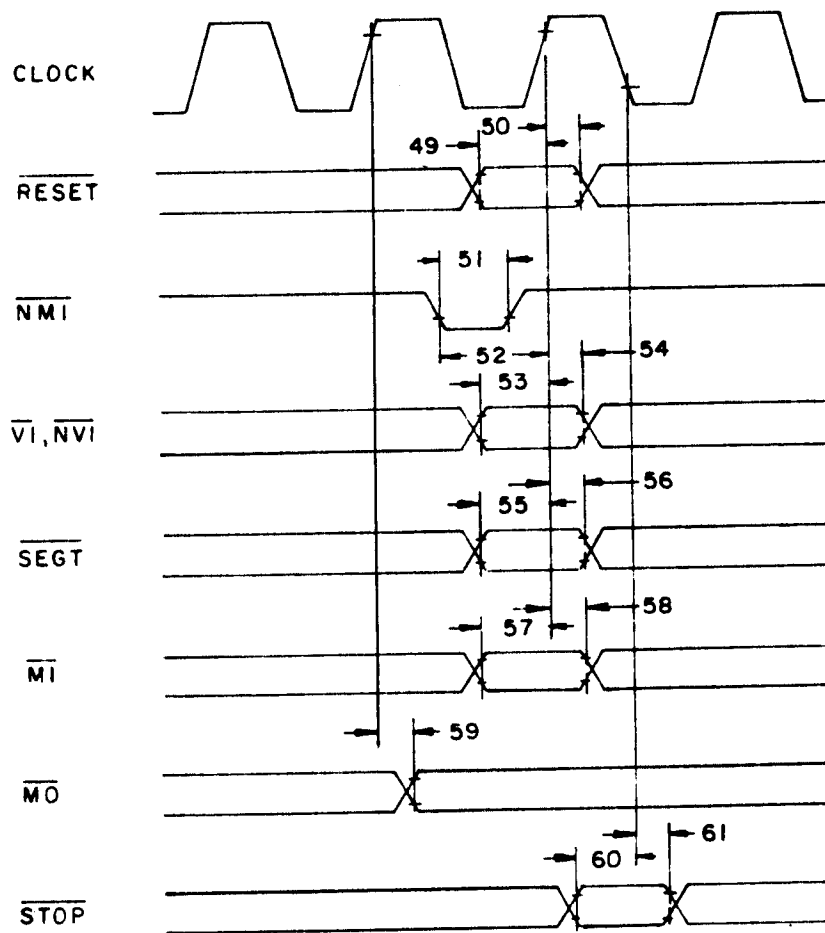


FIGURE 6. AC timing diagram (interrupt and segment trap acknowledge cycle) - Continued.



1/ THE SIGNALS APPLY TO DEVICE TYPES 01 AND 03 ONLY.

FIGURE 6. AC timing diagram (bus request acknowledge cycle) - Continued.



1/ THIS SIGNAL APPLIES TO DEVICE TYPES 01 AND 03 ONLY.

FIGURE 6. AC timing diagram (miscellaneous signals) - Continued.

TABLE V. Test Vectors.

Table V, not printed herein, is a computer listing for use with table III. Each vector identifies activity states by pin number. See 6.2 for information on obtaining the complete table in a compatible output format.

NOTES:

- 1/ When the vectors are performed as specified in table III for subgroups 7, 8, 9, 10, and 11 they verify the dynamic, functional, threshold, and switching parameters at +25°C, -55°C, and +125°C.

TABLE VI. Microprocessor instructions for all device types.

LOAD AND EXCHANGE									
Mnemonics	Operands	Addr. Modes	Clock Cycles*						Operation
			Word, Byte			Long Word			
			NS	SS	SL	NS	SS	SL	
CLR CLRB	dst	R IR DA X	7 8 11 11	- - 12 12	- - 14 15				Clear dst ← 0
EX EXB	R, src	R IR DA X	6 12 15 16	- - 16 16	- - 18 19				Exchange R ← src
LD LDB LDL	R, src	R IM IM IR DA X BA BX	3 7 5 (byte only) 7 9 10 14 14	- - - - 10 10 - -	- - - - 12 13 - -	5 11 - 11 12 13 17 17	- - - - 13 13 - -	- - - - 15 16 - -	Load into Register R ← src
LD LDB LDL	dst, R	R DA X BA BX	8 11 12 14 14	- 12 12 - -	- 14 15 - -	11 14 15 17 17	- 15 15 - -	- 17 18 - -	Load into Memory (Store) dst ← R
LD LDB	dst, IM	IR DA X	11 14 15	- 15 15	- 17 18				Load Immediate into Memory dst ← IM
LDA	R, src	DA X BA BX	12 13 15 15	13 13 - -	15 16 - -				Load Address R ← source address
LDAR	R, src	RA	15	-	-				Load Address Relative R ← source address
LDK	R, src	IM	5	-	-				Load Constant R ← n (n = 0 ... 15)

* NS = Non-segmented SS = Segmented short Output SL = Segmented Long Output

TABLE VI. Microprocessor instructions for all device types - Continued.

LOAD AND EXCHANGE									
Mnemonics	Operands	Addr. Modes	Clock Cycles						Operation
			Word, Byte			Long Word			
			NS	SS	SL	NS	SS	SL	
LDM	R, src, n	IR DA X	11 14 15	- 15 15	- 17 18	+3n			Load Multiple $R \leftarrow \text{src}$ (n consecutive words) (n = 1 ... 16)
LDM	dst, R, n	IR DA X	11 14 15	- 15 15	- 17 18	+3n			Load Multiple (Store Multiple) $\text{dst} \leftarrow R$ (n consecutive words) (n = 1 ... 16)
LDR LDRB LDRL	R, src	RA	14	-	-	17	-	-	Load Relative $R \leftarrow \text{src}$ (range -32768 ... +32767)
LDR LDRB LDRL	dst, R	RA	14	-	-	17	-	-	Load Relative (Store Relative) $\text{dst} \leftarrow R$ (range -32768 ... +32767)
POP POPL	dst, IR	R IR DA X	8 12 15 16	- - 16 16	- - 18 19	12 19 22 23	- - 23 23	- - 25 26	Pop $\text{dst} \leftarrow \text{IR}$ Autoincrement contents of R
PUSH PUSHUL	IR, src	R IM IR DA X	9 12 13 13 14	- - - 14 14	- - - 16 17	12 - 20 20 21	- - - 21 21	- - - 23 24	Push Autodecrement contents of R $\text{IR} \leftarrow \text{src}$
ARITHMETIC									
ADC ADCB	R, src	R	5	-	-	Add with Carry $R \leftarrow R + \text{src} + \text{carry}$			
ADD ADDB ADDL	R, src	R IM IR DA X	4 7 7 9 10	- - - 10 10	- - - 12 13	8 14 14 15 16	- - - 16 16	- - - 18 19	Add $R \leftarrow R + \text{src}$
CP CPB CPL	R, src	R IM IR DA X	4 7 7 9 10	- - - 10 10	- - - 12 13	8 14 14 15 16	- - - 16 16	- - - 18 19	Compare with Register $R - \text{src}$

TABLE VI. Microprocessor instructions for all device types - Continued.

ARITHMETIC								
Mnemonics	Operands	Addr. Modes	Clock Cycles					
			Word		Byte	Long Word		
			NS	SS	SL	NS	SS	SL
CP CPB	dst, IM	IR DA X	11 14 15	- 15 15	- 17 18			
								Compare with Immediate $dst \leftarrow dst - IM$
DAB	dst	R	5	-	-			
								Decimal Adjust
DEC DECB	dst, n	R IR DA X	4 11 13 14	- - 14	- - 16 17			
								Decrement by n $dst \leftarrow dst - n$ (n = 1 ... 16)
DIV DIVL	R, src	R IM IR DA X	95 95 95 96 97	- - - 97 97	- - - 99 100	723 723 723 724 725	- - - 725 728	
								Divide (signed) Word: $R_{n+1} \leftarrow R_n, n+1 \div src$ $R_n \leftarrow remainder$ Long Word: $R_{n+2}, n+3 \leftarrow R_n \dots n+3 \div src$ $R_{n+1} \leftarrow remainder$
EXTS EXTSB EXTSL	dst	R	11	-	-	11	-	-
								Extend Sign Extend sign of low order half of dst through high order half of dst
INC INCB	dst, n	R IR DA X	4 11 13 14	- - 14	- - 16 17			
								Increment by n $dst \leftarrow dst + n$ (n = 1 ... 16)
MULT MULTL	R, src	R IM IR DA X	70 70 70 71 72	- - - 72 72	- - - 74 75	282* 282* 282* 283*284*286* 284*284*287*	- - - - -	
								Multiply (signed) Word: $R_{n+1} \leftarrow R_n + 1 \cdot src$ Long Word: $R_n \dots n+3 \leftarrow R_{n+2}, n+3 \cdot src$ *Plus seven cycles for each 1 in the multiplicand
NEG NEGB	dst	R IR DA X	7 12 15 16	- - 16	- - 18 19			
								Negate $dst \leftarrow 0 - dst$
SBC SBCB	R, src	R	5	-	-			
								Subtract with Carry $R \leftarrow R - src - carry$
SUB SUBB SUBL	R, src	R IM IR DA X	4 7 7 9 10	- - - 10 10	- - - 12 13	8 14 14 15 16	- - - 16 16	
								Subtract $R \leftarrow R - src$

TABLE VI. Microprocessor instructions for all device types - Continued.

LOGICAL									
Mnemonics	Operands	Addr. Modes	Clock Cycles						Operation
			Word, Byte			Long Word			
			NS	SS	SL	NS	SS	SL	
AND ANDB	R, src	R IM IR DA X	4 7 7 9 10	- - - 10 10	- - - 12 13				AND R ← R AND src
COM COMB	dst	R IR DA X	7 12 15 16	- - 16 16	- - 18 19				Complement dst ← NOT dst
OR ORB	R, src	R IM IR DA X	4 7 7 9 10	- - - 10 10	- - - 12 13				OR R ← R OR src
TEST TESTB TESTL	dst	R IR DA X	7 8 11 12	- - 12 12	- - 14 15	13 13 16 17	- - 17 17	- - 19 20	Test dst OR 0
TCC TCCB	cc, dst	R	5	-	-				Test Condition Code Set LSB if cc is true
XOR XORB	R, src	R IM IR DA X	4 7 7 9 10	- - - 10 10	- - - 12 13				Exclusive OR R ← R XOR src

TABLE VI. Microprocessor instructions for all device types - Continued.

PROGRAMS CONTROL									
Mnemonics	Operands	Addr. Modes	Clock Cycles						Operation
			Word, Byte			Long Word			
			NS	SS	SL	NS	SS	SL	
CALL	dst	IR DA X	10 12 13	- 18 18	15 20 21				Call Subroutine Autodecrement SP $\emptyset \text{ SP} \leftarrow \text{PC}$ $\text{PC} \leftarrow \text{dst}$
CALR	dst	RA	10	-	15				Call Relative Autodecrement SP $\emptyset \text{ SP} \leftarrow \text{PC}$ $\text{PC} \leftarrow \text{PC} + \text{dst}$ (range -4094 to +4096)
DJNZ DBJNZ	R, dst	RA	11	-	-				Decrement and Jump if Non-Zero $R \leftarrow R - 1$ If $R \neq 0$: $\text{PC} \leftarrow \text{PC} + \text{dst}$ (range -254 to 0)
IRET*	-	-	13	-	16				Interrupt Return $\text{PS} \leftarrow \emptyset \text{ SP}$ Autoincrement SP
JP	cc, dst	IR IR DA X	10 7 7 8	- - 8 8	15 7 10 11	(taken) (not taken)			Jump Conditional If cc is true: $\text{PC} \leftarrow \text{dst}$
JR	cc, dst	RA	6	-	-				Jump Conditional Relative If cc is true: $\text{PC} \leftarrow \text{PC} + \text{dst}$ (range -256 to +254)
RET	cc	-	10 7	- -	13 7	(taken) (not taken)			Return Conditional If cc is true: $\text{PC} \leftarrow \emptyset \text{ SP}$ Autoincrement SP
SC	src	IM	33	-	39				System Call Autodecrement SP $\emptyset \text{ SP} \leftarrow \text{old PS}$ Push instruction $\text{PS} \leftarrow \text{System Call PS}$
BIT MANIPULATION									
BIT BITB	dst, b	R IR DA X	4 8 10 11	- - 11 11	- - 13 14				Test Bit Static $Z \text{ flag} \leftarrow \text{NOT dst bit}$ specified by b
BIT BITB	dst, R	R	10	-	-				Test Bit Dynamic $Z \text{ flag} \leftarrow \text{NOT dst bit}$ specified by contents of R

* Privileged instruction. Executed in system mode only.

TABLE VI. Microprocessor instructions for all device types - Continued.

BIT MANIPULATION									
Mnemonics	Operands	Addr. Modes	Clock Cycles						Operation
			Word, Byte			Long Word			
			NS	SS	SL	NS	SS	SL	
RES RESB	dst, b	R IR DA X	4 11 13 14	- - 14 14	- - 16 17				Reset Bit Static Reset dst bit specified by b
RES RESB	dst, R	R	10	-	-				Reset Bit Dynamic Reset dst bit specified by contents R
SET SETB	dst, b	R IR DA X	4 11 13 14	- - 14 14	- - 16 17				Set Bit Static Set dst bit specified by b
SET SETB	dst, R	R	10	-	-				Set Bit Dynamic Set dst bit specified by contents of R
TSET TSETB	dst	R IR DA X	7 11 14 15	- - 15 15	- - 17 18				Test and Set S flag ← MSB of dst dst ← all 1s
ROTATE AND SHIFT									
RLDB	R, src	R	9	-	-				Rotate Digit Left
RRDB	R, src	R	9	-	-				Rotate Digit Right
RL RLB	dst, n	R R	6 for n = 1 7 for n = 2						Rotate Left by n bits (n = 1, 2)
RLC RLCB	dst, n	R R	6 for n = 1 7 for n = 2						Rotate Left through Carry by n bits (n = 1, 2)
RR RRB	dst, n	R R	6 for n = 1 7 for n = 2						Rotate Right by n bits (n = 1, 2)
RRC RRCB	dst, n	R R	6 for n = 1 7 for n = 2						Rotate Right through Carry by n bits (n = 1, 2)
SDA SDAB SDAL	dst, R	R	(15 + 3 n)			(15 + 3 n)			Shift Dynamic Arithmetic Shift dst left or right by contents of R

TABLE VI. Microprocessor instructions for all device types - Continued.

ROTATE AND SHIFT									
Mnemonics	Operands	Addr. Modes	Clock Cycles						Operation
			Word, Byte			Long Word			
			NS	SS	SL	NS	SS	SL	
SDL SDLB SDLL	dst, R	R	(15 + 3 n)			(15 + 3 n)			Shift Dynamic Logical Shift dst left or right by contents of R
SLA SLAB SLAL	dst, n	R	(13 + 3 n)			(13 + 3 n)			Shift Left Arithmetic by n bits
SLL SLLB SLLL	dst, n	R	(13 + 3 n)			(13 + 3 n)			Shift Left Logical by n bits
SRA SRAB SRAL	dst, n	R	(13 + 3 n)			(13 + 3 n)			Shift Right Arithmetic by n bits
SRL SRLB SRL	dst, n	R	(13 + 3 n)			(13 + 3 n)			Shift Right Logical by n bits
BLOCK TRANSFER AND STRING MANIPULATION									
CPD CPDB	R _X , src, R _Y , cc	IR	20	-	-				Compare and Decrement R _X - src Autodecrement src address R _Y ← R _Y - 1
CPDR CPDRB	R _X , src, R _Y , cc	IR	(11 + 9 n)						Compare, Decrement and Repeat R _X - src Autodecrement src address R _Y ← R _Y - 1 Repeat until cc is true or R _Y = 0
CPI CPIB	R _X , src, R _Y , cc	IR	20	-	-				Compare and Increment R _X - src Autoincrement src address R _Y ← R _Y + 1
CPIR CPIRB	R _X , src, R _Y , cc	IR	(11 + 9 n)						Compare, Increment and Repeat R _X - src Autoincrement src address R _Y ← R _Y + 1 Repeat until cc is true or R _Y = 0

TABLE VI. Microprocessor instructions for all device types - Continued.

BLOCK TRANSFER AND STRING MANIPULATION									
Mnemonics	Operands	Addr. Modes	Clock Cycles						Operation
			Word, Byte			Long Word			
			NS	SS	SL	NS	SS	SL	
CPSD CPSDB	dst, src, R, cc	IR	25	-	-				Compare String and Decrement dst - src Autodecrement dst and src addresses $R \leftarrow R - 1$
CPSDR CPSDRB	dst, src,	IR	(11 + 14 n)						Compare String, Decrement and Repeat dst - src Autodecrement dst and src addresses $R \leftarrow R - 1$ Repeat until cc is true or $R = 0$
CPSI CPSIB	dst, src, R, cc	IR	25	-	-				Compare String and Incre- ment dst - src Autoincrement dst and src addresses $R \leftarrow R + 1$
CPSIR CPSIRB	dst, src, R, cc	IR	(11 + 14 n)						Compare String, Increment and Repeat dst - src Autoincrement dst and src addresses $R \leftarrow R + 1$ Repeat until cc is true or $R = 0$
LDD LDDB	dst, src, R	IR	20	-	-				Load and Decrement dst $\leftarrow$ src Autodecrement dst and src addresses $R \leftarrow R - 1$
LDDR LDDRB	dst, src, R	IR	(11 + 9 n)						Load, Decrement and Repeat dst $\leftarrow$ src Autodecrement dst and src addresses $R \leftarrow R - 1$ Repeat until $R = 0$
LDI LDIB	dst, src, R	IR	20	-	-				Load and Increment dst $\leftarrow$ src Autoincrement dst and src addresses $R \leftarrow R + 1$
LDIR LDIRB	dst, src, R	IR	(11 + 9 n)						Load, Increment and Repeat dst $\leftarrow$ src Autoincrement dst and src addresses $R \leftarrow R + 1$ Repeat until $R = 0$

TABLE VI. Microprocessor instructions for all device types - Continued.

BLOCK TRANSFER AND STRING MANIPULATION									
Mnemonics	Operands	Addr. Modes	Clock Cycles						Operation
			Word, Byte			Long Word			
			NS	SS	SL	NS	SS	SL	
TRDB	dst, src, R	IR	25	-	-				Translate and Decrement dst $\leftarrow$ src (dst) Autodecrement dst address R $\leftarrow$ R - 1
TRDRB	dst, src, R	IR	(11 + 14 n)						Translate, Decrement and Repeat dst $\leftarrow$ src (dst) Autodecrement dst address R $\leftarrow$ R - 1 Repeat until R = 0
TRIB	dst, src, R	IR	25	-	-				Translate and Increment dst $\leftarrow$ src (dst) Autoincrement dst address R $\leftarrow$ R + 1
TRIRB	dst, src, R	IR	(11 + 14 n)						Translate, Increment and Repeat dst $\leftarrow$ src (dst) Autoincrement dst address R $\leftarrow$ R + 1 Repeat until R = 0
TRTDB	src1, src2, R	IR	25	-	-				Translate and Test. Decrement RH1 $\leftarrow$ src2 (src1) Autodecrement src1 address R $\leftarrow$ R - 1
TRTDRB	src1, src2, R	IR	(11 + 14 n)						Translate and Test. Decrement and Repeat RH1 $\leftarrow$ src2 (src1) Autodecrement src1 address R $\leftarrow$ R - 1 Repeat until R = 0 or RH1 = 0
TRTIB	src1, src2,	IR	25						Translate and Test. Increment RH1 $\leftarrow$ src2 (src1) Autoincrement src1 address R $\leftarrow$ R + 1
TRTIRB	src1, src2, R	IR	(11 + 14 n)						Translate and Test. Increment and Repeat RH1 $\leftarrow$ src2 (src1) Autoincrement src1 address R $\leftarrow$ R + 1 Repeat until R = 0 or RH1 = 0

TABLE VI. Microprocessor instructions for all device types - Continued.

INPUT/OUTPUT									
Mnemonics	Operands	Addr. Modes	Clock Cycles						Operation
			Word, Byte			Long Word			
			NS	SS	SL	NS	SS	SL	
IN*	R, src	IR	10	-	-				Input
INB*		DA	12	-	-				R ← src
IND*	dst, src, R	IR	21	-	-				Input and Decrement
INDB*									dst ← src Autodecrement dst address R ← R - 1
INDR*	dst, src R	IR	(11 + 10 n)						Input, Decrement and Repeat
INDRB*									dst ← src Autodecrement dst address R ← R - 1 Repeat until R = 0
INI*	dst, src R	IR	21	-	-				Input and Increment
INIB*									dst ← src Autoincrement dst address R ← R - 1
INIR*	dst, src, R	IR	(11 + 10 n)						Input, Increment and Repeat
INIRB*									dst ← src Autoincrement dst address R ← R - 1 Repeat until R = 0
OUT*	dst, R	IR	10	-	-				Output
OUTB*		DA	12	-	-				dst ← R
OUTD*	dst, src, R	IR	21	-	-				Output and Decrement
OUTDB*									dst ← src Autodecrement src address R ← R - 1
OTDR*	dst, src, R	IR	(11 + 10 n)						Output, Decrement, and Repeat
OTDRB*									dst ← src Autodecrement src address R ← R - 1 Repeat until R = 0
OUTI*	dst, src, R	IR	21	-	-				Output and Increment
OUTIB*									dst ← src Autoincrement src address R ← R - 1
OTIR*	dst, src, R	IR	(11 + 10 n)						Output, Increment and Repeat
OTIRB*									dst ← src Autoincrement src address R ← R - 1 Repeat until R = 0

*Privileged instructions. Executed in system mode only.

TABLE VI. Microprocessor instructions for all device types - Continued.

INPUT/OUTPUT									
Mnemonics	Operands	Addr. Modes	Clock Cycles						Operation
			Word, Byte			Long Word			
			NS	SS	SL	NS	SS	SL	
SIN* SINB*	R, src	DA	12	-	-				Special Input R ← src
SIND* SINDB*	dst, src, R	IR	21	-	-				Special Input and Decrement dst ← src Autodecrement dst address R ← R - 1
SINDR* SINDRB*	dst, src, R	IR	(11 + 10 n)						Special Input, Decrement Repeat dst ← src Autodecrement dst address R ← R - 1 Repeat until R = 0
SINI* SINIB*	dst, src, R	IR	21	-	-				Special Input and Increment dst ← src Autoincrement dst address R ← R - 1
SINIR* SINIRB*	dst, src, R	IR	(11 + 10 n)						Special Input, Increment and Repeat dst ← src Autoincrement dst address R ← R - 1 Repeat until R = 0
SOUT* SOUTB*	dst, src	DA	12	-	-				Special Output dst ← src
SOUTD* SOUTDB*	dst, src R	IR	21	-	-				Special Output and and Decrement dst ← src Autodecrement src address R ← R - 1 Repeat until R = 1
SOTDR* SOTDRB*	dst, src, R	IR	(11 + 10 n)						Special Output, Decrement and Repeat dst ← src Autodecrement src address R ← R - 1 Repeat until R = 0
SOUTI* SOUTIB*	dst, src, R	IR	21	-	-				Special Output and Incre- ment dst ← src Autoincrement src address R ← R - 1
SOTIR* SOTIRB*	dst, src, R	R	(11 + 10 n)						Special Output, Increment and Repeat dst ← src Autoincrement src address R ← R - 1 Repeat until R = 0

*Privileged instructions. Executed in system mode only.

TABLE VI. Microprocessor instructions for all device types - Continued.

CPU CONTROL									
Mnemonics	Operands	Addr. Modes	Clock Cycles						Operation
			Word, Byte			Long Word			
			NS	SS	SL	NS	SS	SL	
COMFLG	flags	-	7	-	-				Complement Flag (Any combination of C, Z, S, P/V)
DI*	int	-	6	-	-				Disable Interrupt (Any combination of NVI, VI)
EI*	int	-	6	-	-				Enable Interrupt (Any combination of NVI, VI)
HALT*	-	-	(8 + 3 n)						HALT
LDCTL*	CTLR, src	R	7	-	-				Load into Control Register CTLR ← src
LDCTL*	dst, CTLR	R	7	-	-				Load into Control Register dst ← CTLR
LDCTLB	FLGR, src	R	7	-	-				Load into Flag Byte Register FLGR ← src
LDCTLB	dst, FLGR	R	7	-	-				Load from Flag Byte Register dst ← FLGR
LDPS*	src	IR DA X	12 16 17	- 20 20	16 22 23				Load Program Status PS ← src
MBIT*	-	-	-	7	-				Test Multi-Micro Bit Set S if $\overline{M}_1$ is Low; reset S if $\overline{M}_1$ is High.
MREQ*	dst	R	(12 + 7 n)						Multi-Micro Request
MRES*	-	-	5	-	-				Multi-Micro Reset
MSET*	-	-	5	-	-				Multi-Micro Set
NOP	-	-	7	-	-				No Operation

TABLE VI. Microprocessor instructions for all device types - Continued.

CPU CONTROL									
Mnemonics	Operands	Addr. Modes	Clock Cycles						Operation
			Word, Byte			Long Word			
			NS	SS	SL	NS	SS	SL	
RESFLG	flag	-	7	-	-				Reset Flag (Any combination of C, Z, S, P/V)
SETFLG	flag	-	7	-	-				Set Flag (Any combination of C, Z, S, P/V)

*Privileged instruction. Executed in system mode only.

TABLE VI. Microprocessor instructions for all device types - Continued.

CONDITION CODES			
Code	Meaning	Flag settings	CC Field
	Always false	-	0000
	Always true	-	1000
Z	Zero	Z = 1	0110
NZ	Not zero	Z = 0	1110
C	Carry	C = 1	0111
NC	No Carry	C = 0	1111
PL	Plus	S = 0	1101
MI	Minus	S = 1	0101
NE	Not equal	Z = 0	1110
EQ	Equal	Z = 1	0110
OV	Overflow	P/V = 1	0100
NOV	No overflow	P/V = 0	1100
PE	Parity is even	P/V = 1	0100
PO	Parity is odd	P/V = 0	1100
GE	Greater than or equal (signed)	(S XOR P/V) = 0	1001
LT	Less than (signed)	(S XOR P/V) = 1	0001
GT	Greater than (signed)	(Z OR (S XOR P/V)) = 0	1010
LE	Less than or equal (signed)	(Z OR (S XOR P/V)) = 1	0010
UGE	Unsigned greater than or equal	C = 0	1111
ULT	Unsigned less than	C = 1	0111
UGT	Unsigned greater than	(C = 0) AND (Z = 0) = 1	1011
ULE	Unsigned less than or equal	(C OR Z) = 1	0011
Note that some condition codes have identical flag settings and binary fields in the instruction: Z = EQ, NZ = NE, C = ULT, NC = UGE, OV = PE, NOV = PO			
STATUS LINE CODES			
ST ₃ - ST ₀	Definition		
0000	Internal operation		
0001	Memory refresh		
0010	I/O reference		
0011	Special I/O reference (e.g., to an MMU)		
0100	Segment trap acknowledge		
0101	Non-maskable interrupt acknowledge		
0110	Non-vectored interrupt acknowledge		
0111	Vectored interrupt acknowledge		
1000	Data memory request		
1001	Stack memory request		
1010	Data memory request (EPU)		
1011	Stack memory request (EPU)		
1100	Program reference, nth word		
1101	Instruction fetch, first word		
1110	EPU transfer		
1111	Reserved		

b. Steady state life test (method 1005 of MIL-STD-883).

(1) Test condition D or E using the circuit shown on figure 4.

(2) $T_A = +125^\circ\text{C}$, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

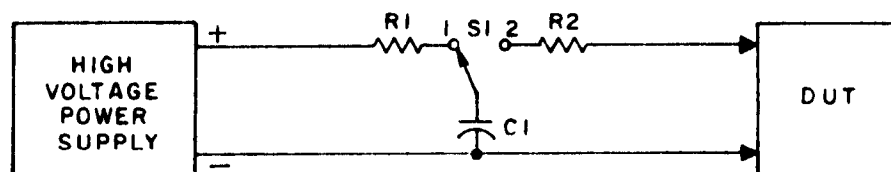
c. Constant acceleration in accordance with test condition D of method 2001 of MIL-STD-883.

4.5 Methods of inspection. Methods of inspection shall be as follows:

4.5.1 Voltage and current. All voltage values given are referenced to the microcircuit ground terminal. Current values given are conventional and are positive when flowing into the referenced terminal.

4.5.2 High-voltage (V_{ZAP}) test of input protection circuits. The following terminals, NMI, MREQ, AD_{13} and BUSAK of the device under test (DUT) shall be subjected to a voltage pulse from a 100 pF source charged to 400 V. This destructive test shall be conducted as follows using the test circuit shown on figure 7.

- a. Measure I_{IH} and I_{IL} at the inputs selected as stated above at 25°C . These measurements shall be made in accordance with table III herein. The test limits for each single terminal measurement of I_{IH} and I_{IL} shall be as specified in table III.
- b. Apply the test voltage ($V_{ZAP} = 400\text{ V}$) to the same terminals selected for leakage current measurements. Apply V_{ZAP} in a 2 mode sequence as shown below and by charging C_1 to V_{ZAP} with S_1 in position 1 and then switching to position 2.
 - (1) Terminal (-) to GND.
 - (2) Terminal (+) to GND.
- c. Within 24 hours repeat the I_{IH} and I_{IL} measurements on the same terminals as performed above. After the V_{ZAP} test a DUT exhibiting leakage currents in excess of the specified limits is defective.



$V_{ZAP} = 400\text{ V}$ minimum charge on C_1 .
 $1\text{ M}\Omega < R_1 < 5\text{ M}\Omega$.
 $R_2 = 1.5\text{ kilohms } \pm 5\%$.
 $C_1 = 100\text{ pF } \pm 10\%$.
 $S_1 = \text{Hg-wetted "bounceless" relay.}$
 All pins are at ground except the DUT pin being tested.

FIGURE 7. High voltage (V_{ZAP}) test circuit.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Test vector table. Table V (test vectors), which forms a part of this specification, is not printed herein because of its extreme length and complexity; and, even when presented as hard copy, it requires conversion to on-line format. When the entire sequence of vector groups is needed for driving devices as part of an inspection, a test program output should be obtained in a form compatible with test system architecture. The preparing activity, or Defense Electronics Supply Center as its agent, may be consulted for information on obtaining such output. For reference purposes, Rome Air Development Center (RADC-RBRM) and Defense Electronics Supply Center (DESC-ECS) each maintain a limited quantity of dated, hard copy printouts of this table.

6.3 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.4 Ordering data. The contract or purchase order should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirement for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to qualifying activity, if applicable.
- e. Requirements for failure analysis, (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These special requirements shall not affect the part number.
- h. Requirements for "JAN" marking.

6.5 Terms and definitions. The abbreviations, terms, symbols, and definitions used herein (including terms and symbols for device terminals) are defined in MIL-M-38510, MIL-STD-1331, and as follows:

AD₀-AD₁₅
(Address/Data bus)

Inputs/outputs, active high, 3-state.
These multiplexed address and data lines are used both for I/O and to address memory. AD₁₅ = MSB.

AS
(Address strobe)

Output, active low, 3-state. The rising edge of AS indicates addresses are valid.

BUSAK
(Bus Acknowledge)

Output, active low. A low on this line indicates the CPU has relinquished control of the bus. This occurs after completion of the current machine cycle. BUSAK goes inactive one clock cycle after the synchronization of BUSRQ being released.

<u>BUSRQ</u> (Bus request)	<u>Input, active low.</u> This line must be driven low to request the bus from the CPU. It is sampled for being active at the beginning of each machine cycle. When it is released, it is synchronized with the next rising clock edge.
<u>DS</u> (Data strobe)	<u>Output, active low, 3-state.</u> This line times the data in and out of the CPU.
<u>MREQ</u> (Memory request)	<u>Output, active low, 3-state.</u> A low on this line indicates that the address/data bus hold a memory address.
<u>MI, MO</u> (Multi-Micro In, Multi-Micro Out)	<u>Input and output, active low.</u> These two lines form a resource-request daisy chain that allows one CPU in a multi-microprocessor system to access a shared resource. MI is sampled on the rising edge of T3 of the last machine cycle of any instruction and internally latched.
<u>NMI</u> (Non-Maskable Interrupt)	<u>Edge triggered, input, active low.</u> A high-to-low transition on NMI requests, a non-maskable interrupt. The NMI interrupt has the highest priority of the three types of interrupts. The internal NMI latch is sampled on the rising edge of T3 of the last machine cycle of any instruction.
<u>NVI</u> (Non-Vectored Interrupt)	<u>Input, active low.</u> A low on this line requests a non-vectored interrupt. It is sampled on the rising edge of T3 of the last machine cycle of any instruction.
<u>CLK</u> (System Clock)	<u>Input.</u> CLK is a 5 V single-phase time-base input.
<u>RESET</u> (Reset)	<u>Input, active low.</u> A low on this line resets the CPU. RESET must be active for at least five clock cycles.
<u>R/W</u> (Read/Write)	<u>Output, low = write, 3-state.</u> R/W indicates that the CPU is reading from, or writing to memory or I/O.
<u>ST0-ST3</u> (Status)	<u>Outputs, active high, 3-state.</u> These lines specify the CPU status.
<u>STOP</u> (Stop)	<u>Input, active low.</u> This input can be used to single-step instruction execution. It is sampled on the last falling clock edge preceding any first instruction fetch cycle.
<u>VI</u> (Vectored Interrupt)	<u>Input, active low.</u> A low on this line requests a vectored interrupt. It is sampled on the rising edge of T3 of the last machine cycle of any instruction.
<u>WAIT</u> (Wait)	<u>Input, active low.</u> This line indicates to the CPU that the memory or I/O device is not ready for data transfer. It is sampled on the falling edge of T2 and any subsequent WAIT states.
<u>B/W</u> (Byte/Word)	<u>Output, low = word, 3-state.</u> This signal defines the type of memory reference on the 16-bit address/data bus.
<u>N/S</u> (Normal/System Mode)	<u>Output, low = system mode, 3-state.</u> N/S indicates the CPU is in the normal or system mode.

SN₀-SN₆
(Segment Number)

Outputs, active high, 3-state. These lines provide the 7-bit segment number used to address one of 128 segments by the memory management unit. Output by device types 01 and 03 only. SN₆ = MSB.

SEGT
(Segment Trap)

Input, active low. The memory management unit interrupts the CPU with a low on this line when the MMU detects a segmentation trap. Input on the 01 and 03 device types only. It is sampled on the rising edge of T3 of the last machine cycle of any instruction.

6.6 Logistic support. Lead material and finishes (see 3.3), are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead finish "C" (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.7 Handling. MOS integrated circuits should be handled with certain precautions to avoid damage due to the accumulation of static charge. These NMOS devices are fabricated with a silicon gate technology, including input protection, which reduces the susceptibility to damage; however, the following handling practices are recommended:

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment and tools.
- c. Handling of devices by the leads should be avoided.
- d. Devices should be stored in conductive carriers.
- e. Avoid uses of plastic, rubber, or silk in MOS areas.

6.8 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types, and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military-device
type

01
02
03
04

Generic-industry
type

Z8001 CPU
Z8002 CPU
Z8001A CPU
Z8002A CPU

Custodians:
Army - ER
Navy - EC
Air Force - 17

Preparing activity:
Air Force - 17
(Project 5962-0563)

Review activities:
Army - AR, MI
Navy - SH, OS
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Agent:
DLA - ES