

INCH POUND

MIL-M-38510/507B
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SUPERSEDING
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MILITARY SPECIFICATION

MICROCIRCUITS, MEMORY, DIGITAL, CMOS ULTRAVIOLET ERASABLE PROGRAMMABLE ARRAY LOGIC, MONOLITHIC SILICON

Inactive for new design after 28 July 1995.

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS, erasable programmable array logic microcircuits which employ an EPROM cell as the programming element. Two product assurance classes (B and S) and a choice of case outlines and lead finishes are provided and are reflected in the complete part or identifying number (PIN). For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device type. The device types are as follows:

<u>Device type</u>	<u>Circuit</u>	<u>t_{PD}</u>
01	22 input, 10 output, AND-OR logic array	30 ns
02	22 input, 10 output, AND-OR logic array	25 ns
03	22 input, 10 output, AND-OR logic array	20 ns
04	22 input, 10 output, AND-OR logic array	15 ns

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
K	GDFP2-F24, CDFP3-F24	24	flat package (transparent lid to permit UV light erasure)
L	GDIP3-T24, CDIP4-T24	24	dual in line package (transparent lid to permit UV light erasure)
3	CQCC1-N28	28	square chip carrier package (transparent lid to permit UV light erasure)

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to memory@dsccl.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil>.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-3.0 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}) ^{1/}	(See MIL-STD-1835)
Output voltage applied in high Z state	-0.5 V dc to +7.0 V dc
Output sink current	16 mA
Maximum power dissipation (P_D)	1.2 W
Maximum junction temperature (T_J)	+175°C
Data retention	10 years minimum

1.4 Recommended operating conditions.

Supply voltage range	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and standards. The following specifications and standards form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, (except for associated detail specification sheets or MS standards), the text of this specification takes precedence. Nothing in this specification, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3). When manufacturer programmed devices are delivered to the user, an altered item drawing shall be prepared by the contracting activity to specify the required program configuration.

^{1/} Must withstand the added P_D due to short circuit condition (e.g., I_{OS}).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Truth tables.

3.3.2.1 Unprogrammed or erased devices. The truth tables for unprogrammed devices shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.4), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed.

3.3.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this specification.

3.3.3 Logic diagram. The logic diagram for unprogrammed devices shall be as specified on figure 3.

3.3.4 Case outlines. Case outlines shall be in accordance with 1.2.3 herein.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I. The electrical tests for each subgroup are described in table I. Any additional detailed information or electrical test requirements not covered in table I (i.e., pin for pin conditions and testing sequence) shall be maintained and available upon request from the qualifying activity.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity.

3.8 Processing EPLD's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.8.1 Erasure of EPLD's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.7.

3.8.2 Programmability of EPLD's. When, specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6.

3.8.3 Verification of erasure of programmability of EPLDS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535. Qualification data for subgroups 7 and 8 shall be attributes only.

4.3 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted prior to qualification and conformance inspection. The following additional criteria shall apply:

- a. Delete the sequence specified in 3.1.9 through 3.1.13 of method 5004 and substitute lines 1 through 5 of table II herein.
- b. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- c. Interim and final electrical tests shall be as specified in table II, except interim electrical tests prior to burn in are optional at the discretion of the manufacturer.
- d. Post dynamic burn in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter measurements.
- e. Additional screening for space level product shall be as specified in MIL-PRF-38535.
- f. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Step 1 through 3 are performed at the wafer level.)
 - (1) Program a minimum of 50 percent of the total number of cells, including the slowest programming cell. The remaining cells shall provide a worst case speed pattern.
 - (2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C, or 2 hours at +300°C for unassembled devices only.
 - (3) Perform margin test using $V_m = +5.7$ V at +25°C using loose timing (i.e., $t_{ACC} = 1$ μ S).
 - (4) Perform dynamic burn in (see 4.3b).
 - (5) Perform margin test using $V_m = +5.7$ V at +25°C using loose timing (i.e., $t_{ACC} = 1$ μ S).
 - (6) Perform electrical tests (see 4.3c).
 - (7) Erase (see 3.8.1). Devices may be submitted for groups A, B, C, and D testing.
 - (8) Verify erasure (see 3.8.3).

The maximum unbiased bake temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 of table III of MIL-PRF-38535 shall be omitted.
- c. All devices selected for testing shall be programmed with a minimum of 50 percent of the total number of cells programmed. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups B, C, and D testing).
- d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

- a. Electrical parameters shall be as specified in table II herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- c. The devices selected for testing shall be programmed with a minimum of 50 percent of the total number of cells programmed. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. The devices selected for testing shall be programmed with a minimum of 50 percent of the total number of cells programmed. After completion of all testing, the devices shall be erased and verified.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Programming procedure. The programming specifications on figure 5, figure 6, in table III, table IV, table V, table VI, table VII, table VIII, and the following procedures shall be used for programming the device:

- a. Initially and after each erasure, all cells, with the exception of the security bit, are in the "0" state. A "1" indicates that an unprogrammed location is to be programmed and a "0" indicates that an unprogrammed location is to remain unprogrammed. All locations to be programmed are addressed as row and column locations. Table V through table VIII provide the specific address for each addressed location to be programmed.
- b. The programming flow chart on figure 6 describes the sequence of operations for programming the Normal and Phantom arrays, the Normal and Phantom Output Enable product terms, the Set and Preset product terms, the Top Test product term, the Bottom Test product term, and the Architecture bits. The sequencing and timing of the signals is shown on figure 5a. All setup, hold, and delay times must be met, and the sequence of operations should be strictly followed. Proper sequencing of all power and supervoltages is essential for reliable programming of the device.
- c. After all locations are programmed, a verify of all words is required as shown on figure 5. When performing this verify only operation, eliminate the program portion of the cycle but maintain the setup and hold timing relative to the verify pulse. Under no circumstances should the verify signal be held low and the addresses toggled as it violates address setup and hold times. The overprogram pulse in step 10 of figure 6 is a variable, "4" times the initial value when programming the Normal, Phantom, Top Test, Bottom Test and Output Enable product terms and "8" times the initial value when programming the Architecture bits.
- d. The security cell is programmed per figure 5b with a single 50 ms pulse on I_{11} . A supervoltage on I_3 is used to verify the security cell after V_{PP} has been removed from I_0 . Data in is represented as a supervoltage on I_2 and verified as a TTL signal output on the same pin. A "0" on I_2 indicates that the security bit has been programmed, and a "1" indicates that the security has not been programmed.

TABLE I. Electrical performance characteristics.

Parameter	Symbol	Test conditions T _C = -55°C to +125°C	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	V _{CC} = 4.5 V, V _{IL} = 0.0 V V _{IH} = 5.0 V, I _{OH} = -2.0 mA	1,2,3 (3006)	All	2.4		V
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, V _{IL} = 0.0 V V _{IH} = 5.0 V, I _{OL} = 12 mA	1,2,3 (3007)	All		0.5	V
Input high level voltage <u>1</u> /	V _{IH}	V _{CC} = 4.5 V	1,2,3 (3008)	All	2.0		V
Input low level voltage <u>1</u> /	V _{IL}	V _{CC} = 4.5 V	1,2,3 (3008)	All		0.8	V
High impedance output leakage current <u>2</u> /	I _{OZL}	V _{CC} = 5.5 V, V _{IL} = 0.0 V V _{IH} = 5.0 V, V _O = 0.0 V	1,2,3 (3020)	All	-40		μA
High impedance output leakage current <u>2</u> /	I _{OZH}	V _{CC} = 5.5 V, V _{IL} = 0.0 V V _{IH} = 5.0 V, V _O = 5.5 V	1,2,3 (3021)	All		40	μA
High level input current	I _{IH}	V _{CC} = 5.5 V, V _{IH} = 5.5 V	1,2,3 (3010)	All		10	μA
Low level input current	I _{IL}	V _{CC} = 5.5 V, V _{IL} = 0.0 V	1,2,3 (3009)	All	-10		μA
Supply current	I _{CC}	V _{CC} = 5.5 V I/O = open Pins (I ₀ - I ₁₁) = 0.0 V	1,2,3 (3005)	All		120	mA
Output short circuit current <u>3</u> / <u>4</u> /	I _{OS}	V _{CC} = 5.5 V, V _O = 0.5 V	1,2,3 (3011)	All	-30	-90	mA
Input capacitance <u>4</u> /	C _I	V _{CC} = 5.0 V, V _I = 0.0 V T _C = +25°C, f = 1 MHz (see 4.4.1d)	4 (3012)	All		10	pF
Output capacitance <u>4</u> /	C _O	V _{CC} = 5.0 V, V _O = 0.0 V T _C = +25°C, f = 1 MHz (see 4.4.1d)	4 (3012)	All		10	pF
Input or feedback to nonregistered output	t _{PD}	V _{CC} = 4.5 V See figure 4	9,10,11 (3003)	01		30	ns
				02		25	
				03		20	
				04		15	
Clock to output <u>5</u> /	t _{CO}		9,10,11 (3003)	01		20	ns
				02		15	
				03		15	
				04		10	
Input to output enable	t _{PZH}		9,10,11 (3003)	01		25	ns
				02		25	
				03		20	
				04		15	
Input to output enable	t _{PZL}		9,10,11 (3003)	01		25	ns
				02		25	
				03		20	
				04		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics, Continued.

Parameter	Symbol	Test conditions T _C = -55°C to +125°C	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
Input to output disable	t _{PHZ}	V _{CC} = 4.5 V See figure 4	9,10,11 (3003)	01		25	ns
				02		25	
				03		20	
				04		15	
Input to output disable	t _{PLZ}		9,10,11 (3003)	01		25	ns
				02		25	
				03		20	
				04		15	
Clock pulse width <u>4</u>	t _{WH}		9,10,11 (3003)	01	20		ns
				02	15		
				03	15		
				04	6		
Clock pulse width <u>4/</u>	t _{WL}		9,10,11 (3003)	01	20		ns
				02	15		
				03	15		
				04	6		
Setup time	t _S	9,10,11 (3003)	01	20		ns	
			02	18			
			03	17			
			04	12			
Hold time	t _H	9,10,11 (3003)	All	0		ns	
Maximum clock frequency <u>6/</u>	f _{MAX}	9,10,11 (3003)	01	25		MHz	
			02	30			
			03	31.2			
			04	45			
Asynchronous reset pulse width	t _{AW}	9,10,11 (3003)	01	30		ns	
			02	25			
			03	20			
			04	15			
Asynchronous reset recovery time	t _{AR}	9,10,11 (3003)	01	30		ns	
			02	25			
			03	20			
			04	15			
Asynchronous reset to registered output reset	t _{AP}	9,10,11 (3003)	01		30	ns	
			02		25		
			03		25		
			04		20		

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ} .

3/ For test purposes, not more than one output should be shorted at a time. Short circuit test duration should not exceed one second.

4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

5/ Test applies only to registered outputs.

6/ f_{MAX} is derived by testing t_S and t_{CO} and is not tested directly. $f_{MAX} = 1/(t_S + t_{CO})$.

TABLE II. Burn – in and electrical test requirements.

Line no.	MIL-PRF-38535 Test requirements	Class S devices <u>1/</u> <u>2/</u>			Class B devices <u>1/</u> <u>2/</u>		
		Reference paragraph	Table I <u>3/</u> subgroups	Table IX Delta <u>4/</u> limits	Reference paragraph	Table I <u>3/</u> subgroups	Table IX Delta <u>4/</u> limits
1	Interim electrical parameters		1			1	
2	Static burn – in I	4.3b	Required				
3	Same as line 1		1*	Δ			
4	Static burn – in II	4.3b	Required				
5	Same as line 1		1*	Δ			
6	Dynamic burn – in	4.3b	Required		4.3b	Required	
7	Same as line 1	4.3d	1*				
8	Final electrical test parameters		1*, 2, 3, 7, 8, 9, 10, 11 <u>5/</u>	Δ		1*, 2, 3, 7, 8, 9, 10, 11	
9	Group A test requirements	4.4.1	1, 2, 3, 7, 8, 9, 10, 11		4.4.1	1, 2, 3, 7, 8, 9, 10, 11	
10	Group B end-point electrical test parameters when using the method 5005 QCI option.	4.4.2	1, 2, 3, 7, 8, 9, 10, 11	Δ			
11	Group C end-point electrical test parameters		1, 2, 3, 7, 8, 9, 10, 11		4.4.3	1, 2, 3, 7, 8 <u>5/</u> <u>6/</u>	Δ
12	Group D end-point electrical test parameters	4.4.4	1, 2, 3, 7, 8		4.4.4	1, 2, 3, 7, 8	

1/ Blank spaces indicate tests are not applicable.

2/ For subgroups 9, 10, and 11 only the worst value measured per device need be recorded when variables data is required (e.g., during qualification).

3/ * indicates PDA applies to subgroup 1.

4/ Δ indicates delta limit shall be required only on table IX, subgroup 1, where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1). Refer to table IX for required parameters and limits to be tested.

5/ The device manufacturer may at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).

6/ For class B, delta limits shall be required on initial qualification or after any design changes which may affect the parameters listed in table IX. Delta values shall be computed with reference the previous interim electrical parameters.

Device types	01, 02, 03, and 04	
Case outlines	K, L	3
Terminal number	Terminal Symbol	
1	CP/I ₀	NC
2	I ₁	CP/ I ₀
3	I ₂	I ₁
4	I ₃	I ₂
5	I ₄	I ₃
6	I ₅	I ₄
7	I ₆	I ₅
8	I ₇	NC
9	I ₈	I ₆
10	I ₉	I ₇
11	I ₁₀	I ₈
12	GND	I ₉
13	I ₁₁	I ₁₀
14	I/O ₀	GND
15	I/O ₁	NC
16	I/O ₂	I ₁₁
17	I/O ₃	I/O ₀
18	I/O ₄	I/O ₁
19	I/O ₅	I/O ₂
20	I/O ₆	I/O ₃
21	I/O ₇	I/O ₄
22	I/O ₈	NC
23	I/O ₉	I/O ₅
24	V _{CC}	I/O ₆
25	---	I/O ₇
26	---	I/O ₈
27	---	I/O ₉
28	---	V _{CC}

FIGURE 1. Terminal Connections.

Truth Table																					
Input pins												Output pins									
CP/ I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	I ₈	I ₉	I ₁₀	I ₁₁	I/O ₀	I/O ₁	I/O ₂	I/O ₃	I/O ₄	I/O ₅	I/O ₆	I/O ₇	I/O ₈	I/O ₉
X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:

1. Z = High impedance
2. X = Irrelevant

FIGURE 2. Truth tables (unprogrammed).

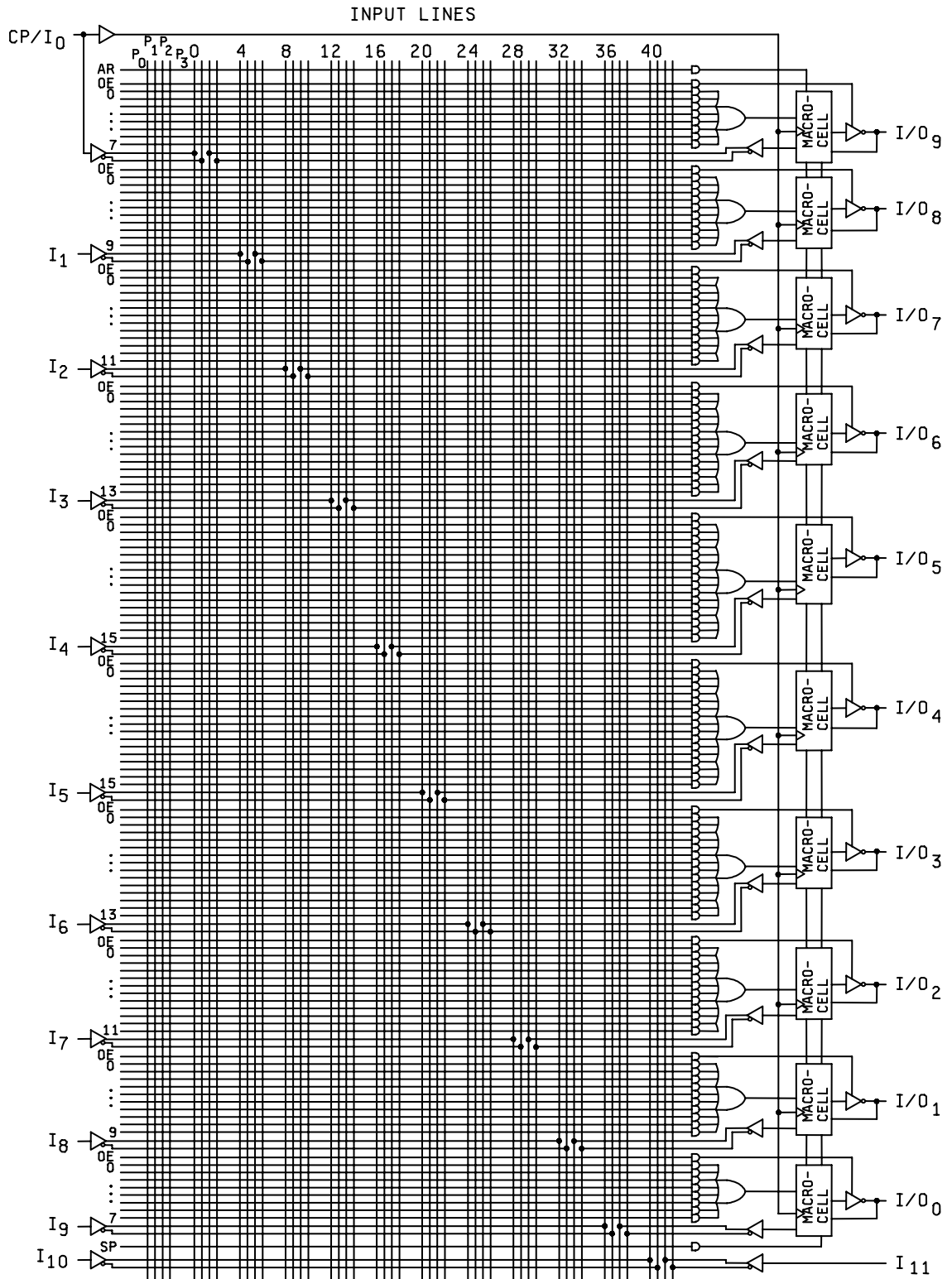


FIGURE 3. Logic diagram (Unprogrammed) .

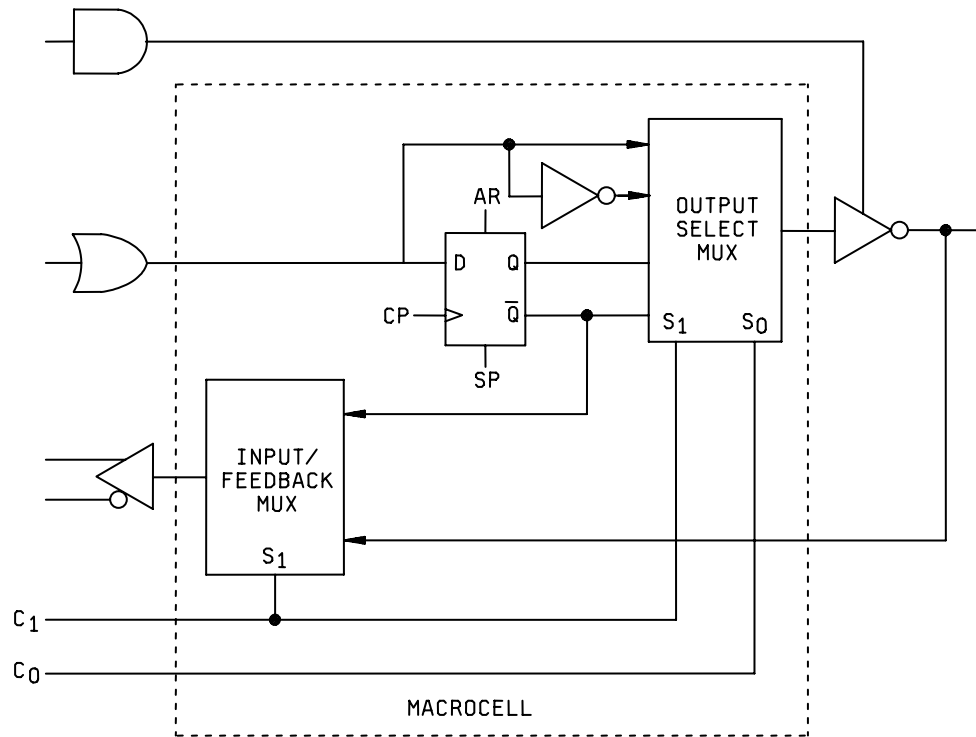
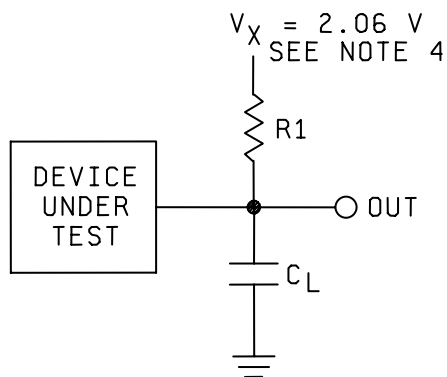


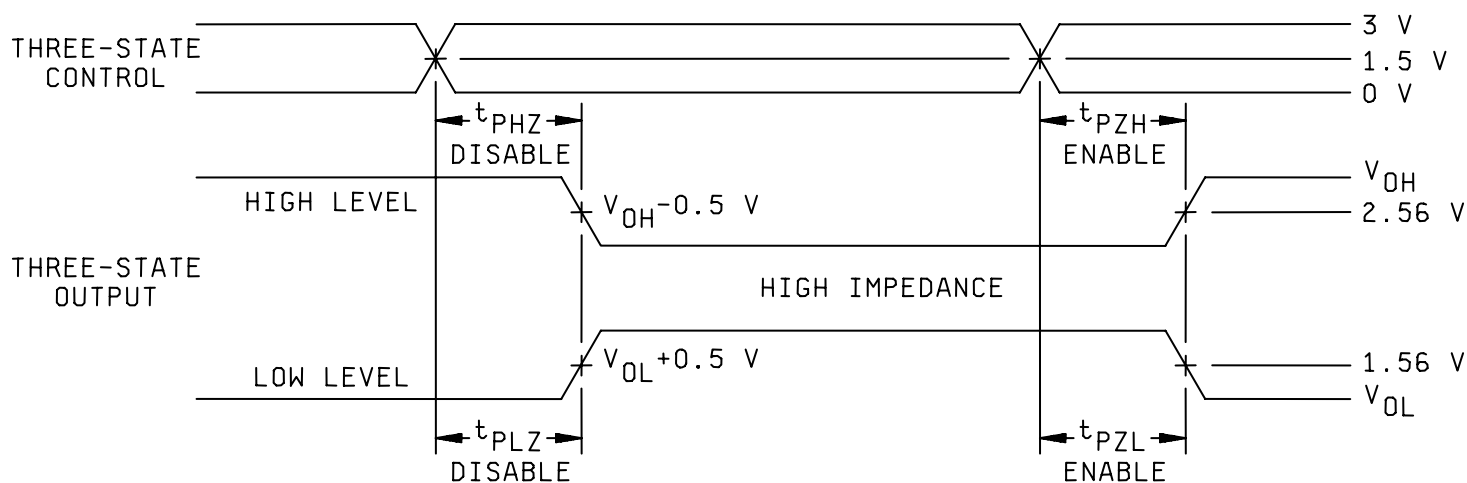
FIGURE 3. Logic diagram (Unprogrammed)– Continued.



NOTES:

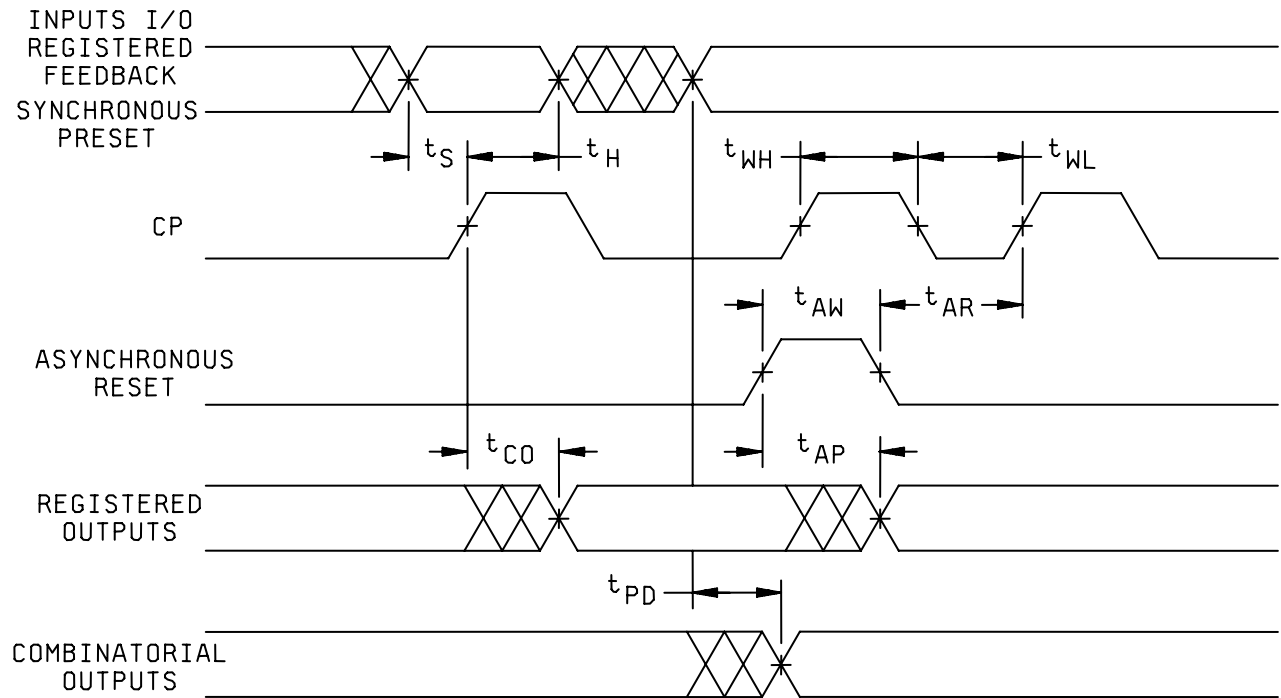
1. $C_L = 50$ pF minimum, including jig and probe capacitance.
 t_{PHZ} and t_{PLZ} are specified with $C_L = 5$ pF.
 $R1 = 105$ ohms ± 1 percent.
2. Outputs may be under load simultaneously.
3. $V_{IH} = 3.0$ V, $V_{IL} = 0.0$ V.
4. For t_{PZH} , t_{PZL} , t_{PHZ} , and t_{PLZ} :

Test	V_X	Output Measurement level
t_{PHZ}	2.06	2.56 V
t_{PZL}	2.06	1.56 V
t_{PHZ}	1.5	$V_{OH} - 0.5$ V
t_{PLZ}	2.60	$V_{OL} + 0.5$ V

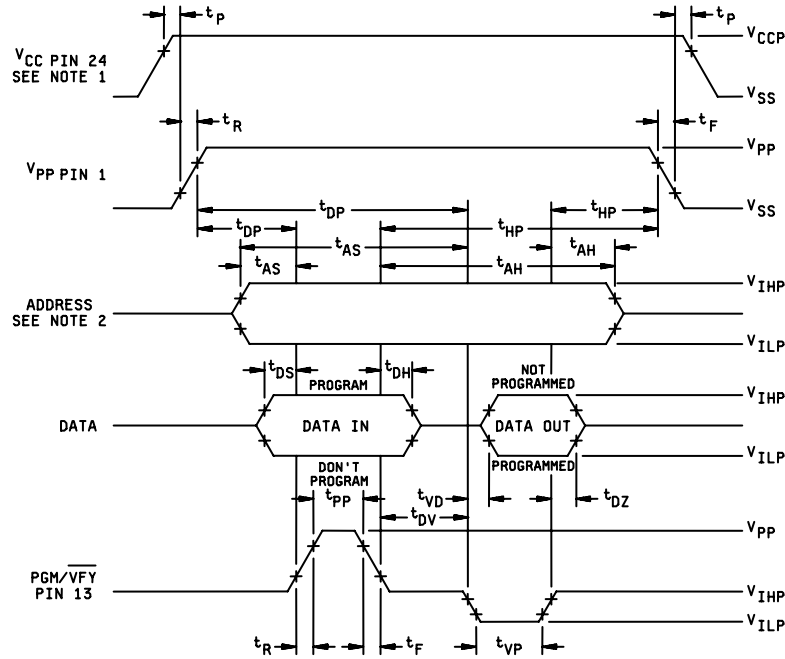


OUTPUT CONTROL SWITCHING WAVEFORM

FIGURE 4. Switching time test circuit and waveforms.

FIGURE 4. Switching time test circuit and waveforms. Continued.

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Notes:

1. Power, V_{PP} and V_{CC} should not be cycled for each program / verify cycle, but may remain static during programming.
2. For programming $\overline{OE}$ Product Terms and Architecture bits, pin 11 (A9) must go to V_{PP} and satisfy t_{AS} and t_{AH} .

FIGURE 5a. Programming waveforms.

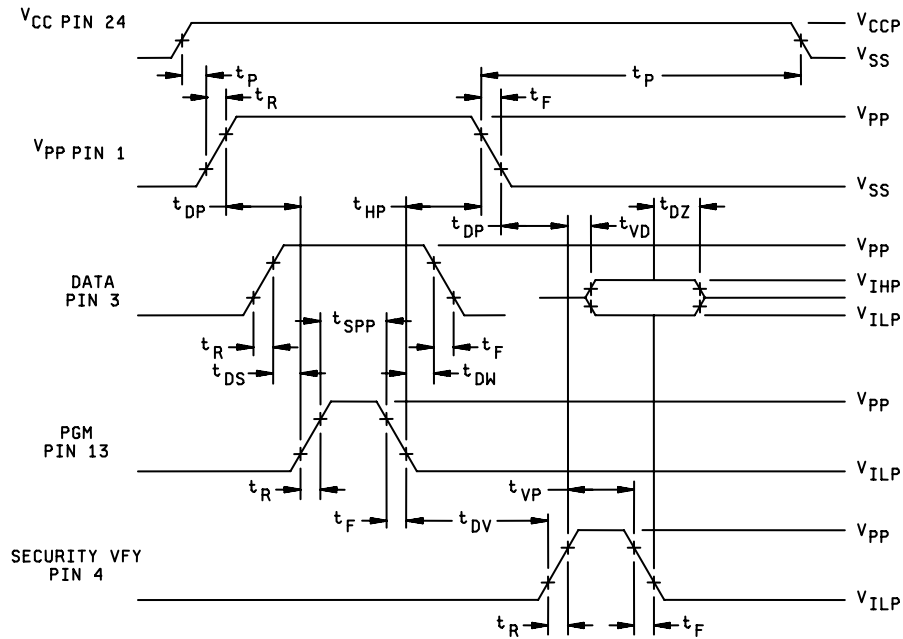
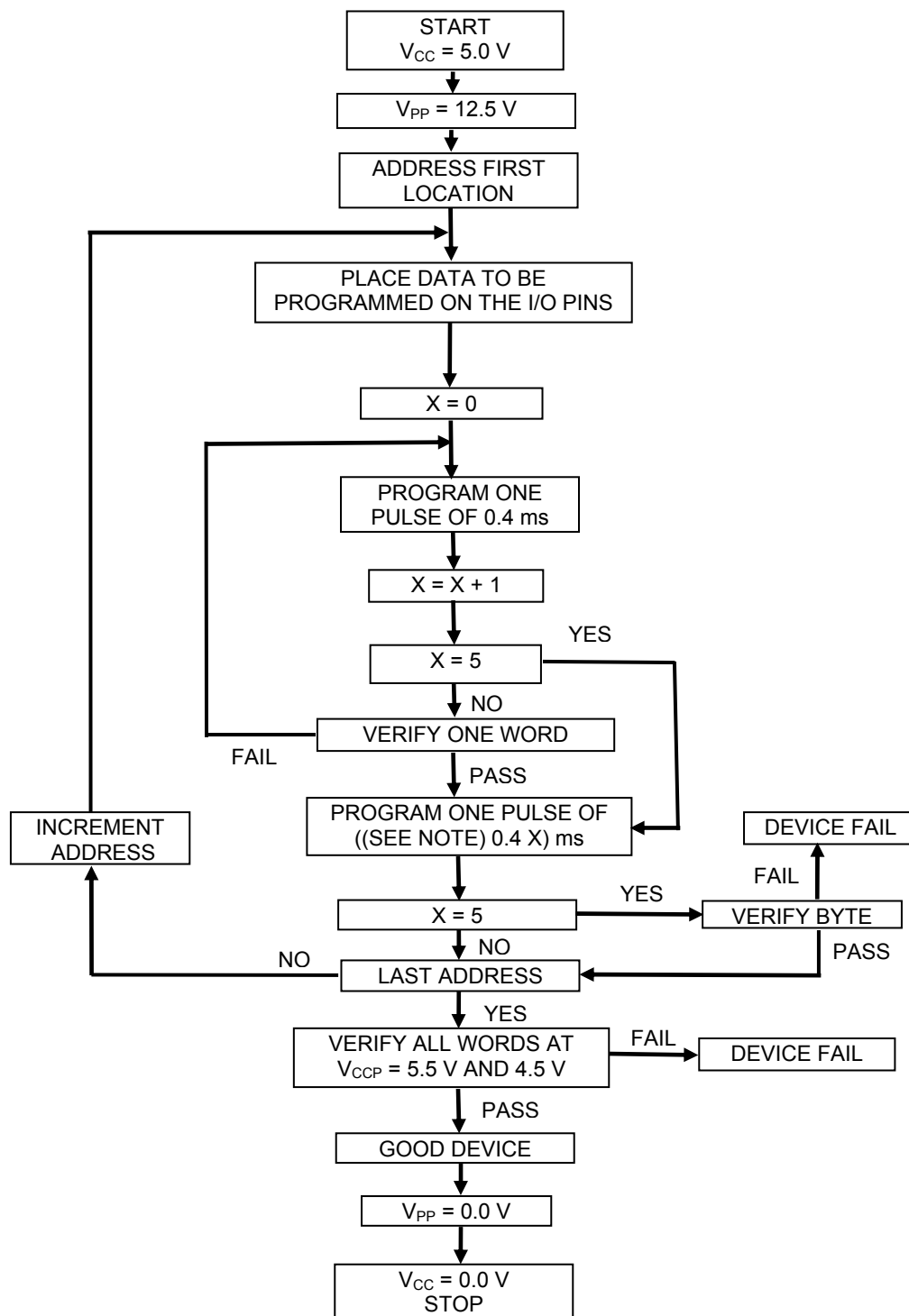


FIGURE 5b. Programming waveforms for security cell.



NOTE: This value is "41" for programming the NORMAL array, PHANTOM array TOP TEST, BOTTOM TEST and OUTPUT ENABLE PRODUCT TERMS. The value is "8" when programming ARCHITECTURE BITS.

FIGURE 6. Programming flowchart.

TABLE III. Operating modes. 1/

		Pin Identification																	
Feature	Mode	CPI ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	I ₈	I ₉	I ₁₀	I ₁₁	IO ₀	IO ₃	IO ₆	IO ₁ IO ₂ IO ₄ IO ₅ IO ₇ IO ₈	IO ₉	
Main Array Product	Program	PP	Table V						Table VI				PP	Data In					
	Inhibit	PP											HP	High Z					
	Verify 2/	PP											LP	Data out					
OE Product Terms	Program	PP	Table V						HP	HP	HP	PP	PP	Data In					
	Inhibit	PP							HP	HP	HP	PP	HP	High Z					
	Verify	PP							HP	HP	HP	PP	LP	Data out					
SyncSet Async 3/ Reset TopTest BotTest	Program	PP	Table V						HP	HP	HP	HP	PP	Data In	Data In	Data In	LP	Data In	
	Inhibit	PP							HP	HP	HP	HP	HP	Z	Z	Z	Z	Z	
	Verify	PP							HP	HP	HP	HP	LP	Data Out	Data Out	Data Out	Driven	Data Out	
Architecture Bits	Program	PP	HP	HP	HP	HP	HP	HP	LP	Table VII		PP	PP	Data In					
	Inhibit	PP	HP	HP	HP	HP	HP	HP	LP			PP	HP	High Z					
	Verify	PP	HP	HP	HP	HP	HP	HP	LP			PP	LP	Data out					
Security Bit	Program	PP	LP	PP	LP	LP	LP	LP	LP	LP	LP	LP	PP	LP	LP	LP	LP	LP	
	Verify	LP	LP	Data Out	PP	LP	LP	LP	LP	LP	LP	LP	LP	Driven Outputs					
PAL Mode Operatn	Normal	CP/I	I	I	I	I	I	I	I	I	I	I	I	I/O					
	Phantom	NA	I	NA	NA	NA	PP	I	NA	NA	I	I	NA	Output					
	TopTest	I	I	I	I	I	I	I	I	PP	I	I	I	NA				Out	
	BotTest	I	I	I	I	I	I	I	I	I	PP	I	I	Out	NA				
	RPreld	4/	NA	NA	NA	NA	NA	NA	PP	NA	NA	NA	LP	Data In					
Phantom Array P Terms	Program	PP	LP	LP	Table VIII		LP	PP	Table VI				PP	Data In					
	Inhibit	PP	LP	LP			LP	PP					HP	High Z					
	Verify	PP	LP	LP			LP	PP					LP	Data Out					
Phantom OE P Terms	Program	PP	LP	LP	Table VIII		LP	PP	HP	HP	HP	PP	PP	Data In					
	Inhibit	PP	LP	LP			LP	PP	HP	HP	HP	PP	HP	High Z					
	Verify	PP	LP	LP			LP	PP	HP	HP	HP	PP	LP	Data Out					

1/ Voltage legend:

LP = Low level input programming voltage (V_{ILP}).
 HP = High level input programming voltage (V_{IHP}).
 PP = Program voltage (V_{PP}).
 Z = High impedance.

2/ It is necessary to toggle $\overline{OE}$ (I_{11}) high during all address transitions while in the program verify/blank check mode.

3/ Data In and Data Out for programming Synchronous Set, Asynchronous Reset, Top Test and Bottom Test is programmed and verified on the following pins:

I/O₀ = Bottom Test
 I/O₃ = Synchronous Set
 I/O₆ = Asynchronous Reset
 I/O₉ = Top Test

4/ The preload clock on CP/I₀ loads the Registers on a low going high transition.

TABLE IV. Programming characteristics.

Parameter	Symbol	Conditions $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$	Device types	Limits		Unit
				Min	Max	
Programming voltage	V_{PP}		All	12.0	13.0	V
Supply voltage during programming	V_{CCP}		All	4.75	5.25	V
Input high voltage during programming	V_{IHP}		All	3.0	V_{CCP}	V
Input low voltage during programming	V_{ILP}		All	-3.0	0.4	V
Output high voltage	V_{OH}		All	2.4		V
Output low voltage	V_{OL}		All		0.4	V
Programming supply current	I_{PP}		All		40	mA
Delay to programming voltage	t_P		All	20		ms
Delay to program	t_{DP}		All	1		μs
Hold from program or verify	t_{HP}		All	1		μs
V_{PP} rise and fall time	$t_{R, F}$		All	50		ns
Address setup time	t_{AS}		All	1		μs
Address hold time	t_{AH}		All	1		μs
Data setup time	t_{DS}		All	1		μs
Data hold time	t_{DH}		All	1		μs
Programming pulse width	t_{PP}		All	0.4	10	ms
Programming pulse width for security	t_{SPP}		All	50		ms
Delay from program to verify	t_{DV}		All	2		μs
Delay to data out	t_{VD}		All		1	μs
Verify pulse width	t_{VP}		All	2		μs
Verify to high Z	t_{DZ}		All		1	μs

TABLE V. Input term addresses.

Input term	Pin name					
	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆
0	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}
1	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}
2	V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}
3	V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}
4	V _{ILP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}
5	V _{IHP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}
6	V _{ILP}	V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}
7	V _{IHP}	V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}
8	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}
9	V _{IHP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}
10	V _{ILP}	V _{IHP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}
11	V _{IHP}	V _{IHP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}
12	V _{ILP}	V _{ILP}	V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}
13	V _{IHP}	V _{ILP}	V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}
14	V _{ILP}	V _{IHP}	V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}
15	V _{IHP}	V _{IHP}	V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}
16	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{ILP}
17	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{ILP}
18	V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{ILP}
19	V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{ILP}
20	V _{ILP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{IHP}	V _{ILP}
21	V _{IHP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{IHP}	V _{ILP}
22	V _{ILP}	V _{IHP}	V _{IHP}	V _{ILP}	V _{IHP}	V _{ILP}
23	V _{IHP}	V _{IHP}	V _{IHP}	V _{ILP}	V _{IHP}	V _{ILP}
24	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{IHP}	V _{ILP}
25	V _{IHP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{IHP}	V _{ILP}
26	V _{ILP}	V _{IHP}	V _{ILP}	V _{IHP}	V _{IHP}	V _{ILP}
27	V _{IHP}	V _{IHP}	V _{ILP}	V _{IHP}	V _{IHP}	V _{ILP}
28	V _{ILP}	V _{ILP}	V _{IHP}	V _{IHP}	V _{IHP}	V _{ILP}
29	V _{IHP}	V _{ILP}	V _{IHP}	V _{IHP}	V _{IHP}	V _{ILP}
30	V _{ILP}	V _{IHP}	V _{IHP}	V _{IHP}	V _{IHP}	V _{ILP}
31	V _{IHP}	V _{IHP}	V _{IHP}	V _{IHP}	V _{IHP}	V _{ILP}
32	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}
33	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}
34	V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}
35	V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}
36	V _{ILP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{IHP}
37	V _{IHP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{IHP}
38	V _{ILP}	V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{IHP}
39	V _{IHP}	V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{IHP}
40	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{IHP}
41	V _{IHP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{IHP}
42	V _{ILP}	V _{IHP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{IHP}
43	V _{IHP}	V _{IHP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{IHP}

TABLE VI. Product term addresses.

Product term	Pin name			
	I ₇	I ₈	I ₉	I ₁₀
0	V _{ILP}	V _{ILP}	V _{ILP}	V _{ILP}
1	V _{IHP}	V _{ILP}	V _{ILP}	V _{ILP}
2	V _{ILP}	V _{IHP}	V _{ILP}	V _{ILP}
3	V _{IHP}	V _{IHP}	V _{ILP}	V _{ILP}
4	V _{ILP}	V _{ILP}	V _{IHP}	V _{ILP}
5	V _{IHP}	V _{ILP}	V _{IHP}	V _{ILP}
6	V _{ILP}	V _{IHP}	V _{IHP}	V _{ILP}
7	V _{IHP}	V _{IHP}	V _{IHP}	V _{ILP}
8	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}
9	V _{IHP}	V _{ILP}	V _{ILP}	V _{IHP}
10	V _{ILP}	V _{IHP}	V _{ILP}	V _{IHP}
11	V _{IHP}	V _{IHP}	V _{ILP}	V _{IHP}
12	V _{ILP}	V _{ILP}	V _{IHP}	V _{IHP}
13	V _{IHP}	V _{ILP}	V _{IHP}	V _{IHP}
14	V _{ILP}	V _{IHP}	V _{IHP}	V _{IHP}
15	V _{IHP}	V _{IHP}	V _{IHP}	V _{IHP}

TABLE VII. Architecture bit addressing.

Architecture bit	I ₈	I ₉
Output polarity (C ₀)	V _{ILP}	V _{ILP}
Register / Nonregister output (C ₁)	V _{IHP}	V _{ILP}

TABLE VIII. Phantom input term addresses.

Phantom input term	I ₃	I ₄
P ₀	V _{ILP}	V _{ILP}
P ₁	V _{IHP}	V _{ILP}
P ₂	V _{ILP}	V _{IHP}
P ₃	V _{IHP}	V _{IHP}

TABLE IX. Delta limits at ± 25 °C.

Parameter <u>1</u> /	Device types
	All
I _{CC}	± 2 mA
I _{OZH}	± 10% of specified value
I _{OZH}	± 10% of specified value

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ).

4.7 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (A). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm². The erasure time with this dosage is approximately 35 minutes using an ultraviolet lamp with a 12000 µW/cm² power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm² (1 week at 12000 µW/cm²). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but it is not mandatory)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of the specification.
- b. PIN and compliance identifier, if applicable (see 1.2).
- c. Requirement for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirement for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to the acquiring activity in addition to notification to the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- g. Requirement for product assurance options.
- h. Requirements for special lead lengths or lead forming, if applicable. These requirements will not affect the PIN. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- i. Requirements for programming the device, including processing option.
- j. Requirements for "JAN" marking.
- k. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

GND	Electrical ground (common terminal)
V _{IN}	Voltage level at an input terminal.
I _{IN}	Current flowing into an input terminal.

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the PIN. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.8.1) and programmed by the maintenance activity, except where use of quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic industry type. Generic industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

<u>Device type</u>	<u>Commercial type</u>
01	C22V10-30
02	C22V10-25
03	C22V10-20
04	C22V10-15

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extent of the changes.

Custodians:
 Army – CR
 Navy - EC
 Air Force – 11
 DLA - CC

Preparing activity:

DLA - CC

Review activities:
 Army – MI, SM
 Navy –AS, CG, MC, SH, TD
 Air Force – 03, 19, 99

(Project 5962-2005-049)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://assist.daps.dla.mil>.