

INCH POUND

MIL-M-38510/505C
24 JANUARY 2006
SUPERSEDING
MIL-M-38510/505B
7 SEPTEMBER 2005

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR PROGRAMMABLE LOGIC, MONOLITHIC SILICON

Inactive for new design after 28 July 1995.

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, bipolar, programmable logic microcircuits which employ titanium tungsten resistors as the fusible link or programming element. Two product assurance classes (B and S) and a choice of case outlines and lead finishes are provided and are reflected in the complete part or identifying number (PIN). For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein..

1.2.1 Device type. The device type is as follows:

<u>Device type</u>	<u>Circuit</u>
01	20 input 8 output AND-OR invert gate array
02	20 input 8 output registered AND-OR gate array
03	20 input 6 output registered AND-OR gate array
04	20 input 4 output registered AND-OR gate array

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outline. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
L	GDIP3-T24, CDIP4-T24	24	Dual in line
3	CQCC1-N28	28	Square leadless chip carrier

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to memory@dsc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil>.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +12.0 V dc
Input voltage range	-1.5 V dc to +12.0 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}) <u>1/</u>	(See MIL-STD-1835)
Output voltage applied	-1.5 V dc to +12.0 V dc
Output sink current	100 mA
Maximum power dissipation (P_D) <u>2/</u>	1.2 W
Maximum junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage	2.0 V dc
Maximum low level input voltage	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and standards. The following specifications and standards form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Heat sinking is recommended to reduce the junction temperature.

2/ Must withstand the added P_D due to short circuit condition; e.g., I_{OS} test.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3). When manufacturer programmed devices are delivered to the user, an altered item drawing shall be prepared by the contracting activity to specify the required program configuration.

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Truth tables.

3.3.2.1 Unprogrammed devices. The truth tables for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of fuses shall be programmed or at least 25 percent of the total number of fuses to any altered item drawing.

3.3.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.3.3 Logic diagrams. The logic diagrams for unprogrammed devices shall be as specified on figure 3.

3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case temperature range.

3.6 Electrical test requirements. Electrical test requirements shall be as specified in table II and (where applicable), the altered item drawing for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, by device class, are specified in table II.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity.

3.8 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.8.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.3.2.1, tables II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.8.2 Manufacturer programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Parameter	Symbol	Test condition <u>1/</u> -55° ≤ T _C ≤ +125° 4.5 V ≤ V _{CC} ≤ 5.5 V	Device type	Limits		Unit
				Min	Max	
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _I = - 18 mA	All		-1.5	V
High level output voltage	V _{OH}	V _{CC} = 4.5 V, V _{IL} = 0.0 V V _{IH} = 3.0 V, I _{OH} = -2 mA	All	2.4		V
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, V _{IL} = 0.0 V V _{IH} = 3.0 V, I _{OL} = 12 mA	All		0.5	V
High level input voltage	V _{IH}	V _{CC} = 5.5 V	All	2.0		V
Low level input voltage	V _{IL}	V _{CC} = 5.5 V	All		0.8	V
High level input current	I _{IH}	V _{CC} = 5.5 V, V _I = 2.4 V <u>2/</u>	All		25	μA
Low level input current	I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V <u>2/</u>	All		-0.25	mA
Output short circuit current	I _{OS}	V _{CC} = 5.5 V, V _O = 0 V <u>3/</u>	All	-30	-250	mA
Input current	I _I	V _{CC} = 5.5 V, V _I = 5.5 V	All		1.0	mA
Off-state output current	I _{OZL}	V _{CC} = 5.5 V, V _{IL} = 0.0 V V _{IH} = 3.0 V, V _O = 0.4 V <u>2/</u>	All		-100	μA
Off-state output current	I _{OZH}	V _{CC} = 5.5 V, V _{IL} = 0.0 V V _{IH} = 3.0 V, V _O = 2.4 V <u>2/</u>	All		100	μA
Supply current	I _{CC}	V _{CC} = 5.5 V	01,02 03,04		210	mA
Propagation delay data input to output	t _{PHL}	See figure 4 <u>4/</u> C _L = 45 pF minimum	01,03 04		30	ns
Propagation delay data input to output	t _{PLH}		01,03 04		30	ns
Propagation delay high impedance to output high	t _{PZH}		01,03 04		30	ns
Propagation delay high impedance to output low	t _{PZL}		01,03 04		30	ns
Propagation delay output high to high impedance	t _{PHZ}		01,03 04		30	ns
Propagation delay output low to high impedance	t _{PLZ}		01,03 04		30	ns
Propagation delay high impedance to output high (pin 13 to output enable), (pin 15 for case 3)	t _{PZH}	See figure 4 <u>5/</u> C _L = 45 pF minimum	02,03 04		25	ns
Propagation delay high impedance to output low (pin 13 to output enable), (pin 15 for case 3)	t _{PZL}		02,03 04		25	ns
Propagation delay output high to high impedance (pin 13 to output disable), (pin 15 for case 3)	t _{PHZ}		02,03 04		25	ns
Propagation delay output low to high impedance (pin 13 to output disable), (pin 15 for case 3)	t _{PLZ}		02,03 04		25	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Parameter	Symbol	Test condition <u>1/</u> $-55^{\circ} \leq T_C \leq +125^{\circ}$ $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$	Device type	Limits		Unit
				Min	Max	
Clock to output	t_{PCH}	See figure 4 <u>5/</u> $C_L = 45 \text{ pF}$ minimum	02,03 04		20	ns
Minimum clock pulse width	t_{PCL}		02,03 04	20		ns
Minimum setup time	t_{SU}		02,03 04	30		ns
Minimum hold time	t_H		All	0		ns
Maximum clock frequency	f_{MAX}		02,03 04		20	MHz

1/ All voltages referenced to ground.2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZX} .3/ Only one output shorted at a time. Equivalent I_0 test may be performed $V_0 = 2.25 \text{ V}$, -15 mA minimum to -125 mA maximum.4/ Applies to nonregistered outputs only, with internal output enables.5/ Applies to registered outputs only, with external output enables (pin 13).TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-PRF-38535 test requirements	Subgroups (per table III)	
	Class S devices	Class B devices
Interim electrical parameters (pre burn-in)	1	1
Final electrical test parameters for unprogrammed devices	1*, 2, 3, 7*, 8	1*, 2, 3, 7*
Final electrical test parameters for programmed devices	1*, 2, 3, 7*, 8, 9, 10, 11	1*, 2, 3, 7*, 8, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group B electrical test parameters when using the method 5005 QCI option.	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical parameters	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8
Group D end-point electrical parameters	1, 2, 3, 7, 8	1, 2, 3, 7, 8

1/ (*) indicates PDA applies to subgroups 1 and 7.2/ Any or all subgroups may be combined when using high-speed testers.3/ Subgroup 7 and 8 shall consist of verifying the pattern specified.4/ Subgroup 8 requirements are for programmed devices only.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535. Qualification data for subgroups 7, 8, 9, 10, and 11 shall be attributes only.

4.3 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted prior to qualification, and conformance inspection. The following additional criteria shall apply:

- a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Additional screening for space level product shall be as specified in MIL-PRF-38535.
- d. All devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn in.

4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 of table III of MIL-PRF-38535 shall be omitted.
- c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.3.2.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturers option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.
- d. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of the specified tests of subgroups 1, 2, and 3 designated for programmed devices only. If any device fails, the lot shall be rejected. At the manufacturers option, the sample may be increased to 20 total devices with no more than 2 total devices failing.
- e. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturers option the sample may be increased to 20 total devices with no more than four total device failures allowable.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

- a. Electrical parameters shall be as specified in table II herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- c. For qualification, at least 50 percent of the sample selected for life testing shall be programmed (see 3.3.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the life test.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535 and as follows:

End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Programming / verifying procedure for circuit A, B, and C. Use the programming specifications on figure 5a, figure 6a, and table III for circuit A; use figure 5b, figure 6a, and table VI for circuit B; use figure 5c, figure 6b, and table IX for circuit C; and the following procedures shall be used for programming the device.

4.6.1 Preverification.

4.6.1.1 Circuits A and B.

- a. Raise V_{CC} to 5.0 volts.
- b. Raise output disable pin, OD, to V_{IHH} .
- c. Select an input line by specifying inputs and L/R as shown in table IV for circuit A, and table VII for circuit B.
- d. Select a product line by specifying A0, A1, and A2 one of eight select as shown in table V for circuit A, and table VIII for circuit B.
- e. Pulse the clock pin and verify (with clock at V_{IL}) that the output pins, 00 through 03, are in the state corresponding to an unblown fuse. Use the minimum timing conditions as specified on figure 5a for circuit A, and figure 5b for circuit B.

- (1) For verified unblown condition, continue procedure from 4.6.1.1c through 4.6.1.1e.
- (2) For verified blown condition, stop procedure.

4.6.1.2 Circuit C.

- a. Raise V_{CC} to 5.0 V.
- b. Raise PGM ENABLE pin to V_{IHH} .
- c. Select an Input line by applying appropriate logic levels to PI pins.
- d. Select a Product line by applying appropriate logic levels to PA pins.
- e. Pulse PGM VERIFY pin to V_{IH} using the minimum timing conditions specified in Table IX, and verify that the outputs 00-07 are in the state corresponding to an unblown fuse.
 - (1) For verified unblown condition, continue procedure from 4.6.1.1c to 4.6.1.1e.
 - (2) For verified blown condition stop procedure.

4.6.2 Programming algorithm.4.6.2.1 Circuits A and B.

- a. Rise output disable pin, OE, to V_{IHH} .
- b. Lower clock pin to V_{IL} .
- c. Select an input line as specified in 4.6.1.1c.
- d. Select a product line as specified in 4.6.1.1d.
- e. Raise V_{CC} to V_{IHH} .
- f. Program the fuse by pulsing the output pins of the selected group (one at a time) to V_{IHH} (see figure 5a for circuit A, and figure 5b for circuit B).
- g. Lower V_{CC} to 5.0 volts.
- h. Repeat this procedure from 4.6.2.1c until pattern is complete.

4.6.2.2 Circuit C.

- a. Raise PGM ENABLE pin to V_{IHH} .
- b. Select an input as in 4.6.1.2c.
- c. Select a product line as in 4.6.1.2d.
- d. Raise $\overline{OE}$ to V_{IH} .
- e. Raise selected PO pin to V_{IHH} .
- f. Program the fuse by pulsing V_{CC} to V_{IHH} .
- g. Remove output voltage.
- h. Repeat this procedure from 4.6.2.2b until entire pattern is complete.

4.6.3 First verification pass for all fuse locations.

4.6.3.1 Circuits A and B.

- a. Raise V_{CC} to 4.5 volts.
- b. Select input line as specified in 4.6.1.1c.
- c. Select a product line as specified in 4.6.1.1d.
- d. Pulse the clock pin and verify (with clock at V_{IL}) that the output pins, 00 through 03 are in the correct state.
 - (1) For verified output state, continue procedure.
 - (2) For overblown conditions, stop procedure.
 - (3) For underblown condition, reject part.
- e. Repeat this procedure from 4.6.3.1b until the entire array is exercised.

4.6.3.2 Circuit C.

- a. Raise V_{CC} to 4.5 V.
- b. Raise PGM ENABLE pin to V_{IHH} .
- c. Select an input line as specified in 4.6.1.2c.
- d. Select a product line as specified in 4.6.1.2d.
- e. Pulse PGM VERIFY pin and verify that the outputs 00-07 are in the correct state.
 - (1) For verified output condition continue the procedure.
 - (2) For overblown conditions, stop procedure.
 - (3) For underblown condition, reject part.
- f. Repeat this procedure from 4.6.3.1c until the entire array is exercised.

4.6.4 High voltage verify for all fuse locations.

4.6.4.1 Circuits A and B.

- a. Raise V_{CC} to 5.5 volts.
- b. Repeat from 4.6.3.1b to 4.6.3.1d until the entire array is exercised.

Programming should be attempted at room temperature, 15°C to 30°C. To prevent further programming, security fuses may be blown. Raise V_{CC} to 6.0 volts, and raise pins 1 and 11 to V_P for 10 milliseconds to 1 second.

4.6.4.2 Circuit C.

- a. Raise V_{CC} to 5.5 V.
- b. Repeat procedure from 4.6.3.2c until the entire array is exercised.

Security fuse information: The security fuse is programmed using procedure in 4.6.2.2 omitting steps 4.6.2.2e and 4.6.2.2h.

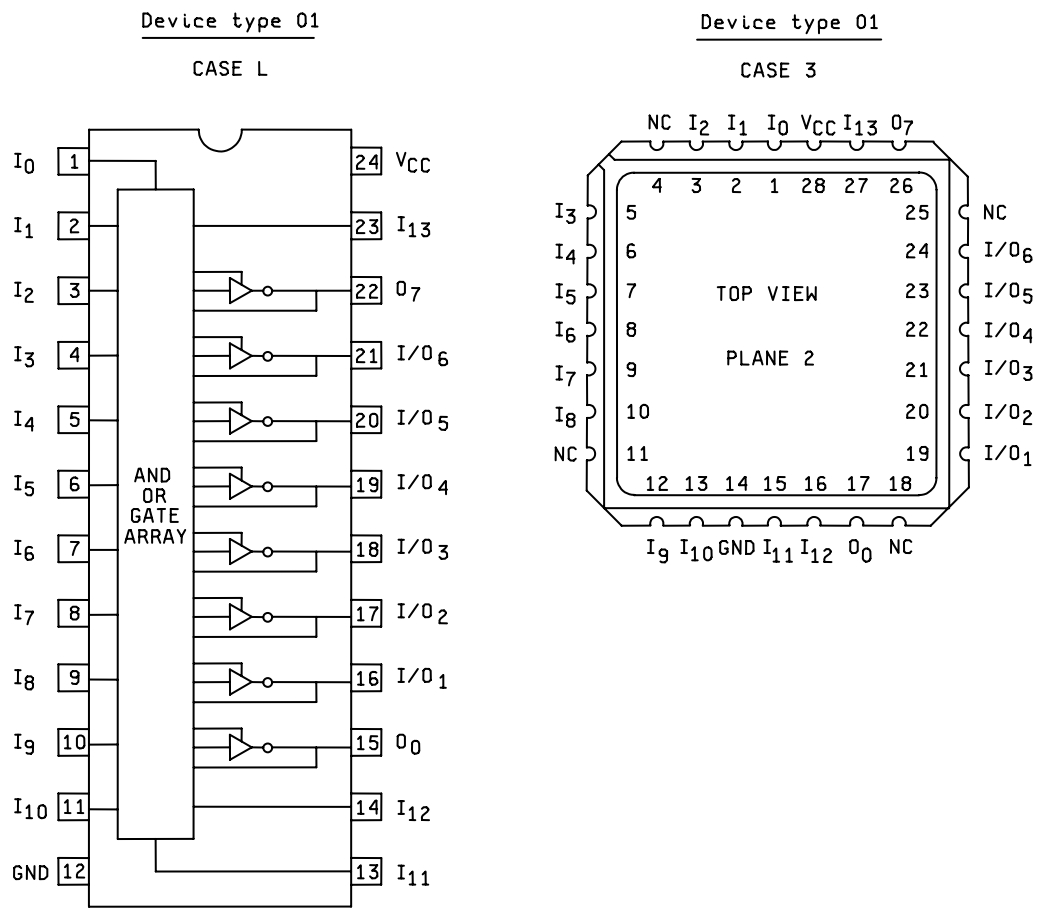
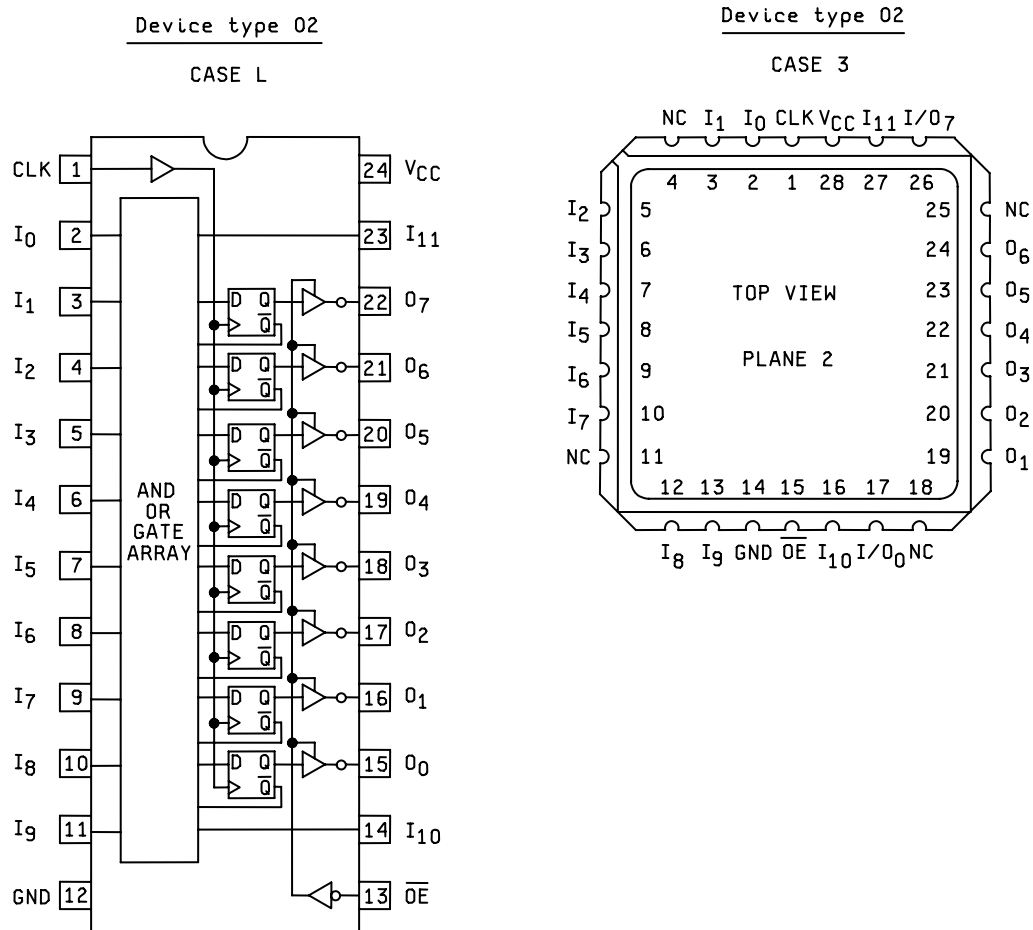
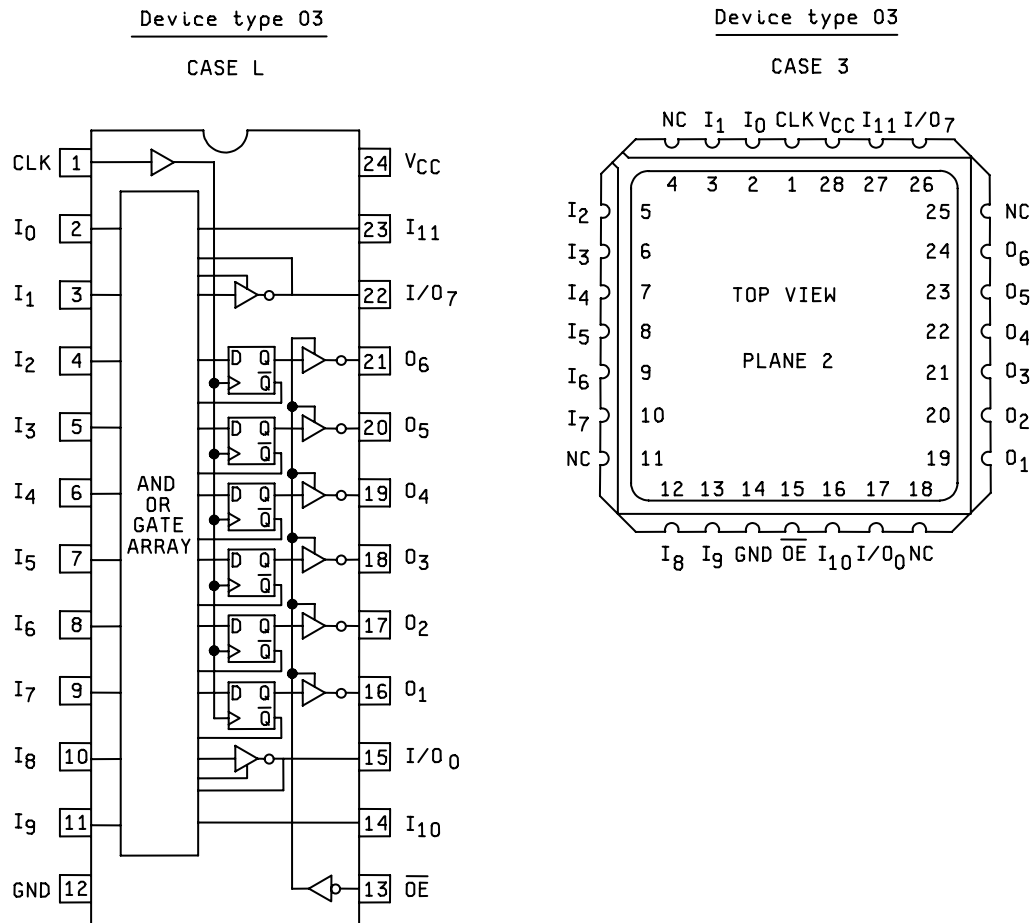
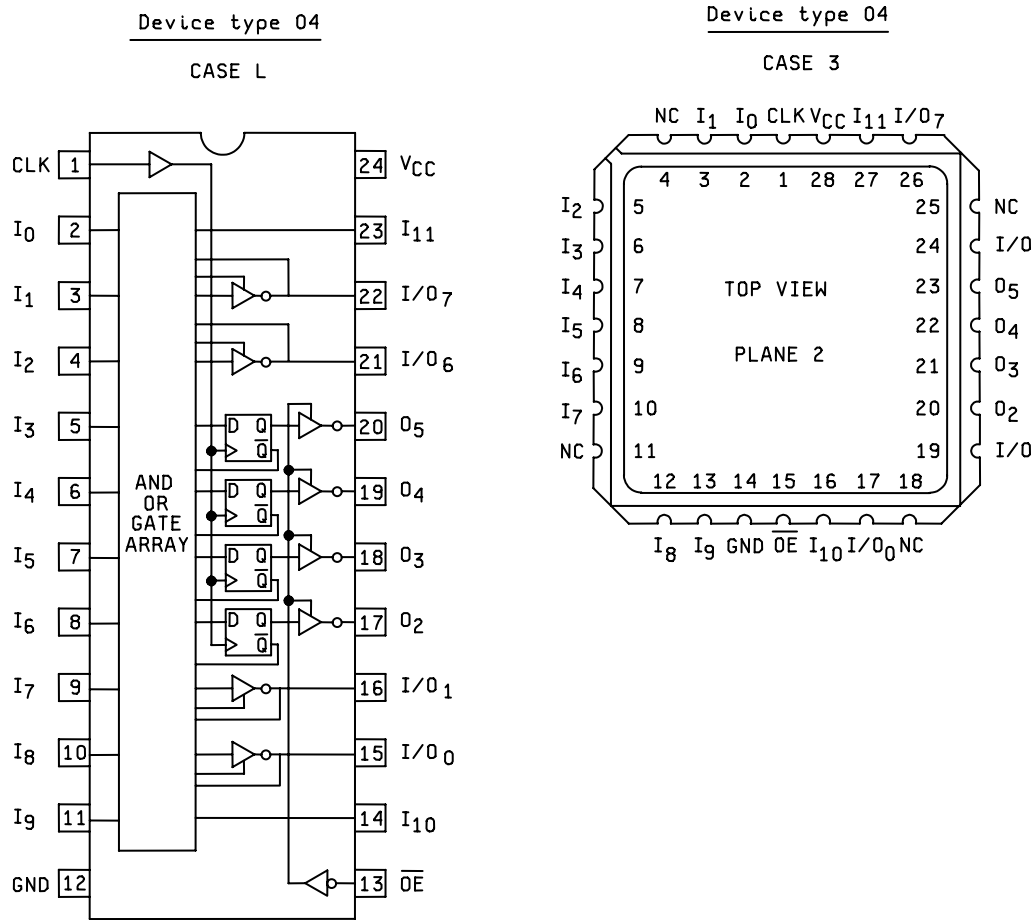


FIGURE 1. Terminal Connections.

FIGURE 1. Terminal Connections - Continued.

FIGURE 1. Terminal Connections - Continued.

FIGURE 1. Terminal Connections - Continued.

Device type 01

INPUTS														OUTPUTS							
I ₁₃	I ₁₂	I ₁₁	I ₁₀	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	O ₇	I/O ₆	I/O ₅	I/O ₄	I/O ₃	I/O ₂	I/O ₁	O ₀
X	X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z

Device type 02

INPUTS														OUTPUTS							
$\overline{OE}$	I ₁₁	I ₁₀	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	CLK	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₀
H	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	X	X	CLK	H	H	H	H	H	H	H	H

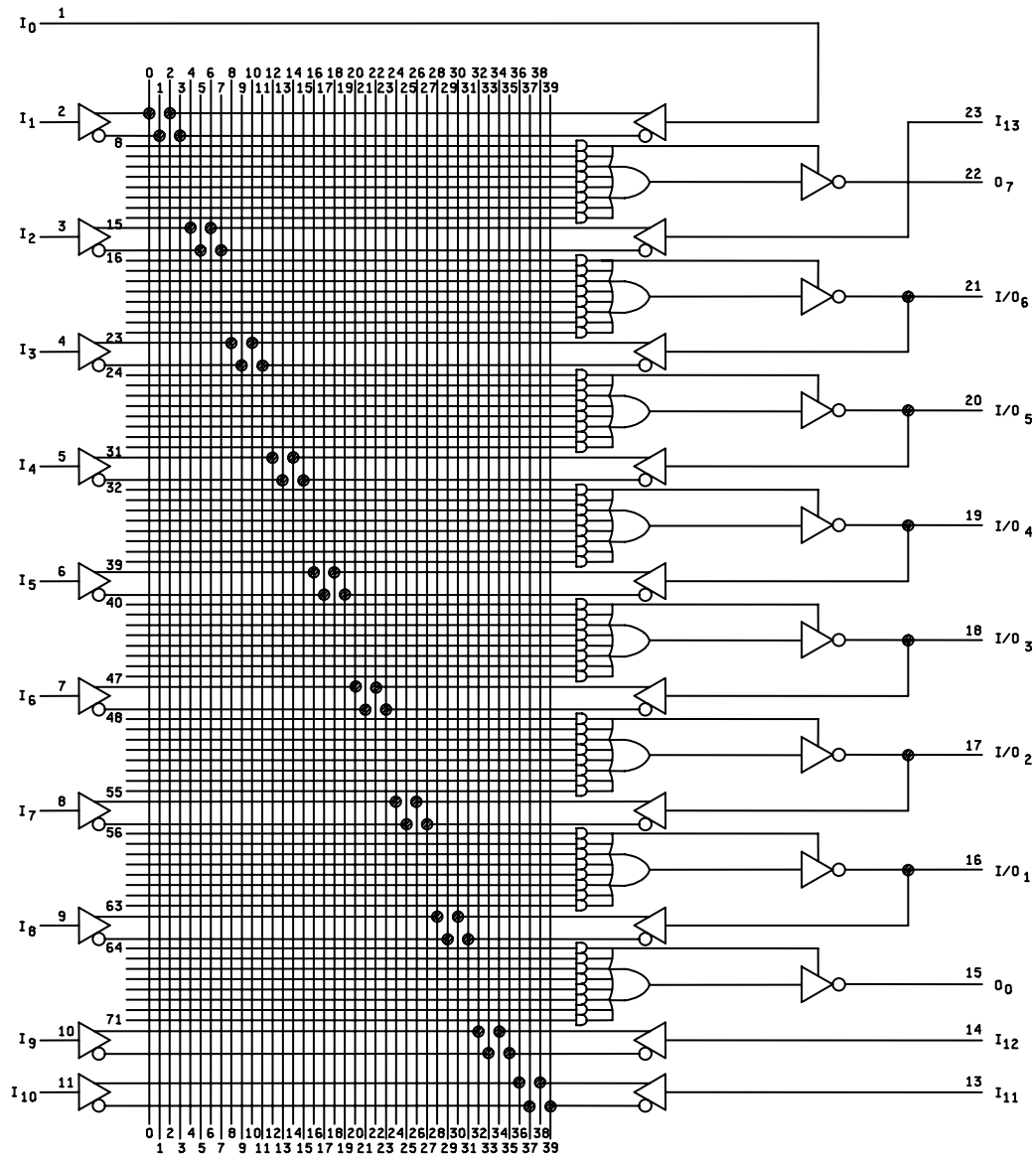
Device type 03

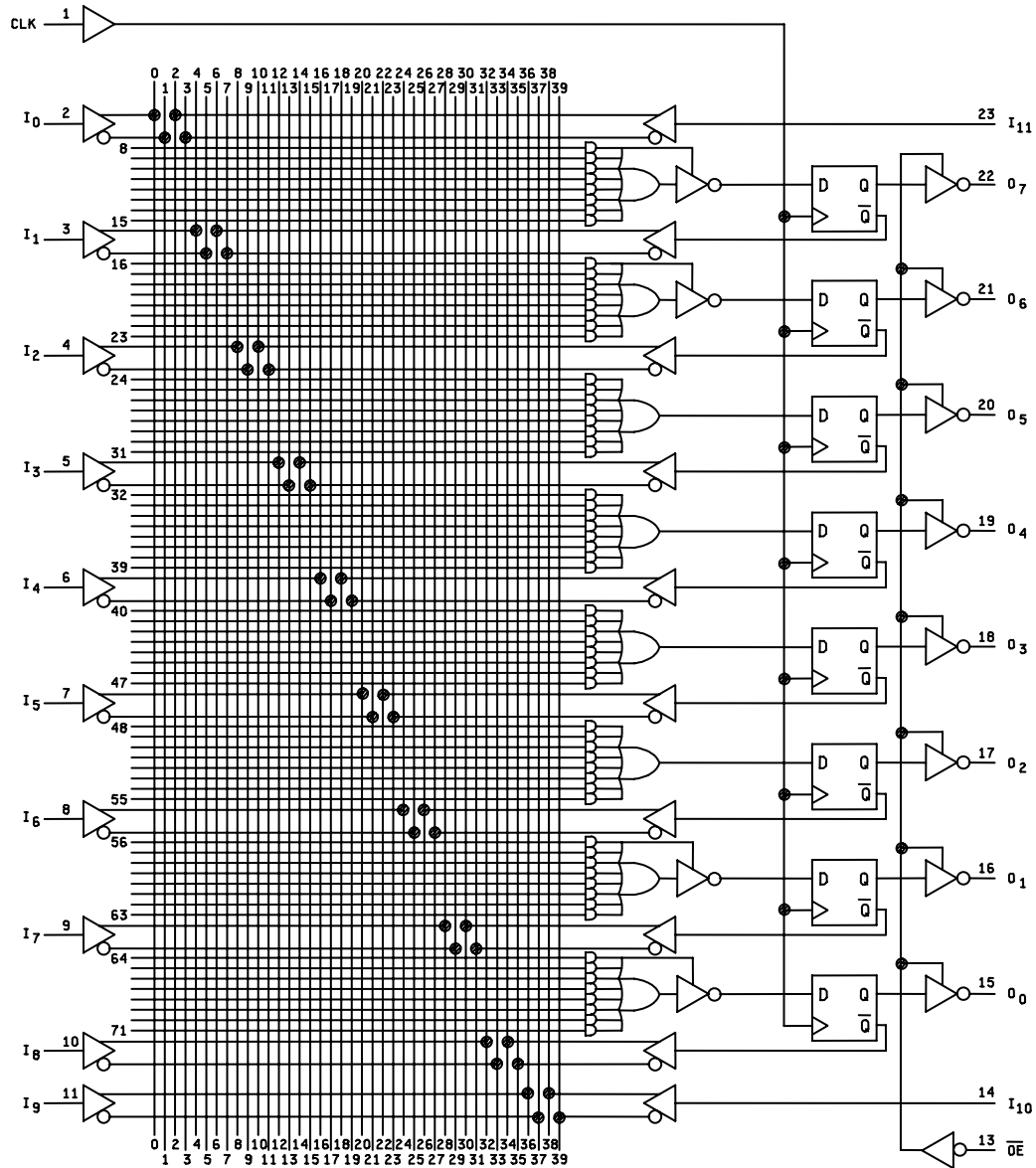
INPUTS														OUTPUTS							
$\overline{OE}$	I ₁₁	I ₁₀	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	CLK	I/O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	I/O ₀
H	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	H	H	H	H	H	H	Z

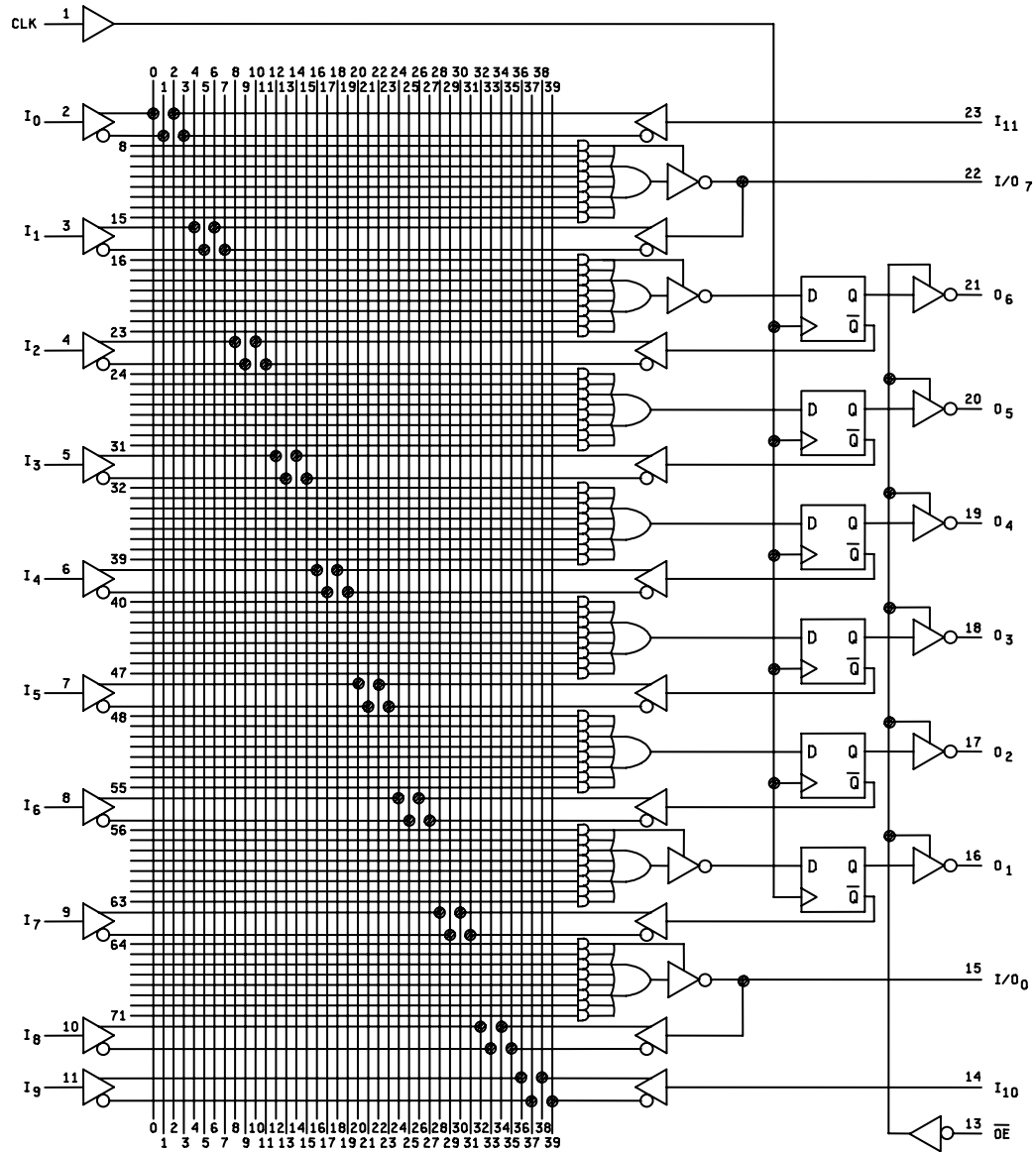
Device type 04

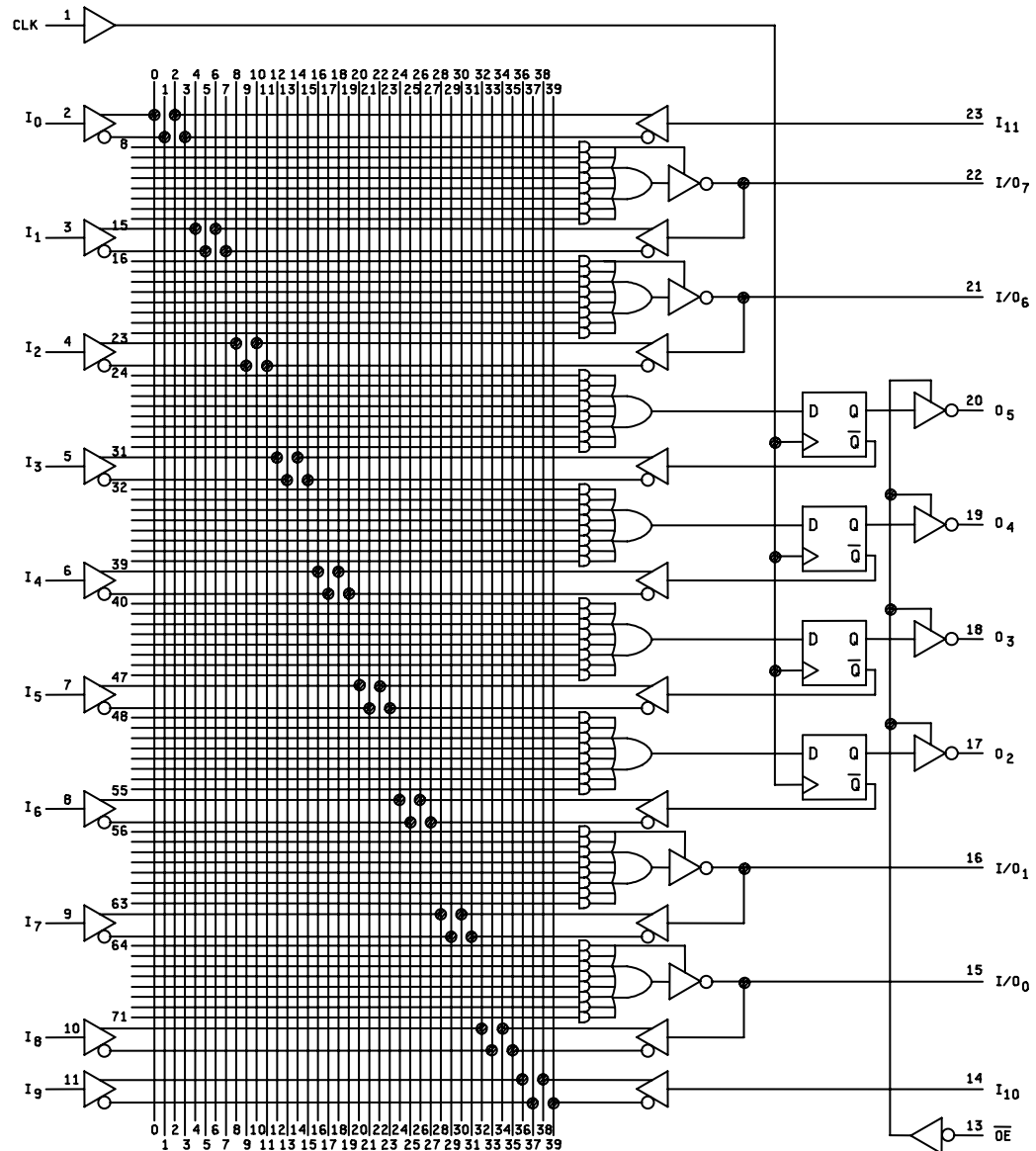
INPUTS														OUTPUTS							
$\overline{OE}$	I ₁₁	I ₁₀	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	CLK	I/O ₇	I/O ₆	O ₅	O ₄	O ₃	O ₂	I/O ₁	I/O ₀
H	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	Z	Z	Z	Z	Z	Z
L	X	X	X	X	X	X	X	X	X	X	X	X	CLK	Z	Z	H	H	H	H	Z	Z

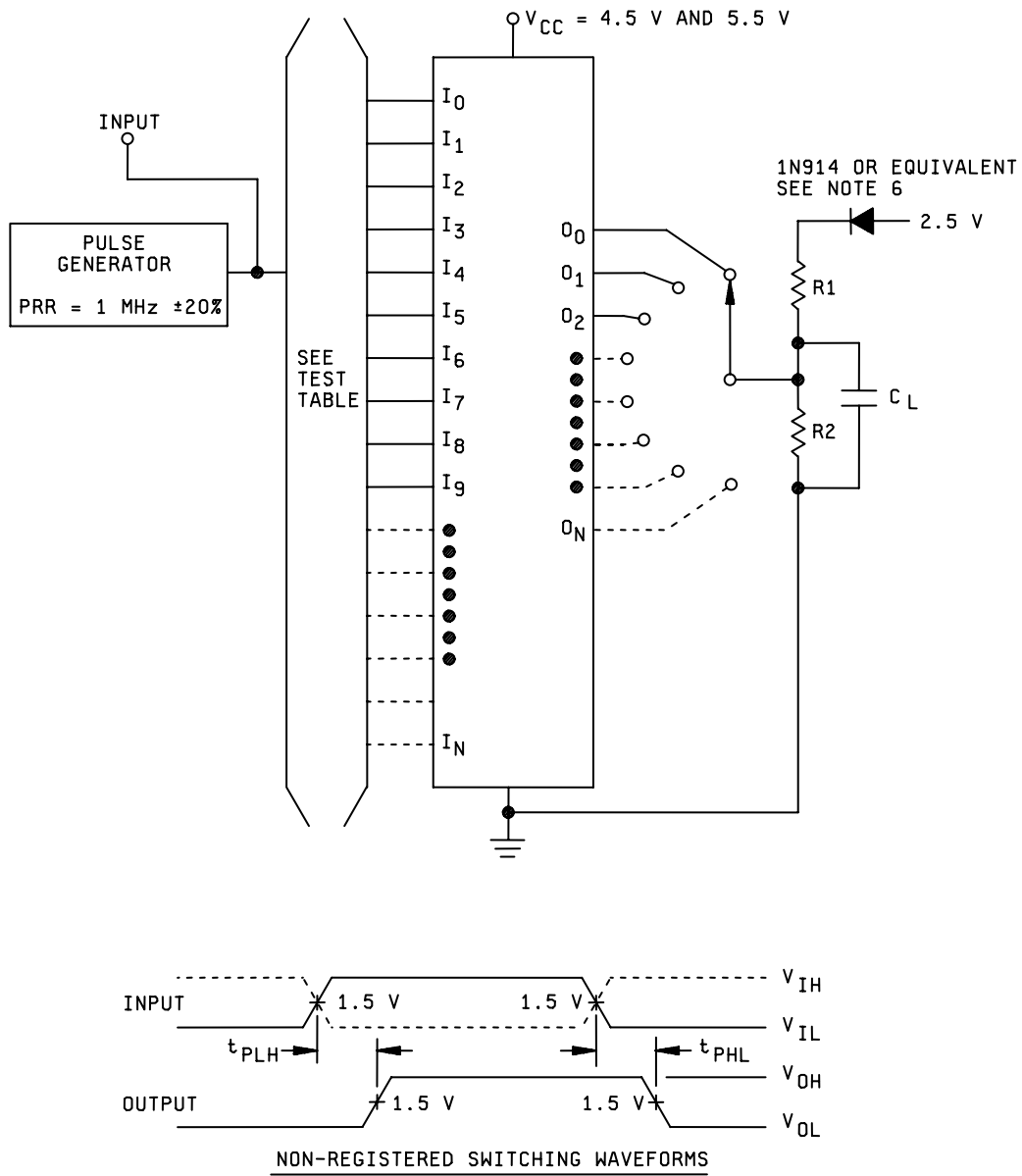
FIGURE 2. Truth tables (unprogrammed).

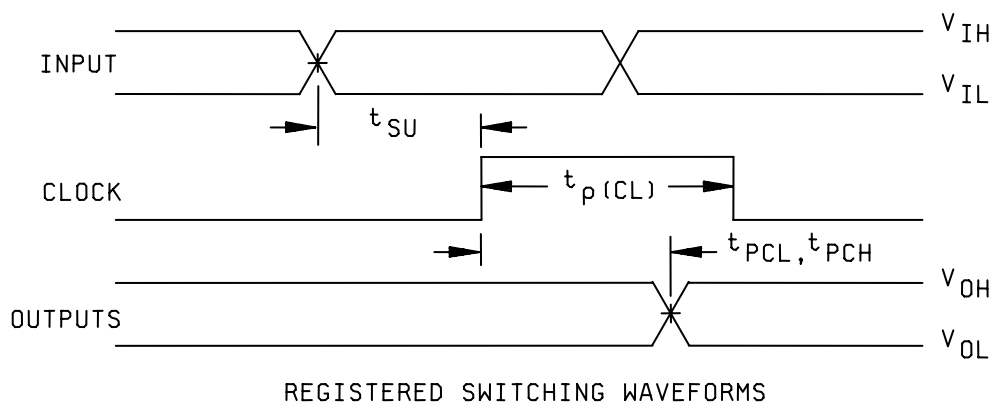
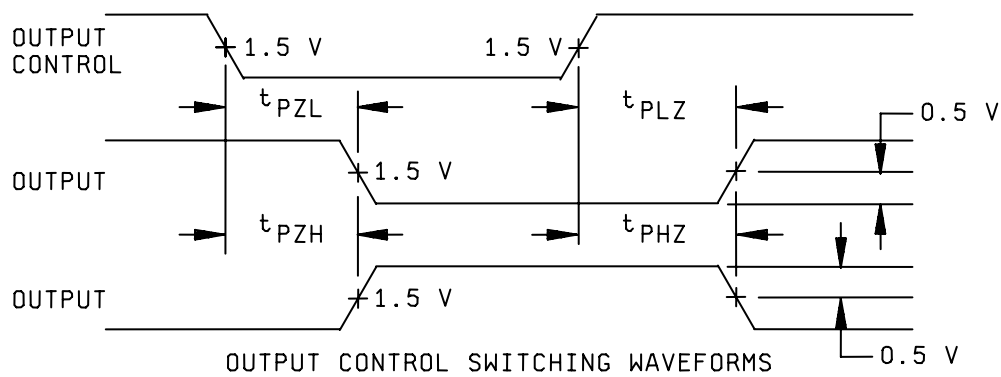
Device type 01FIGURE 3. Unprogrammed Logic diagram .

Device type 02FIGURE 3. Unprogrammed Logic diagram – Continued.

Device type 03FIGURE 3. Unprogrammed Logic diagram – Continued.

Device type 04FIGURE 3. Unprogrammed Logic diagram – Continued.

FIGURE 4. Switching time test circuit and waveforms.

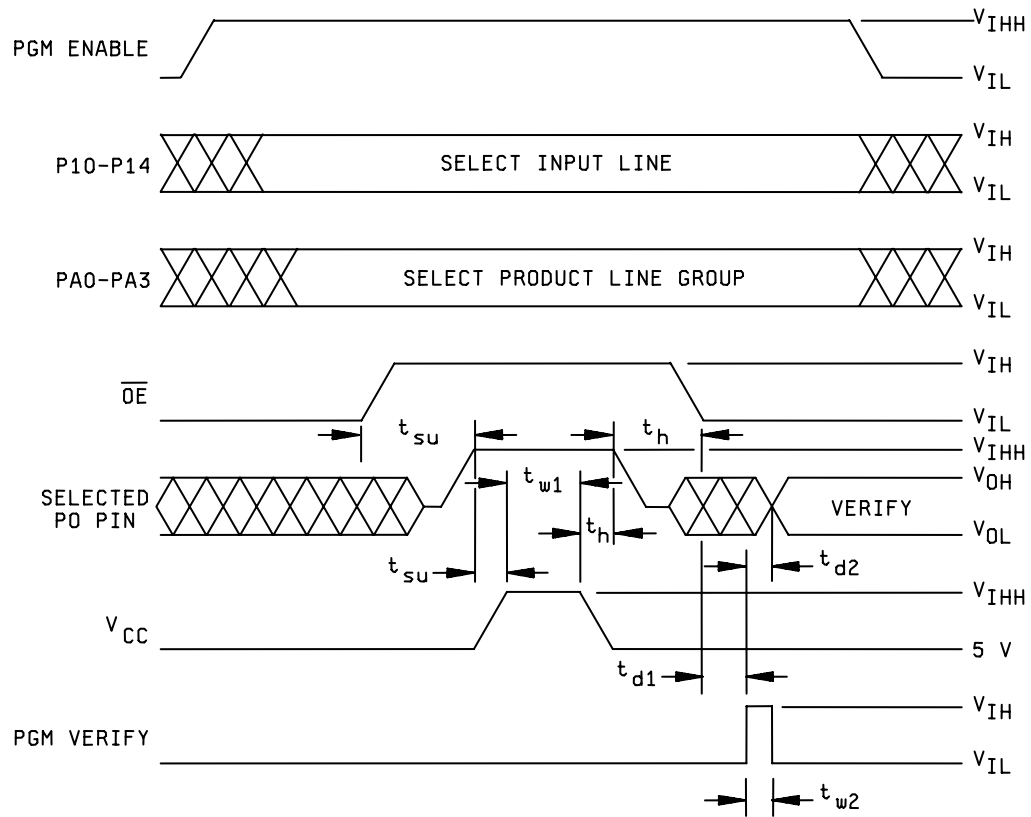


NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting device.
2. $C_L = 45 \text{ pF}$ minimum, including jig and probe capacitance; $R1 = 390 \Omega \pm 5\%$; $R2 = 750 \Omega \pm 5\%$.
3. Outputs may be under load simultaneously.
4. Requirements for $t_p(C_L)$, t_{SU} , and t_H are established by setting parameters to the limits in table I and observing proper output state changes.
5. $V_{IH} = 3.0 \text{ V}$; $V_{IL} = 0.0 \text{ V}$.
6. For circuit C, the diode / $V_{BIAS} = 2.5 \text{ V}$ may be replaced with switch S1, and V_{BIAS} of 5.0 V . S1 is open for t_{PZH} , t_{PHZ} , and F_{max} tests.

FIGURE 4. Switching time test circuit and waveforms - Continued.

Circuit C

FIGURE 5c. Programming waveforms - Continued.

Pin number	Products 0 thru 39	Products 40 thru 79
1	O ₀	CLOCK
2	I ₀	I ₀
3	I ₁	I ₁
4	I ₂	I ₂
5	I ₃	I ₃
6	I ₄	I ₄
7	I ₅	I ₅
8	I ₆	I ₆
9	I ₇	I ₇
10	I ₈	I ₈
11	I ₉	I ₉
12	GND	GND
13	CLOCK	O _D
14	L/R	O ₄
15	A ₀	O ₃
16	A ₁	O ₂
17	A ₂	O ₁
18	NC	O ₀
19	O ₄	NC
20	O ₃	A ₂
21	O ₂	A ₁
22	O ₁	A ₀
23	O ₀	L/R
24	V _{CC}	V _{CC}

FIGURE 6a. Programming pin identification for circuit A and B.

Pin number	Products
1	PGM VERIFY
2	P10
3	P11
4	P12
5	P13
6	P14
7	P15
8	PA8
9	PA9
10	PA10
11	PGM ENABLE
12	GND
13	$\overline{OE}$
14	NOT USED
15	P07
16	P06
17	P05
18	P04
19	P03
20	P02
21	P01
22	P00
23	NOT USED
24	V _{CC}

FIGURE 6b. Programming pin identification for circuit C - Continued.

TABLE III. Programming characteristics for circuit A.

Symbol	Parameters	Limits			Unit
		Min	Typ	Max	
V_{IHH}	Program-level input voltage	11.5	11.75	12.0	V
I_{IHH}	Program-level input current	Output program pulse		50	mA
		Output disable, OD		50	
		All other inputs		10	
I_{CCH}	Program supply current			900	mA
T_P	Program pulse width	10	20	50	μ s
t_d	Delay time	100			ns
---	Program pulse duty cycle			20	%
V_P	Program/verify – protect input voltage	18	18.5	19	V
I_P	Program/verify – protect input current			400	mA
T_{PP}	Security fuse programming pulse width	10	40	70	μ s
	Security fuse programming duty cycle			50	%
t_{RP}	Rise time of output programming and address pulses	1	1.5	10	V/ μ s
t_{RP}	Rise time of security use programming pulses	1	1.5	10	V/ μ s
V_{CCPP}	V_{CC} value during security fuse programming	5.75	6.0	6.25	V
	V_{CC} value for first verify	4.75	5.0	5.25	
	V_{CC} value for high V_{CC} verify	5.4	5.5	5.6	
	V_{CC} value for low V_{CC} verify	4.4	4.5	4.6	

TABLE IV. Input line select for circuit A.

Input line number	Pin identification										
	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

Voltage legend:

L = Low level input voltage (V_{IL}).
 H = High level input voltage (V_{IH}).
 HH = High level program voltage (V_{IHH}).
 Z = High impedance (e.g., 10 k Ω to 5.0 V).

TABLE V. Product line select for circuit A.

Product line number	Pin identification							
	O ₄	O ₃	O ₂	O ₁	O ₀	A ₂	A ₁	A ₀
0, 40	Z	Z	Z	Z	HH	Z	Z	Z
1, 41	Z	Z	Z	Z	HH	Z	Z	HH
2, 42	Z	Z	Z	Z	HH	Z	HH	Z
3, 43	Z	Z	Z	Z	HH	Z	HH	HH
4, 44	Z	Z	Z	Z	HH	HH	Z	Z
5, 45	Z	Z	Z	Z	HH	HH	Z	HH
6, 46	Z	Z	Z	Z	HH	HH	HH	Z
7, 47	Z	Z	Z	Z	HH	HH	HH	HH
8, 48	Z	Z	Z	HH	Z	Z	Z	Z
9, 49	Z	Z	Z	HH	Z	Z	Z	HH
10, 50	Z	Z	Z	HH	Z	Z	HH	Z
11, 51	Z	Z	Z	HH	Z	Z	HH	HH
12, 52	Z	Z	Z	HH	Z	HH	Z	Z
13, 53	Z	Z	Z	HH	Z	HH	Z	HH
14, 54	Z	Z	Z	HH	Z	HH	HH	Z
15, 55	Z	Z	Z	HH	Z	HH	HH	HH
16, 56	Z	Z	HH	Z	Z	Z	Z	Z
17, 57	Z	Z	HH	Z	Z	Z	Z	HH
18, 58	Z	Z	HH	Z	Z	Z	HH	Z
19, 59	Z	Z	HH	Z	Z	Z	HH	HH
20, 60	Z	Z	HH	Z	Z	HH	Z	Z
21, 61	Z	Z	HH	Z	Z	HH	Z	HH
22, 62	Z	Z	HH	Z	Z	HH	HH	Z
23, 63	Z	Z	HH	Z	Z	HH	HH	HH
24, 64	Z	HH	Z	Z	Z	Z	Z	Z
25, 65	Z	HH	Z	Z	Z	Z	Z	HH
26, 66	Z	HH	Z	Z	Z	Z	HH	Z
27, 67	Z	HH	Z	Z	Z	Z	HH	HH
28, 68	Z	HH	Z	Z	Z	HH	Z	Z
29, 69	Z	HH	Z	Z	Z	HH	Z	HH
30, 70	Z	HH	Z	Z	Z	HH	HH	Z
31, 71	Z	HH	Z	Z	Z	HH	HH	HH
32, 72	HH	Z	Z	Z	Z	Z	Z	Z
33, 73	HH	Z	Z	Z	Z	Z	Z	HH
34, 74	HH	Z	Z	Z	Z	Z	HH	Z
35, 75	HH	Z	Z	Z	Z	Z	HH	HH
36, 76	HH	Z	Z	Z	Z	HH	Z	Z
37, 77	HH	Z	Z	Z	Z	HH	Z	HH
38, 78	HH	Z	Z	Z	Z	HH	HH	Z
39, 79	HH	Z	Z	Z	Z	HH	HH	HH

Voltage legend;

HH = High level program voltage (V_{IHH}).Z = High impedance (e.g., 10 k Ω to 5.0 V).

TABLE VI. Programming characteristics for circuit B.

Symbol	Parameter		Limits			Units
			Min	Typ	Max	
V_{IHH}	Program-level input voltage		11.0	11.5	12.0	V
I_{IHH}	Program-level input current	Output program pulse			50	mA
		OE, L/R			25	
		All other inputs			5	
I_{CCH}	Program supply current				400	mA
T_P	Program pulse width		10		50	μ s
t_d	Delay time		100			ns
---	Program pulse duty cycle				25	%
V_P	Program verify protect-input voltage			20		V
I_P	Program verify protect-input current				400	mA
t_{dv}	Delay time to verify		100			μ s
V_{PH}	Programming pulse		11.0	11.5	12.0	V

TABLE VII. Input line select for circuit B.

Input line number	Pin identification										L/R
	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

Voltage legend:

L = Low level input voltage (V_{IL}).H = High level input voltage (V_{IH}).HH = High level program voltage (V_{IHH}).Z = High impedance (e.g., 10 k Ω to 5.0 V).

TABLE VIII. Product line select for circuit B.

Product line number	Pin identification							
	O ₄	O ₃	O ₂	O ₁	O ₀	A ₂	A ₁	A ₀
0, 40	Z	Z	Z	Z	HH	Z	Z	Z
1, 41	Z	Z	Z	Z	HH	Z	Z	HH
2, 42	Z	Z	Z	Z	HH	Z	HH	Z
3, 43	Z	Z	Z	Z	HH	Z	HH	HH
4, 44	Z	Z	Z	Z	HH	HH	Z	Z
5, 45	Z	Z	Z	Z	HH	HH	Z	HH
6, 46	Z	Z	Z	Z	HH	HH	HH	Z
7, 47	Z	Z	Z	Z	HH	HH	HH	HH
8, 48	Z	Z	Z	HH	Z	Z	Z	Z
9, 49	Z	Z	Z	HH	Z	Z	Z	HH
10, 50	Z	Z	Z	HH	Z	Z	HH	Z
11, 51	Z	Z	Z	HH	Z	Z	HH	HH
12, 52	Z	Z	Z	HH	Z	HH	Z	Z
13, 53	Z	Z	Z	HH	Z	HH	Z	HH
14, 54	Z	Z	Z	HH	Z	HH	HH	Z
15, 55	Z	Z	Z	HH	Z	HH	HH	HH
16, 56	Z	Z	HH	Z	Z	Z	Z	Z
17, 57	Z	Z	HH	Z	Z	Z	Z	HH
18, 58	Z	Z	HH	Z	Z	Z	HH	Z
19, 59	Z	Z	HH	Z	Z	Z	HH	HH
20, 60	Z	Z	HH	Z	Z	HH	Z	Z
21, 61	Z	Z	HH	Z	Z	HH	Z	HH
22, 62	Z	Z	HH	Z	Z	HH	HH	Z
23, 63	Z	Z	HH	Z	Z	HH	HH	HH
24, 64	Z	HH	Z	Z	Z	Z	Z	Z
25, 65	Z	HH	Z	Z	Z	Z	Z	HH
26, 66	Z	HH	Z	Z	Z	Z	HH	Z
27, 67	Z	HH	Z	Z	Z	Z	HH	HH
28, 68	Z	HH	Z	Z	Z	HH	Z	Z
29, 69	Z	HH	Z	Z	Z	HH	Z	HH
30, 70	Z	HH	Z	Z	Z	HH	HH	Z
31, 71	Z	HH	Z	Z	Z	HH	HH	HH
32, 72	HH	Z	Z	Z	Z	Z	Z	Z
33, 73	HH	Z	Z	Z	Z	Z	Z	HH
34, 74	HH	Z	Z	Z	Z	Z	HH	Z
35, 75	HH	Z	Z	Z	Z	Z	HH	HH
36, 76	HH	Z	Z	Z	Z	HH	Z	Z
37, 77	HH	Z	Z	Z	Z	HH	Z	HH
38, 78	HH	Z	Z	Z	Z	HH	HH	Z
39, 79	HH	Z	Z	Z	Z	HH	HH	HH

Voltage legend:

HH = High level program voltage, V_{HH} .Z = High impedance (e.g., 10 k Ω to 5.0 V).

Table IX. Programming characteristics for circuit C.

Symbol	Description		Min	Nom	Max	Unit
V _{CC}	Verify level supply voltage		5.25	5.50	5.75	V
V _{IH}	High level input voltage		2.40		5.50	V
V _{IL}	Low level input voltage				.50	V
V _{IHH}	Program pulse voltage		10.25	10.50	10.75	V
I _{IHH}	Program pulse current	PO		20	50	mA
		PGM, ENA, $\overline{OE}$		10	25	mA
		PI, PA		10	25	mA
		I _{CC}			500	mA
t _{w1}	Program pulse duration at PO		10		50	μs
t _{su}	Set up time		100			ns
t _h	Hold time		100			ns
t _{d1}	Delay time from $\overline{OE}$ low to PGM verify		100			ns
t _{d2}	Delay time from PGM verify to valid output		200			ns
t _{w2}	Pulse duration at PGM verify		100			ns

Table X. Input line select for circuit C.

INPUT LINE NUMBER	Input line number address pin states						
	PI0	PI1	PI2	PI3	PI4	PI5	HEX
00	L	L	L	L	L	L	00
01	L	L	L	L	L	H	01
02	L	L	L	L	H	L	02
03	L	L	L	L	H	H	03
04	L	L	L	H	L	L	04
05	L	L	L	H	L	H	05
06	L	L	L	H	H	L	06
07	L	L	L	H	H	H	07
08	L	L	H	L	L	L	08
09	L	L	H	L	L	H	09
10	L	L	H	L	H	L	0A
11	L	L	H	L	H	H	0B
12	L	L	H	H	L	L	0C
13	L	L	H	H	L	H	0D
14	L	L	H	H	H	L	0E
15	L	L	H	H	H	H	0F
16	L	H	L	L	L	L	10
17	L	H	L	L	L	H	11
18	L	H	L	L	H	L	12
19	L	H	L	L	H	H	13
20	L	H	L	H	L	L	14
21	L	H	L	H	L	H	15
22	L	H	L	H	H	L	16
23	L	H	L	H	H	H	17
24	L	H	H	L	L	L	18
25	L	H	H	L	L	H	19
26	L	H	H	L	H	L	1A
27	L	H	H	L	H	H	1B
28	L	H	H	H	L	L	1C
29	L	H	H	H	L	H	1D
30	L	H	H	H	H	L	1E
31	L	H	H	H	H	H	1F
32	H	L	L	L	L	L	20
33	H	L	L	L	L	H	21
34	H	L	L	L	H	L	22
35	H	L	L	L	H	H	23
36	H	L	L	H	L	L	24
37	H	L	L	H	L	H	25
38	H	L	L	H	H	L	26
39	H	L	L	H	H	H	27
SF	H	H	H	H	H	H	3F

Table XI. Product term addressing for circuit C.

PRODUCT TERMS								ADDRESS PIN STATES		
PO0	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PA8	PA9	PA10
00	08	16	24	32	40	48	56	L	L	L
01	09	17	25	33	41	49	57	L	L	H
02	10	18	26	34	42	50	58	L	H	L
03	11	19	27	35	43	51	59	L	H	H
04	12	20	28	36	44	52	60	H	L	L
05	13	21	29	37	45	53	61	H	L	H
06	14	22	30	38	46	54	62	H	H	L
07	15	23	31	39	47	55	63	H	H	H
SF → ----	----	----	----	----	----	----	----	X	X	H ←SF

SF – Security fuse (does not require voltage to the PO pin).

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but it is not mandatory)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of the specification.
- b. PIN and compliance identifier, if applicable (see 1.2).
- c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirement for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to the acquiring activity in addition to notification to the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- g. . Requirement for product assurance options.
- h. Requirements for special carriers, lead lengths or lead forming. If applicable, these requirements will not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- i. Requirement for programming the device, including processing option.
- j. Requirements for "JAN" marking.
- k. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

GND	Electrical ground (common terminal)
V _{IN}	Voltage level at an input terminal.
V _{IC}	Input clamp voltage.
I _{IN}	Current flowing into an input terminal.

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish A (see 3.4). Longer length leads and lead forming will not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.8.1) and programmed by the maintenance activity, except where use of quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic industry type. Generic industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

<u>Device type</u>	<u>Commercial type</u>	<u>Fusible Link</u>
01	PAL20L8A	TiW
02	PAL20R8A	TiW
03	PAL20R6A	TiW
04	PAL20R4A	TiW

6.8 Manufacturers' designations. Manufacturers' circuits included in this specification are designated as shown in table XII.

<u>Table XII. Manufacturers' designations</u>			
<u>Device Type</u>	<u>Monolithic Memories</u>	<u>National</u>	<u>Texas Instruments</u>
	<u>Circuits</u>		
	<u>A</u>	<u>B</u>	<u>C</u>
01	X (CECD/50364) 1/	X (CCXP/27014) 1/	X (CGO/01295) 1/
02	X	X	X
03	X	X	X
04	X	X	X

1/ Symbol / FSCM number.

6.9 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue.

Custodians:
 Army –CR
 Navy - EC
 Air Force - 11
 DLA-CC

Preparing activity:

DLA - CC

Review activities:
 Army – MI, SM
 Navy – AS, CG, MC, SH, TD
 Air Force – 03, 19, 99

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NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://assist.daps.dla.mil>.