INCH POUND

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MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR FIELD PROGRAMMABLE LOGIC ARRAY (FPLA) 16 x 48 x 8, MONOLITHIC SILICON

Inactive for new design after 28 July 1995.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, bipolar, field programmable logic array (FPLA) microcircuits which employ thin film nichrome resistors (NICr) as the fusible link or programming element. Three product assurance classes and a choice of case outline / lead material and finish are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device type. The device types are as follows:

Device type	Circuit
01	16 x 48 x 8 logic array with uncommitted collector
02	16 x 48 x 8 logic array with active pull-up and a third high-impedance state output.

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28, CDIP2-T28	28	Dual in line package

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to memory@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

1.3 Absolute maximum ratings.

Supply voltage range ..... -0.5 V dc to 7.0 V dc
Input voltage range ..... 0.5 V dc at -10. mA to 5.5 V dc
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +260°C
Thermal resistance, junction-to-case (θ_{JC}) 1/..... 27 °C / W
Output voltage applied ..... -0.4 V dc to +5.5 V dc
Output sink current ..... 9.6 mA
Maximum power dissipation, (P_D) 2/ ..... 2.0 W
Maximum junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage ..... 4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage ..... 2.0 V dc
Maximum low level input voltage ..... 0.8 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

2.0 APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and standards. The following specifications and standards form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Heat sinking is recommended to reduce the junction temperature.
2/ Must withstand the added P_D due to short circuit condition (e.g., I_{OS}) test.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3). When manufacturer programmed devices are delivered to the user, an altered item drawing shall be prepared by the procuring activity to specify the required program configuration.

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Truth tables.

3.3.2.1 Unprogrammed devices. The truth tables for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test as per table A-I (a minimum of 50% of the total number of gates programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.3.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.3.3 Logic diagrams. The logic diagram shall be as specified on figure 3.

3.3.4 Case outlines. Case outlines shall be in accordance with MIL-STD-1835 and 1.2.3 herein.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.6 Electrical test requirements. Electrical test requirements shall be as specified in table III and (where applicable), the altered item drawing for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualifications, and quality conformance, by device class, are specified in table II.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity.

3.8 Processing options. Since the FPLA is an unprogrammed device capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.8.1 Unprogrammed FPLA delivered to the user. All testing shall be verified through group A testing as defined in 3.3.2.1, tables II and III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.8.2 Manufacturer programmed FPLA delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/	Device types	Limits		Unit
				Min	Max	
High-level output voltage	V_{OH}	V_{CC} = 4.5 V; I_{OH} = -2 mA	02	2.4		V
Low-level output voltage	V_{OL}	V_{CC} = 5.5 V; I_{OL} = 9.6 mA	01,02		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V; I_{IN} = -18 mA	01,02		-1.2	V
Maximum collector cut-off current	I_{CEX}	V_{CC} = 5.5 V; V_O = 5.5 V	01		100	µA
High-impedance (off-state) output high current	I_{OHZ}	V_{CC} = 5.5 V; V_O = 5.5 V	02		100	µA
High-impedance (off-state) output low current	I_{OLZ}	V_{CC} = 5.5 V; V_O = 0.45 V	02		-60	µA
High-level input current	I_{IH}	V_{CC} = 5.5 V; V_{IN} = 5.5 V	01,02		50	µA
Low-level input current	I_{IL}	V_{CC} = 5.5 V; V_{IN} = 0.45 V	01,02	-1	-250	µA
Short circuit output current	I_{OS} 2/	V_{CC} = 5.5 V; V_{OUT} = GND	02	-10	-85	mA
Supply current	I_{CC}	V_{CC} = 5.5 V; V_{IN} = 0; outputs = open	01,02		180	mA
Propagation delay time high-to-low level logic, input to output	t_{PHL1} (t_{IA})	V_{CC} = 4.5 V and 5.5 V; C_L = 30 pF (See figure 4)	01,02		80	ns
Propagation delay time low-to-high level logic, input to output	t_{PLH1} (t_{IA})		01,02		80	ns
Propagation delay time high-to-low level logic, enable to output	t_{PHL2} (t_{EC})		01,02		50	ns
Propagation delay time low-to-high level logic, enable to output	t_{PLH2} (t_{CO})		01,02		50	ns

1/ Complete terminal conditions shall be specified in table III.

2/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (per table III) 2/, 3/	
	Class S devices	Class B devices
Interim electrical parameters (pre burn-in)	1	1
Final electrical test parameters for unprogrammed devices	1*, 2, 3, 7*, 8	1*, 2, 3, 7*, 8
Final electrical test parameters for programmed devices	1*, 2, 3, 7*, 8, 9, 10, 11	1*, 2, 3, 7*, 8, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group B electrical test parameters When using the method 5005 QCI option	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical parameters	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8
Group D end-point electrical parameters	1, 2, 3, 7, 8	1, 2, 3, 7, 8

1/ (*) indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroup 7 and 8 shall consist of verifying the pattern specified.

Pin Number Case X	Device Type 01 and 02
1	FE
2	I_7
3	I_6
4	I_5
5	I_4
6	I_3
7	I_2
8	I_1
9	I_0
10	F_7
11	F_6
12	F_5
13	F_4
14	GND
15	F_3
16	F_2
17	F_1
18	F_0
19	$\overline{CE}$
20	I_{15}
21	I_{14}
22	I_{13}
23	I_{12}
24	I_{11}
25	I_{10}
26	I_9
27	I_8
28	V_{CC}

FIGURE 1. Terminal connections.

Circuit Type	$\overline{CE}$	Address																Output level								Device type
		I_{15}	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
A	L	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	L [1]	L [1]	L [1]	L [1]	L [1]	L [1]	L [1]	L	01, 02
B	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	01, 02
A, B	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1/	1/	1/	1/	1/	1/	1/	1/	01
A, B	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	02

NOTES:

1. Output disabled.
2. X = Input may be high, low level, open circuit or as defined in Appendix A.
3. L = Low
4. H = High
5. Hi Z = High impedance.

FIGURE 2. Truth table (unprogrammed).

DEVICE TYPES 01 AND 02

CIRCUIT A

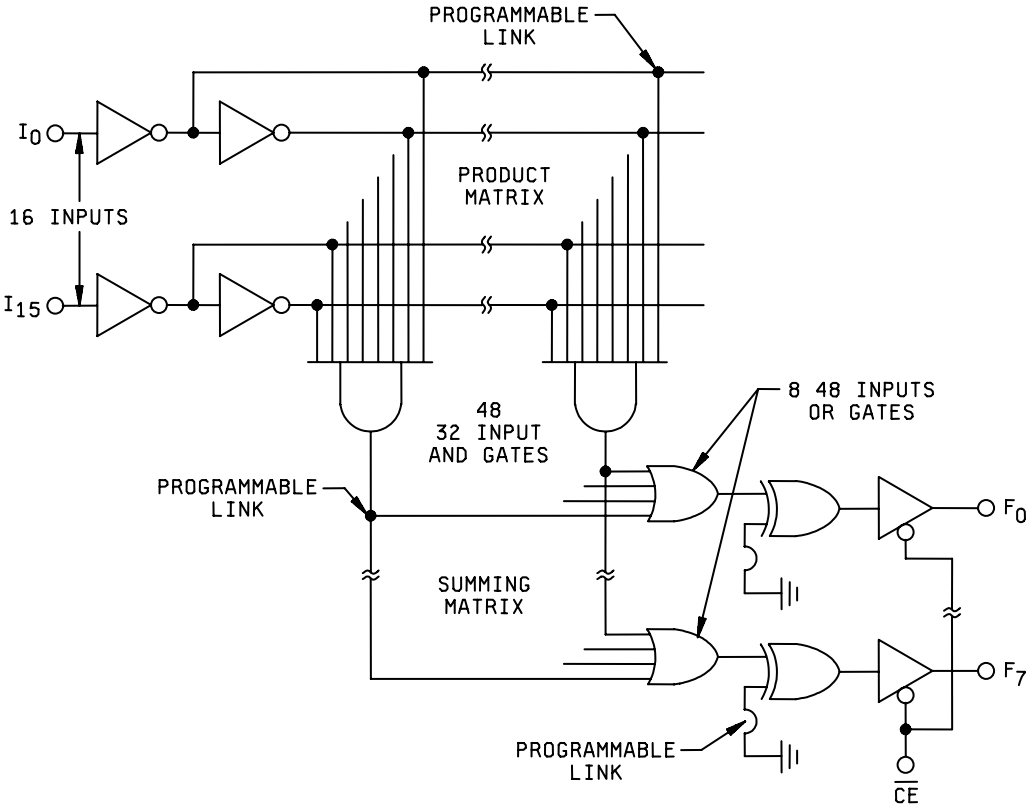


FIGURE 3. Logic diagram.

DEVICE TYPES 01 AND 02

CIRCUIT B

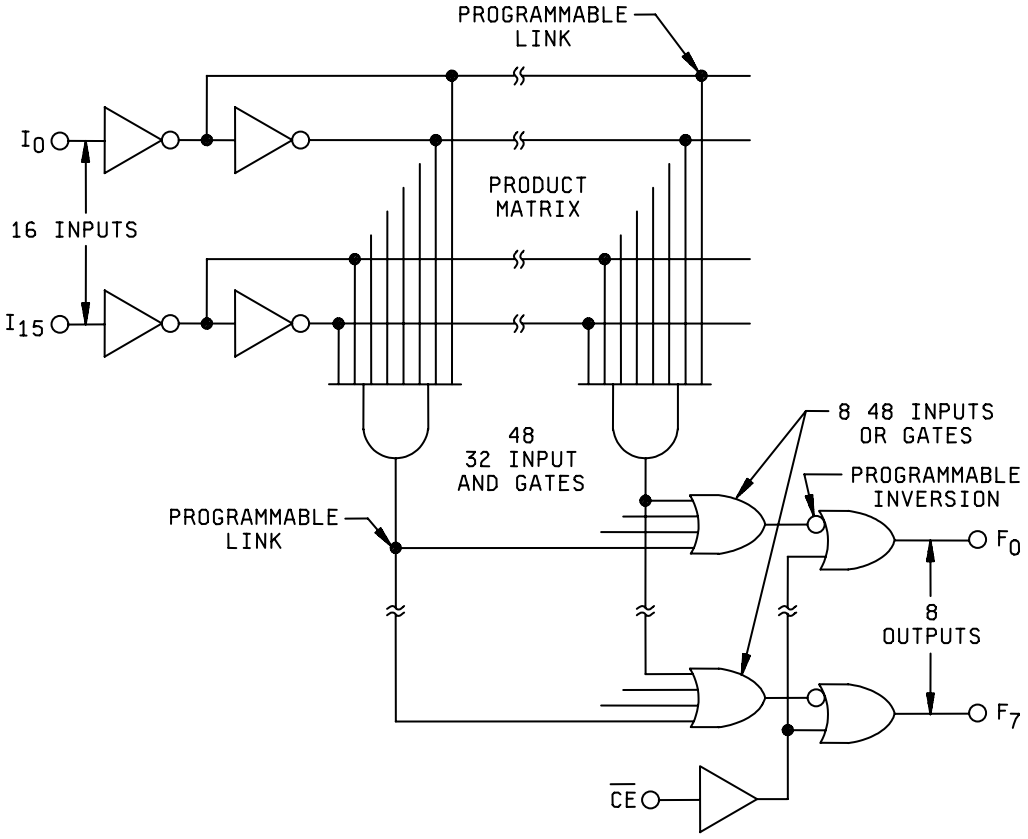
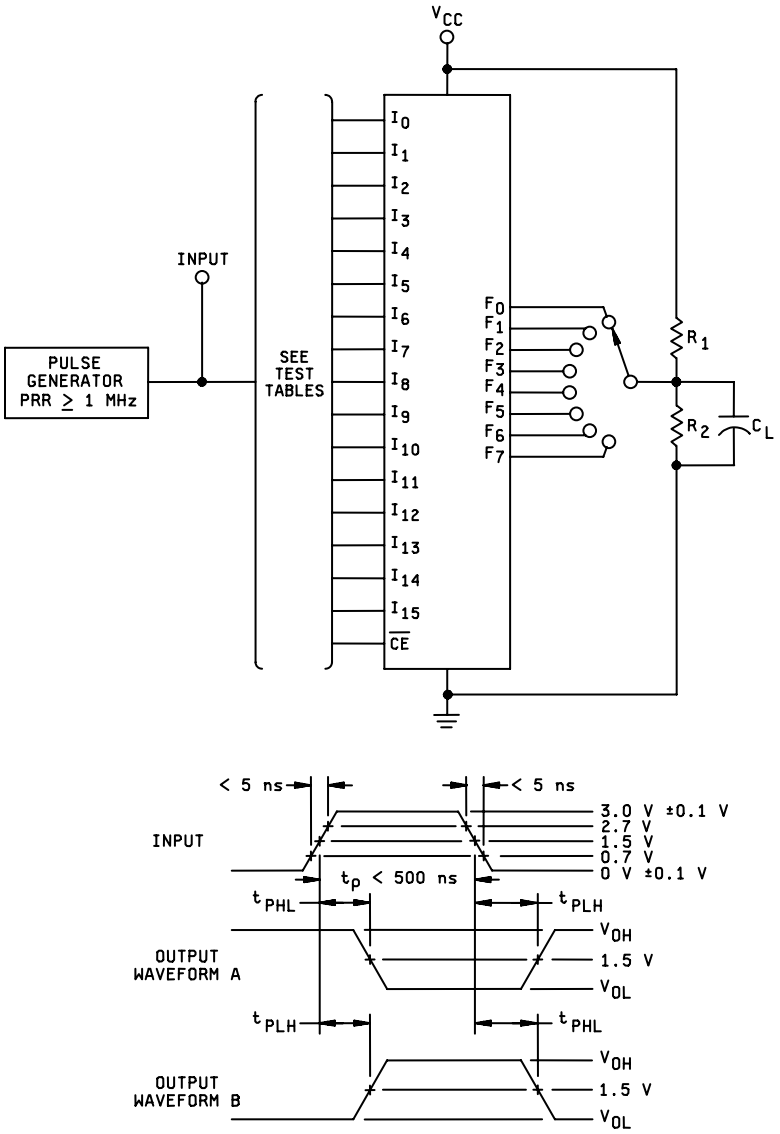


FIGURE 3. Logic diagram. - Continued.



NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting FPLA.
2. C_L = 30 pF minimum, including jig and probe capacitance; R1 = 300 Ω ± 25% and R2 = 600 Ω ±20%.
3. Outputs may be under load simultaneously.

FIGURE 4. Switching time test circuit.

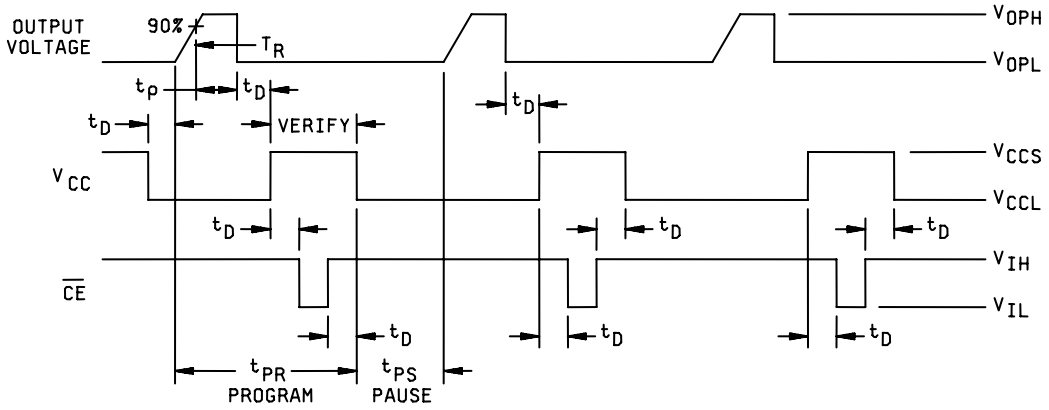


FIGURE 5A. Output polarity program – verify sequence.

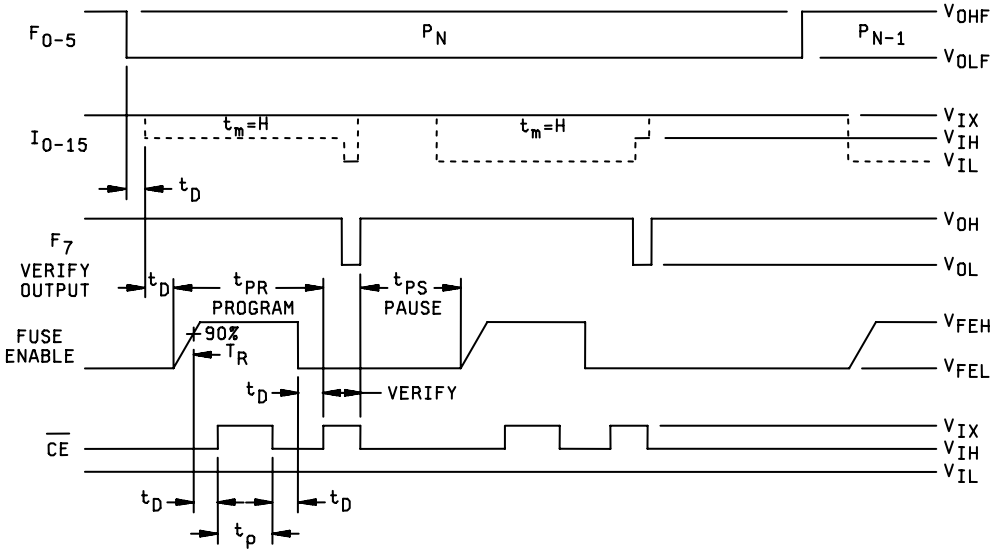


FIGURE 5B. "AND" matrix program – verify sequence.

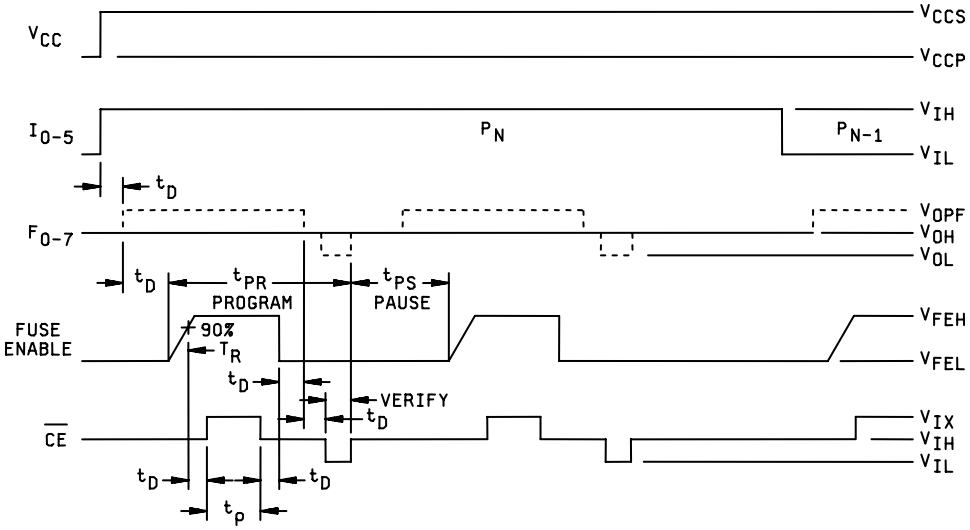


FIGURE 5C. "OR" matrix program – verify sequence.
FIGURE 5. Typical program – verify sequence circuit A.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535. Qualification data for subgroups 7, 8, 9, 10, and 11 shall be attributes only.

4.3 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted prior to qualification, and conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

d. All devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn in.

4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Tests shall be as specified in table II.

b. Subgroups 4, 5, and 6 of table III of MIL-PRF-38535 shall be omitted.

c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve (12) devices shall be submitted to programming (see 3.3.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturers option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.

d. For unprogrammed devices, ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail in all three subgroups, the lot shall be rejected. At the manufacturers option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

a. Water drop test. This test shall be added to group B for class S devices. The devices selected for subgroup 2 (b) testing shall be a sealed, electrically good unprogrammed device which has passed the applicable screening and group A electrical test requirements. The device shall be carefully delidded and functionally verified to contain no programmed bits. Power shall be applied (or continually cycled through its test sequence), for the duration of the test. A drop of deionized water (resistivity of 5 megohms minimum at the point of use and at 25°C) shall be placed on the memory element containing nichrome film resistors so as to completely cover a minimum of 25 percent of the memory bits without touching any bonding pads, wires, or exposed metallization. Examination the water drop at 20 X magnification during placement with a micropipette is sufficient to determine coverage. The water drop shall be allowed to remain with the device under power for a minimum of 3 minutes duration. The power shall be removed, the device dried, and the device functionally verified to contain no programmed bit. Failure of any functional test which results from an open thin nichrome resistor (other than test equipment induced) shall fail the lot.

b. Electrical parameters shall be as specified in table II herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

c. For qualification, at least 50 percent of the sample selected for life testing shall be programmed (see 3.3.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the life test.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535; end point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Programming procedure for circuit A. The programming specifications in table IV and the following procedures shall be used for programming the device.

4.6.1 Output polarity.

4.6.1.1 Program active low (F_P function). Program output polarity before programming “AND” matrix and “OR” matrix. Program 1 output at a time. (S) links of unused outputs are not required to be fused.

a. Set GND (pin 14), and FE (pin 1) to 0 V.

b. Set V_{CC} (pin 28) to V_{CCL}.

c. Set $\overline{CE}$ (pin 19), and I_0 through I_{15} to V_{IH}.

d. Apply V_{OPH} to the appropriate output, and remove after a period t_p.

e. Repeat step D to program other outputs.

4.6.1.2 Verify output polarity.

a. Set GND (pin 14) to 0 V, and V_{CC} (pin 28) to V_{CCS}.

b. Enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.

c. Address a non-existent P-term by applying V_{IH} to all inputs I_0 through I_{15}.

d. Verify output polarity by sensing the logic state of outputs F_0 through F_7. All outputs at a high logic level are programmed active low (F_P function), while all outputs at a low logic level are programmed active high (F_P function).

e. Return V_{CC} to V_{CCP} or V_{CCL}.

f. For class S and B devices, if any output polarity does not verify as programmed, it shall be considered a programming reject. For class C devices, if any output does not verify as programmed, repeat 4.6.1.1 one time only. Outputs which fail to program the second time shall be considered programming rejects.

4.6.2 "AND" Matrix.

4.6.2.1 Programming input variable. Program one input at a time and one P-term at a time. All input variable links of unused P-terms are not required to be fused. However, unused input variables must be programmed as Don't Care for all programmed P-terms.

a. Set GND (pin 14) to 0 V, and V_{CC} (pin 28) to V_{CCP}.

b. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.

c. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

d. Address the P-term to be programmed (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5 with F_0 as LSE. Use standard TTL logic levels V_{OHF} and V_{OLF}.

e. If the P-term contains neither I_0 or $\overline{I}_0$ (input is a Don't care), fuse both I_0 and $\overline{I}_0$ links by executing both steps f and g, before continuing with step k.

f. If the P-term contains I_0, set to fuse the $\overline{I}_0$ link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute steps h, i, and j.

g. If the P-term contains $\overline{I}_0$, set to fuse the I_0 link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute steps h, i, and j.

h. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.

i. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period of t_P.

j. After t_D delay, return FE input to V_{FEL}.

k. Disable programmed input by returning I_0 to V_{IX}.

l. Repeat steps e through k for all other input variables.

m. Repeat steps d through e for all other P-terms.

n. Remove V_{IX} from all input variables.

4.6.2.2 Verify input variable.

a. Set GND (pin 14) to 0 V, V_{CC} (pin28) to V_{CCP}, and FE (pin 1) to V_{FEL}.

b. Enable F_7 output by setting CE to V_{IX}.

c. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

d. Address the P-term to be verified (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5.

e. Interrogate input variable I_0 as follows:

1. Lower the input voltage to I_0 from V_{IX} to V_{IH}, and sense the logic state of output F_7.

2. Lower the input voltage to I_0 from V_{IH} to V_{IL}, and sense the logic state of output F_7.

f. The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	Input variable state contained in P-term 1/
0	1	$\overline{I}_0$
1	0	
0	0	I_0
1	1	
0	1	Don't Care
1	1	
0	0	(I_0), $(\overline{I}_0)$
1	0	

1/ Two tests are required to uniquely determine the state of the input variable contained in the P-term.

g. Disable verified input by returning to I_0 to V_{IX}.

h. Repeat steps e and g for all other input variables.

i. Repeat steps d through h for all other P-terms.

j. Remove V_{IX} from all input variables.

k. For class S and B devices, if any gate does not verify as programmed, it shall be considered a programming reject.

4.6.3 "OR" (Sum) Matrix.

4.6.3.1 Program product term. Program one output at a time for a P-term at the time. All P_n links in the "OR" matrix corresponding to unused outputs and unused P-terms are not required to be fused.

a. Set GND (pin 14) to 0 V, and V_{CC} (pin 28) to V_{CCS}.

b. Disable the chip by setting $\overline{CE}$ (pin 19) to V_{IH}.

c. Set inputs I_6 through I_{15} to V_{IH} or V_{IL}.

d. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as LSB.

e. If the P-term is contained in output functions F_0 (F_0 = 1 or F_0 = 0), go to step g, (fusing cycle not required).

f. If the P-term is not contained in output function F_0 (F_0 = 0 or F_0 = 1), set to fuse the P_n link by forcing output F_0 to V_{OPF}.

g. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.

h. After t_D delay, pulse the CE input from V_{IH} to V_{IX} for a period t_P.

i. After t_D delay, return FE input to V_{FEL}.

j. After t_D delay, remove V_{OPF} from output F_0.

k. Repeat steps e through j for all other output functions.

l. Repeat steps d through k for all other P-terms.

m. Remove V_{CCS} from V_{CC}.

4.6.3.2 Verify product term.

a. Set GND (pin 14) to 0 V, and V_{CC} (pin 28) to V_{CCS}.

b. Enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.

c. Set inputs I_0 through I_{15} to V_{IH} and V_{IL}.

d. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5.

e. To determine the status of the P_n link in the "OR" matrix for each output function F_P or F_P sense, the state of outputs F_0 through F_7. The status of the link is given by the following truth table:

Output		P-term link
Active high (F_P)	Active low (F_P°)	
0	1	Fused
1	0	Present

f. Repeat steps d and e for all other P-terms.

g. Remove V_{CCS} from V_{CC}.

h. For class S and B devices, if any bit does not verify as programmed it shall be considered a programming reject.

4.7 Programming procedure for circuit B. The programmed specifications on table V and the following procedures shall be used for programming the device.

4.7.1 Program "PRODUCT (AND)" matrix.

4.7.1.1 All 48 AND gates of the product matrix are fuse linked to both the true and false lines of every input buffer in the initial unprogrammed state. The initial logic expression for the 48 unprogrammed AND gates is I_0 ° I_0 ° I_1 ° I_1 ° I_{15} ° I_{15} (where I_n or I_n is defined to be an input term). Programming the fuse located by the selection of an input line, 'i_n" and the mth AND gate replaces the input term I_n with "1" in the logic expression for the mth AND gate.

a. Connect pin 28 (V_{CC}) to 5.0 V.

b. Connect pin 14 (GND) to ground.

c. Connect pin 19 ($\overline{CE}$) to a TTL HIGH level.

d. Apply TTL levels to pins 10 through 13, 15, and 16 (F_7 through F_2) to address an on chip one of forty eight decoder to select the AND gate to be programmed (F_7 = LSB and F_2 = MSB).

e. Apply 12.0 V to all input pins (I_0 through I_{15}).

f. Apply the proper TTL level to an Ix input pin as follows (program one input at a time):

1. If the product term to be programmed contains the input term Ix (where x = 0 through 15), lower the Ix pin to a TTL HIGH level.
2. If the product term to be programmed contains the input term Ix, lower the $\overline{I}$ x to a TTL LOW level.
3. If the product term does not contain the input terms $\overline{I}$ x or Ix (i.e., Ix is a DON'T CARE input), perform steps f1, g, f2, and g.

g. Apply a 15 V programming pulse to pin 1 (FE) according to the programming specification table.

h. Repeat steps e through g for each input of the selected product term.

i. Repeat steps d through h for all other product terms to be programmed.

j. Program one input at a time.

k. All unused inputs of programmed product terms must be programmed as DON'T CARES.

l. Inputs of unused product lines are not required to be programmed.

m. Pin 18 (F_0) is in the read mode (open collector). Care must be taken so that this pin is either left open, grounded, or loaded such that the current flowing into the pin does not exceed 16 mA.

4.7.1.2 Verify "PRODUCT (AND)" matrix.

a. Connect pin 28 (V_{CC}) to 5.0 V.

b. Connect pin 14 (GND) to ground.

c. Connect pin 19 ($\overline{CE}$) to a TTL HIGH level.

d. Apply TTL levels to pins 10 through 13, 15, and 16 (F_7 through F_2) to address an on chip one of forty-eight decoder to select the AND gate to be verified (F_7 = LSB and F_2 = MSB).

e. Apply 10.8 V to all input pins (I_0 through I_{15}).

f. Test the state of the Ix input as follows:

1. Lower the Ix pin to a TTL HIGH level and sense the voltage on pin 18 (F_0).

2. Lower the Ix pin to a TTL LOW and sense the voltage on pin 18 (F_0).

g. The state of the Ix input is determined as follows:

	Ix = TTL HIGH	Ix = TTL LOW	Condition of Ix for selected product term.
Level at output F_0	H	H	Don't Care
	H	L	Ix IN P-term
	L	H	Ix IN P-term unprogrammed
	L	L	

NOTES:
1. F_0 in this mode functions as an open collector output, H = ≥ 2.0 V, L ≤ 0.8 V.
2. The table above is valid regardless of the polarity (active HIGH or active LOW) of F_0.
3. Pin 1 (FE) should be either floating or grounded.

4.7.2 Program summing matrix.

4.7.2.1 All 8 OR gates of the summing matrix are fuse linked to the outputs of the AND gates in the initial unprogrammed state. The initial logic expressions (sum of products) of the eight unprogrammed OR gates is P0 + P1 + P2 + º º º + P47 where Pm is the product term programmed into the mth AND gate. Programming the fuse located by the selection of the mth AND gate and the nth summing line replaces the product term Pm with '0' in the logic expression of the nth OR gate. The nth summing line is selected by the selection of the nth output buffer where n = 1 through 8.

a. Connect pin 28 (V_{CC}) to 5.0 V.

b. Connect pin 14 (GND) to ground.

c. Connect pin 19 ($\overline{CE}$) to a TTL HIGH level.

d. Apply TTL levels to pins 4 through 9 (I_5 through I_0) to address an on chip one of forty-eight decoder to select the AND gate to be programmed (I_0 = LSB and I_5 = MSB).

e. Apply a TTL HIGH level to pins 20 and 21 (I_{15} and I_{14}).

f. Connect the remaining input pins to 12.0 V.

g. Apply an 18 V programming pulse (see programming specification table) at the pin of the output to be programmed. Other output pins should be either left open or tied to a TTL HIGH level.

h. Progran one output pin at a time.

i. All unused product lines are not required to be programmed.

4.7.2.2 Verify summing matrix.

a. Connect pin 28 (V_{CC}) to 5.0 V.

b. Connect pin 14 (GND) to ground.

c. Connect pin 19 ($\overline{CE}$) to a TTL LOW level.

d. Apply TTL levels to pins 4 through 9 (I_5 through I_0) to address an on chip one of forty eight decoder to select the AND gate to be verified (I_0 = LSB and I_5 = MSB).

e. Apply a TTL HIGH level to pins 20 and 22 (I_{15} and I_{13}).

f. Connect the remaining input pins to 12.0 V.

g. Sense the voltage on the output pin to be verified. The programming of the selected product line to the output line can be determined as follows:

Output Reads	Fuse Link
L	Blown (inactive)
H	Unblown (active)

h. Repeat steps d through g with V_{CC} at 4.4 V (LOW V_{CC} read).

i. The condition of the fuse link can be determined from the table above regardless of the polarity (active HIGH or active LOW) of the output buffer being verified.

4.7.3 Program output polarity.

4.7.3.1 The initial unprogrammed state of all eight output buffers is active LOW or inverting. To program an output buffer into the active HIGH or non-inverting state, proceed as follows:

a. Connect pin 28 (V_{CC}) to 5.0 V.

b. Connect pin 14 (GND) to ground.

c. Connect pin 19 ($\overline{CE}$) to a TTL HIGH level.

d. Apply a TTL HIGH level to pins 4 through 9 (I_5 through I_0).

e. Apply a TTL HIGH level to pin 20 (I_{15}).

f. Connect the remaining input pins to 12.0 V.

g. Apply an 18 V programming pulse (see programming specifications table) to the pin of the output to be programmed. Other output pins should be either left open or tied to a TTL HIGH level.

h. Program one output at a time.

4.7.3.2 Verify output polarity.

a. Connect pin 28 (V_{CC}) to 5.0 V.

b. Connect pin 14 (GND) to ground.

c. Connect pin 19 ($\overline{CE}$) to a TTL LOW level.

d. Apply a TTL HIGH level to pins 4 through 9 (I_5 through I_0).

e. Apply a TTL HIGH level to pins 21 and 22 (I_{14} and I_{13}).

f. Connect the remaining input pins to 12.0 V.

g. Sense the voltage on the pin of the output buffer to be verified. The condition of the output can be determined as follows:

Output reads	Output state
H	Active LOW
L	Active HIGH

h. Repeat with V_{CC} at 4.4 V (LOW V_{CC} read).

4.7.4 Summary of pin voltage – circuit B. In addition to verifying the Product (AND) Matrix, Summing Matrix, and Output Polarity separately after programming, a complete logic verification (normal read) with V_{CC} at 5.0 V is recommended after a device has been fully programmed. Table VI summarizes the full programming and verifying procedures.

TABLE III. Group A inspection for device type 01.

Subgroup	Symbol	MIL-STD-883 method	Case X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit
			Test no.	FE	I7	I6	I5	I4	I3	I2	I1	I0	F7	F6	F5	F4	GND	F3	F2	F1	F0	CE	I15	I14	I13	I12	I11	I10	I9	I8	V_{CC}		Min	Max	
1 T_C=25°C	V_{IC}		1								-18mA	-18mA					GND														4.5V	I0		-1.2	V
			2														"														"	I1		"	"
			3							-18mA							"														"	I2		"	"
			4						-18mA								"														"	I3		"	"
			5					-18mA									"														"	I4		"	"
			6				-18mA										"														"	I5		"	"
			7			-18mA											"														"	I6		"	"
			8		-18mA												"														"	I7		"	"
			9														"													-18mA	"	I8		"	"
			10														"												-18mA		"	I9		"	"
			11														"											-18mA			"	I10		"	"
			12														"										-18mA				"	I11		"	"
			13														"									-18mA					"	I12		"	"
			14														"								-18mA						"	I13		"	"
			15														"							-18mA							"	I14		"	"
			16														"						-18mA								"	I15		"	"
			17														"					-18mA									"	$\overline{CE}$		"	"
	V_{OL}	3007	18		-/	4/	4/	4/	4/	4/	4/	4/					"						4/	4/	4/	4/	4/	4/	4/	4/	5.5V	F0		0.5	"
		"	19		"	"	"	"	"	"	"	"					"						"	"	"	"	"	"	"	"	"	F1		"	"
		"	20	4	"	"	"	"	"	"	"	"					"			-9.6mA	-9.6mA		"	"	"	"	"	"	"	"	"	F2		"	"
		"	21		"	"	"	"	"	"	"	"					"	-9.6mA	-9.6mA				"	"	"	"	"	"	"	"	"	F3		"	"
		"	22		"	"	"	"	"	"	"	"				-9.6mA	"						"	"	"	"	"	"	"	"	"	F4		"	"
		"	23		"	"	"	"	"	"	"	"			-9.6mA		"						"	"	"	"	"	"	"	"	"	F5		"	"
		"	24		"	"	"	"	"	"	"	"		-9.6mA			"						"	"	"	"	"	"	"	"	"	F6		"	"
		"	25		"	"	"	"	"	"	"	"	-9.6mA				"						"	"	"	"	"	"	"	"	"	F7		"	"
	I_{IL}	3009	26									0.45V					"														"	I0	-1	-250	µA
		"	27								0.45V						"														"	I1	"	"	"
		"	28							0.45V							"														"	I2	"	"	"
		"	29						0.45V								"														"	I3	"	"	"
		"	30					0.45V									"														"	I4	"	"	"
		"	31				0.45V										"														"	I5	"	"	"
		"	32			0.45V											"														"	I6	"	"	"
		"	33		0.45V												"														"	I7	"	"	"
		"	34														"													0.45V	"	I8	"	"	"
		"	35														"												0.45V		"	I9	"	"	"
		"	36														"											0.45V			"	I10	"	"	"
		"	37														"										0.45V				"	I11	"	"	"
		"	38														"									0.45V					"	I12	"	"	"
		"	39														"								0.45V						"	I13	"	"	"
		"	40														"							0.45V							"	I14	"	"	"
		"	41														"						0.45V								"	I15	"	"	"
		"	42														"					0.45V									"	$\overline{CE}$	"	"	"
	I_{IH}	3010	43									5.5V					"														"	I0			"
		"	44								5.5V						"														"	I1		"	"
		"	45							5.5V							"														"	I2	50	"	"
		"	46						5.5V								"														"	I3		"	"
		"	47					5.5V									"														"	I4		"	"
		"	48				5.5V										"														"	I5		"	"
		"	49			5.5V											"														"	I6		"	"
		"	50		5.5V												"														"	I7		"	"
		"	51														"													5.5V	"	I8		"	"
		"	52														"												5.5V		"	I9		"	"
		"	53														"											5.5V			"	I10		"	"
		"	54														"										5.5V				"	I11		"	"
		"	55														"									5.5V					"	I12		"	"
		"	56														"								5.5V						"	I13		"	"
		"	57														"							5.5V							"	I14		"	"
		"	58														"						5.5V								"	I15		"	"
		"	59														"					5.5V									"	$\overline{CE}$		"	"

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 – Continued.

Subgroup	Symbol	MIL-STD-883 method	Case X Test no.	1 FE	2 I7	3 I6	4 I5	5 I4	6 I3	7 I2	8 I1	9 I0	10 F7	11 F6	12 F5	13 F4	14 GND	15 F3	16 F2	17 F1	18 F0	19 CE	20 I15	21 I14	22 I13	23 I12	24 I11	25 I10	26 I9	27 I8	28 V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C=25°C	I_{CEX}		60														GND					4.5V									5.5V	F0			µA
			61														"					"									"	F1			"
			62														"					"									"	F2			"
			63														"	5.5V	5.5V	5.5V	5.5V	"									"	F3	100	"	"
			64														"					"									"	F4		"	"
			65												5.5V	5.5V	"					"									"	F5		"	"
			66											5.5V			"					"									"	F6		"	"
			67										5.5V				"					"									"	F7		"	"
	I_{CC}	3005	68		GND	GND	GND	GND	GND	GND	GND	GND					"					GND	GND	GND	GND	GND	GND	GND	GND	GND	"	V_{CC}		180	mA
2	Same tests and terminal conditions as in subgroup 1, except T_C = 125°C.																																		
3	Same tests and terminal conditions as in subgroup 1, except T_C = -55°C.																																		
7 T_C=25°C	Func-tional test		69		1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	GND	1/	1/	1/	1/	GND	1/	1/	1/	1/	1/	1/	1/	1/	1/	(8) Outputs	1	1/	
8	Same tests and terminal conditions as in subgroup 7, except T_C = -55°C.																																		
9 T_C=25°C	t_{PHL1}	3003 Fig. 4	70		2/	2/	2/	2/	2/	2/	2/	2/	3/	3/	3/	3/	GND	3/	3/	3/	3/	GND	2/	2/	2/	2/	2/	2/	2/	2/	2/	(8) Outputs	80		ns
	t_{PLH1}		71		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		80	"
	t_{PHL2}		72		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		50	"
	t_{PLH2}		73		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		50	"
10	Same tests, terminal conditions and limits as subgroup 9, except T_C = 125°C.																																		
11	Same tests, terminal conditions and limits as subgroup 9, except T_C = -55°C.																																		

1/ The functional tests shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II). The functional tests shall be accomplished as defined in Appendix A for unprogrammed devices.

2/ (Programmed device) The test will check all inputs, gates, and outputs that have been programmed. Propagation test for t_{PHL1}, t_{PLH1}, t_{PHL2}, t_{PLH2} is also measured. This test shall be performed with V_{CC} = 4.5 V, and V_{CC} = 5.5 V.

3/ The outputs are loaded per figure 4.

4/ For programmed devices, select an appropriate set of inputs to acquire the desired output state.

TABLE III. Group A inspection for device type 02.

Subgroup	Symbol	MIL-STD-883 method	Case X Test no.	1 FE	2 I7	3 I6	4 I5	5 I4	6 I3	7 I2	8 I1	9 I0	10 F7	11 F6	12 F5	13 F4	14 GND	15 F3	16 F2	17 F1	18 F0	19 CE	20 I15	21 I14	22 I13	23 I12	24 I11	25 I10	26 I9	27 I8	28 V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C=25°C	V_{IC}		1									-18mA					GND														4.5V	I0		-1.2	V
			2								-18mA						"														"	I1		"	"
			3							-18mA							"														"	I2		"	"
			4						-18mA								"														"	I3		"	"
			5					-18mA									"														"	I4		"	"
			6				-18mA										"														"	I5		"	"
			7			-18mA											"														"	I6		"	"
			8		-18mA												"														"	I7		"	"
			9														"													-18mA	"	I8		"	"
			10														"												-18mA		"	I9		"	"
			11														"											-18mA			"	I10		"	"
			12														"										-18mA				"	I11		"	"
			13														"									-18mA					"	I12		"	"
			14														"								-18mA						"	I13		"	"
			15														"							-18mA							"	I14		"	"
			16														"						-18mA								"	I15		"	"
			17														"					-18mA									"	$\overline{CE}$		"	"
	V_{OL}	3007	18	4	_/	4/	4/	4/	4/	4/	4/	4/					"				9.6mA		4/	4/	4/	4/	4/	4/	4/	4/	5.5V	F0		0.5	"
		"	19		"	"	"	"	"	"	"	"					"			9.6mA			"	"	"	"	"	"	"	"	"	F1		"	"
		"	20		"	"	"	"	"	"	"	"					"		9.6mA				"	"	"	"	"	"	"	"	"	F2		"	"
		"	21		"	"	"	"	"	"	"	"					"	9.6mA					"	"	"	"	"	"	"	"	"	F3		"	"
		"	22		"	"	"	"	"	"	"	"				9.6mA	"						"	"	"	"	"	"	"	"	"	F4		"	"
		"	23		"	"	"	"	"	"	"	"			9.6mA		"						"	"	"	"	"	"	"	"	"	F5		"	"
		"	24		"	"	"	"	"	"	"	"		9.6mA			"						"	"	"	"	"	"	"	"	"	F6		"	"
		"	25		"	"	"	"	"	"	"	"	9.6mA				"						"	"	"	"	"	"	"	"	"	F7		"	"
	V_{OH}	3006	26	"		"	"	"	"	"	"	"					"				-2mA		"	"	"	"	"	"	"	"	4.5V	F0	2.4	"	"
		"	27		"	"	"	"	"	"	"	"					"			-2mA			"	"	"	"	"	"	"	"	"	F1	"	"	"
		"	28		"	"	"	"	"	"	"	"					"		-2mA				"	"	"	"	"	"	"	"	"	F2	"	"	"
		"	29		"	"	"	"	"	"	"	"					"	-2mA					"	"	"	"	"	"	"	"	"	F3	"	"	"
		"	30		"	"	"	"	"	"	"	"				-2mA	"						"	"	"	"	"	"	"	"	"	F4	"	"	"
		"	31		"	"	"	"	"	"	"	"			-2mA		"						"	"	"	"	"	"	"	"	"	F5	"	"	"
		"	32		"	"	"	"	"	"	"	"		-2mA			"						"	"	"	"	"	"	"	"	"	F6	"	"	"
		"	33		"	"	"	"	"	"	"	"	-2mA				"						"	"	"	"	"	"	"	"	"	F7	"	"	"
	I_{IL}	3009	34									0.45V					"														5.5V	I0	-1	-250	μA
		"	35								0.45V						"														"	I1	"	"	"
		"	36							0.45V							"														"	I2	"	"	"
		"	37						0.45V								"														"	I3	"	"	"
		"	38					0.45V									"														"	I4	"	"	"
		"	39				0.45V										"														"	I5	"	"	"
		"	40			0.45V											"														"	I6	"	"	"
		"	41		0.45V												"														"	I7	"	"	"
		"	42														"													0.45V	"	I8	"	"	"
		"	43														"												0.45V		"	I9	"	"	"
		"	44														"											0.45V			"	I10	"	"	"
		"	45														"										0.45V				"	I11	"	"	"
		"	46														"									0.45V					"	I12	"	"	"
		"	47														"								0.45V						"	I13	"	"	"
		"	48														"							0.45V							"	I14	"	"	"
		"	49														"						0.45V								"	I15	"	"	"
		"	50														"					0.45V									"	$\overline{CE}$	"	"	"

See footnotes at end of table.

TABLE III. Group A inspection for device type 02.

Subgroup	Symbol	MIL-STD-883 method	Case X Test no.	1 FE	2 I7	3 I6	4 I5	5 I4	6 I3	7 I2	8 I1	9 I0	10 F7	11 F6	12 F5	13 F4	14 GND	15 F3	16 F2	17 F1	18 F0	19 CE	20 I15	21 I14	22 I13	23 I12	24 I11	25 I10	26 I9	27 I8	28 V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C=25°C	I_{IH}	3010	51								5.5V	5.5V					GND														5.5V	I0		50	µA
		"	52						5.5V	5.5V							"														"	I1		"	"
		"	53					5.5V									"														"	I2		"	"
		"	54				5.5V										"														"	I3		"	"
		"	55			5.5V											"														"	I4		"	"
		"	56		5.5V												"														"	I5		"	"
		"	57														"														"	I6		"	"
		"	58														"														"	I7		"	"
		"	59														"												5.5V		"	I8		"	"
		"	60														"											5.5V			"	I9		"	"
		"	61														"										5.5V				"	I10		"	"
		"	62														"									5.5V					"	I11		"	"
		"	63														"								5.5V						"	I12		"	"
		"	64														"							5.5V							"	I13		"	"
		"	65														"						5.5V								"	I14		"	"
		"	66														"														"	I15		"	"
		"	67														"					5.5V									"	$\overline{CE}$		"	"
	I_{OZH}		68	4/	4/	4/	4/	4/	4/	4/	4/	4/					"				5.5V	GND	4/	4/	4/	4/	4/	4/	4/	"	F0	100		"
			69	"	"	"	"	"	"	"	"	"					"					"	"	"	"	"	"	"	"	"	"	F1		"	"
			70	"	"	"	"	"	"	"	"	"					"		5.5V			"	"	"	"	"	"	"	"	"	"	F2		"	"
			71	"	"	"	"	"	"	"	"	"					"	5.5V		5.5V		"	"	"	"	"	"	"	"	"	"	F3		"	"
			72	"	"	"	"	"	"	"	"	"			5.5V		"					"	"	"	"	"	"	"	"	"	"	F4		"	"
			73	"	"	"	"	"	"	"	"	"				5.5V	"					"	"	"	"	"	"	"	"	"	"	F5		"	"
			74	"	"	"	"	"	"	"	"	"		5.5V			"					"	"	"	"	"	"	"	"	"	"	F6		"	"
			75	"	"	"	"	"	"	"	"	"	5.5V				"					"	"	"	"	"	"	"	"	"	"	F7		"	"
	I_{OLZ}		76	"	"	"	"	"	"	"	"	"					"				0.45V	"	"	"	"	"	"	"	"	"	"	F0		-60	"
			77	"	"	"	"	"	"	"	"	"					"					"	"	"	"	"	"	"	"	"	"	F1		"	"
			78	"	"	"	"	"	"	"	"	"					"		0.45V			"	"	"	"	"	"	"	"	"	"	F2		"	"
			79	"	"	"	"	"	"	"	"	"					"	0.45V		0.45V		"	"	"	"	"	"	"	"	"	"	F3		"	"
			80	"	"	"	"	"	"	"	"	"				0.45	"					"	"	"	"	"	"	"	"	"	"	F4		"	"
			81	"	"	"	"	"	"	"	"	"			0.45		"					"	"	"	"	"	"	"	"	"	"	F5		"	"
			82	"	"	"	"	"	"	"	"	"		0.45			"					"	"	"	"	"	"	"	"	"	"	F6		"	"
			83	"	"	"	"	"	"	"	"	"	0.45				"					"	"	"	"	"	"	"	"	"	"	F7		"	"
	I_{OS}	3011	84	"	"	"	"	"	"	"	"	"					"				GND	"	"	"	"	"	"	"	"	"	"	F0	-10	-85	mA
		"	85	"	"	"	"	"	"	"	"	"					"					"	"	"	"	"	"	"	"	"	"	F1	"	"	"
		"	86	"	"	"	"	"	"	"	"	"					"		GND			"	"	"	"	"	"	"	"	"	"	F2	"	"	"
		"	87	"	"	"	"	"	"	"	"	"				GND	"	GND		GND		"	"	"	"	"	"	"	"	"	"	F3	"	"	"
		"	88	"	"	"	"	"	"	"	"	"			GND		"					"	"	"	"	"	"	"	"	"	"	F4	"	"	"
		"	89	"	"	"	"	"	"	"	"	"		GND			"					"	"	"	"	"	"	"	"	"	"	F5	"	"	"
		"	90	"	"	"	"	"	"	"	"	"					"					"	"	"	"	"	"	"	"	"	"	F6	"	"	"
		"	91	"	"	"	"	"	"	"	"	"	GND				"					"	"	"	"	"	"	"	"	"	"	F7	"	"	"
	I_{CC}	3005	92		GND	GND	GND	GND	GND	GND	GND	GND					"					GND	GND	GND	GND	GND	GND	GND	GND	GND	"	V_{CC}		180	mA
2	Same tests and terminal conditions as in subgroup 1, except T_C = 125°C.																																		
3	Same tests and terminal conditions as in subgroup 1, except T_C = -55°C.																																		
7 T_C=25°C	Func-tional test	1/	93		1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	GND	1/	1/	1/	1/	GND	1/	1/	1/	1/	1/	1/	1/	1/	1/	(8) Outputs			
8	Same tests and terminal conditions as in subgroup 7, except T_C = 125°C and T_C = -55°C.																																		
9 T_C=25°C	t_{PHL1}	3003 Fig. 4	94		2/	2/	2/	2/	2/	2/	2/	2/	3/	3/	3/	3/	GND	3/	3/	3/	3/	GND	2/	2/	2/	2/	2/	2/	2/	2/	2/	(8) Outputs			ns
	t_{PLH1}	"	95		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	80	80	"
	t_{PHL2}	"	96		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		50	"
	t_{PLH2}	"	97		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		50	"
10	Same tests, terminal conditions and limits as subgroup 9, except T_C = 125°C.																																		
11	Same tests, terminal conditions and limits as subgroup 9, except T_C = -55°C.																																		

1/ The functional tests shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II). The functional tests shall be accomplished as defined in Appendix A for unprogrammed devices.

2/ (Programmed device) The test will check all inputs, gates, and outputs that have been programmed. Propagation test for t_{PHL1}, t_{PLH1}, $_{PHL2}$, t_{PLH2} is also measured. This test shall be performed with V_{CC} = 4.5 V, and V_{CC} = 5.5 V.

3/ The outputs are loaded per figure 4.

4/ For programmed devices, select an appropriate set of inputs to acquire the desired output state.

TABLE IV. Programming characteristics – Circuit A. 4/

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Type	Max	
V_{CCS} 1/ 2/	V_{CC} supply (program/verify "OR" verify output program)	I_{CCS} = 550 mA, min (Transient or steady state)	8.25	8.5	8.75	V
V_{CCL}	V_{CC} supply (Program output polarity)		0.	0.4	0.8	V
I_{CCS}	I_{CC} limit (Program "OR")	V_{CCS} = + 8.50 ± .25 V	550		1000.	mA
V_{OPH} 2/	Output voltage (Program output polarity)	I_{OPH} = 300 ± 25 mA	16.0	17.0	18.0	V
V_{OP1}	Output voltage (Idle)		0.	0.4	0.8	V
I_{OPH}	Output current limit (Program output polarity)	V_{OPH} = +17 ± 1.0 V	275	300	325	mA
V_{IH}	Input voltage (Logic "1")		2.4		5.5	V
V_{IL}	Input voltage (Logic "0")		0.	0.4	0.8	V
I_{IH}	Input current (Logic "1")	V_{IH} = +5.5 V			50	µA
I_{IL}	Input current (Logic "0")	V_{IL} = 0 V			-500	µA
V_{OHF}	Forced output (Logic "1")		2.4		5.5	V
V_{OLF}	Forced output (Logic "0")		0.	0.4	0.8	V
I_{OHF}	Output current (Logic "1")	V_{OHF} = +5.5 V			100	µA
I_{OLF}	Output current (Logic "0")	V_{OLF} = 0 V			-1	mA
V_{IX}	CE program enable level		9.5	10	10.5	V
I_{IX1}	Input variables current	V_{IX} = +10 V			2.5	mA
I_{IX2}	CE input current	V_{IX} = +10 V			5.0	mA
V_{FEH} 2/	FE supply (Program)	I_{FEH} = 300 ± 25 mA (Transient or steady state)	16.0	17.0	18.0	V
V_{FEL}	FE supply (Idle)		1.25	1.5	1.75	V
I_{FEH}	FE supply current limit	V_{FEH} = + 17 ± 1.0 V	275	300	325	mA
V_{CCP} 1/	V_{CC} supply (Program "AND")	I_{CCP} = 550 mA, min (Transient or steady state)	4.75	5.0	5.25	V
I_{CCP}	I_{CC} limit (Program "AND")	V_{CCP} = + 5.0 ± .25 V	550		1000	mA
V_{OPF}	Forced output (Program)		9.5	10	10.5	V
I_{OPF}	Output current (Program)				10	mA
T_R	Output pulse rise time		10		50	µs
t_P	CE programming pulse width		1		1.5	ms
t_D	Pulse sequence delay		10			µs
T_{PR}	Programming time			.6		ms
$\frac{T_{PR}}{T_{PR} + T_{PS}}$	Programming duty cycle				50	%
F_L	Fusing attempts per link				2	cycle
V_S 3/	Verify threshold		1.4	1.5	1.6	V

1/ Bypass V_{CC} to GND with a 0.01 µf capacitor to reduce voltage spikes.

2/ Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

3/ V_S is the sensing threshold of the FPLA output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

4/ These are specifications which a programming system must satisfy.

5/ T_C = 25 ° C.

TABLE V. Programming specifications - Circuit B.

Symbol	Characteristic	Recommended 1/				Comments
		Min	Value	Max	Units	
V_{IH}	TTL levels	2.4	5.0	5.0	V	Apply to appropriate address and output pins. Do not leave pins open.
V_{IL}		0	0	0.4	V	
$\overline{CE}$	Chip select	2.4	5.0	5.0	V	
V_{OP}	Programming voltage pulse	17.5	18.0	18.5	V	Apply to the appropriate output pin.
t_{PW}	Programming pulse width		0.18	50	ms	
	Duty cycle, programming pulse		20		%	Maximum duty cycle to maintain T_C < 85 °C
t_r	Programming pulse rise time	0.5	1.0	3.0	µs	
	Number of pulses required	1	4	8		
V_{CC}	Power supply voltage	4.9	5.0	5.1	V	
t_c	Case temperature		25	85	°C	
I_{VP}	Programming pulse current max (V_P pin)			200	mA	If pulse generator is used, set current limit to this max value.
I_{OP}	Programming pulse current max (any output pin)			100	mA	If pulse generator is used, set current limit to this max value.
V_{CC}	Low V_{CC} read		4.4	5.0	V	Programming read verify.
V_P	Programming voltage	14.5	15.0	15.5	V	Pin 1

1/ T_C = 25 °C.

TABLE VI. Summary of pin voltages – Circuit B.

	Read	Program product "AND" matrix	Verify product "AND" matrix	Program summing matrix	Verify summing matrix	Program output polarity	Verify output polarity
Pin 1 (FE)	***	18	***	***	***	***	***
Pin 2 (I_7)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 3 (I_6)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 4 (I_5)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 5 (I_4)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 6 (I_3)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 7 (I_2)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 8 (I_1)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 9 (I_0)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 10 (F_7)	Read	TTL	TTL	****	Read	****	Read
Pin 11 (F_6)	Read	TTL	TTL	****	Read	****	Read
Pin 12 (F_5)	Read	TTL	TTL	****	Read	****	Read
Pin 13 (F_4)	Read	TTL	TTL	****	Read	****	Read
Pin 14 (GND)	GND	GND	GND	GND	GND	GND	GND
Pin 15 (F_3)	Read	TTL	TTL	****	Read	****	Read
Pin 16 (F_2)	Read	TTL	TTL	****	Read	****	Read
Pin 17 (F_1)	Read	**	**	****	Read	****	Read
Pin 18 (F_0)	Read	Read	Read	****	Read	****	Read
Pin 19 ($\overline{CE}$)	TTL LOW	TTL HIGH	TTL HIGH	TTL HIGH	TTL LOW	TTL HIGH	TTL LOW
Pin 20 (I_{15})	TTL	12.0*	12.0*	TTL HIGH	TTL HIGH	TTL HIGH	12.0
Pin 21 (I_{14})	TTL	12.0*	12.0*	TTL HIGH	12.0	12.0	TTL HIGH
Pin 22 (I_{13})	TTL	12.0*	12.0*	12.0	TTL HIGH	12.0	TTL HIGH
Pin 23 (I_{12})	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 24 (I_{11})	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 25 (I_{10})	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 26 (I_9)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 27 (I_8)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 28 (V_{CC})	5.0	5.0	5.0	5.0	12.0	5.0	5.0

* For selection of input apply TTL HIGH or TTL LOW
** Left open or TTL HIGH.
*** Left open or grounded.
**** Left open, TTL HIGH, or programming pulse.
The program table is used for coding FPLAs.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but it is not mandatory)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.
b. PIN and compliance identifier, if applicable (see 1.2).
c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
d. Requirement for certificate of compliance, if applicable.
e. Requirements for notification of change of product or process to the acquiring activity in addition to notification to the qualifying activity, if applicable.
f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
g. Requirement for product assurance options.
h. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
i. Requirement for programming the device, including processing option.
j. Requirements for "JAN" marking.
k. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

GND ..... Electrical ground (common terminal)
V_{IN} ..... Voltage level at an input terminal.
V_{IC}.....Input clamp voltage.
I_{IN} ..... Current flowing into an input terminal.

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish A (see 3.4). Longer length leads and lead forming shall not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.8.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic industry type. Generic industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-35810 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Device type	Commercial type
01	Circuit A, Signetics Corp 82S101
01	Circuit B, Fairchild 93458
02	Circuit A, Signetics Corp 82S100
02	Circuit B, Fairchild 93459

6.8 Manufacturers' designations. Manufacturers' circuits included in this specification are designated as shown in table VII.

Table VII. Manufacturers' designations

Device type	Signetics Corp	Fairchild
	Circuits	
	A	B
01	X	X
02	X	X

6.9 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue, due to the extent of the changes.

GATE TEST PROGRAM AND FUNCTIONAL TESTS

A.1 SCOPE

A.1.1 This Appendix A covers the fuse test program to be used for unprogrammed devices, and defines the requirements for functional tests of unprogrammed devices. This Appendix is a mandatory part of this standard. The information contained herein is intended for compliance.

A.2 GATE TEST PROGRAM.

A.2.1 When required, as in paragraph 3.3.2.1, the device may be programmed as shown in table A-I. This program will allow for testing all of the available gates.

A.3 FUSE TESTS FOR DEVICE TYPES 01 AND 02.

A.3.1 Unprogrammed devices – Circuit A.

A.3.1.1 Output polarity fuse check.

Terminal conditions:
V_{CC} = 8.5 V
FE = 1.5 V
CE = GND
All inputs = 3.0 V

a. Sense all outputs for logic low, any high is a failure.

A.3.1.2 "AND" matrix fuse check.

Terminal condition:
V_{CC} = 4.5 V
FE = 1.5 V
CE = 10 V
All inputs = 10 V (except for input being checked)

a. Address all "P" terms with a binary count 0-47, put into F_0 to F_5 with F_0 = LSB and F_5 =MSB.
b. Sense output F_7 for each "P" term. F_7 should also be low and if it goes high, then it means a failure since a fuse is open. The input being checked should be set first to V_{IH} and then V_{IL}. F_7 should remain low in both cases.
c. Repeat b for all inputs, one at a time.
d. Repeat a and then b for all "P" terms and their inputs.

A.3.1.3 "OR" (Sum) matrix fuse check.

Terminal condition:
V_{CC} = 8.5 V
FE = 1.5 V
$I_6 – I_{15}$ = Open
$I_0 – I_{15}$ = Binary Count Input for address
$\overline{CE}$ = GND

a. Sense each output for logic high. Any low is a failure, indicating a fuse open.
b. Sense all output low when binary input count goes to 48. Any high is a failure.

A.3.2 Unprogrammed devices – Circuit B.

A.3.2.1 "AND" (Product) matrix input fuse check.

Terminal conditions: V_{CC} = 5.0 V
$\overline{CE}$ = TTL HIGH

a. Select the product term to be tested by applying a binary address of TTL levels to pins 10 through 13, 15, 16 (F_7 through F_2) (F_7 = LSB, F_2 =MSB).
b. Apply 12.0 V to all input pins (I_0 through I_{15}) except for input Ix being tested.
c. The state of the Ix input fuse will be checked if the truth table below holds. Vary input Ix while monitoring pin 18 (F_0).

Ix	F_0
L	L
H	L

If F_0 is HIGH, then fuse is open indicating a failure.
d. Repeat steps b and c for each input of the selected product term.
e. Repeat steps a through c for all other product items and input fuse tests.

A.3.2.2 "OR" (Sum) matrix fuse check.

Terminal conditions: V_{CC} = 5.0 V
$\overline{CE}$ = TTL LOW

a. Apply TTL levels to pins 4 through 9 (I_5 through I_0) to select the AND gate to be verified (I_0 = LSB and, I_5 = MSB).
b. Apply TTL HIGH level to pins 20 and 22 (I_{15} and I_{13}).
c. Connect the remaining input pins to 12.0 V.
d. Sense the voltage on the output pin to be verified. All unblown fuse links will indicate a high on the output pin.

A.3.2.3 Output polarity fuse check.

Terminal conditions: V_{CC} = 5.0 V
$\overline{CE}$ = TTL LOW

a. Apply TTL HIGH level to pins 4 through 9 (I_5 through I_0), 21 and 22 (I_{14} and I_{13}).
b. Connect remaining pins to 12.0 V.
c. Sense the voltage on the pins of the output buffer to be verified. All output levels should read TTL HIGH.

A.3.3 Programmed devices – Circuits A and B.

Program the device according to the program shown in table A-I.

TABLE A-I. Program tables for test device.

Program table entries						
Input variable			Output function		Output active level	
I_m	$\bar{I}_m$	Don't Care	Prod. Term Present in F_P	Prod. Term not Present in F_P	Active High	Active Low
H	L	— (dash)	A	● (period)	H	L
Note: Enter (—) for unused inputs of used P-terms			Notes: 1. Entries independent of output polarity. 2. Enter (A) for unused outputs of used P-terms.		Notes: 1. Polarity programmed once only. 2. Enter (H) for all unused outputs.	

TABLE A-I. Program tables for test device - Continued.

Product Term																
No.	Input variable															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	—	—	—	—	—	L	—	H	—	—	—	—	—	—	—	H
1	—	—	—	—	—	L	L	H	—	—	—	H	—	—	—	—
2	—	—	—	—	—	L	—	H	—	—	—	—	—	—	H	—
3	—	—	—	—	—	L	L	H	—	—	H	—	—	—	—	—
4	—	—	—	—	—	L	—	H	—	—	—	—	—	H	—	—
5	—	—	—	—	—	L	L	H	—	H	—	—	—	—	—	—
6	—	—	—	—	—	L	—	H	—	—	—	—	H	—	—	—
7	—	—	—	—	—	L	L	H	H	—	—	—	—	—	—	—
8	—	—	—	—	—	L	L	L	—	—	—	H	—	—	—	H
9	—	—	—	—	—	L	L	L	—	—	H	—	—	—	H	—
10	—	—	—	—	—	L	L	L	—	H	—	—	—	H	—	—
11	—	—	—	—	—	L	L	L	H	—	—	—	H	—	—	—
12	—	—	—	—	—	H	H	H	—	—	—	H	—	—	—	—
13	—	—	—	—	—	H	H	H	—	—	H	—	—	—	—	—
14	—	—	—	—	—	H	H	H	—	H	—	—	—	—	—	—
15	—	—	—	—	—	H	H	H	H	—	—	—	—	—	—	—
16	—	—	—	—	L	H	L	L	—	—	—	L	—	—	—	H
17	—	—	—	—	L	H	L	L	—	—	—	H	—	—	—	L
18	—	—	—	—	H	H	L	L	—	—	—	L	—	—	—	L
19	—	—	—	—	H	H	L	L	—	—	—	H	—	—	—	H
20	—	—	—	H	—	H	L	L	—	—	L	—	—	—	H	—
21	—	—	—	H	—	H	L	L	—	—	H	—	—	—	L	—
22	—	—	—	L	—	H	L	L	—	—	L	—	—	—	L	—
23	—	—	—	L	—	H	L	L	—	—	H	—	—	—	H	—
24	—	—	H	—	—	H	L	L	—	L	—	—	—	H	—	—
25	—	—	H	—	—	H	L	L	—	H	—	—	—	L	—	—
26	—	—	L	—	—	H	L	L	—	L	—	—	—	L	—	—
27	—	—	L	—	—	H	L	L	—	H	—	—	—	H	—	—
28	—	H	—	—	—	H	L	L	L	—	—	—	H	—	—	—
29	—	H	—	—	—	H	L	L	H	—	—	—	L	—	—	—
30	—	L	—	—	—	H	L	L	L	—	—	—	L	—	—	—
31	—	L	—	—	—	H	L	L	H	—	—	—	H	—	—	—
32	—	L	—	—	—	H	L	L		—	—	—	H	—	—	—
33	—	L	—	—	—	H	L	L	H	—	—	—	—	—	—	—
34	—	—	—	—	H	H	L	L	—	—	—	—	—	—	—	H
35	—	—	—	—	H	H	L	L	—	—		H	—	—	—	—
36	—	—	—	L	—	H	L	L	—	—		—	—	—	H	—
37	—	—	—	L	—	H	L	L	—	—	H	—	—	—	—	—
38	—	—	L	—	—	H	L	L	—	—	—	—	—	H	—	—
39	—	—	L	—	—	H	L	L	—	H	—	—	—	—	—	—
40	—	—	—	—	—	H	L	L	H	—	—	—	H	—	—	—
41	—	—	—	—	—	H	L	L	—	—	—	H	—	—	—	H
42	—	—	—	—	—	H	L	L	—	—	H	—	—	—	H	—
43	—	—	—	—	—	H	L	L	—	H		—	—	H	—	—
44	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
46	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
47	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L

TABLE A-I. Program tables for test device - Continued.

Active Level								
No.	L	L	L	L	H	H	H	H
	Output Function							
	7	6	5	4	3	2	1	0
0	●	●	●	A	●	●	●	A
1	●	●	●	A	●	●	●	A
2	●	●	A	●	●	●	A	●
3	●	●	A	●	●	●	A	●
4	●	A	●	●	●	A	●	●
5	●	A	●	●	●	A	●	●
6	A	●	●	●	A	●	●	●
7	A	●	●	●	A	●	●	●
8	●	●	●	A	●	●	●	A
9	●	●	A	●	●	●	A	●
10	●	A	●	●	●	A	●	●
11	A	●	●	●	A	●	●	●
12	●	●		A	●	●	●	A
13	●	●	A	●	●	●	A	—
14	●	A	●	●	●	A	●	●
15	A	●	●	●	A	—	●	●
16	●	●	●	A	●	●	●	A
17	●	●	●	●	●	●	●	A
18	●	●	●	●	●	●	●	A
19	●	●	●	●	●	●	●	A
20	●	●	●	●	●	●	A	●
21	●	●	●	●	●	●	A	●
22	●	●	●	●	●	●	A	●
23	●	●	●	●	●	●	A	●
24	●	●	●	●	●	A	●	●
25	●	●	●	●	●	A	●	●
26	●	●	●	●	●	A	●	●
27	●	●	●	●	●	A	●	●
28	●	●	●	●	A	●	●	●
29	●	●	●	●	A	●	●	●
30	●	●	●	●	A	●	●	●
31	●	●	●	●	A	●	●	●
32	●	●	●	A	●	●	●	●
33	●	●	●	A	●	●	●	●
34	●	●	A	●	●	●	●	●
35	●	●	A	●	●	●	●	●
36	●	A	●	●	●	●	●	●
37	●	A	●	●	●	●	●	●
38	A	●	●	●	●	●	●	●
39	A	●	●	●	●	●	●	●
40	●	●	●	A	●	●	●	●
41	●	●	A		●	●	●	●
42	●	A	●	●	●	●	●	●
43	A	●	●	●	●	●	●	●
44	A	A	A	A	A	A	A	A
45	A	A	A	A	A	A	A	A
46	A	A	A	A	A	A	A	A
47	A	A	A	A	A	A	A	A

Custodians:
Army – CR
Navy – EC
Air Force – 11
DLA – CC

Review activities:
Army – MI, SM
Navy – AS, CG, MC, SH, TD
Air Force – 03, 19, 99

Preparing activity:

DLA – CC

(Project 5962-2005-045)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil .