

QUALIFICATION
REQUIREMENTS
REMOVED

MIL-M-38510/473A(NASA)
30 September 1983
SUPERSEDING
MIL-M-38510/473(NASA)
17 November 1980

MILITARY SPECIFICATION
MICROCIRCUITS, DIGITAL, CMOS,
MONOLITHIC 8-BIT INPUT/OUTPUT PORT

INACTIVE FOR NEW DESIGN AFTER DATE OF THIS REVISION

This specification is approved for use by George C. Marshall Space Flight Center, National Aeronautics and Space Administration, and is available for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic silicon, silicon gate CMOS microcircuit. One product assurance class and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number.

1.2 Part number. The complete part number shall be as specified in MIL-M-38510, except that the "JAN" or "J" certification shall not be used.

1.2.1 Device type. The device type shall be as follows:

<u>Device type</u>	<u>Circuit</u>
01	8-bit input/output port

1.2.2 Case outline. The case outline shall be designated as follows:

<u>Outline letter</u>	<u>Case outline, MIL-M-38510, Appendix C</u>
J	D-3 (24-lead, 1/2" x 1-1/4"), dual-in-line package
K	F-6 (24-lead, 3/8" x 5/8"), flat-package

1.3 Absolute maximum ratings.

Storage-temperature range (T_{stg})	- - - - -	-65°C to +150°C
Operating temperature range (T_C)	- - - - -	-55°C to +125°C
Supply voltage range ($V_{DD} - V_{SS}$)	- - - - -	-0.5 to +13 V
Power dissipation per package (P_D):		
For $T_C = -55^\circ\text{C}$ to $+100^\circ\text{C}$	- - - - -	500 mW
For $T_C = +100^\circ\text{C}$ to $+125^\circ\text{C}$	- - - - -	Derate linearly at 12 mW/°C to 200 mW
Device dissipation per output transistor:		
For $T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$	- - - - -	100 mW
Input voltage range, all inputs	- - - - -	-0.5 to $V_{DD} + 0.5$ V
DC input current, any one input	- - - - -	+10 mA
Lead temperature (during soldering):		
At distance 1/16 + 1/32 inch (1.59 + 0.79 mm)		
from case for 10 s maximum	- - - - -	+265°C
Maximum junction temperature (T_J)	- - - - -	+150°C
Thermal resistance, junction to case (θ_{JC}):		
Case J	- - - - -	0.0833°C/mW
Case K	- - - - -	0.15°C/mW
Junction resistance, junction to case (T_J)	- - - - -	150°C

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to George C. Marshall Space Flight Center, ATTN: EG02, Marshall Space Flight Center, Alabama 35812, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions. (At $T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$.)

Supply voltage range ($V_{DD} - V_{SS}$)	- - - -	4.5 to 11 V dc
Input low (V_{IL}) voltage range	- - - -	0 to 1.5 V at $V_{DD} = 5$ V
		0 to 3 V at $V_{DD} = 10$ V
Input high (V_{IH}) voltage range	- - - -	3.5 V to 5 V at $V_{DD} = 5$ V
		7 V to 10 V at $V_{DD} = 10$ V
Case operating temperature range	- - - -	-55°C to $+125^\circ\text{C}$

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional and logic diagrams. The functional and logic diagrams shall be as specified on figures 2a and 2b.

3.2.3 Functional description. The functional description shall be as specified in the truth table and timing diagram on figure 3.

3.2.4 Case outline. The case outlines shall be as specified in MIL-M-38510 and 1.2.3 herein.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510.

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	Limits		Unit
			Min	Max	
Positive clamping input to V_{DD}	$V_{IC(POS)}$	$T_C = 25^\circ C$, $V_{DD} = 0$ V $V_{SS} = \text{Open}$, Output = Open, $I_I = 1$ mA		1.5	V
Negative clamping input to V_{SS}	$V_{IC(NEG)}$	$T_C = 25^\circ C$, $V_{DD} = \text{Open}$, $V_{SS} = 0$ V, Output = Open, $I_I = -1$ mA		-1.5	V
Quiescent supply current	I_{SS}	$V_{DD} = 13$ Vdc, any combination of inputs		20	μA
High level output voltage	V_{OH1}	$V_{DD} = 10$ Vdc, $I_{OH} \leq 1$ μA (see table III V_I)	9.95		V
Low level output voltage	V_{OL1}	$V_{DD} = 10$ Vdc, $I_{OL} \leq 1$ μA (see table III V_I)		0.05	V
Output high (source) current	I_{OH1}	$V_{DD} = 5$ V, $V_{OH1} = 4.6$ V	-1.5		mA
	I_{OH2}	$V_{DD} = 10$ V, $V_{OH2} = 9.5$ V	-3.0		
Output low (sink) current	I_{OL1}	$V_{DD} = 5$ V, $V_{OL1} = 0.4$ V	2.0		mA
	I_{OL2}	$V_{DD} = 10$ V, $V_{OL2} = 0.5$ V	4.0		
High impedance three-state output leakage current	I_Z	$V_{DD} = 13$ V (see table III for V_I)		± 1.0	μA
Input current, high	I_{IH}	$V_{DD} = 13$ V, $V_I = 13$ V		100	nA
Input current, low	I_{IL}	$V_{DD} = 13$ V, $V_I = 0$		-100	nA
Clear time (CLR to D0 0-7)	t_{CLR}	$V_{DD}=5$ V, mode: output port, $C_L=50$ pF		336	ns
		$V_{DD}=10$ V, mode: output port, $C_L=50$ pF		140	ns
Data output time (CLK to D0 0-7)	t_{OD}	$V_{DD}=5$ V, mode: output port, $C_L=50$ pF	55	395	ns
		$V_{DD}=10$ V, mode: output port, $C_L=50$ pF	23	156	ns
Service request output time, low to high or high to low level (CS or CLK to SR/SR)	t_{SR}	$V_{DD}=5$ V, mode: output port, $C_L=50$ pF	30	225	ns
		$V_{DD}=10$ V, mode: output port, $C_L=50$ pF	13	90	ns
Transition time, low to high level (D0 0-7 or SR/SR)	t_{TLH}	$V_{DD}=5$ V, mode: output port, $C_L=50$ pF		84	ns
		$V_{DD}=10$ V, mode: output port, $C_L=50$ pF		44	ns
Transition time, high to low level (D0 0-7 or SR/SR)	t_{THL}	$V_{DD}=5$ V, mode: output port, $C_L=50$ pF		76	ns
		$V_{DD}=10$ V, mode: output port, $C_L=50$ pF		40	ns
Data access time (CS1/CS1 and CS2 to D0 0-7)	t_{CA}	$V_{DD}=5$ V, mode: input port, $C_L=50$ pF	58	488	ns
		$V_{DD}=10$ V, mode: input port, $C_L=50$ pF	24	186	ns
Minimum data setup time <u>1/</u>	t_{DS}	$V_{DD}=5$ V, or 10 V, mode: output port	0		ns
Minimum data hold time <u>2/</u>	t_{DH}	$V_{DD}=5$ V, mode: output port		164	ns
		$V_{DD}=10$ V, mode: output port		76	ns
Minimum clock pulse width <u>2/</u>	t_{WS}	$V_{DD}=5$ V, mode: output port		170	ns
		$V_{DD}=10$ V, mode: output port		70	ns

1/ Worst case forcing condition for tests 206 and 267 in table III.

2/ Worst case forcing condition for tests 154-169, 206, 215-230, and 267 in table III.

4.6 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container. The "JAN" or "J" certification mark shall not be used.

4.7 Manufacturer eligibility. To be eligible to supply microcircuits to this specification, a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line, not necessarily the line producing the device type described herein.

4.8 Certification. Certification in accordance with MIL-M-38510 is not required for this device.

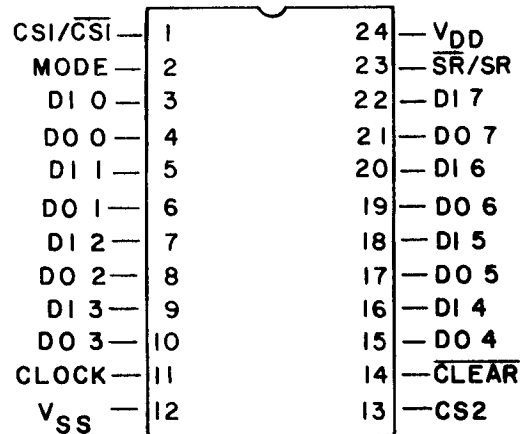
TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III) Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	1
Interim electrical parameters (after static burn-in I and static burn-in II) (method 5004)	N/A
Final electrical test parameters (method 5004)	1*,2,7*,8
Group A test requirements (method 5005)	1,2,7,8,9
Groups B electrical parameters (method 5005)	None
Group B V _{ZAp} (method 5005)	See 4.5.2
Groups C end-point electrical parameters (method 5005)	1,2,7,8
Additional electrical subgroups for group C periodic inspections	10
Group D end point electrical parameters (method 5005)	1,2,7,8

*PDA applies to subgroups 1 and 7 (see 4.2b).

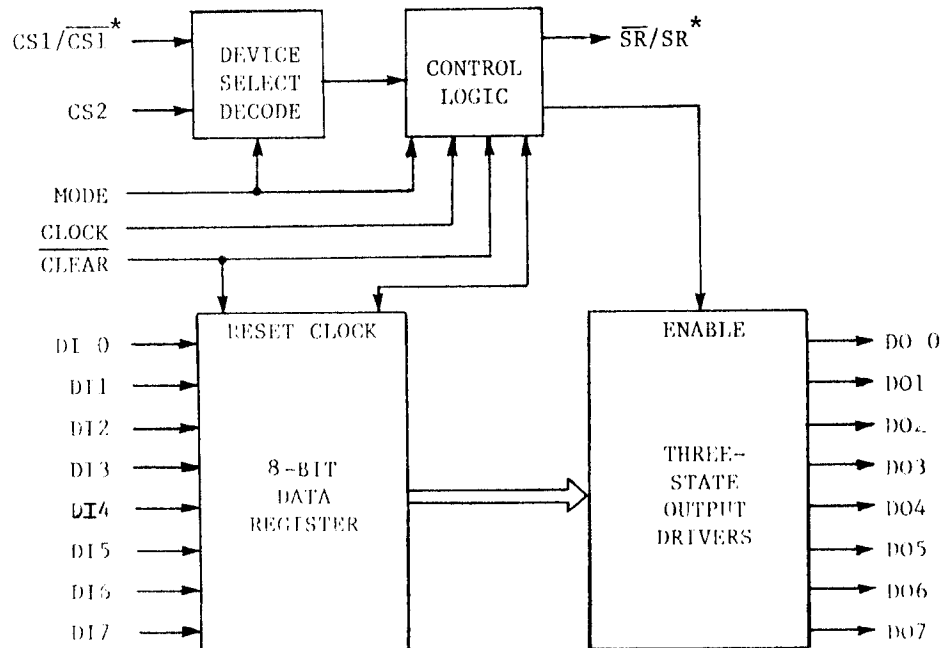
5. QUALITY ASSURANCE PROVISIONS

5.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, as applicable, except as modified herein.



CS1/ $\overline{\text{CS}}\overline{\text{T}}$:	Chip Select	DI 0 - DI 7:	Data In
CS2:	Chip Select	$\overline{\text{SR}}/\text{SR}$:	Service Request
DO 0 - DO 7:	Data Out	MODE:	Input port (0) Output port (1)

FIGURE 1. Terminal connections.



POLARITY DEPENDS ON MODE

FIGURE 2a. Functional diagram.

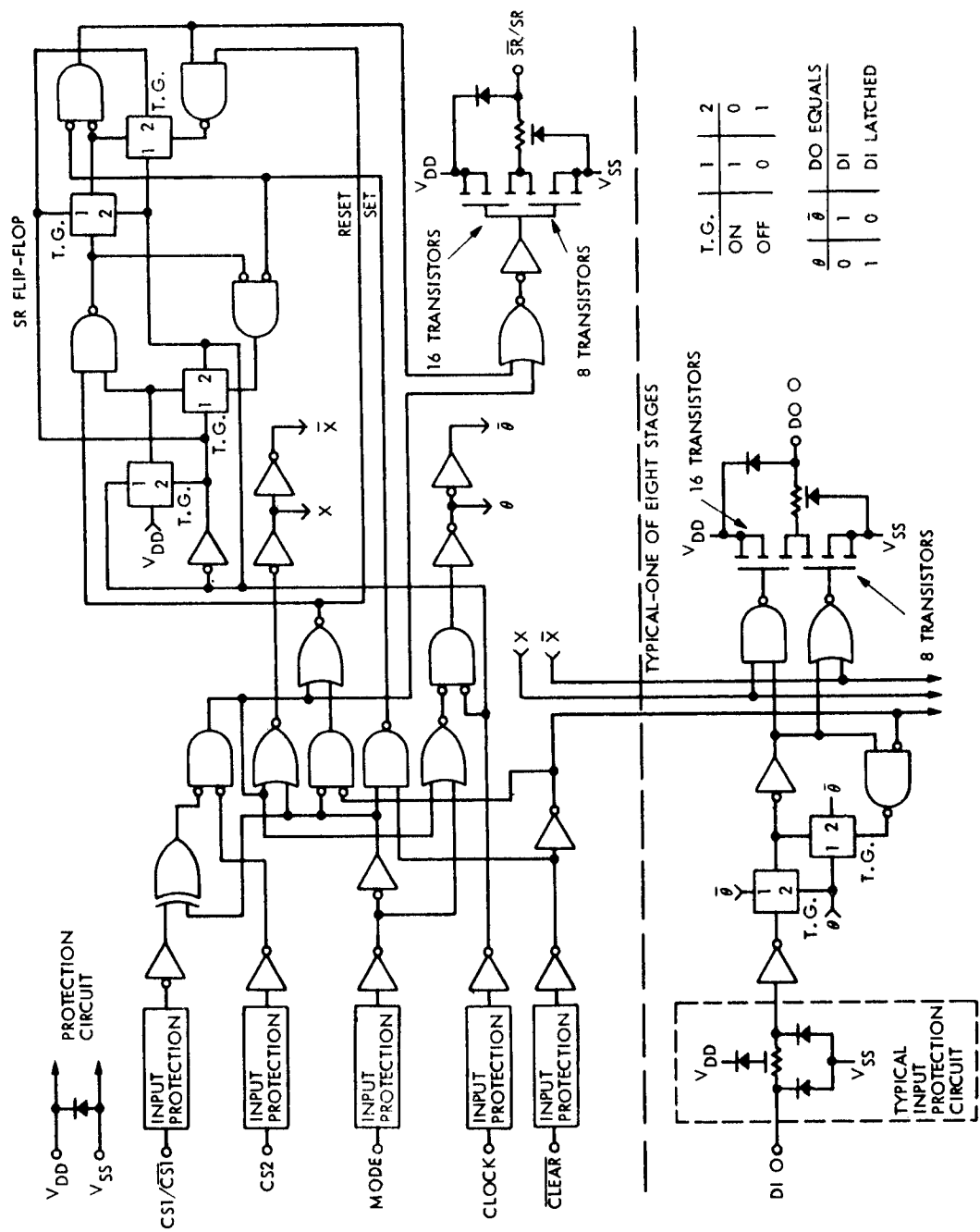


FIGURE 2b. Logic diagram.

MODE = 0

CLOCK	$\overline{CS1} \cdot CS2$	$\overline{CLEAR}$	Data outputs
X	0	X	High impedance
0	1	0	0
0	1	1	Data in latched
1	1	X	Data in

$\overline{SR} = 0$	$\overline{SR} = 1$
CLOCK 1 $\rightarrow$ 0 OR $\overline{CS1} \cdot CS2$ 0 $\rightarrow$ 1	$\overline{CS1} + CS2$ 1 $\rightarrow$ 0

a. Input port operation

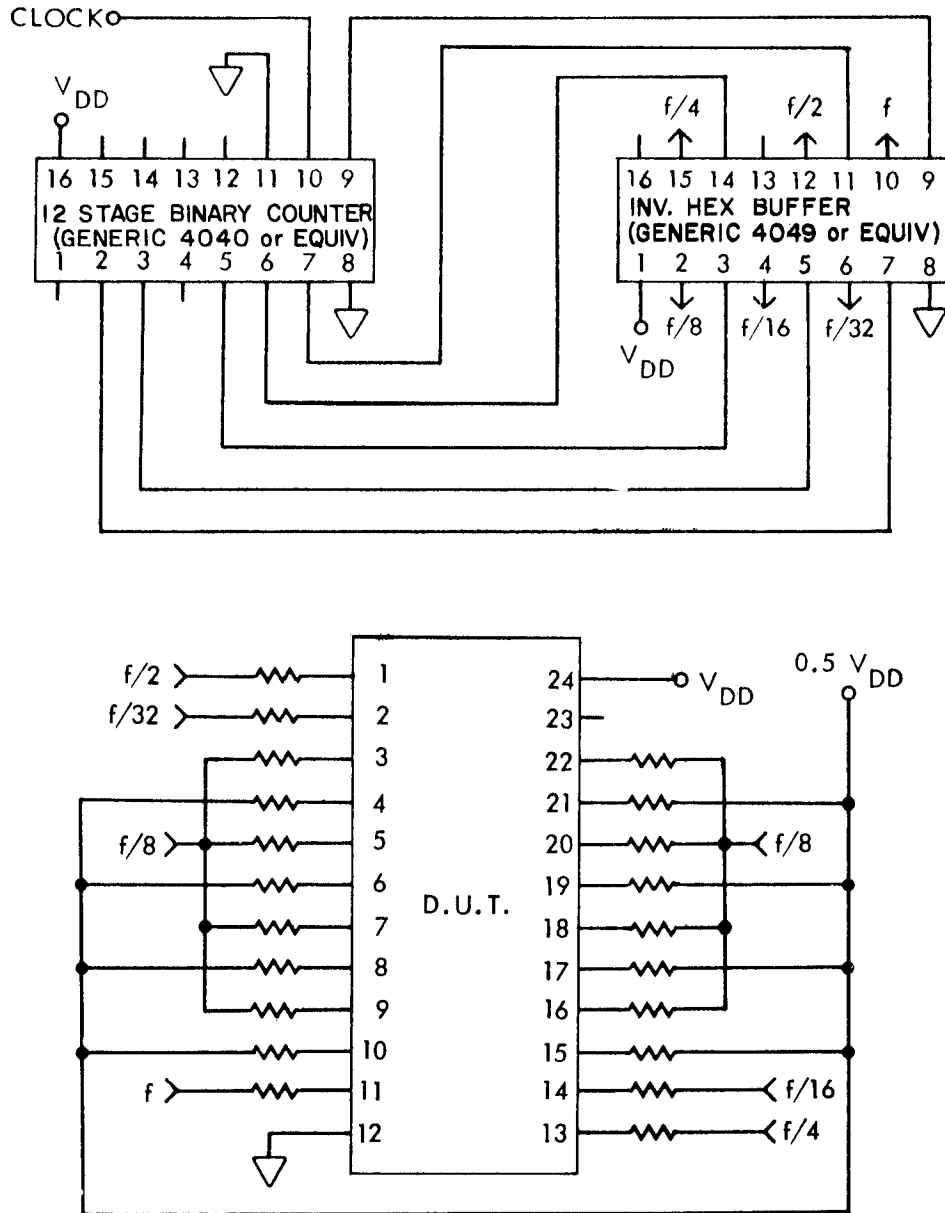
MODE = 1

CLOCK	$\overline{CS1} \cdot CS2$	$\overline{CLEAR}$	Data outputs
0	X	0	0
0	X	1	Data in latched
X	0	1	Data in latched
1	1	X	Data in

SR = 0	SR = 1
CLOCK 1 $\rightarrow$ 0 OR $\overline{CLEAR}$ 1 $\rightarrow$ 0	$\overline{CS1} \cdot CS2$ 1 $\rightarrow$ 0

b. Output port operation

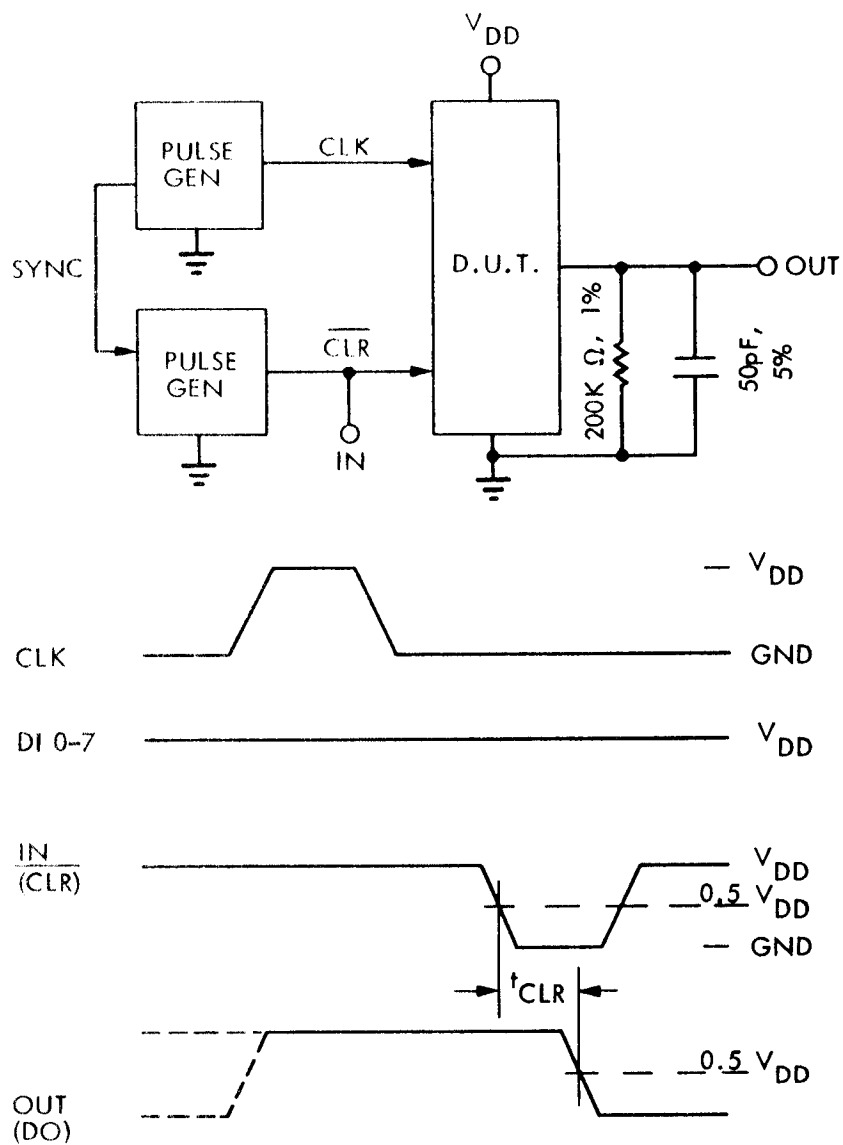
FIGURE 3. Truth tables.



NOTES:

1. All resistors shall be 0 to 47 k Ω .
2. Clock: 200 kHz square wave, amplitude = V_{DD} .
3. $V_{DD} = 13$ V.

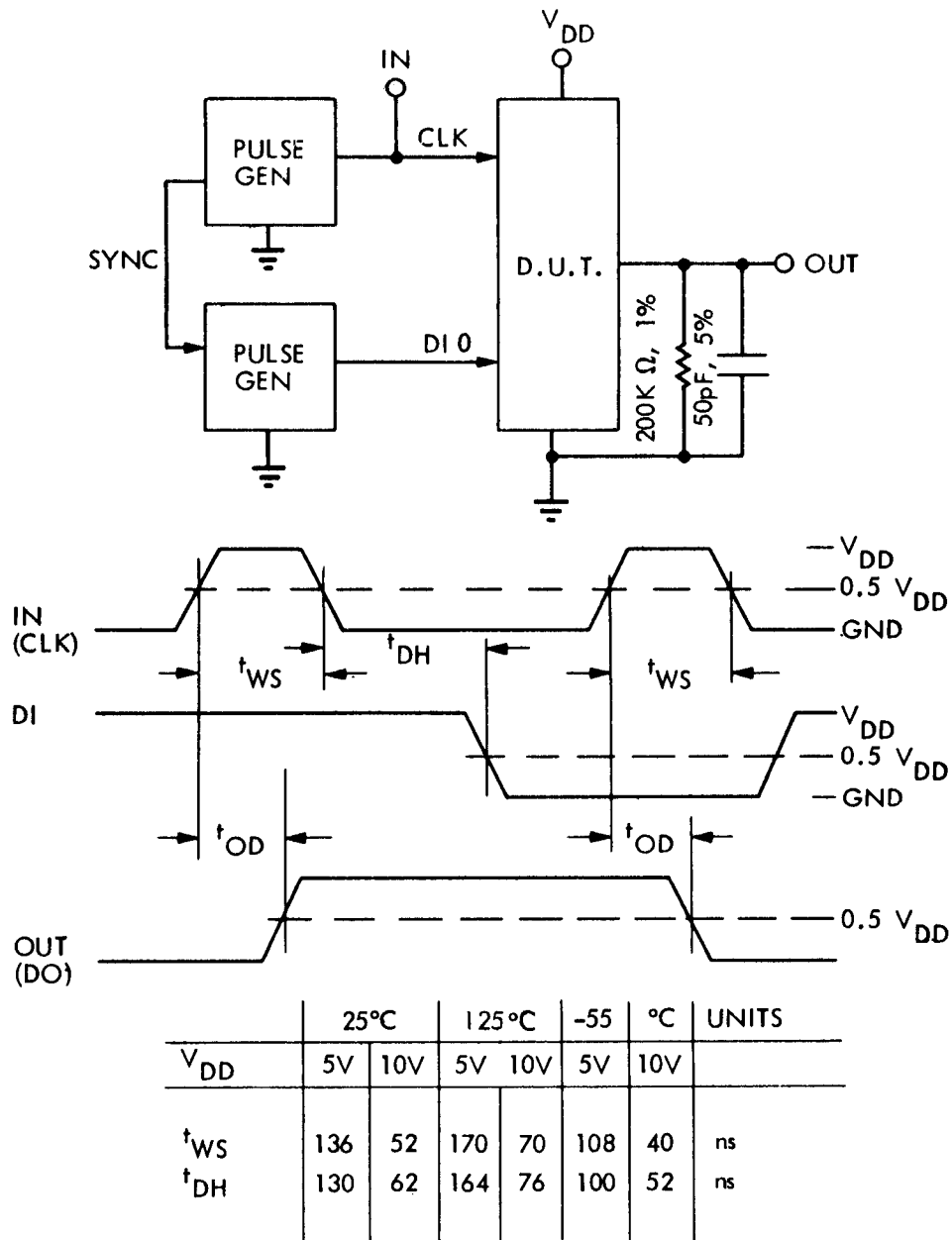
FIGURE 4. Dynamic burn-in and operating life test circuit.



NOTES:

1. Pulse generator outputs: Amplitude = V_{DD} , t_{TLH} and t_{THL} = 10 ± 2 ns.
2. See table III for complete terminal connections.
3. Load capacitance includes wiring and probe capacitance.

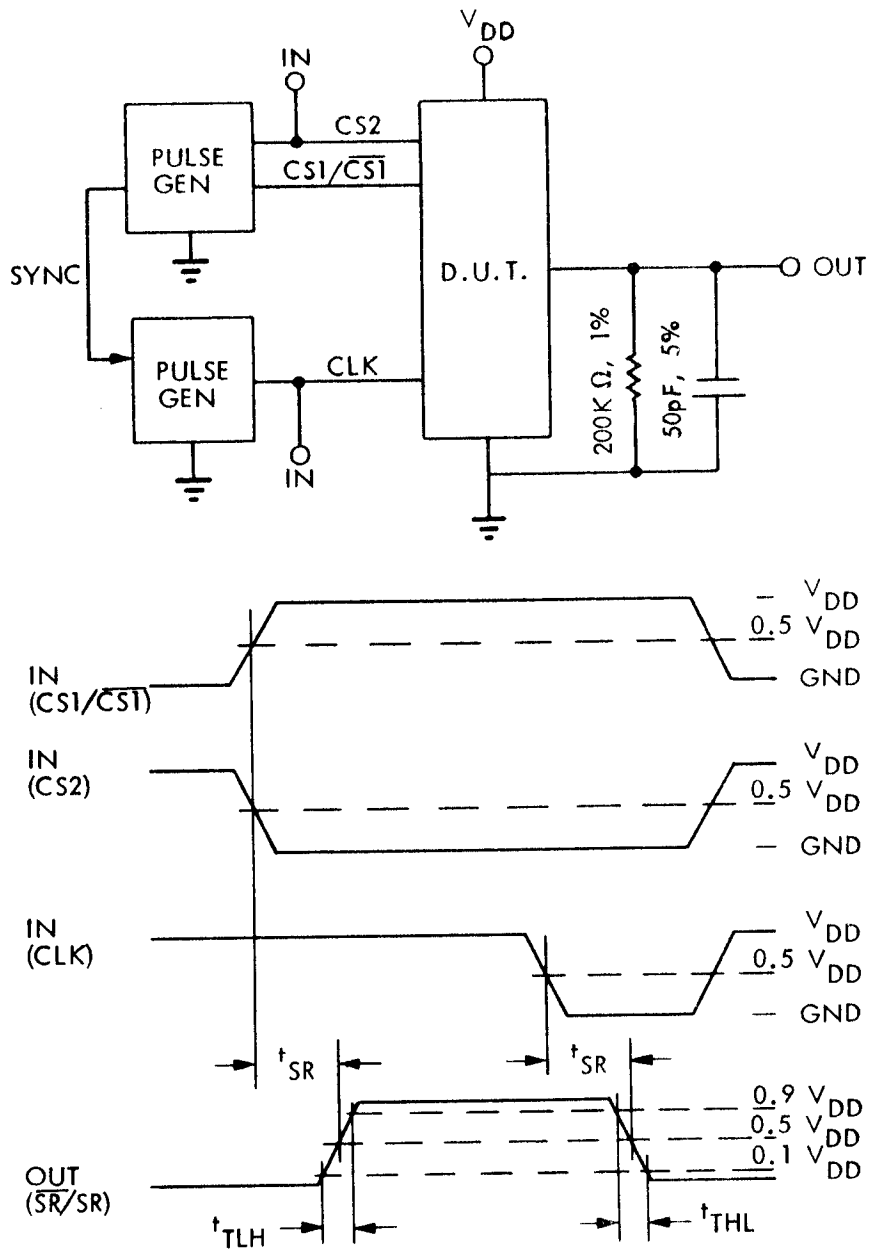
FIGURE 5a. Clear switching time test circuits and waveforms.



NOTES:

1. Pulse generator outputs: Amplitude = V_{DD} , t_{TLH} and $t_{THL} = 10 \pm 2$ ns.
2. See table III for complete terminal connections.
3. Load capacitance includes wiring and probe capacitance.

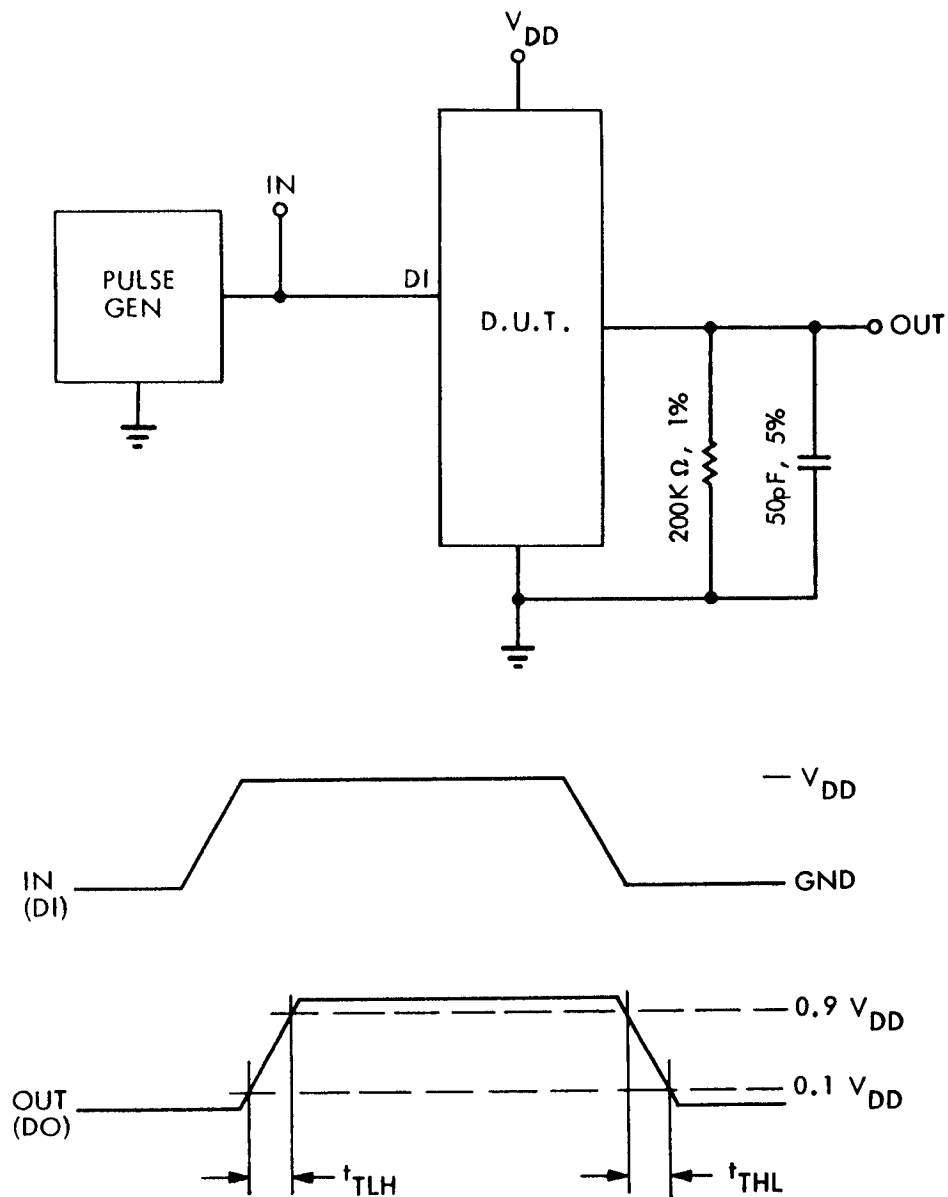
FIGURE 5b. Data output switching time test circuits and waveforms.



NOTES:

1. Pulse generator outputs: Amplitude = V_{DD} , t_{TLH} and t_{THL} = 10 ± 2 ns.
2. See table III for complete terminal connections.
3. Load capacitance includes wiring and probe capacitance.

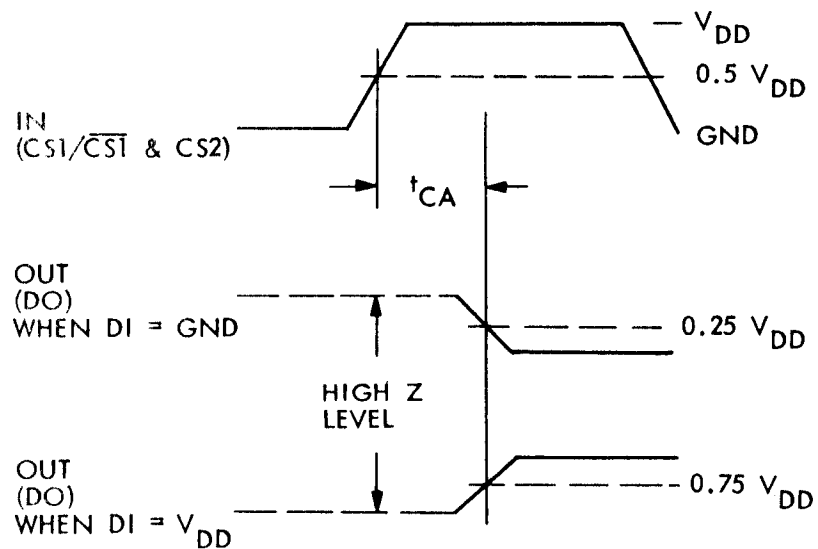
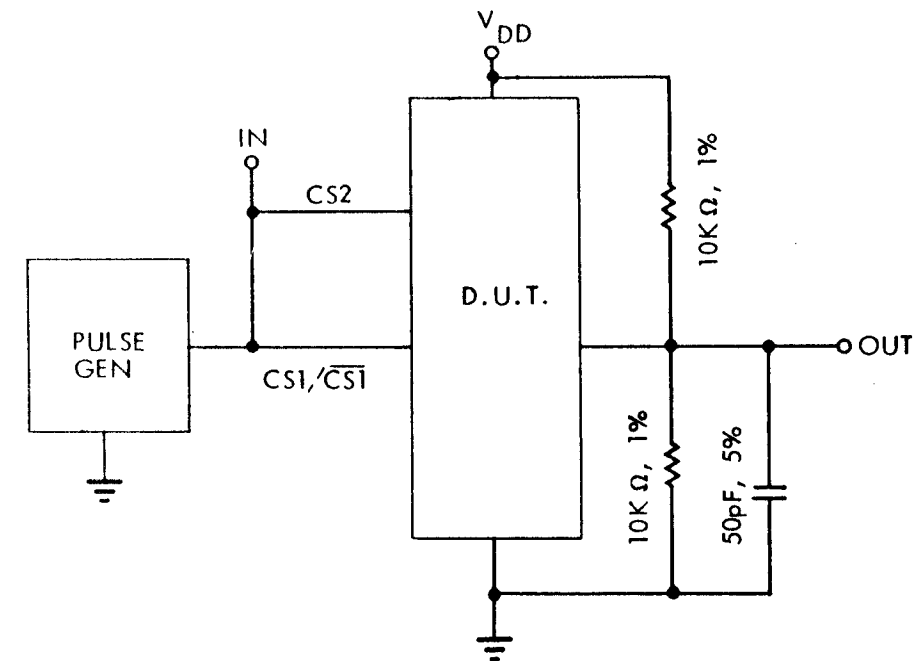
FIGURE 5c. Transition and service request switching times test circuit and waveforms.



NOTES:

1. Pulse generator outputs: Amplitude = V_{DD} , t_{TLH} and $t_{THL} = 10 \pm 2$ ns.
2. See table III for complete terminal connections.
3. Load capacitance includes wiring and probe capacitance.

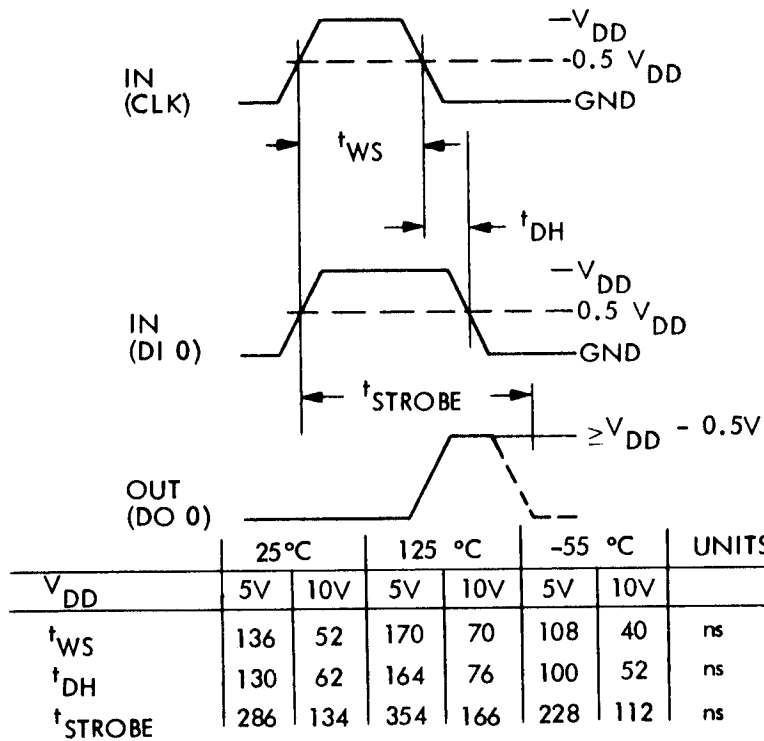
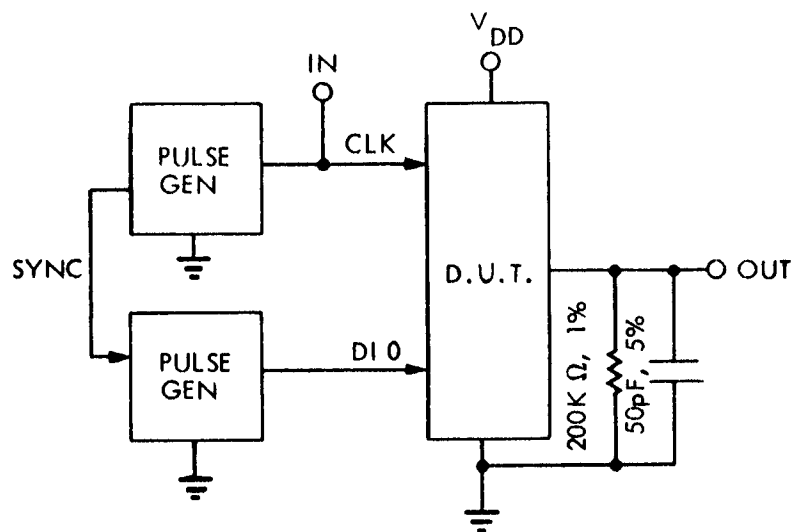
FIGURE 5d. Transition switching times test circuits and waveforms.



NOTES:

1. Pulse generator outputs: Amplitude = V_{DD} , t_{TLH} and t_{THL} = 10 ± 2 ns.
2. See table III for complete terminal connections.
3. Load capacitance includes wiring and probe capacitance.

FIGURE 5e. Data access switching times test circuit and waveforms.

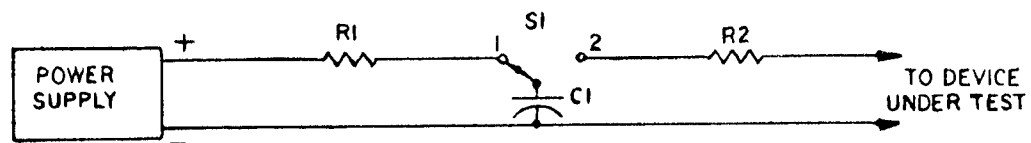


THE REQUIREMENTS OF THIS TEST SHALL BE MET IF THE OUTPUT IS $\geq V_{DD} - 0.5V$ AT THE STROBE TIME.

NOTES:

1. Pulse generator outputs: Amplitude = V_{DD} , t_{TLH} and t_{THL} = 10 ± 2 ns.
2. See table III for complete terminal connections.
3. Load capacitance includes wiring and probe capacitance.

FIGURE 5f. Worst case clock pulse width, data setup, and data hold times test circuit and waveforms.



$R1$ = appropriate current limiting resistance

$R2$ = 1.5 k Ω

$C1$ = 100 pF

V_{zap} = 400 V charge on $C1$.

$S1$ = Hg-wetted "bounceless" relay

FIGURE 6. High voltage (V_{ZAP}) test circuits.

TABLE III. Group A Inspection.

Symbol	MIL-STD-883 method	Cases V _A K	Terminal conditions and limits 2/																								Subgroup 1 T _C = 25 °C			Subgroup 2 T _C = 125 °C			Subgroup 3 T _C = -55 °C			Unit																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
			Test	Mode	CS1/CS2	DI 0	DI 3	DI 4	DI 5	DI 6	DI 7	CLK	CS 2	V _{SS}	CS 2	CLK	DI 0	DI 3	DI 4	DI 5	DI 6	DI 7	SR/SR	V _{DD}	Measured terminal	Min	Max	Min	Max	Min	Max																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
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See footnotes at end of table.

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TABLE III. Group A inspection - Continued.

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See footnotes at end of table.

TABLE III. Group A Inspection - Continued.

Symbol	MIL-STD-883C Method	Cases J, K	Terminal conditions and limits 17														Subgroup 2 T _C = 125 °C			Subgroup 3 T _C = -55 °C			Unit											
			Symbol	CS1/CS2	Mode	D0 0	D0 1	D0 1	D0 1	D0 2	D0 3	CLK	V _{SS}	CS 2	CLK	D0 4	D0 4	D0 5	D0 5	D0 6	D0 6	D0 7		D0 7	SR/SR	V _{DD}	Measured Terminal							
																							Test no.					1	2	3	4	5	6	7
ESD1	3003 Fig. 5b	ESD1	141	GND	V _{DD}	OUT	GND	GND	GND	GND	IN	GND	V _{DD}	V _{DD}	OUT	GND	GND	GND	GND	GND	GND	GND	GND	GND	5.0 V	CLK to CLK	70	315	90	395	55	245	ns	
			142	"	"	OUT	GND	OUT	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			143	"	"	"	V _{DD}	OUT	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			144	"	"	OUT	GND	OUT	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			145	"	"	"	"	"	V _{DD}	OUT	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			146	"	"	"	"	"	GND	OUT	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			147	"	"	"	"	"	"	"	V _{DD}	OUT	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			148	"	"	"	"	"	"	"	GND	OUT	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			149	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			150	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
ESD1	3004 Fig. 5c	ESD1	151	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"		
			152	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"		
			153	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			154	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			155	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			156	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
			157	IN	"	"	"	"	"	"	"	"	V _{DD}	"	IN	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
			158	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
			159	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
			160	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
ESD1	3004 Fig. 5d	ESD1	161	GND	V _{DD}	OUT	IN	OUT	IN	OUT	IN	OUT	V _{DD}	V _{DD}	OUT	GND	GND	GND	GND	GND	GND	GND	GND	5.0 V	CLK to CLK	70	315	90	395	55	245	ns		
			162	"	"	OUT	GND	OUT	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			163	"	"	"	V _{DD}	OUT	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			164	"	"	OUT	GND	OUT	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			165	"	"	"	"	"	V _{DD}	OUT	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			166	"	"	"	"	"	GND	OUT	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			167	IN	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			168	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
			169	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
			170	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
ESD1	3004 Fig. 5e	ESD1	171	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"		
			172	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			173	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"	
			174	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
			175	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
			176	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
			177	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
			178	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
			179	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"
			180	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CLK to CLK	"	"	"	"	"	"	"	"

See footnotes at end of table.

Terminal conditions and limits

See footnotes at end of table.

TABLE III. Group A inspection - Continued.

[illegible]

Terminals not designated shall be open.

Leakage currents (I_{CS} , I_{IP} , I_{IL} , and I_{PL} , subgroup 3, shall be performed using the test pattern and acceptance numbers per the LTPD specified in method 5005 of MIL-STD-883C.

a. I_{IP} measurements shall be made at time slots 11, 5, 9, 7, 9, 21, 40, 44, and 45.

Input levels shall be 0 Vdc.

Output levels shall be 0 Vdc, 1 Vpp. All outputs shall be open.

b. Perform the functional test using the test pattern and expected outputs shown in Table 1.

Input levels shall be 0 Vdc and 1 Vpp.

Output levels shall be 0 Vdc and 1 Vpp.

TABLE IV. Functional test pattern.

	Name	Pin #	Time Slot																							
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
I N P U T S	CS1/CS1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	CS2	13	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	MODE	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	CLOCK	11	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	CLEAR	14	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
I N P U T S	DI 0	3	1	1	1	1	0	0	0	1	1	0	1	0	0	1	0	1	0	1	1	0	1	0	1	1
	DI 1	5	1	1	1	1	1	1	0	0	1	0	1	0	1	0	1	0	1	1	0	1	1	0	1	1
	DI 2	7	1	1	1	1	0	0	0	1	1	0	1	0	1	0	1	1	0	1	1	0	1	1	1	0
	DI 3	9	1	1	1	1	1	1	0	0	1	0	1	1	0	1	1	0	1	1	0	1	1	1	1	1
	DI 4	16	1	1	1	1	0	0	0	1	1	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1
	DI 5	18	1	1	1	1	1	1	0	0	1	0	1	0	1	1	0	1	0	1	0	1	1	1	1	1
	DI 6	20	1	1	1	1	0	0	0	1	1	0	1	0	0	1	0	0	1	0	1	0	1	1	1	1
	DI 7	22	1	1	1	1	1	1	0	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	1	1
O U T P U T S	DO 0	4	Z	Z	Z	Z	0	0	0	0	1	0	1	0	0	1	0	1	0	1	1	0	1	0	1	1
	DO 1	6	Z	Z	Z	Z	0	1	1	1	0	1	0	1	0	1	0	1	0	1	1	0	1	1	0	1
	DO 2	8	Z	Z	Z	Z	0	0	0	0	1	0	1	0	1	0	1	1	0	1	1	0	1	1	1	0
	DO 3	10	Z	Z	Z	Z	0	1	1	1	0	1	0	1	1	0	1	1	0	1	1	0	1	1	1	1
	DO 4	15	Z	Z	Z	Z	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	1
	DO 5	17	Z	Z	Z	Z	0	1	1	1	0	1	0	1	1	0	1	0	1	0	1	0	1	1	1	1
	DO 6	19	Z	Z	Z	Z	0	0	0	0	1	0	1	0	0	1	0	0	1	0	1	0	1	1	1	1
	DO 7	21	Z	Z	Z	Z	0	1	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	1	1	1
	SR/SR	23	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: Z DENOTES HIGH IMPEDANCE STATE

				Time																																															
Name		Pin #	Slot	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48																								
I N P U T S	CS1/CS1	1		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	1																								
	CS2	13		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1																								
	MODE	2		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1																									
	CLOCK	11		1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0																									
	CLEAR	14		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1																									
	DI 0	3		1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1																								
	DI 1	5		1	1	1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1	1	1	1	1																								
	DI 2	7		1	1	1	1	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1	1	1	1	1																								
	DI 3	9		0	1	1	1	1	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1	1	1	1	1																								
	DI 4	16		1	0	1	1	1	0	0	0	0	1	0	0	0	0	1	1	0	0	0	1	1	1	1	1																								
DI 5	18		1	1	0	1	1	0	0	1	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1																									
DI 6	20		1	1	1	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1																									
DI 7	22		1	1	1	1	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1																									
O U T P U T S	DO 0	4		1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	Z	Z	Z	Z	0	0	0	0	0																							
	DO 1	6		1	1	1	1	1	0	0	0	0	0	0	0	1	0	1	1	Z	Z	Z	Z	0	0	0	0	0																							
	DO 2	8		1	1	1	1	1	0	0	0	0	0	0	1	0	0	1	1	Z	Z	Z	Z	0	0	0	0	0																							
	DO 3	10		0	1	1	1	1	0	0	0	0	0	1	0	0	0	1	1	Z	Z	Z	Z	0	0	0	0	0																							
	DO 4	15		1	0	1	1	1	0	0	0	0	1	0	0	0	0	1	1	Z	Z	Z	Z	0	0	0	0	0																							
	DO 5	17		1	1	0	1	1	0	0	1	0	0	0	0	0	0	1	1	Z	Z	Z	Z	0	0	0	0	0																							
	DO 6	19		1	1	1	0	1	0	1	0	0	0	0	0	0	0	1	1	Z	Z	Z	Z	0	0	0	0	0																							
	DO 7	21		1	1	1	1	0	1	0	0	0	0	0	0	0	0	1	1	Z	Z	Z	Z	0	0	0	0	0																							
	SR/SR	23		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0																							

		Time Slot														
		Pin #	49	50	51	52	53	54	55	56	57	58	59			
I N P U T S	CS1/ <u>CS1</u>	1		1	0	0	0	0	0	0	0	0	1			
	CS2	13		0	1	1	1	0	0	0	0	1	1			
	MODE	2		1	1	1	1	1	1	1	1	1	1			
	CLOCK	11		0	0	1	0	0	1	0	0	1	0			
	<u>CLEAR</u>	14		1	1	1	1	1	1	1	1	1	1			
I N P U T S	DI 0	3		1	1	1	1	1	1	1	1	1	0			
	DI 1	5		1	1	1	1	1	1	1	0	0	1			
	DI 2	7		1	1	1	1	1	1	1	1	1	0			
	DI 3	9		1	1	1	1	1	1	1	0	0	1			
	DI 4	16		1	1	1	1	1	1	1	1	1	0			
	DI 5	18		1	1	1	1	1	1	1	0	0	1			
	DI 6	20		1	1	1	1	1	1	1	1	1	0			
	DI 7	22		1	1	1	1	1	1	1	0	0	1			
O U T P U T S	DO 0	4		0	0	1	1	1	1	1	1	1	1			
	DO 1	6		0	0	1	1	1	1	1	1	0	0			
	DO 2	8		0	0	1	1	1	1	1	1	1	1			
	DO 3	10		0	0	1	1	1	1	1	1	0	0			
	DO 4	15		0	0	1	1	1	1	1	1	1	1			
	DO 5	17		0	0	1	1	1	1	1	1	0	0			
	DO 6	19		0	0	1	1	1	1	1	1	1	1			
	DO 7	21		0	0	1	1	1	1	1	1	0	0			
	<u>SR</u> /SR	23		0	0	0	0	1	1	0	0	0	1			

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following modifications and additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
 - (1) The burn-in test as described in 3.1.10 of method 5004 shall be performed as indicated. (3.1.11 and 3.1.12 are not required; 3.1.9 is required for class B devices.)
 - (2) For class B devices, the circuit shown on figure 4 shall be used.
- b. The percent defective allowable (PDA) is specified as 10 percent for class B devices based on failures from group A, subgroups 1 and 7 (after cooldown) of final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroups 1 and 7 after burn-in, divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot. The lot shall be accepted or rejected based on the PDA for the applicable device class.
- c. Interim and final electrical parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

4.3 Qualification inspection. Qualification inspection is not required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Generic test data (see 6.6) may be used to satisfy the requirements for groups C and D inspections. Quality conformance inspection shall be completed on the specific devices covered by this specification before they are shipped.

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in table II of method 5005 of MIL-STD-883 and as follows:

- a. A special subgroup shall be added to the group B inspection requirements for class B devices and shall consist of the test, conditions, and limits specified in 4.5.2. The LTPD for this subgroup shall be 15.

4.4.3 Group C inspection. Group C inspection shall consist of the test subgroups and LTPD values shown in table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = 125^\circ\text{C}$ minimum.
- c. Additional electrical subgroups as specified in table II shall be added to the group C inspection requirements for class B devices.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal unless otherwise specified. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 High voltage (V_{ZAP}) test of input protection circuits. Unless otherwise specified, all input terminals (up to a maximum of four) of the device under test (DUT) shall be subjected to a voltage pulse from a 100 pF source charged to 400 V (see figure 6). This destructive test shall be conducted in the following sequence:

a. Measure I_{IH} and I_{IL} at inputs selected, as stated above, at 25°C and $V_{DD} = 13$ V. Also measure I_{SS} at 25°C and $V_{DD} = 13$ V. These measurements shall be made in accordance with table III herein. The test limits for a single terminal measurement of I_{IH} and I_{IL} shall be 100 nA maximum.

b. With S_1 in position 1, charge C_1 to 400 V. With S_1 in position 2, apply the test voltage (V_{ZAP}) to the same terminal selected for leakage current measurements. Apply V_{ZAP} in a 3 pulse sequence as follows:

- (1) Input (-) to V_{DD} .
- (2) Input (+) to V_{SS} .
- (3) Input (+) to Output.

In each case, V_{ZAP} shall be applied by charging C_1 to 400 V with S_1 in position 1 and then switching to position 2.

c. Within 24 hours, repeat the I_{SS} measurement and the I_{IH} and the I_{IL} measurements on the same terminals as performed above. At this time a DUT exhibiting leakage currents in excess of the specified limits is defective.

4.6 Data reporting. When specified in the acquisition document, a copy of the following data, as applicable, shall be supplied:

- a. Attributes data for all screening tests (see 4.2) and variables data for all static burn-in, dynamic burn-in, and operating life tests (see 3.5).
- b. The quality conformance inspection data (see 4.4).
- c. Final electrical parameters data (see 4.2c).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. These devices require electrostatic protection.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.3 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot, to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirement for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to contracting activity, if applicable.
- e. Requirements for failure analysis (including required test condition of MIL-STD-883, method 5003), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	- - - - -	Ground. Zero voltage potential.
T _A	- - - - -	Free air temperature.
t _{CA} , t _{CLR} , t _{OD} , t _{SR}	- - - - -	Propagation delay times, input to output, see table I and figure 5.
t _{THL}	- - - - -	Fall time. Time duration during which the amplitude of the trailing edge of the input forcing condition or waveform is decreasing from 90 to 10 percent of the maximum amplitude.
t _{TLH}	- - - - -	Rise time. Time duration during which the amplitude of the leading edge of the input forcing condition or waveform is increasing from 10 to 90 percent of the maximum amplitude.
V _{DD}	- - - - -	Positive supply voltage.
V _{SS}	- - - - -	Negative supply voltage.
I _{SS}	- - - - -	Quiescent supply current.
I _Z	- - - - -	High impedance state leakage current at any output.

6.5 Logistic support. Lead materials and finishes (see 3.3), are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.6 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process and from the same plant as the die represented. Group D (see 4.4.4) generic data shall be on date codes no more than one year old and on the same package type (see terms, definitions, and symbols of MIL-M-38510) and from the same plant as the package represented. The vendor is required to retain the generic data for a period of not less than 36 months from the date of shipment.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device</u> <u>type</u>	<u>Generic-industry</u> <u>type</u>
01	1852

6.8 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

6.9 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodian:
NASA - NA

Preparing activity:
NASA - NA

Review activities:
DLA - ES

(Project 5962-K646-3)

Agent:
DLA - ES