

QUALIFICATION
REQUIREMENTS
REMOVED

MIL-M-38510/423A
9 August 1983
SUPERSEDING
MIL-M-38510/423(USAF)
8 February 1980

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, SCHOTTKY TTL,
SYSTEM CONTROLLER AND BUS DRIVER, MONOLITHIC SILICON

INACTIVE FOR NEW DESIGN AFTER
DATE OF THIS REVISION

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, Schottky TTL system controller/bus driver microcircuits. One product assurance class and a choice of case outline and lead finishes are provided for each type and are reflected in the complete part number.

1.2 Part number. The complete part number shall be as specified in MIL-M-38510. With the exception that the "JAN" or "J" certification mark shall not be used.

1.2.1 Device type. Device type shall be as shown in the following:

<u>Device type</u>	<u>Circuit</u>
01	System controller/bus driver

1.2.2 Device class. Device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Letter</u>	<u>Case outline, MIL-M-38510, appendix C</u>
Z	See figure 1 (28-lead, 5/8" x 1-1/2", dual-in-line pack)

1.3 Absolute maximum ratings.

DC output current, into outputs - - - -	50 mA
Supply voltage range (V_{CC}) - - - - -	-0.5 to 7.0 Vdc
Input voltage range - - - - -	-1.0 to 7.0 Vdc
Storage temperature range - - - - -	-65° to 150°C
Maximum power dissipation, P_D 1/ - - -	
Device type 01 - - - - -	1.2 Wdc
Lead temperature (soldering), 10 seconds - - - - -	300°C
Thermal resistance, junction to case - -	$\theta_{JC} = 30^\circ\text{C/W}$ for dual-in-line pack
Junction temperature - - - - -	$T_J = 175^\circ\text{C}$

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) - - - - -	4.5 Vdc, minimum to 5.5 Vdc, maximum
Minimum high level input voltage - - -	2.0 Vdc
Maximum low level input voltage - - -	0.8 Vdc

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RBE-2, Griffiss AFB, NY 13441, by using the self addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

Setup time,	
Processor bus to STSTB- - - - -	12 ns minimum
System bus to HLDA- - - - -	10 ns minimum
Hold time,	
Processor bus to STSTB- - - - -	5 ns minimum
System bus to HLDA- - - - -	20 ns minimum
Pulse width,	
STSTB - - - - -	25 ns minimum
Case operating temperature range (T _C) -	-55° to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connection. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outline. Case outline shall as specified in MIL-M-38510 and in 1.2.3 herein.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. Electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Manufacturer eligibility. To be eligible to supply microcircuits to this specification a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line. Not necessarily the line producing the device type described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	Limits		Unit
			Min	Max	
High-level output voltage, control outputs, DB ₀ -DB ₇	V _{OH1}	V _{CC} = 4.5 V; I _{OH} = -1 mA 1/	2.4		V
High-level output voltage, D ₀ -D ₇	V _{OH2}	V _{CC} = 4.5 V; I _{OH} = -10 μ A 1/	3.3		V
Low-level output voltage, control outputs, DB ₀ -DB ₇	V _{OL1}	V _{CC} = 4.5 V; I _{OL} = 10 mA 1/		0.5	V
Low-level output voltage, D ₀ -D ₇	V _{OL2}	V _{CC} = 4.5 V; I _{OL} = 2 mA 1/		0.5	V
Low-level input current, STSTB	I _{IL1}	V _{CC} = 5.5 V; V _{IN} = 0.4 V		-500	μ A
Low-level input current, D ₂ , D ₆	I _{IL2}	V _{CC} = 5.5 V; V _{IN} = 0.4 V		-750	μ A
Low-level input current, all other inputs	I _{IL3}	V _{CC} = 5.5 V; V _{IN} = 0.4 V		-250	μ A
High-level input current, DB ₀ -DB ₇	I _{IH1}	V _{CC} = 5.5 V; V _{IN} = 5.5 V		20	μ A
High-level input current, all other inputs	I _{IH2}	V _{CC} = 5.5 V; V _{IN} = 5.5 V		100	μ A
Output leakage current high, high impedance state, control outputs	I _{ZH}	V _{CC} = 5.5 V; V _{OUT} = 5.5 V		100	μ A
Output leakage current low, high impedance state, control outputs	I _{ZL}	V _{CC} = 5.5 V; V _{OUT} = 0.45 V		-100	μ A
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V; I _{IN} = -5 mA		-1.2	V
Output short circuit current	I _{OS}	V _{CC} = 5.5 V; V _{OUT} = GND	-15	-100	mA
Power supply current	I _{CC}	V _{CC} = 5.5 V; control inputs and D ₀ -D ₇ are GND		210	mA
High-level input current, INTA	I _{INT}	V _{CC} = 5.5 V; V _{IN} = 12.0 V; R _{IN} = 1 k Ω $\pm 10\%$		5	mA
Input capacitance, control inputs	C _{IN}	V _{CC} = 5.0 V; V _{BIAS} = 2.5 V; F = 1.0 MHz		12	pF
Output capacitance, control outputs	C _{OUT}			15	pF
Input/output capacitance, D ₀ -D ₇ , DB ₀ -DB ₇	C _{I/O}			15	pF

1/ V_{IL} = 0 V; V_{IH} = 4.5 V.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	Limits		Unit
			Min	Max	
Propagation delay, STSTB to control outputs	t _{PHL1}	See figure 5	20	75	ns
Propagation delay, DBIN to INTA, I/OR, MEMR	t _{PLH2}			35	ns
Propagation delay, HLDA to INTA, I/OR, MEMR	t _{PLH3}			28	ns
Propagation delay, WR to MEMW, I/OW	t _{PLH4}		5	60	ns
	t _{PHL4}		5	60	ns
Propagation delay, system bus (DB ₀ -DB ₇) to processor bus (D ₀ -D ₇)	t _{PLH5}			45	ns
	t _{PHL5}			45	ns
Processor delay, DBIN to processor bus: Into high impedance state	t _{PHZ1}			45	ns
	t _{PLZ1}			45	ns
Out of high impedance state	t _{PZH1}			45	ns
	t _{PZL1}			45	ns
Propagation delay, processor bus (D ₀ -D ₇) to system bus (DB ₀ -DB ₇)	t _{PLH6}	V _{CC} = 5.0 V	5	40	ns
	t _{PHL6}		5	40	ns
Propagation delay, STSTB to system bus from high impedance state	t _{PZH2}			36	ns
	t _{PZL2}			36	ns
Propagation delay, BUSEN to system bus: Into high impedance state	t _{PHZ3}			35	ns
	t _{PLZ3}			35	ns
Out of high impedance state	t _{PZH3}			35	ns
	t _{PZL3}			35	ns
Setup time, processor bus to STSTB	t _{SLH1}		12		ns
	t _{SHL1}				
Setup time, system bus to HLDA	t _{SLH2}		10		ns
	t _{SHL2}				
Hold time, processor bus to STSTB	t _{HLH1}		5		ns
	t _{HHL1}				
Hold time, system bus to HLDA	t _{HLH2}		20		ns
	t _{HHL2}				
Pulse width, STSTB	t _{WL}		25		ns

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see (see table III) Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7,9, 10,11
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11
Group C end point electrical parameters (method 5005)	N/A
Additional electrical subgroups for group C periodic inspections	N/A
Group D end point electrical parameters (method 5005)	1,2,3

*PDA applies to subgroup 1 (see 4.3c).

3.7 Certification. Certification in accordance with MIL-M-38510 is not required for this device.

3.8 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container. The "JAN" or "J" certification mark shall not be used.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection is not required.

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
 1. Test condition D or E, using the circuit shown on figure 5, or equivalent.
 2. $T_A = 125^\circ\text{C}$ minimum.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. The percent defective allowable for class B devices shall be 10 percent based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

MIL-M-38510/423A

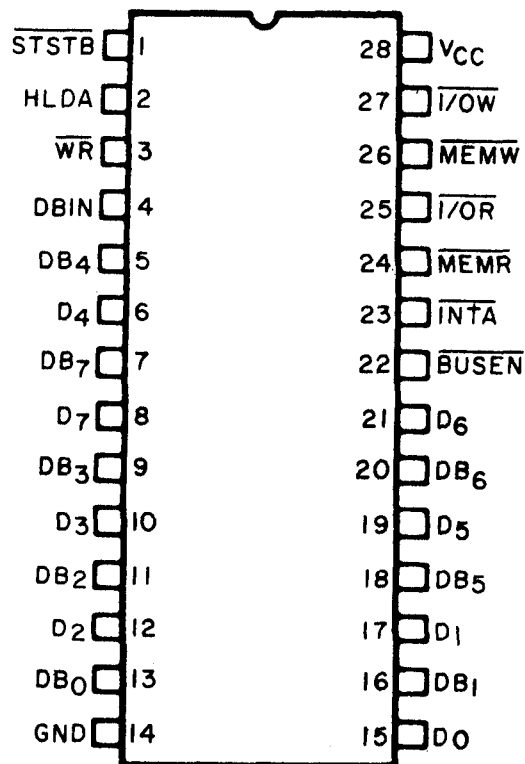
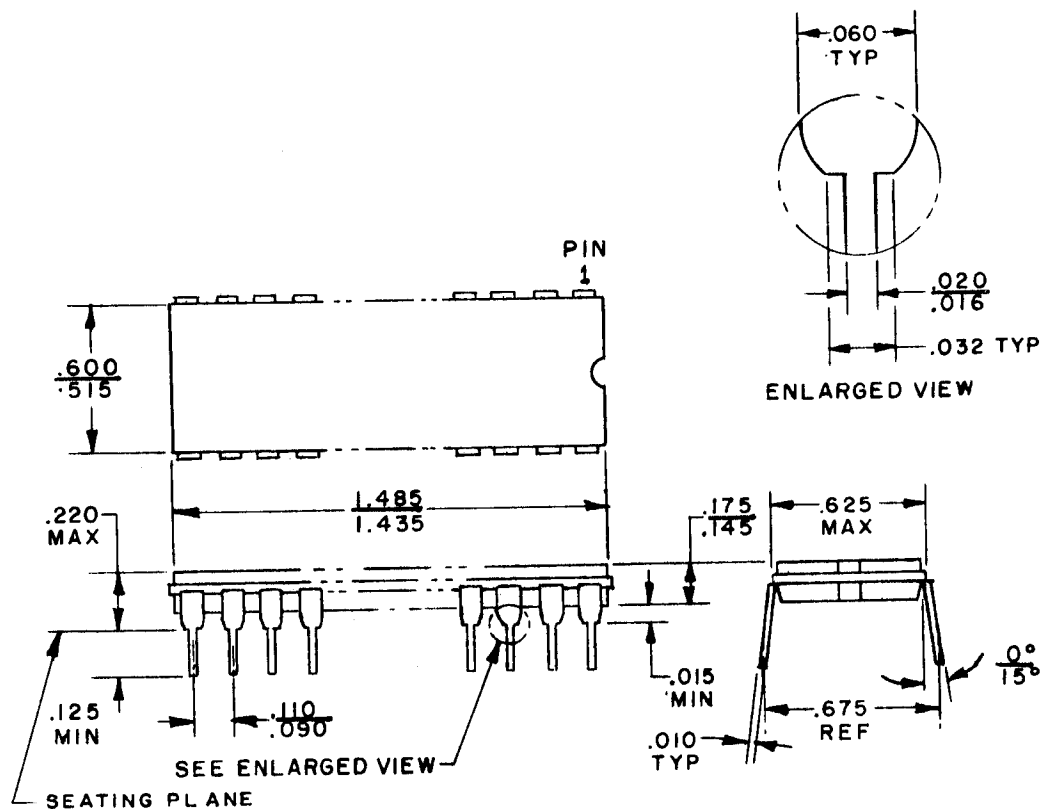


FIGURE 1. Case outline and terminal connections.



Case outline Z

INCHES	MM	INCHES	MM
.010	.25	.145	3.68
.015	.38	.175	4.44
.016	.41	.220	5.59
.020	.51	.515	13.08
.032	.81	.600	15.24
.060	1.52	.625	15.88
.090	2.29	.675	17.14
.110	2.79	1.435	36.45
.125	3.18	1.485	37.72

FIGURE 1. Case outline and terminal connections - Continued.

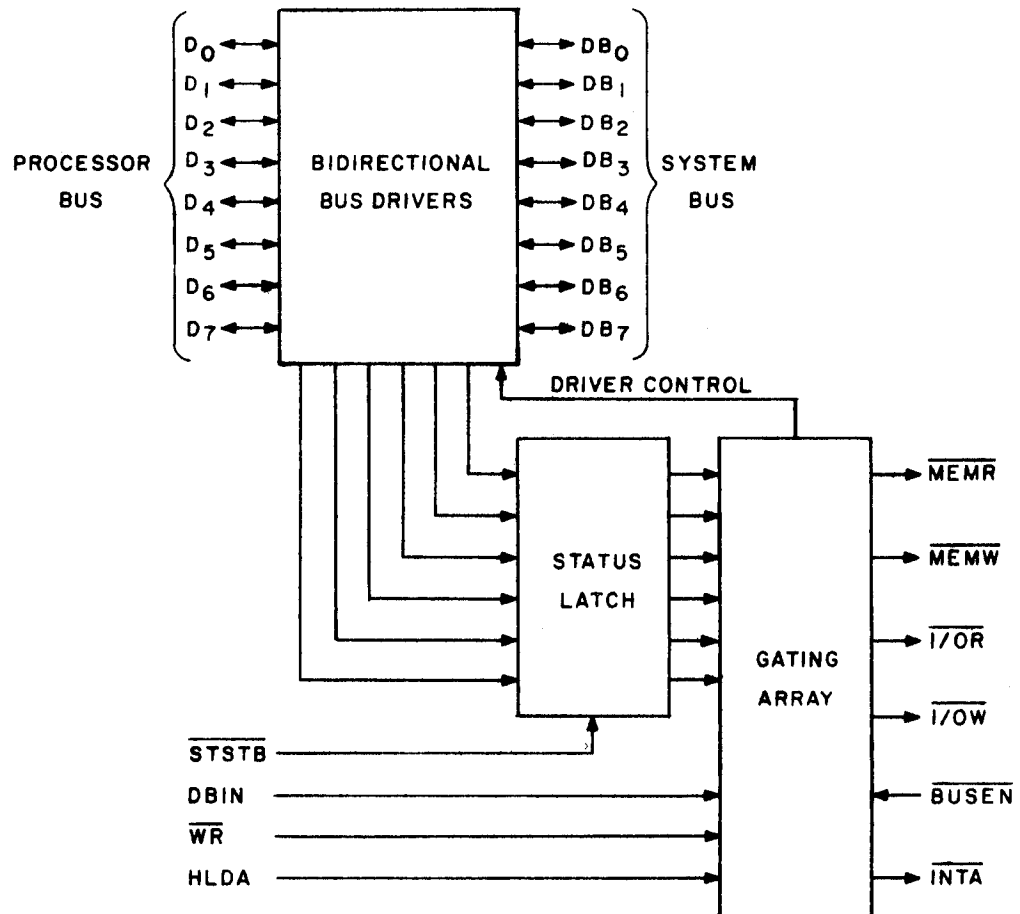


FIGURE 2. Block diagram and truth table.

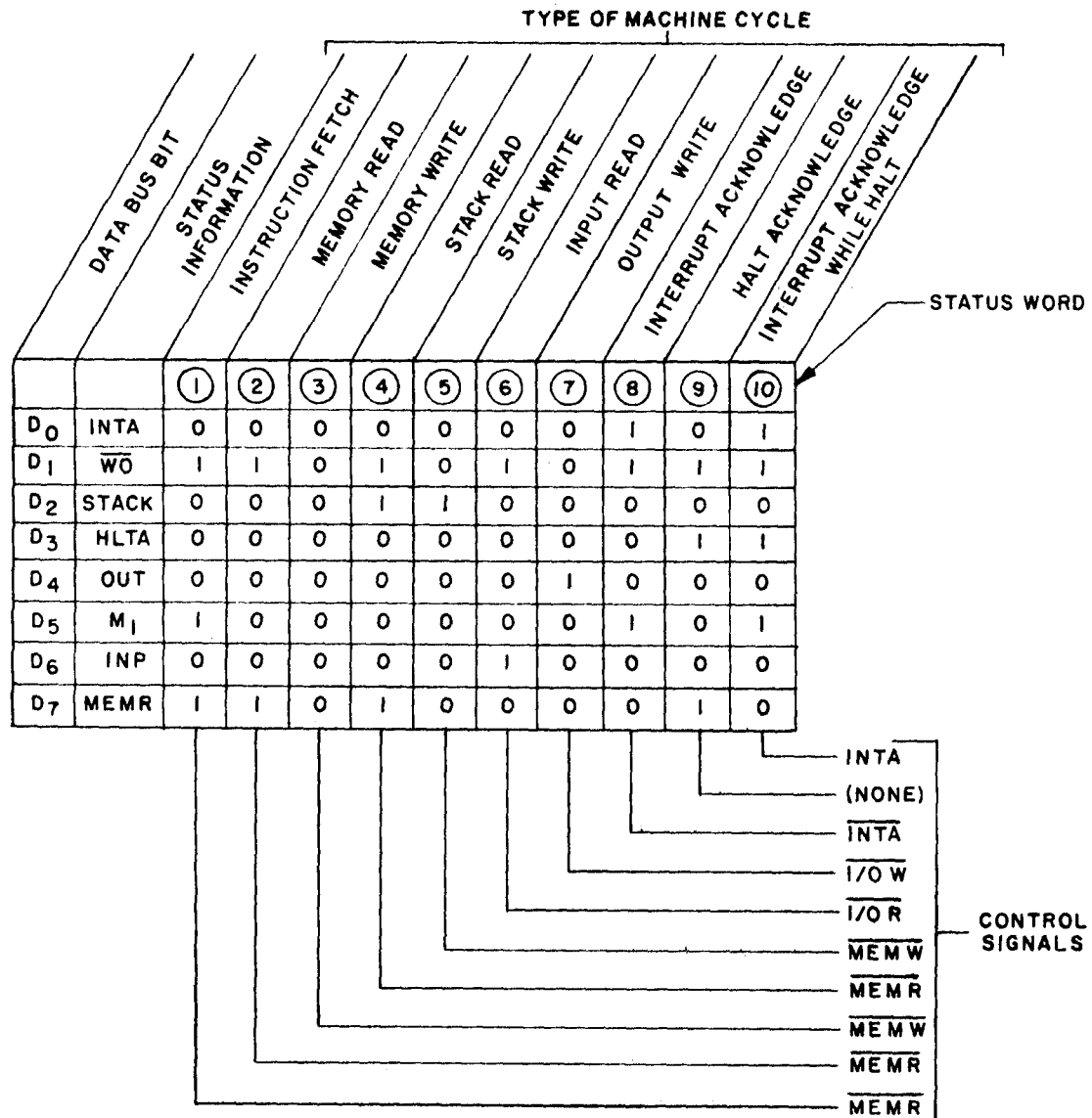


FIGURE 2. Block diagram and truth table - Continued.

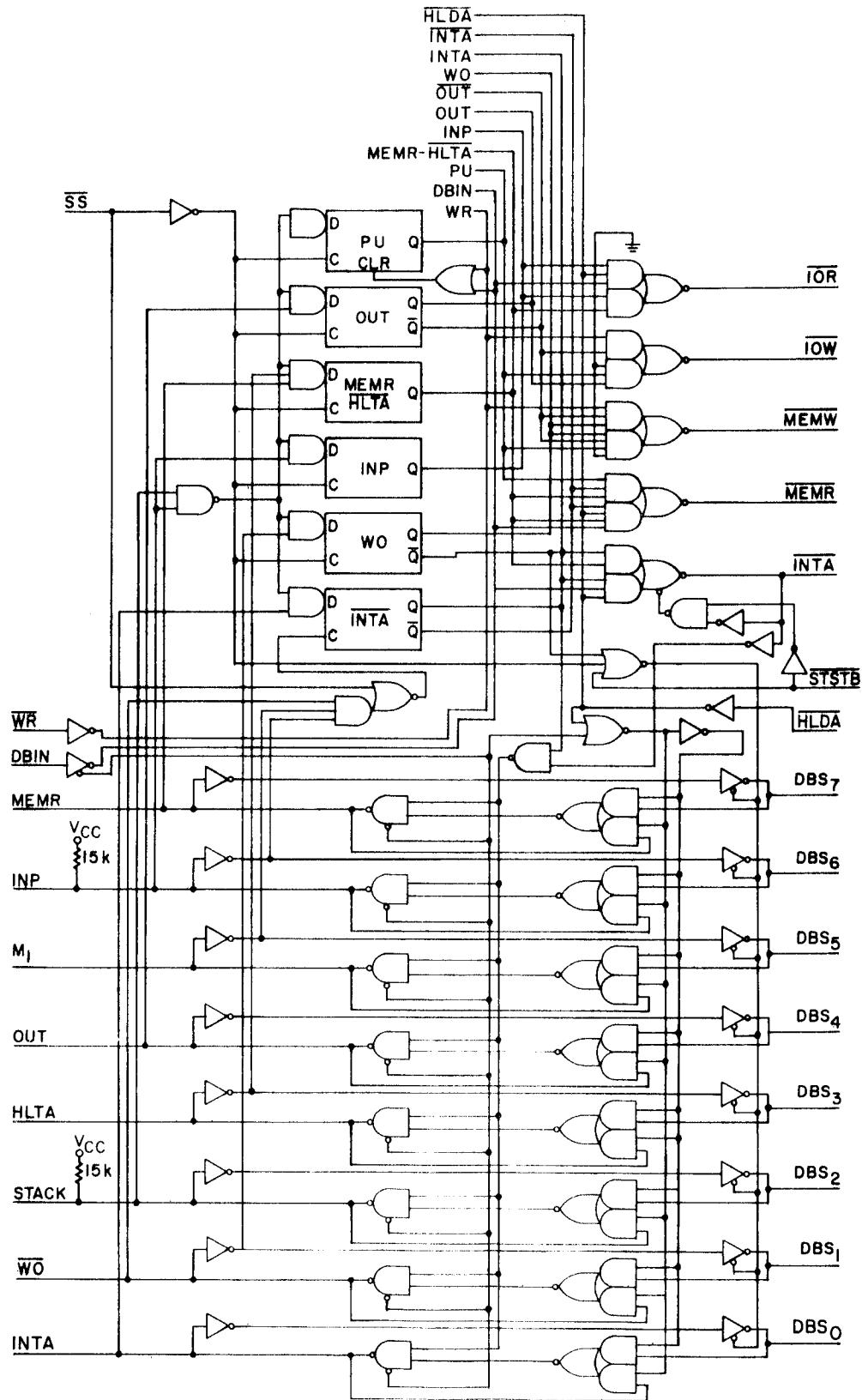


FIGURE 3. Logic diagram.

MIL-M-38510/423A

<u>Pin</u>	<u>Pin name</u>	<u>Schematic</u>
1	$\overline{\text{STSTB}}$	D
2	HLDA	A
3	$\overline{\text{WR}}$	A
4	DB_{IN}	C
5	DB_4	B+E
6	D_4	A+F
7	DB_7	B+E
8	D_7	A+F
9	DB_3	B+E
10	D_3	A+F
11	DB_2	B+E
12	D_2	A+F
13	DB_0	B+E
14	GND	
15	D_0	A+F
16	DB_1	B+E
17	D_1	A+F
18	DB_5	B+E
19	D_5	A+F
20	DB_6	B+E
21	D_6	A+F
22	$\overline{\text{BUSEN}}$	A
23	$\overline{\text{INTA}}$	E
24	$\overline{\text{MEMR}}$	E
25	$\overline{\text{I/OR}}$	E
26	$\overline{\text{MEMW}}$	E
27	$\overline{\text{I/OW}}$	E

FIGURE 4. Schematic circuit.

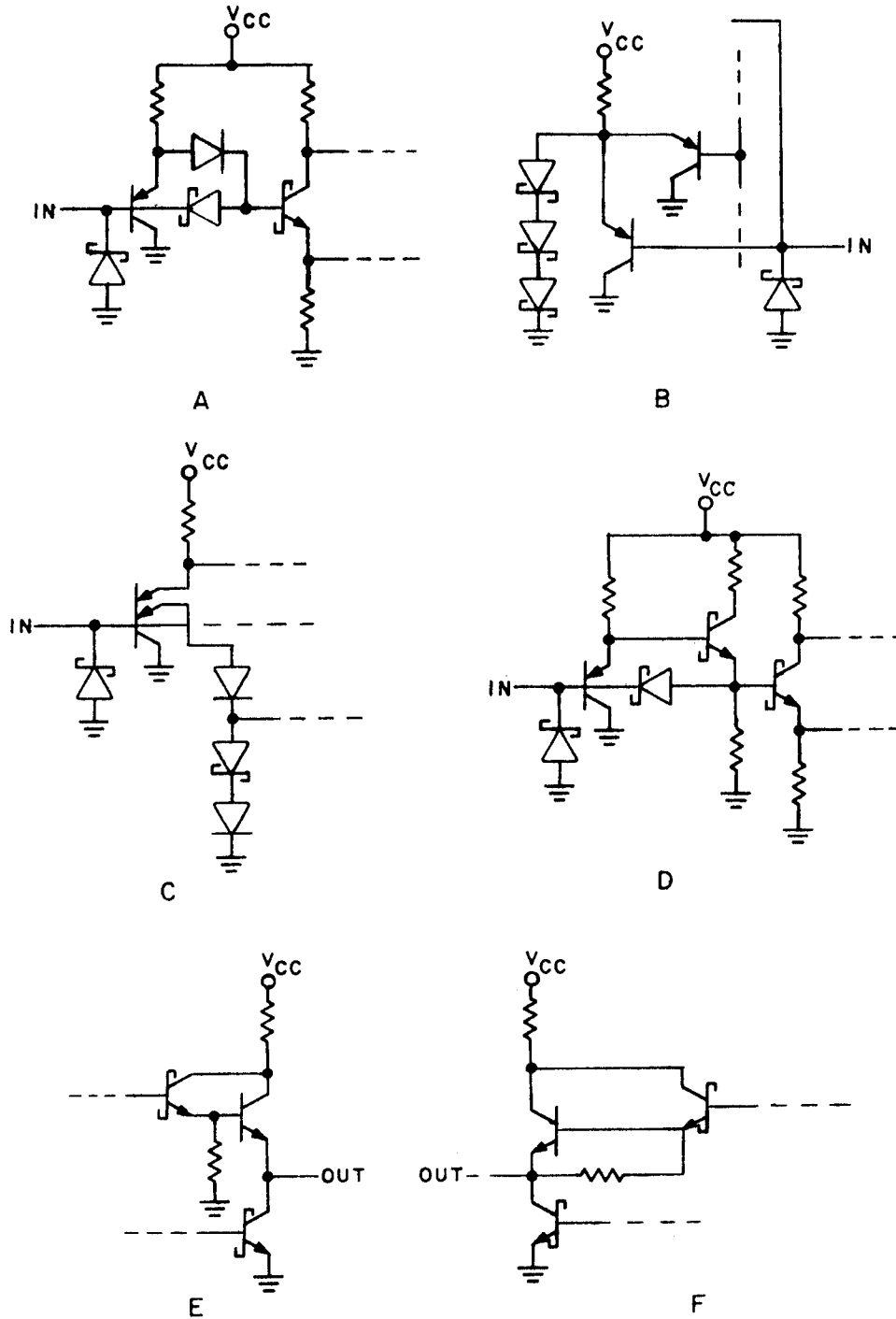
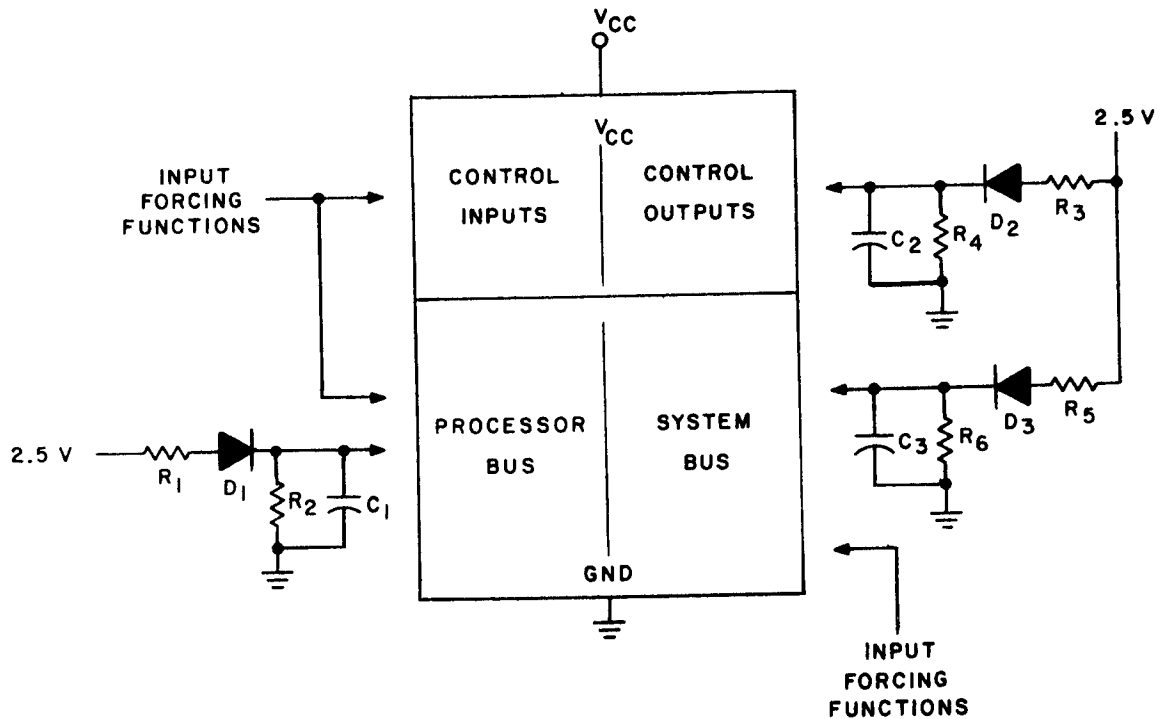


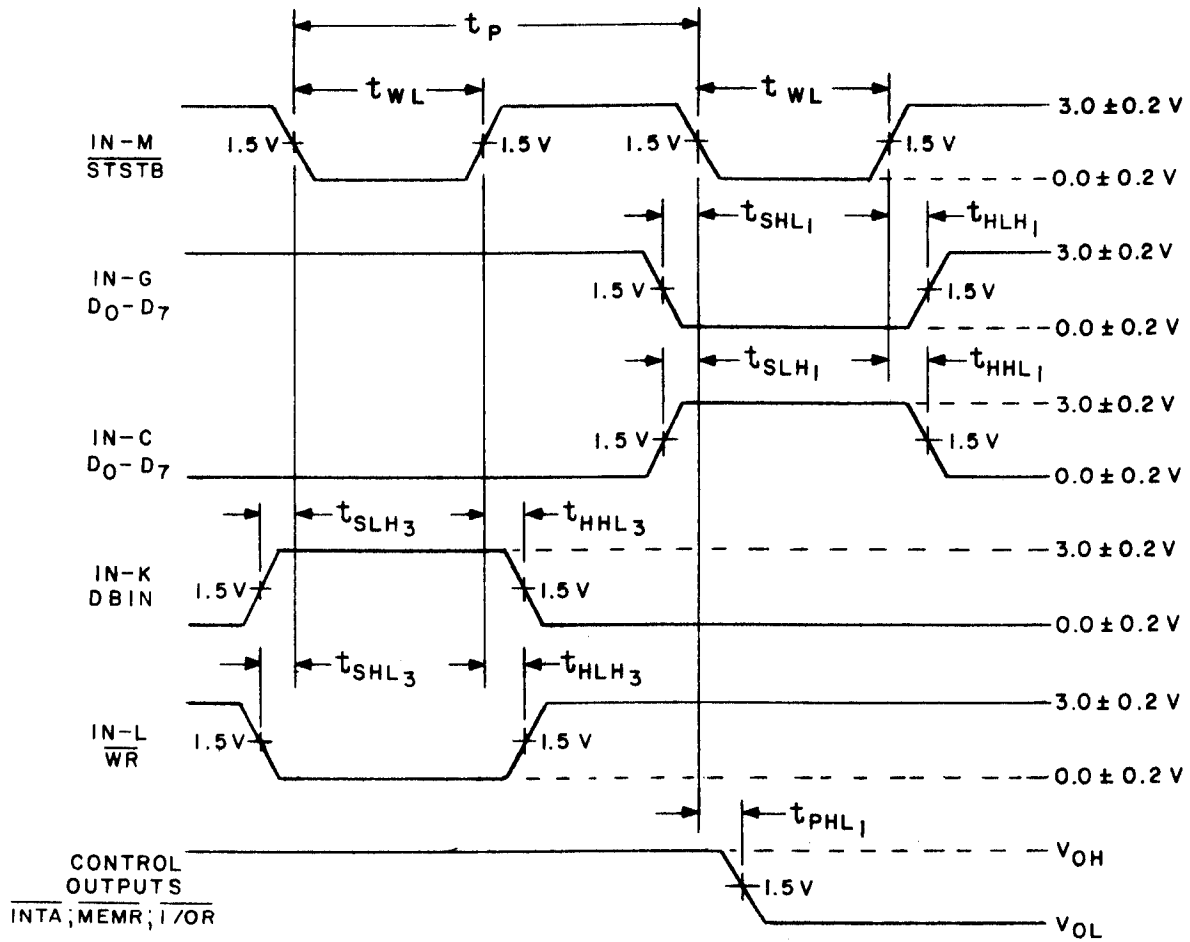
FIGURE 4. Schematic circuit - Continued.



NOTES:

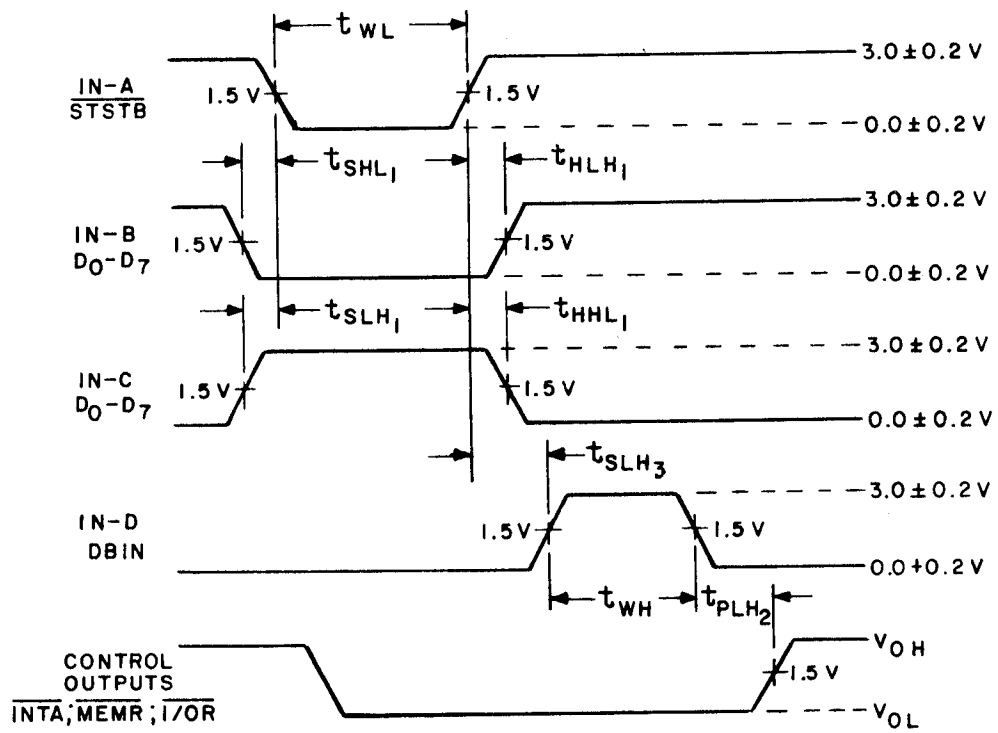
1. $C_1 = 25 \text{ pF}$; $C_2 = C_3 = 100 \text{ pF}$.
2. $R_1 = 600\Omega$; $R_2 = 10 \text{ k}\Omega$; $R_3 = R_5 = 120\Omega$; $R_4 = 3 \text{ k}\Omega$; $R_6 = 2 \text{ k}\Omega$;
all resistors are $\pm 5\%$.
3. $D_1 = D_2 = D_3 = 1\text{N}3064$ or equivalent.
4. $V_{CC} = 5.0 \text{ V}$.
5. Setup times -
 $t_{SLH3} = 30 \text{ ns}$.
 $t_{SHL3} = 30 \text{ ns}$.
6. Hold times -
 $t_{HLH3} = 30 \text{ ns}$.
 $t_{HHL3} = 30 \text{ ns}$.
7. Pulse widths -
 $t_{WH} = 50 \text{ ns}$.
 $t_{WD} = 50 \text{ ns}$.
8. Pulse repetition rate -
 $t_p = 125 \text{ ns}$.

FIGURE 5. Switching waveforms.



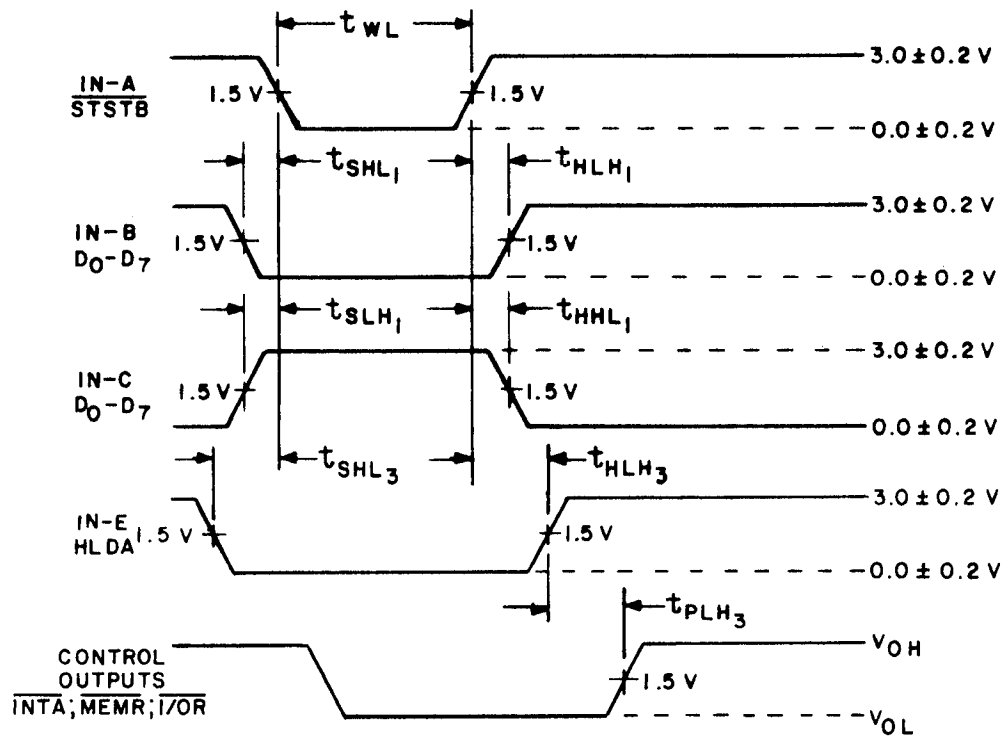
STSTB to control outputs

FIGURE 5. Switching waveforms - Continued.



DBIN to control outputs

FIGURE 5. Switching waveforms - Continued.



HLDA to control outputs

FIGURE 5. Switching waveforms - Continued.

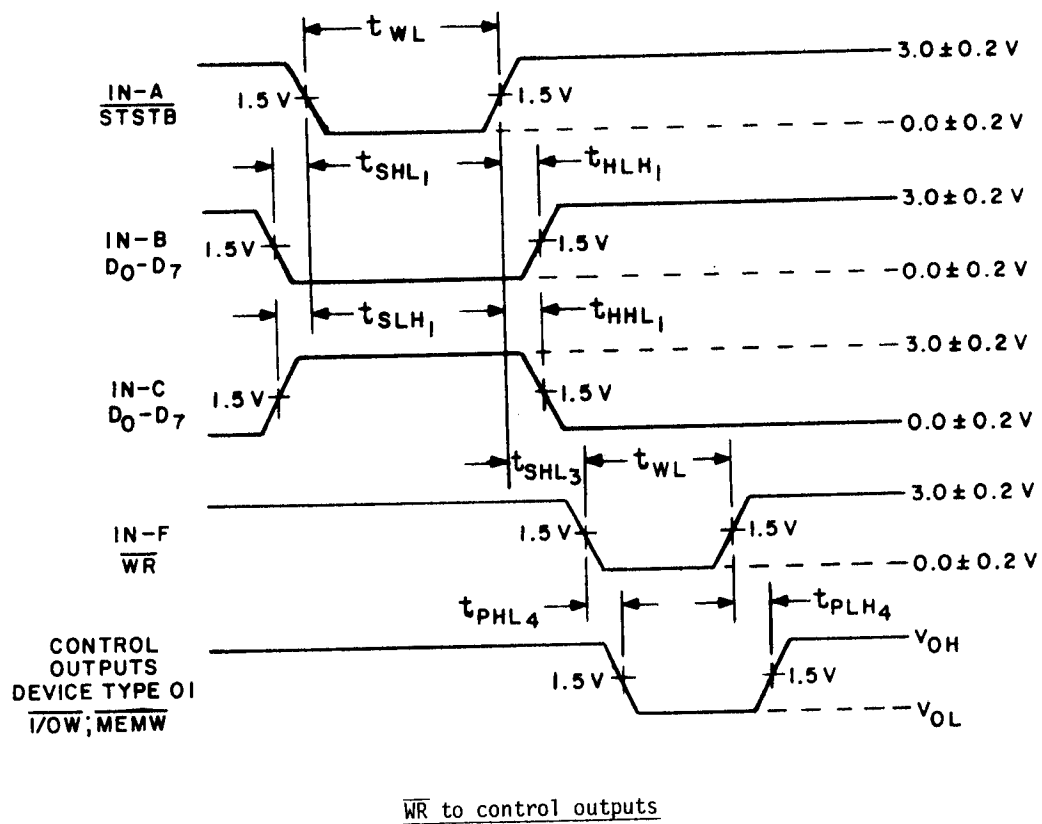
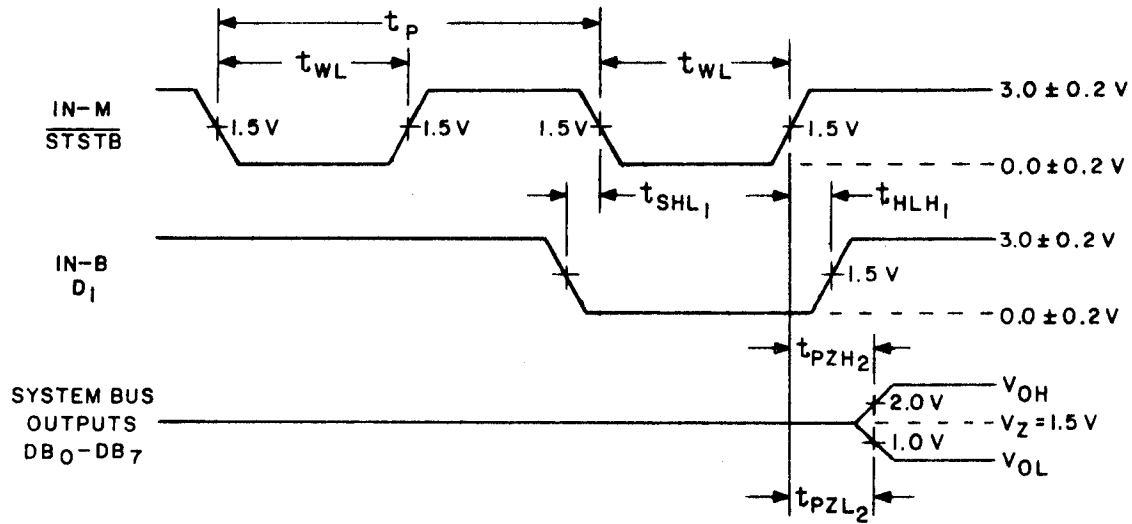
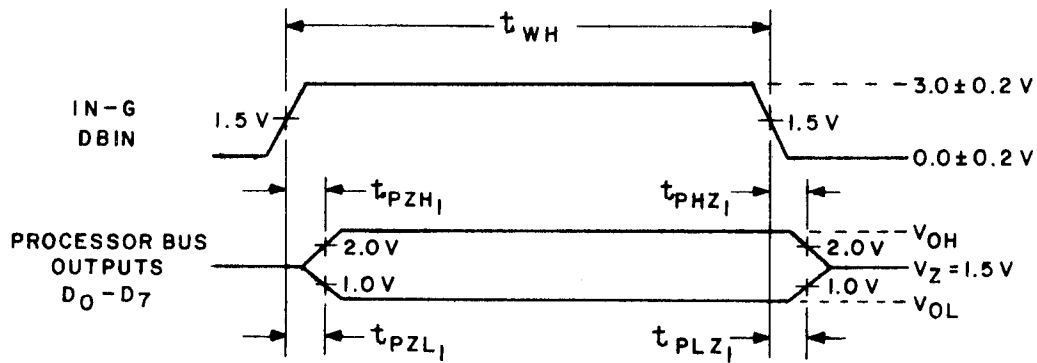


FIGURE 5. Switching waveforms - Continued.



STSTB to system bus - high impedance state



DBIN to processor bus - high impedance state

FIGURE 5. Switching waveforms - Continued.

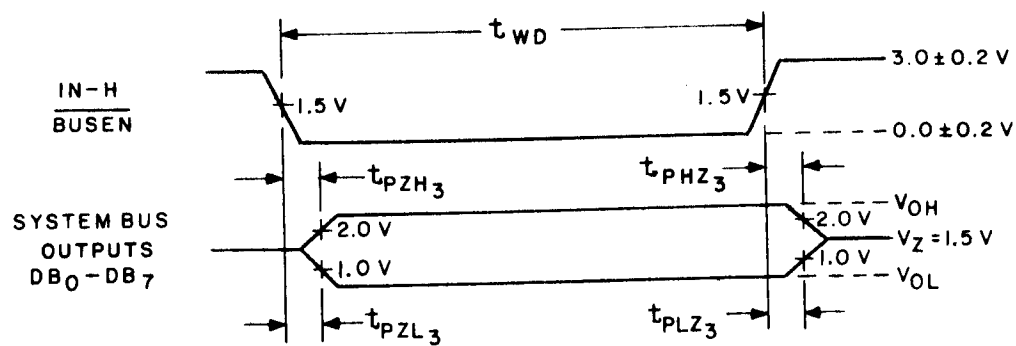
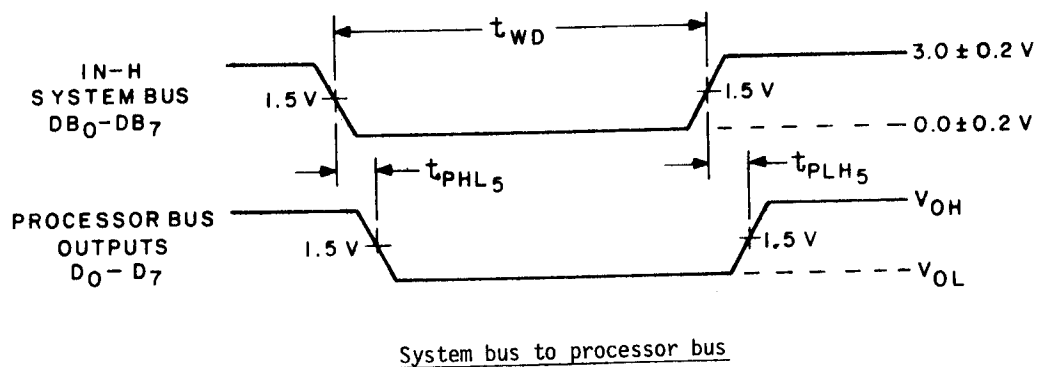
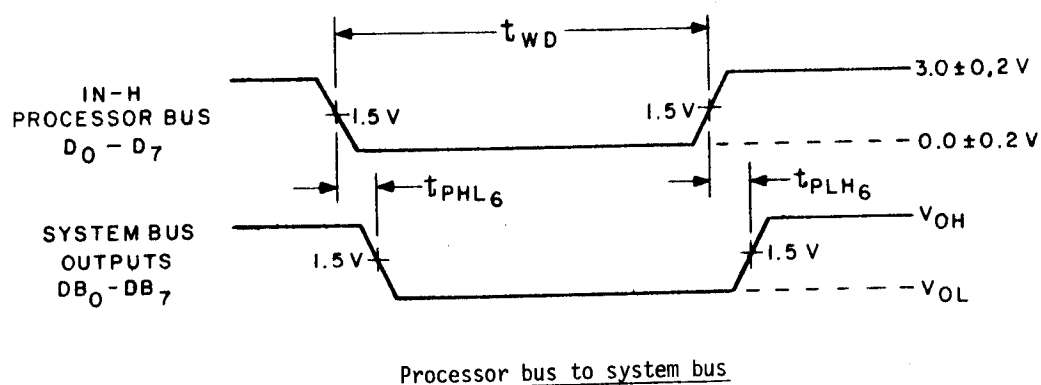
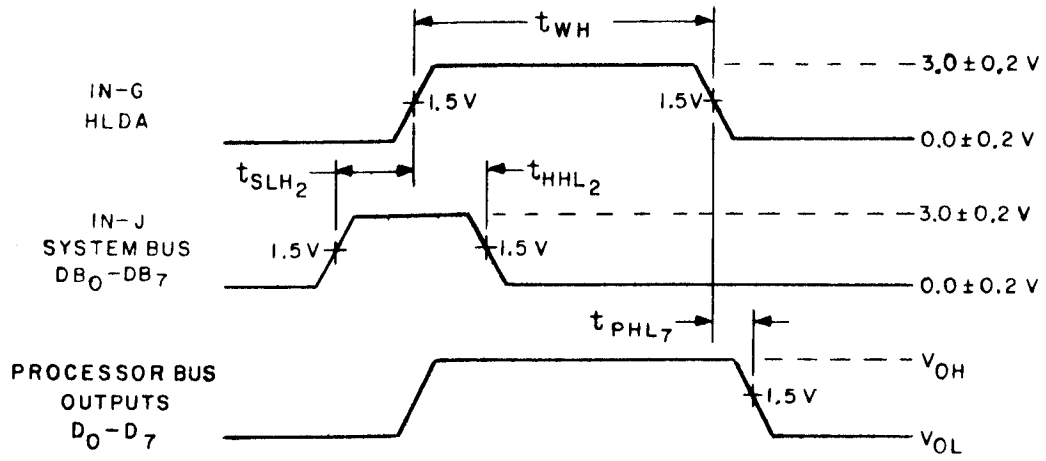
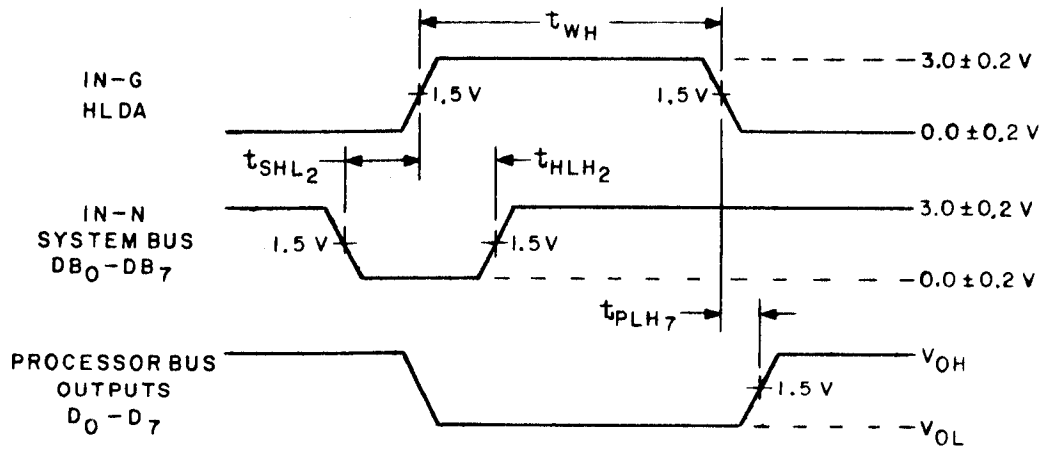


FIGURE 5. Switching waveforms - Continued.

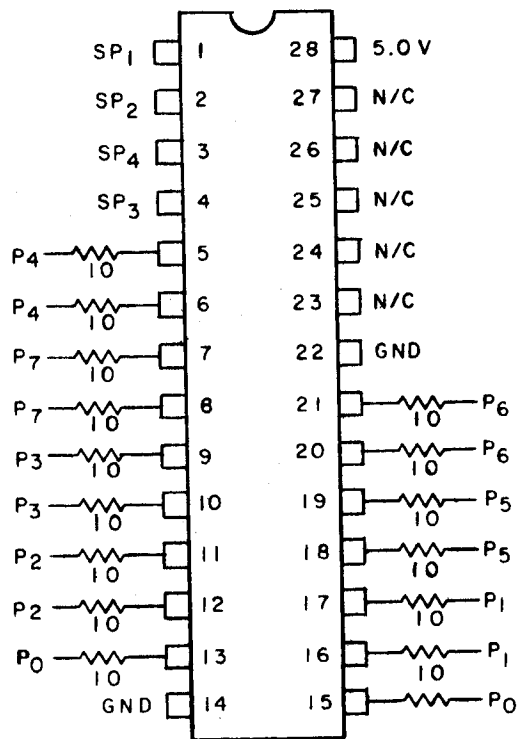
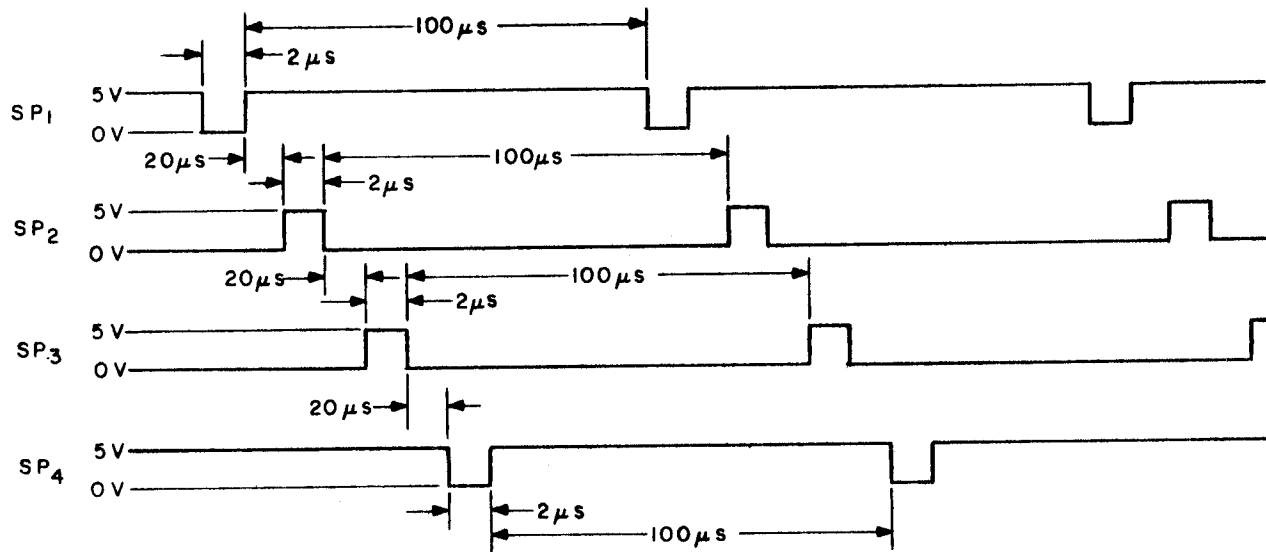


System bus setup/hold time check



System bus setup/hold time check

FIGURE 5. Switching waveforms - Continued.



All resistor values are in kilohms unless otherwise specified.

Pin	Pin name	Stress
1	$\overline{STSTB}$	SP ₁
2	HLDA	SP ₂
3	WR	SP ₄
4	DB _{IN}	SP ₃
5	DB ₄	P ₄
6	D ₄	P ₄
7	DB ₇	P ₇
8	D ₇	P ₇
9	DB ₃	P ₃
10	D ₃	P ₃
11	DB ₂	P ₂
12	D ₂	P ₂
13	DB ₀	P ₀
14	GND	GND
15	D ₀	P ₀
16	DB ₁	P ₁
17	D ₁	P ₁
18	DB ₅	P ₅
19	D ₅	P ₅
20	DB ₆	P ₆
21	D ₆	P ₆
22	BUSEN	GND
23	$\overline{INTA}$	N/C
24	MEMR	N/C
25	I/OR	N/C
26	MEMW	N/C
27	I/OW	N/C
28	V _{CC}	+5.0 V

FIGURE 6. Burn-in circuit and waveforms.

TABLE III. Group A inspection
 Terminal conditions (pins not designated may

Subgroup	Symbol	MIL-STD-883 method	Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			Test No.	STSTB	HLDA	WR	DBIN	DB ₄	D ₄	DB ₇	D ₇	DB ₃	D ₃	DB ₂	D ₂	DB ₀	GND
I T _C =25°C	V _{OH1}	3006	1	C 1/	4.5 V	4.5 V									4.5 V		GND
			2														
			3														
			4														
			5														
			6														
			7														
			8														
			9														
			10														
			11														
			12														
			13														
	V _{OH2}		14		GND		4.5 V	4.5 V	-10 μA	4.5 V	-10 μA	4.5 V	-10 μA	4.5 V	-10 μA	4.5 V	
			15														
			16														
			17														
			18														
			19														
			20														
			21														
			22	C 1/		GND			GND			GND		GND			
	V _{OL1}		23														
			24														
			25														
			26														
			27														
			28														
			29														
			30														
			31														
			32														
			33														
			34														
	V _{OL2}		35		GND		4.5 V	GND	2 mA	GND	2 mA	GND	2 mA	GND	2 mA	GND	
			36														
			37														
			38														
			39														
			40														
			41														
			42														
	I _{IL1}	3009	43	0.4 V													
	I _{IL2}		44		GND		GND							GND	0.4 V		
	I _{IL2}		45														
	I _{IL3}		46					GND	0.4 V	GND	0.4 V	GND	0.4 V			GND	
			47														
			48														
			49														
			50														
			51														
			52														
			53														
			54														
			55														

See footnotes at end of table.

for device type 01.
be high ≥ 2.0 V, low ≤ 0.7 V, or open).

15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit
D ₀	DB ₁	D ₁	DB ₅	D ₅	DB ₆	D ₆	BUSEN	INTA	MEMR	I/OR	MERW	I/OW	VCC		Min	Max	
4.5 V	-1 mA	4.5 V	-1 mA	4.5 V	-1 mA	4.5 V	4.5 V ↓ GND ↓ 4.5 V	-1 mA	-1 mA	-1 mA	-1 mA	-1 mA	4.5 V	23 24 25 26 27 5 7 9 11 13 16 18 20	2.4		V
-10 μ A	4.5 V	-10 μ A	4.5 V	-10 μ A	4.5 V	-10 μ A	4.5 V ↓ GND							6 8 10 12 15 17 19 21	3.3		
4.5 V GND ↓ GND	4.5 V 4.5 V 4.5 V GND GND	4.5 V 4.5 V 4.5 V GND GND	4.5 V 4.5 V 4.5 V GND GND	4.5 V GND ↓ GND	4.5 V GND ↓ GND	4.5 V GND ↓ GND	4.5 V GND ↓ GND	10 mA	10 mA	10 mA	10 mA	10 mA		23 24 25 26 27 5 7 9 11 13 16 18 20		0.5	
2 mA	GND	2 mA	GND	2 mA	GND	2 mA	4.5 V ↓ GND						5.5 V ↓ GND	6 8 10 12 15 17 19 21			
					GND	0.4 V	4.5 V ↓ GND							12 21		-500 -750	μ A
0.4 V	GND	0.4 V	GND	0.4 V			4.5 V ↓ GND							6 8 10 15 17 19 5 7 9 11		-250	

TABLE III. Group A inspection
Terminal conditions (pins not designated may

Subgroup	Symbol	MIL-STD-883 method	Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			Test No.	STSTB	HLDA	WR	DBIN	DB ₄	D ₄	DB ₇	D ₇	DB ₃	D ₃	DB ₂	D ₂	DB ₀	GND
1 T _C =25°C	I _{IL3}	3009	56				GND									0.4 V	GND
			57														
			58														
			59														
			60					0.4 V	4.5 V								
			61							0.4 V	4.5 V						
			62									0.4 V	4.5 V				
			63											0.4 V	4.5 V		
			64													0.4 V	
			65														
			66														
			67														
	I _{IH1}	3010	68					5.5 V	GND								
			69							5.5 V	GND						
			70									5.5 V	GND				
			71											5.5 V	GND		
			72													5.5 V	
			73														
			74														
			75														
			76					5.5 V	4.5 V								
			77							5.5 V	4.5 V						
			78									5.5 V	4.5 V				
			79											5.5 V	4.5 V		
			80													5.5 V	
			81														
			82														
			83														
	I _{IH2}		84	5.5 V													
			85		5.5 V												
			86			5.5 V											
			87				5.5 V										
			88														
			89		GND		GND	GND	5.5 V								
			90							GND	5.5 V						
			91									GND	5.5 V				
			92											GND	5.5 V		
			93													GND	
			94														
			95														
			96														
			97					4.5 V	5.5 V								
			98							4.5 V	5.5 V						
	I _{IH}		105	C 1/	4.5 V	4.5 V										4.5 V	
			106														
			107														
			108														
			109														
			110		GND	GND			GND				GND				
			111														
			112														
			113														
			114						4.5 V								

See footnotes at end of table.

for device type 01 -Continued.
be high ≥ 2.0 V, low ≤ 0.7 V, or open).

15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit
D ₀	DB ₁	D ₁	DB ₅	D ₅	DB ₆	D ₆	BUSEN	INTA	MEMR	I/OR	MERW	I/OW	V _{CC}		Min	Max	
GND	0.4 V	GND	0.4 V	GND	0.4 V	GND	4.5 V						5.5 V	13 16 18 20 5 7 9 11 13 16 18 20		-250	μ A
4.5 V	0.4 V	4.5 V	0.4 V	4.5 V	0.4 V	4.5 V											
GND	5.5 V	GND	5.5 V	GND	5.5 V	GND								5 7 9 11 13 16 18 20 5 7 9 11 13 16 18 20		20	
4.5 V	5.5 V	4.5 V	5.5 V	4.5 V	5.5 V	4.5 V											
5.5 V	GND	5.5 V	GND	5.5 V	GND	5.5 V	5.5 V 4.5 V							1 2 3 4 22 6 8 10 12 15 17 19 21 6 8 10 12 15 17 19 21		100	
5.5 V	4.5 V	5.5 V	4.5 V	5.5 V	4.5 V	5.5 V		5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		23 24 25 26 27 23 24 25 26 27			
4.5 V GND	4.5 V 4.5 V 4.5 V GND GND	4.5 V GND	4.5 V GND	4.5 V GND	4.5 V GND	4.5 V GND 4.5 V GND GND		5.5 V	5.5 V	5.5 V	5.5 V	5.5 V					

TABLE III. Group A inspection
 Terminal conditions (pins not designated may

Subgroup	Symbol	MIL-STD-883 method	Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			Test No.	STSTB	HLDA	WR	DBIN	DB ₄	D ₄	DB ₇	D ₇	DB ₃	D ₃	DB ₂	D ₂	DB ₀	GND
I T _C =25°C	I _{ZL}		115	C 1/	4.5 V	4.5 V									4.5 V		GND
			116														
			117														
			118														
			119														
			120		GND	GND			GND		GND	GND	GND		GND		
			121														
			122														
			123														
			124						4.5 V								
	C _{IN}		125	2.5 V													
			126		2.5 V												
			127			2.5 V											
			128				2.5 V										
			129														
	C _{OUT}		130														
			131														
			132														
			133														
			134														
	C _{I/O}		135		GND		GND	GND	2.5 V								
			136							GND	2.5 V						
			137									GND	2.5 V				
			138											GND	2.5 V		
			139													GND	
			140														
			141														
			142														
			143					2.5 V	GND								
			144							2.5 V	GND						
	I _{OS}	3011	151	C 1/	4.5 V	4.5 V									4.5 V		
			152														
			153														
			154														
			155														
			156				GND	GND	4.5 V								
			157							GND	4.5 V						
			158									GND	4.5 V				
			159											GND	4.5 V	GND	
			160												GND		
	I _{CC}	3005	172	C 1/		GND	GND		GND		GND		GND		GND		
			173														
			174														
			175														
			176														
			177														
			178														
			179														
			180														
			181														

See footnotes at end of table.

MIL-M-38510/423A

for device type 01 -Continued.
be high ≥ 2.0 V, low ≤ 0.7 V, or open).

15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit
D ₀	DB ₁	D ₁	DB ₅	D ₅	DB ₆	D ₆	BUSEN	INTA	MEMR	I/OR	MERW	I/OW	VCC		Min	Max	
4.5 V GND		4.5 V GND GND		4.5 V GND		GND GND 4.5 V GND GND	4.5 V	0.45 V	0.45 V	0.45 V	0.45 V	0.45 V	5.5 V	23 24 25 26 27 23 24 25 26 27		-100	μA
							2.5 V						5.0 V	1 2 3 4 22		12	pF
							GND	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V		23 24 25 26 27		15	
2.5 V GND	GND	2.5 V GND	GND	2.5 V GND	GND	2.5 V GND	4.5 V							6 8 10 12 15 17 19 21 5 7 9 11 13 16 18 20			
4.5 V GND	GND	4.5 V GND	GND	4.5 V GND	GND	4.5 V GND	4.5 V	GND	GND	GND	GND	GND	5.5 V	23 24 25 26 27 5 7 9 11 13 16 18 20 6 8 10 12 15 17 19 21	-15	-100	mA
GND	4.5 V	GND	4.5 V	GND	4.5 V	GND	4.5 V							28		210	

TABLE III. Group A inspection
Terminal conditions (pins not designated may

Subgroup	Symbol	MIL-STD-883 method	Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			Test No.	STSTB	HLDA	WR	DBIN	DB4	D4	DB7	D7	DB3	D3	DB2	D2	DB0	GND
1	V_{IC}		173	-5 mA	-5 mA	-5 mA	-5 mA	-5 mA	-5 mA	-5 mA	-5 mA	-5 mA	-5 mA	-5 mA	-5 mA	-5 mA	GND
$T_C = 25^\circ C$			174														
			175														
			176														
			177														
			178	C 1/	GND		4.5 V	-5 mA							GND		
			179														
			180														
			181														
			182														
			183														
			184														
			185														
			186														
			187														
			188														
			189														
			190														
			191														
			192														
			193														
2	Same tests, terminal conditions, and limits for subgroup 1, except $T_C = 125^\circ C$ and V_{IC} tests are omitted.																
3	Same tests, terminal conditions, and limits for subgroup 1, except $T_C = -55^\circ C$ and V_{IC} tests are omitted.																
7	Functional tests	3014	194	B	X	X	B	X	X	X	X	X	X	X	X	X	GND
$T_C = 25^\circ C$			195		A	A		Z	A	Z	A	Z	B	Z	B	Z	
			196			A			B				A		A		
			197			A			A				B		B		
			198			A			B				H		A		
			199			A			A				H		A		
			200	A		A		H	A	H		L	L		A	H	
			201			A			B				H		A		
			202			A			A				H		A		
			203			A			B				H		A		
			204	B		A		Z	B	Z		Z	Z		A	B	
			205	B		A		Z	B	Z		Z	Z		A		
			206	B		A		Z	B	Z		Z	Z		A		
			207	A		A		L	B	H		L	L		A		
			208	A		A		H	A	H		H	L		A		
			209	A		A		H	A	H		H	L		A		
			210	B	B	A		Z	B	Z		Z	Z		A		
			211	B		B			A								
			212	B		A			B								
			213	A		A			A								
			214			A			B								
			215			B			A								
			216			A			B								
			217			Z			Z								
			218			X			X								
			219			Z			Z								
			220	B		A			A								
			221			A			A								
			222			B			B								
			223			A			A								
			224			A			A								
			225			A			A								
			226	A		Z			Z								
			227	A		X			X								
			228	A													

See footnotes at end of table.

MIL-M-38510/423A

for device type 01 -Continued.
be high ≥ 2.0 V, low ≤ 0.7 V, or open).

15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit
D ₀	DB ₁	D ₁	DB ₅	D ₅	DB ₆	D ₆	BUSEN	INTA	MEMR	I/OR	MERW	I/OW	V _{CC}		Min	Max	
-5 mA	-5 mA	-5 mA	-5 mA	-5 mA	-5 mA	GND ↓ -5 mA	-5 mA 4.5 V ↓ GND						4.5 V	1 2 3 4 5 6 7 8 9 10 11 12 13 15 16 17 18 19 20 21		-1.2	V

X A B A ↓ A A B ↓ A Z X Z A A A B B A A Z X	X Z ↓ L ↓ Z Z Z L H H Z	X B ↓ A ↓ B B B Z X Z B ↓ Z X	X Z ↓ L L L L Z Z Z H H H Z	X B A B ↓ A ↓ B B B Z X Z B ↓ A A Z X	X Z ↓ H ↓ Z Z Z H H H Z	X A B A ↓ B ↓ A A A H X Z B A B A ↓ Z X	X B ↓ ↓	X L H L H L L L L H ↓ ↓	X H ↓ L H L L L H	X L H L H L L L L H H L L L L H ↓ ↓	X H ↓ L H H H L H	X H H H L H H H L H ↓ L H	V _{CC} ↓ L H L H	All outputs ↓ ↓	See 2/ through 6/

TABLE III. Group A inspection
Terminal conditions (pins not designated may

Subgroup	Symbol	MIL-STD-883 method	Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			Test No.	STSTB	HLDA	WR	DBIN	DB4	D4	DB7	D7	DB3	D3	DB2	D2	DB0	GND
7	Functional tests	3014	229	A	B	B	B	Z	Z	Z	Z	Z	Z	Z	Z	Z	GND
T _C =25°C			230	B	B	B	B	Z	B		A		B		A		
			231														
			232														
			233			A											
			234								B						
			235														
			236														
			237														
			238		A												
			239		B												
			240														
			241														
			242														
			243														
			244	A					A		A						
			245						A								
			246						Z								
			247						H								
			248		A				H								
			249		B				H								
			250						Z								
			251						Z								
			252						L								
			253						H								
			254						L								
			255						L								
			256						Z								
			257	B					B								
			258	B					B								
			259	A					B								
			260						A								
			261						A								
			262						B								
			263						B								
			264						X								
			265						X								
			266						X								
			267						X								
			268	B					Z								
			269	A					B								
			270						X								
			271						X								
			272						Z								
			273						X								
			274						Z								
			275						A								
			276						X								
			277						Z								
			278						X								
			279						X								
			280						Z								
			281						H								
			282						H								
			283						H								
			284						L								
			285						L								
			286						L								
			287						H								
			288						L								
			289	A					L								

See footnotes at end of table.

MIL-M-38510/423A

for device type 01 -Continued.
be high ≥ 2.0 V, low ≤ 0.7 V, or open).

15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit		
D ₀	DB ₁	D ₁	DB ₅	D ₅	DB ₆	D ₆	BUSEN	INTA	MEMR	I/OR	MERW	I/OW	V _{CC}		Min	Max			
Z B ↓ A B B A A A B ↓ Z H H H Z Z L ↓ Z A ↓ B B Z X X Z A Z X Z X Z B B Z X X Z H H L L L H H	Z ↓ A ↓ B B A A Z Z L H H L X ↓ Z L X ↓ B B A A B ↓	Z B B A ↓ B B A ↓ Z H H H Z Z L L H H Z B B A A B A Z X X Z B B Z X X Z L L L H H L L L	Z ↓ A ↓ B B A B Z Z Z H H L H X ↓ Z H X ↓ Z H X ↓ B B A A B ↓	Z B ↓ A B B B A A Z H H H Z Z L H L L Z A ↓ B A Z X X Z A A Z X Z X Z A A Z X X Z L L L H H L L L	Z ↓ A A A B A B ↓ Z Z Z L H H L H X ↓ Z H X ↓ Z L X ↓ A A B B B A A B B	Z A A B ↓ A A A Z H H H Z Z L ↓ Z B B B A A B A Z X X Z A A Z X Z X Z B B Z X X Z H H L L L H L	B ↓ A A B ↓ A B ↓ A B ↓ A ↓	H ↓ L H H H L L L H ↓ Z Z H ↓ L Z L L H ↓ Z H L ↓ H ↓ Z ↓	H ↓ L H H H L H L Z Z L ↓ H H Z H ↓ Z H L ↓ H ↓ Z ↓	H H L H ↓ Z Z H ↓ Z H H L ↓ Z L H ↓ Z ↓	H ↓ L ↓ Z Z H ↓ Z H ↓ Z H ↓ Z ↓	V _{CC} ↓	All outputs						
																		See 2/ through 6/	

See
2/ through 6/

TABLE III. Group A inspection
Terminal conditions (pins not designated may

Subgroup	Symbol	MIL-STD-883 method	Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			Test No.	STSTB	HLDA	WR	DBIN	DB ₄	D ₄	DB ₇	D ₇	DB ₃	D ₃	DB ₂	D ₂	DB ₀	GND
7 T _C =25°C	Functional tests	3014	290	A	B	A	B	Z	Z	Z	Z	Z	Z	Z	Z	Z	GND
			291					Z	B	Z	A	Z	A	Z	B	Z	
			292					Z	A	Z	B	Z	B	Z	A	Z	
			293					A	Z	B	Z	B	Z	A	Z	A	
			294					B	Z	A	Z	A	Z	B	Z	B	
			295						L	B	L	B	L		L		
			296						H	B	H	B	H		H		
			297	B			A		L	B	L	B	L		L		
8	Repeat subgroup 7 at T _C = -55°C and T _C = 125°C.																
9 T _C =25°C	t _{PHL1}	3003	298	IN-M	4.5 V	4.5 V	IN-K								IN-C		GND
			299	IN-M	4.5 V	4.5 V	IN-K								IN-B		
			300	IN-M	4.5 V	4.5 V	IN-K								IN-B		
	t _{PLH2}		301	IN-A	GND		IN-D								GND		
			302		GND		IN-D										
			303		GND		IN-D										
	t _{PLH3}		304		IN-E		4.5 V										
			305		IN-E		4.5 V										
			306		IN-E		4.5 V										
	t _{PHL4} 2/		307			IN-F			IN-B								
			308						IN-C								
	t _{PLH4}		309						IN-B								
			310						IN-C								
	t _{PZH1}		311		GND		IN-G	4.5 V	OUT	4.5 V	OUT	4.5 V	OUT	4.5 V	OUT	4.5 V	
			312														
			313														
			314														
			315														
			316														
			317														
			318														
	t _{PZH1}		319					4.5 V	OUT	4.5 V	OUT	4.5 V	OUT	4.5 V	OUT	4.5 V	
			320														
			321														
			322														
			323														
			324														
			325														
			326														
	t _{PLZ1}		327					GND	OUT	GND	OUT	GND	OUT	GND	OUT	GND	
			328														
			329														
			330														
			331														
			332														
			333														
			334														
	t _{PZL1}		335					GND	OUT	GND	OUT	GND	OUT	GND	OUT	GND	
			336														
			337														
			338														
			339														
			340														
			341														
			342														

See footnotes at end of table.

MIL-M-38510/423A

for device type 01 -Continued.
be high ≥ 2.0 V, low ≤ 0.7 V, or open).

15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit
D ₀	DB ₁	D ₁	DB ₅	D ₅	DB ₆	D ₆	BUSEN	INTA	MEMR	I/OR	MERW	I/OW	V _{CC}		Min	Max	
Z B A Z Z L H L	Z Z Z B A B ↓	Z A B Z Z L H L	Z Z B A B B B	Z A B Z Z L H L	Z Z A B ↓	Z B A Z Z L H L	A ↓	Z ↓ +12 V +12 V	Z ↓	Z ↓	Z ↓	Z ↓	V _{CC} ↓	All outputs ↓	See 2/ through 6/		

IN-C IN-B		IN-B IN-B		IN-C IN-B		IN-B IN-C IN-C	GND ↓	OUT ↓	OUT ↓	OUT ↓			5.0 V ↓	23 24 25	20 ↓	75 75 75	ns
IN-C IN-B				IN-C ↓		IN-C ↓		OUT ↓	OUT ↓	OUT ↓				23 24 25		35 35 35	
IN-C IN-B				↓		IN-C ↓		OUT ↓	OUT ↓	OUT ↓				23 24 25		28 28 28	
		GND								OUT ↓	OUT ↓			26 27	5 ↓	60 ↓	
		GND								OUT ↓	OUT ↓			26 27			
OUT 4.5 V	OUT 4.5 V	OUT 4.5 V	OUT 4.5 V	OUT 4.5 V	OUT 4.5 V	OUT 4.5 V	4.5 V ↓							6 8 10 12 15 17 19 21		45 ↓	
OUT 4.5 V	OUT 4.5 V	OUT 4.5 V	OUT 4.5 V	OUT 4.5 V	OUT 4.5 V	OUT 4.5 V								6 8 10 12 15 17 19 21			
OUT GND	OUT GND	OUT GND	OUT GND	OUT GND	OUT GND	OUT GND								6 8 10 12 15 17 19 21			
OUT GND	OUT GND	OUT GND	OUT GND	OUT GND	OUT GND	OUT GND	↓							6 8 10 12 15 17 19 21		↓	↓

TABLE III. Group A inspection
Terminal conditions (pins not designated may

Subgroup	Symbol	MIL-STD-883 method	Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			Test No.	STSTB	HLDA	WR	DBIN	DB ₄	D ₄	DB ₇	D ₇	DB ₃	D ₃	DB ₂	D ₂	DB ₀	GND
9 T _C = 25°C	t _{pZH2} ↓	3003	343	IN-M			GND	OUT	4.5 V		OUT	4.5 V		OUT	4.5 V		GND
			344														
			345														
			346														
			347														
			348														
			349														
			350														
	t _{pZL2} ↓		351					OUT	GND	OUT	GND	OUT	GND	OUT	GND	OUT	
			352														
			353														
			354														
			355														
			356														
			357														
			358														
	t _{pZH3} 2/ ↓		359	C 1/ 4.5 V				OUT	4.5 V		OUT	4.5 V		OUT	4.5 V		
			360														
			361														
			362														
			363														
			364														
			365														
			366														
	t _{pZH3} 2/ ↓		367	C 1/ 4.5 V				OUT	4.5 V		OUT	4.5 V		OUT	4.5 V		
			368														
			369														
			370														
			371														
			372														
			373														
			374														
	t _{pZL3} 2/ ↓		375	C 1/ 4.5 V				OUT	GND	OUT	GND	OUT	GND	OUT	GND	OUT	
			376														
			377														
			378														
			379														
			380														
			381														
			382														
	t _{pLZ3} 2/ ↓		383	C 1/ 4.5 V				OUT	GND	OUT	GND	OUT	GND	OUT	GND	OUT	
			384														
			385														
			386														
			387														
			388														
			389														
			390														
	t _{pHLS} ↓		391		GND		4.5 V	IN-H	OUT	IN-H	OUT	IN-H	OUT	IN-H	OUT	IN-H	
			392														
			393														
			394														
			395														
			396														
			397														
			398														

See footnotes at end of table.

MIL-M-38510/423A

for device type 01 -Continued.
be high ≥ 2.0 V, low ≤ 0.7 V, or open).

15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit
D ₀	DB ₁	D ₁	DB ₅	D ₅	DB ₆	D ₆	BUSEN	INTA	MEMR	I/OR	MERW	I/OW	V _{CC}		Min	Max	
4.5 V	OUT	4.5 V	OUT	4.5 V	OUT	GND ↓ 4.5 V	GND ↓						5.0 V ↓	5 7 9 11 13 16 18 20		36	ns
GND	OUT	GND	OUT	GND	OUT	GND ↓	GND ↓						↓	5 7 9 11 13 16 18 20		↓	↓
4.5 V	OUT	4.5 V	OUT	4.5 V	OUT	GND ↓ 4.5 V	IN-H ↓						5.0 V ↓	- 5 7 9 11 13 16 18 20	-	35	ns
4.5 V	OUT	4.5 V	OUT	4.5 V	OUT	GND ↓ 4.5 V	IN-H ↓						5.0 V ↓	- 5 7 9 11 13 16 18 20	-	35	ns
GND	OUT	GND	OUT	GND	OUT	GND ↓	IN-H ↓						5.0 V ↓	- 5 7 9 11 13 16 18 20	-	35	ns
GND	OUT	GND	OUT	GND	OUT	GND ↓	IN-H ↓						5.0 V ↓	- 5 7 9 11 13 16 18 20	-	35	ns
GND	OUT	GND	OUT	GND	OUT	GND ↓	IN-H ↓						5.0 V ↓	- 5 7 9 11 13 16 18 20	-	35	ns
OUT	IN-H	OUT	IN-H	OUT	IN-H	OUT	4.5 V ↓						↓	6 8 10 12 15 17 19 21		45	ns

TABLE III. Group A inspection
Terminal conditions (pins not designated may

Subgroup	Symbol	MIL-STD-883 method	Case	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
			Test No.	STSTB	HLDA	WR	DBIN	DB ₄	D ₄	DB ₇	D ₇	DB ₃	D ₃	DB ₂	D ₂	DB ₀	GND	
9 T _C = 25°C	τ _{PLH5}	3003	399		GND		4.5 V	IN-H	OUT		IN-H	OUT					GND	
			400															
			401															
			402															
			403															
			404															
			405															
			406															
	τ _{PHL6}		407	C 1/ 4.5 V				GND	OUT	IN-H		OUT	IN-H					GND
			408															
			409															
			410															
			411															
			412															
			413															
			414															
	τ _{PLH6}		415	C 1/ 4.5 V				GND	OUT	IN-H		OUT	IN-H					GND
			416															
			417															
			418															
			419															
			420															
			421															
			422															
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = 125°C.																	
11	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = -55°C.																	

1/ C =  2.7 V min
0 V +0.2 V

2/ The tests in subgroups 7 and 8 shall be run in sequence.

3/ Input voltages: A = 2.0 V; B = 0.8 V.

4/ Output voltages: H = 3.3 V for D₀ - D₇ only; H = 2.4 V for all other outputs; L = 0.5 V for all outputs.

5/ X = Don't care.

6/ Z = High impedance state. It must be checked at every data point noted in subgroup 7:

a. A forcing voltage and resulting current for outputs D₂ and D₆ must meet the following:

Forcing voltage	Limit for resulting current
0.4 V	-750 μA max
5.5 V	100 μA max

b. For all other high impedance outputs (excluding D₂ and D₆) either of the two test procedures may be followed:

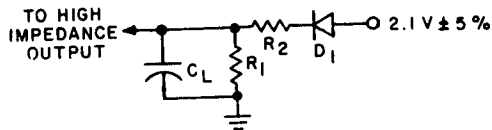
1. A forcing voltage and the resulting current must meet the following:

Pins	Forcing voltage	Limit for resulting current
DB ₀ -DB ₇ ; D ₀ ; D ₁ ; D ₃ -D ₅ ; D ₇	0.4 V	-250 μA max
DB ₀ -DB ₇	5.5 V	20 μA max
D ₀ ; D ₁ ; D ₃ -D ₅ ; D ₇	5.5 V	100 μA max

2. A load as shown below is connected to the output. The output voltage shall be measured from 70 μs to 100 μs after the high impedance control line is enabled. the resultant voltage at the output pin shall be: 1.0 V ≤ V_{OUT} ≤ 2.0 V.

for device type 01 -Continued.
be high ≥ 2.0 V, low ≤ 0.7 V, or open).

15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit
D ₀	DB ₁	D ₁	DB ₅	D ₅	DB ₆	D ₆	$\overline{\text{BUSEN}}$	$\overline{\text{INTA}}$	$\overline{\text{MEMR}}$	$\overline{\text{I/OR}}$	$\overline{\text{MERW}}$	$\overline{\text{I/OW}}$	V _{CC}		Min	Max	
OUT	IN-H	OUT	IN-H	OUT	IN-H	OUT	4.5 V						5.0 V	6 8 10 12 15 17 19 21		45	ns
IN-H	OUT	GND	IN-H	OUT	IN-H	GND	GND						5.0 V	5 7 9 11 13 16 18 20	5	40	ns
IN-H	OUT	GND	IN-H	OUT	IN-H	GND	GND						5.0 V	5 7 9 11 13 16 18 20	5	40	ns



Output	R ₁	R ₂
D ₀ , D ₁ , D ₃ -D ₅ , D ₇	332 kΩ ±5%	536Ω ±5%
DB ₀ - DB ₇	237 kΩ ±5%	105Ω ±5%

D₁ = 1N3064, or equivalent.

C_L = 40 ±5 pF (includes tester, wiring, probe, and lead capacitance).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Generic test data (see 6.6) may be used to satisfy the requirements for group C and D inspections. Quality conformance inspection shall be completed on the specific devices covered by this specification before they are shipped.

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, 6, and 8 of table 1 of method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 1 (C_{IN}, C_{OUT}, C_{I/O} measurement) shall be performed only after process or design changes which may affect design capacitance.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. Electrical parameters shall be as specified in table II herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End point electrical parameters shall be as specified in table II herein.
- b. Subgroups 3 and 4 shall be added to the group C inspection requirements for class B devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.
- c. Steady-state life-test (method 1005 of MIL-STD-883) conditions.
 1. Test condition D or E, using the circuit shown on figure 4, or equivalent.
 2. T_A = 125°C, minimum.
 3. Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510.

4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be as specified in MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.3 Ordering data. The contract or purchase order should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to contracting activity if applicable.
- e. Requirements for packaging and packing.
- f. Requirements for special carriers, lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND-	- - - - -	Electrical ground (common terminal)
VIN-	- - - - -	Voltage level at an input terminal
FOSC-	- - - - -	Oscillating frequency

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.6 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than one year old and on a die in the same microcircuit group (See Appendix E of MIL-M-38510) with the same material, design and process and from the same plant as the die represented. Group D generic data (see 4.4.4) shall be on date codes no more than one year old and on the same package type (see terms, definitions and symbols of MIL-M-38510) and from the same plant as the package represented. The vendor is required to retain the generic data for a period of not less than 36 months from the date of shipment.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device
<u>type</u>
01

Generic-industry
<u>type</u>
8228

6.8 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

6.9 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:

Army - ER
Navy - EC
Air Force - 17

Preparing activity:

Air Force - 17

Review activities:

Army - AR, MI
Air Force - 11, 19, 85, 99
Navy - OS, SH
DLA - ES

(Project 5962-0603-6)

User activities:

Army - SM
Navy - AS, CG, MC

Agent:

DLA - ES