

INCH-POUND

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SUPERSEDING
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MILITARY SPECIFICATION

MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 262,144-BIT STATIC
RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies
of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS, 262,144-bit, static random access memory microcircuits. Two product assurance classes (S and B) and a choice of case outlines and lead finishes are provided and are reflected in the complete Part or Identifying Number (PIN) (see 6.6). The term Part or Identifying Number (PIN) is equivalent to the term part number which was previously used in this specification.

1.2 Classification.

1.2.1 Device types. The device types shall be as follows:

<u>Device type</u>	<u>Circuit organization</u>	<u>Access time</u>
01	262,144 x 1-bit SRAM	45 ns
02	262,144 x 1-bit SRAM	35 ns
03	65,536 x 4-bit SRAM	45 ns
04	65,536 x 4-bit SRAM	35 ns
05, 14	65,536 x 4-bit SRAM with <u>OE</u>	45 ns
06, 15	65,536 x 4-bit SRAM with <u>OE</u>	35 ns
07	32,768 x 8-bit SRAM with <u>OE</u>	55 ns
08	32,768 x 8-bit SRAM with <u>OE</u>	45 ns
09	32,768 x 8-bit SRAM with <u>OE</u>	35 ns
10	262,144 x 1-bit SRAM	25 ns
11	65,536 x 4-bit SRAM	25 ns
12, 16	65,536 x 4-bit SRAM with <u>OE</u>	25 ns
13	32,768 x 8-bit SRAM with <u>OE</u>	25 ns
17	32,768 x 8-bit SRAM with <u>OE</u>	20 ns
18	262,144 x 1-bit SRAM	20 ns
19	65,536 x 4-bit SRAM	20 ns
20	65,536 x 4-bit SRAM with <u>OE</u>	20 ns
21	65,536 x 4-bit SRAM with <u>OE</u> (low power)	45 ns
22	65,536 x 4-bit SRAM with <u>OE</u> (low power)	35 ns
23	65,536 x 4-bit SRAM with <u>OE</u> (low power)	25 ns
24	65,536 x 4-bit SRAM with <u>OE</u> (low power)	20 ns
25	32,768 x 8-bit SRAM with <u>OE</u> (low power)	45 ns
26	32,768 x 8-bit SRAM with <u>OE</u> (low power)	35 ns
27	32,768 x 8-bit SRAM with <u>OE</u> (low power)	25 ns
28	32,768 x 8-bit SRAM with <u>OE</u> (low power)	20 ns

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, (RBE-2), Griffiss AFB, NY 13441-5700, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A

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Device type	Circuit organization	Access time
29	65,536 x 4-bit SRAM (low power)	45 ns
30	65,536 x 4-bit SRAM (low power)	35 ns
31	65,536 x 4-bit SRAM (low power)	25 ns
32	65,536 x 4-bit SRAM (low power)	20 ns
33	262,144 x 1-bit SRAM (low power)	45 ns
34	262,144 x 1-bit SRAM (low power)	35 ns
35	262,144 x 1-bit SRAM (low power)	25 ns
36	262,144 x 1-bit SRAM (low power)	20 ns

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline(s). For device classes B and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below.

Outline letter	Case outline (see MIL-M-38510, appendix C)
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
M	F-12 (28-lead, .740" x .420" x .130"), flat package
N	C-11 (28-terminal, .560" x .358" x .120"), rectangular chip carrier package
T	C-12 (32-terminal, .560" x .458" x .120"), rectangular chip carrier package
U	C-11A (28-terminal, .560" x .358" x .075"), rectangular chip carrier package
X	D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package
Y	D-15 (28-lead, 1.485" x .310" x .230"), dual-in-line package
Z	F-11 (28-lead, .740" x .380" x .090"), flat package

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases K, L, M, N, T, U, X, Y, and Z	See MIL-M-38510, appendix C
Output voltage applied in high Z state	-0.5 V dc to +7.0 V dc
Maximum power dissipation (P_D)	1.0 W
Maximum junction temperature (T_J)	+175°C 3/

1.4 Recommended operating conditions.

Supply voltage	4.5 V dc minimum to 5.5 V dc maximum
High level input voltage (V_{IH})	2.2 V dc to V_{CC}
Low level input voltage (V_{IL})	-0.5 V dc to 0.3 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. For use guidelines, not tested.
- 2/ Unless otherwise specified, all voltages referenced to V_{SS} (V_{SS} = ground).
- 3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.1.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.1.2 Truth table. The truth table shall be as specified on figure 2.

3.1.3 Schematic circuits. The schematic circuits shall be submitted to the preparing activity prior to the inclusion of a manufacturer's device in this specification and shall be submitted to the qualifying activity as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained and available upon request.

3.1.4 Case outlines. The case outlines shall be in accordance with MIL-M-38510 and 1.2.3 herein.

3.1.5 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

3.1.6 Die overcoat. Polyamide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-M-38510, inspection lot - class B paragraph) shall be subjected to and pass the internal moisture content test at 5,000 ppm (method 1018 of MIL-STD 883), the frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.2 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the case operating temperature range specified. A pin for pin conditions and testing sequence for table I parameters shall be maintained and available upon request from the qualifying activity.

3.3 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I. Any additional detailed information of electrical test requirements not covered in table I (i.e., pin for pin conditions and testing sequence) shall be maintained and available upon request from the qualifying activity.

3.4 Correctness of indexing and marking. All devices shall be subjected to the final electrical tests specified in table II after PIN marking to verify that they are correctly indexed and identified by PIN. Optionally, an approved electrical test may be devised especially for this requirement.

3.5 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 41 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.1.1 Burn-in and life test circuits. Burn-in and life test circuits shall be constructed so that the devices are stressed at the maximum operating conditions stated in 4.2c, or equivalent as approved by the qualifying activity.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 7 of table II herein.
- b. Static burn-in (method 1015 of MIL-STD-883, test condition A).
 - (1) All inputs and common input/outputs shall be connected through R1 to V_{CC} . Separate outputs may be open or connected to $V_{CC}/2 \pm 0.5$ V. Resistor R1 is optional on both inputs and open outputs when V_{CC} is not applied, and required on outputs connected to $V_{CC}/2$. $R1 = 2$ kilohms $\pm 5\%$.
 - (2) $V_{CC} = 5.75$ V ± 0.25 V.
- c. Dynamic burn-in (method 1015 of MIL-STD-883, test condition D).
 - (1) All inputs and common input/outputs shall be connected through R1 to the pulse generator. Separate outputs may be open or connected to $V_{CC}/2 \pm 0.5$ V. Resistor R1 is optional on both inputs and open outputs when V_{CC} is not applied, and required on outputs connected to $V_{CC}/2$. $R1 = 2$ kilohms $\pm 5\%$.
 - (2) $V_{CC} = 5.75$ V ± 0.25 V.
 - (3) All pulse generators have the following characteristics: $V_{IL} = -0.25$ V minimum to $+0.25$ V maximum; $V_{IH} = +2.75$ V minimum to $+3.25$ V maximum; 50% $\pm 15\%$ duty cycle.
 - (4) Input frequencies for device types 01, 02, 10, 18, and 34 through 36 are as follows:

$$\overline{CE} = V_{IL}, \overline{WE} = V_{IL}, D_{OUT} = \text{open.}$$

$$F = 500 \text{ kHz } \pm 20\% \text{ minimum.}$$

$$A_0 = F, A_1 = F/2, A_2 = F/4, A_3 = F/8, A_4 = F/16, A_5 = F/32, A_6 = F/64,$$

$$A_7 = F/128, A_8 = F/256, A_9 = F/512, A_{10} = F/1024, A_{11} = F/2048,$$

$$A_{12} = F/4096, A_{13} = F/8192, A_{14} = F/16384, A_{15} = F/32768, A_{16} = F/65536,$$

$$A_{17} = F/131072, D_{IN} = F/262144.$$

- (5) Input frequencies for device types 03, 04, 11, 19, and 29 through 32 are as follows:

$$\begin{aligned} \overline{CE} &= V_{IL}, \overline{OE} = V_{IL} \\ F &= 500 \text{ kHz } \pm 20\% \text{ minimum.} \\ A_0 &= F, A_1 = F/2, A_2 = F/4, A_3 = F/8, A_4 = F/16, A_5 = F/32, A_6 = F/64, \\ A_7 &= F/128, A_8 = F/256, A_9 = F/512, A_{10} = F/1024, A_{11} = F/2048, \\ A_{12} &= F/4096, A_{13} = F/8192, A_{14} = F/16384, A_{15} = F/32768, I/O_0 = F/65536, \\ I/O_1 &= F/65536, I/O_2 = F/65536, I/O_3 = F/65536. \end{aligned}$$

- (6) Input frequencies for device types 05, 06, and 16 are as follows:

$$\begin{aligned} \overline{CE}_1 &= V_{IL}, \overline{CE}_2 = V_{IL}, \overline{WE} = V_{IL}, \overline{OE} = V_{CC} \\ F &= 500 \text{ kHz } \pm 20\% \text{ minimum.} \\ A_0 &= F, A_1 = F/2, A_2 = F/4, A_3 = F/8, A_4 = F/16, A_5 = F/32, A_6 = F/64, \\ A_7 &= F/128, A_8 = F/256, A_9 = F/512, A_{10} = F/1024, A_{11} = F/2048, \\ A_{12} &= F/4096, A_{13} = F/8192, A_{14} = F/16384, A_{15} = F/32768, I/O_0 = F/65536, \\ I/O_1 &= F/65536, I/O_2 = F/65536, I/O_3 = F/65536. \end{aligned}$$

- (7) Input frequencies for device types 07, 08, 09, 13, 17, and 25 through 28 are as follows:

$$\begin{aligned} \overline{CE} &= V_{IL}, \overline{OE} = V_{IL}, \overline{OE} = V_{CC} \\ F &= 500 \text{ kHz } \pm 20\% \text{ minimum.} \\ A_0 &= F, A_1 = F/2, A_2 = F/4, A_3 = F/8, A_4 = F/16, A_5 = F/32, A_6 = F/64, \\ A_7 &= F/128, A_8 = F/256, A_9 = F/512, A_{10} = F/1024, A_{11} = F/2048, \\ A_{12} &= F/4096, A_{13} = F/8192, A_{14} = F/16384, I/O_0 = F/32768, I/O_1 = F/32768, \\ I/O_2 &= F/32768, I/O_3 = F/32768, I/O_4 = F/32768, I/O_5 = F/32768, I/O_6 = F/32768, \\ I/O_7 &= F/32768. \end{aligned}$$

- (8) Input frequencies for device types 12, 14, 15, and 20 through 24 are as follows:

$$\begin{aligned} \overline{CE} &= V_{IL}, \overline{OE} = V_{IL}, \overline{OE} = V_{CC} \\ F &= 500 \text{ kHz } \pm 20\% \text{ minimum.} \\ A_0 &= F, A_1 = F/2, A_2 = F/4, A_3 = F/8, A_4 = F/16, A_5 = F/32, A_6 = F/64, \\ A_7 &= F/128, A_8 = F/256, A_9 = F/512, A_{10} = F/1024, A_{11} = F/2048, \\ A_{12} &= F/4096, A_{13} = F/8192, A_{14} = F/16384, A_{15} = F/32768, I/O_0 = F/65536, \\ I/O_1 &= F/65536, I/O_2 = F/65536, I/O_3 = F/65536. \end{aligned}$$

- d. Interim and final electrical parameters shall be as specified in table II herein.
- e. For class S or B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.1 Percent defective allowable (PDA).

- a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.
- b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.
- c. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

TABLE I. Electrical performance characteristics.

Parameter	Symbol	Test conditions $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ $\text{GND} = 0 \text{ V}$ $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ unless otherwise specified	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -4.0 \text{ mA}$ $V_{IL} = 0.8 \text{ V}$, $V_{IH} = 2.2 \text{ V}$	1,2,3 (3006)	ALL	2.4		V
Low level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 8.0 \text{ mA}$ $V_{IL} = 0.8 \text{ V}$, $V_{IH} = 2.2 \text{ V}$	1,2,3 (3007)	ALL		0.4	V
Input high level <u>1/</u> voltage	V_{IH}	$V_{CC} = 5.5 \text{ V}$	1,2,3	ALL	2.2		V
Input low level <u>1/</u> voltage	V_{IL}	$V_{CC} = 4.5 \text{ V}$	1,2,3	ALL		0.8	V
High impedance output leakage current <u>2/</u>	I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_O = 5.5 \text{ V}$ $V_{IL} = 0.0 \text{ V}$, $V_{IH} = 5.0 \text{ V}$	1,2,3 (3021)	ALL		10	μA
	I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.0 \text{ V}$ $V_{IL} = 0.0 \text{ V}$, $V_{IH} = 5.0 \text{ V}$	1,2,3 (3020)		-10		
High level input current	I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_{IH} = 5.5 \text{ V}$	1,2,3 (3010)	ALL		10	μA
Low level input current	I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_{IL} = 0.0 \text{ V}$	1,2,3 (3009)	ALL	-10		μA
Supply current	I_{CC1}	$V_{CC} = 5.5 \text{ V}$, $I_{OUT} = 0 \text{ mA}$ $\overline{\text{CE}} = V_{IL}$, $f = f_{\text{max}}$ <u>3/</u>	1,2,3 (3005)	01-06, 10,11, 12,14, 15,16, 24,28, 32,36		130	mA
				07-09, 13, 17-20		160	
				21,25, 29,33		100	
				22,26, 30,34		110	
				23,27, 31,35		120	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Test conditions -55°C ≤ T _C ≤ +125°C GND = 0 V 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
Standby supply current, TTL levels	I _{CC2}	V _{CC} = 5.5 V, f = 0 CE = V _{IH} , all other inputs = V _{IL} or V _{IH}	1,2,3 (3005)	All		20	mA
Standby supply current, CMOS levels 4/	I _{CC3}	V _{CC} = 5.5 V, f = 0 CE = V _{CC} - 0.2 V, all other inputs = 0.3 V or V _{CC} - 0.2 V	1,2,3 (3005)	01-20		20	mA
				21-36		10	
Data retention current	I _{CC4}	V _{CC} = 3.0 V, f = 0 CE ≥ V _{CC} - 0.2 V, all other inputs = 0.3 V or V _{CC} - 0.2 V	1,2,3 (3005)	21-36		625	μA
Input capacitance 4/	C _I	V _{CC} = 5.0 V, V _I = 0.0 V T _C = 25°C, f = 1 MHz (see 4.4.1d)	4 (3012)	All		8	pF
Output capacitance 4/	C _O	V _{CC} = 5.0 V, V _O = 0.0 V T _C = 25°C, f = 1 MHz (see 4.4.1d)	4 (3012)	All		8	pF
Functional tests	ε/	V _{CC} = 4.5 V	7,8 (3014)	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Test conditions -55°C ≤ T _C ≤ +125°C GND = 0 V 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
Read cycle							
Address to data valid	t _{AVQV}	See figure 4 as applicable	9,10,11 (3003)	17-20, 24,28, 32,36		20	ns
				10,11, 12,13, 16,23, 27,31, 35		25	
				02,04, 06,09, 15,22, 26,30, 34		35	
				01,03, 05,08, 14,21, 25,29, 33		45	
				07		55	
Data hold from address	t _{AVQX}		9,10,11 (3003)	ALL	3		ns
CE low to data valid	t _{ELQV}		9,10,11 (3003)	17-20, 24,28, 32,36		20	ns
				10,11, 12,13, 16,23, 27,31, 35		25	
				02,04, 06,09, 15,22, 26,30, 34		35	
				01,03, 05,08, 14,21, 25,29, 33		45	
				07		55	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Test conditions -55°C ≤ T _C ≤ +125°C GND = 0 V 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
Read cycle - continued							
$\overline{\text{OE}}$ low to data valid	OLQV	See figure 4 as applicable	9,10,11 (3003)	08,09, 14,15		20	ns
				05		30	
				06,07		25	
				17,20, 23,24, 27,28		10	
				12,13, 16,21, 22,25, 26		15	
$\overline{\text{OE}}$ low to low Z <u>4/</u>	OLQX		9,10,11 (3003)	05,06, 07,08, 09,12, 13,14, 15,16, 17,20, 21-28	0		ns
$\overline{\text{OE}}$ high to high Z <u>4/</u> <u>6/</u>	OHQZ		9,10,11 (3003)	05,06, 09,14, 15		20	ns
				12,13, 16,21, 22,25, 26		15	
				17,20, 23,24, 27,28		10	
				07		30	
				08		25	
$\overline{\text{CE}}$ low to low Z <u>4/</u>	ELQX		9,10,11 (3003)	ALL	5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Test conditions -55°C ≤ T _C ≤ +125°C GND = 0 V 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
Read cycle - continued							
$\overline{\text{CE}}$ high to high Z <u>4/ 6/</u>	t _{EHQZ}	See figure 4 as applicable	9,10,11 (3003)	01-09, 14,15, 29,30, 33,34		20	ns
				10-13, 16,21, 22,25, 26,31, 35		15	
				17-20, 23,24, 27,28, 32,36		10	
$\overline{\text{CE}}$ low to power <u>4/</u> up	t _{ELPU}		9,10,11 (3003)	ALL	0		ns
$\overline{\text{CE}}$ high to power down <u>4/</u>	t _{EHPD}		9,10,11 (3003)	17-20, 24,28, 32,36		20	ns
				10-13, 16,23, 27,31, 35		25	
				01,02, 04,06, 07,08, 09,15, 22,26, 30,32, 34		35	
				03,05, 14,21, 25,29		45	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Test conditions -55°C ≤ T _C ≤ +125°C GND = 0 V 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
Write cycle							
CE low to write end	ELWH ELEH	See figure 4 as applicable	9,10,11 (3003)	17-20, 24,28, 32,36	15		ns
				10-13, 16,22, 23,26, 27,31, 35	20		
				21,25	25		
				02,04, 06,09, 15,30, 34	30		
				03,05, 14,29	35		
				01,08, 33	40		
				07	50		
Address setup to write end	AVWH AVEH		9,10,11 (3003)	17,20, 24,28, 32,36	15		ns
				22,23, 26,27	20		
				04,06, 10-13, 15,16, 21,25, 30,31, 35	25		
				02,09, 34	30		
				03,05, 14,29	35		
				01,08, 33	40		
				07	50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Test conditions -55°C ≤ T _C ≤ +125°C GND = 0 V 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
Write cycle - continued							
Address hold from write end	t _{WHAX} t _{EHAX}	See figure 4 as applicable	9,10,11 (3003)	ALL	2		ns
Address setup to write start	t _{AVWL} t _{AVEL}		9,10,11 (3003)	ALL	0		ns
WE pulse width	t _{WLWH} t _{WLEH}		9,10,11 (3003)	17-20, 24,28, 32,36	5		ns
				22,23, 26,27	0		
		01,02, 04,06, 08-12, 13,15, 16,21, 25,30, 31,33, 34,35		5			
		07		0			
		03,05, 14,29		5			
Data setup to write end	t _{DVWH} t _{DVEH}	9,10,11 (3003)	17-20, 24,28, 32,36	0		ns	
			10-13, 16,22, 23,26, 27,31, 35	5			
			02,03, 04,05, 06,08, 09,14, 15,21, 25,29, 30,34	0			
			01,07, 33	5			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Test conditions -55°C ≤ T _C ≤ +125°C GND = 0 V 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
Write cycle - continued							
Data hold from write	t _{WHDX} t _{EHDX}	See figure 4 as applicable	9,10,11 (3003)	ALL	0		ns
WE low to high Z 4/ 6/	t _{WLQZ}		9,10,11 (3003)	17-20, 24, 28, 32, 36		10	ns
				03-06, 09-16, 21-23, 25-27, 29-31, 35		15	
				01, 02, 08, 33, 34		20	
				07		25	
WE high to low Z 4/	t _{WHQX}		9,10,11 (3003)	ALL	0		ns

- 1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- 2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.
- 3/ f_{MAX} = 1/t_{AVQV}.
- 4/ Tested initially and after any design or process changes which affect that parameter, therefore shall be guaranteed to the limits specified in table I.
- 5/ Functional tests shall include the test table and other test patterns used for fault detection as approved by the qualifying activity. Inputs are tested using V_{IL} = 0.8 V, V_{IH} = 2.2 V. Outputs are measured at V_{OL} < 1.5 V, V_{OH} > 1.5 V.
- 6/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input, with C_L = 5 pF (including scope and jig). See figure 4 as applicable.

TABLE II. Electrical test requirements.

Line no.	MIL-STD-883 test requirements	Class S device ^{1/}			Class B device ^{1/ 2/}		
		Reference paragraph	Table I subgroups ^{2/}	Table III delta limits ^{3/}	Reference paragraph	Table I subgroups ^{2/}	Table III delta limits ^{3/}
1	Interim electrical parameters (method 5004)		1,7,9			1, ,9 or 2,8, ,10	
2	Static burn-in (method 1015)	4.2a 4.5.2	Required			Not required	
3	Same as line 1	4.5.3	1*	Δ			
4	Dynamic burn-in (method 1015)	4.2a 4.5.2	Required		4.2a 4.5.2	Required	
5	Same as line 1		1*	Δ			
6	Final electrical parameters (method 5004)	4.5.3	1*,2,3,4, 7,8A,8B,9, 10,11			1*,2,3,4, 7,8A,8B, 9,10,11	
7	Group A test requirements (method 5005)	4.4.1	1,2,3,4, 7,8A,8B, 9,10,11		4.4.1	1,2,3,4, 7,8A,8B, 9,10,11	
8	Group B end-point electrical parameters (method 5005)	4.4.2 4.5.3	1,2,3,7, 8A,8B,9, 10,11	Δ	4.4.2		
9	Group C end-point electrical parameters (method 5005)				4.4.3 4.5.3	1,2,3,7, 8A,8B	Δ
10	Group D end-point electrical parameters (method 5005)	4.4.4	1,2,3,7, 8A,8B		4.4.4	1,2,3,7, 8A,8B	

^{1/} Blank spaces indicate tests are not applicable.^{2/} * indicates PDA applies to subgroup 1 (see 4.2.1).^{3/} Δ indicates delta limit (see table III) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1).

Device types	01,02,10,18 33-36		03,04,11, 19,29-32		05,06, 16	07-09, 13,17, 25-28	07-09, 13,17, 25-28	12,14,15, 20-24	
Case outlines	K,L	U,N	K,L	U,N	Y,Z,U	X,Y,Z, U,N,M	T	X,Y,M	N
Terminal number	Terminal symbol								
1	A	A	A	NC	NC	A	NC	NC	NC
2	A	A	A	A	A	A	A	A	A
3	A	A	A	A	A	A	A	A	A
4	A	NC	A	A	A	A	A	A	A
5	A	A	A	A	A	A	A	A	A
6	A	A	A	A	A	A	A	A	A
7	A	A	A	A	A	A	A	A	A
8	A	A	A	A	A	A	A	A	A
9	A	A	A	A	A	A	A	A	A
10	OUT	A	A	A	A	A	A	A	A
11	WE	D _{OUT}	CE	A	A	I/O	A	A	A
12	GND	NC	GND	CE	CE ₁	I/O	NC	CE	CE
13	WE	WE	WE	NC	OE	I/O	I/O	OE	OE
14	IN	GND	I/O	GND	GND	GND	I/O	GND	GND
15	A	CE	I/O	NC	WE	I/O	I/O	WE	NC
16	A	D _{IN}	I/O	WE	I/O	I/O	GND	I/O	WE
17	A	A	I/O	I/O	I/O	I/O	NC	I/O	I/O
18	A	NC	A	I/O	I/O	I/O	I/O	I/O	I/O
19	A	A	A	I/O	I/O	I/O	I/O	I/O	I/O
20	A	A	A	I/O	CE ₂	CE	I/O	NC	I/O
21	A	A	A	A	NC	A	I/O	NC	A
22	A	A	A	A	A	OE	I/O	A	A
23	A	A	A	A	A	A	CE	A	A
24	CC	A	V _{CC}	A	A	A	A	A	A
25	A	A	A	A	A	A	OE	A	A
26	A	NC	A	A	A	A	NC	A	A
27	A	A	NC	A	A	WE	A	A	NC
28	A	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	A	V _{CC}	V _{CC}
29	A	A	A	A	A	A	A	A	A
30	A	A	A	A	A	A	A	A	A
31	A	A	A	A	A	A	A	A	A
32	A	A	A	A	A	A	A	A	A

NC = no connection

FIGURE 1. Terminal connections.

Device types 01-04, 10, 11, 18, 19, 29-36

Mode	$\overline{CE}$	$\overline{WE}$	Inputs/ outputs	Power
Not selected	High	X	High Z	Standby
Read	Low	High	Data out	Active
Write	Low	Low	Data in	Active

Device types 05, 06, 16

Mode	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Inputs/ outputs	Power
Not selected	High	X	X	X	High Z	Standby
Not selected	X	High	X	X	High Z	Standby
Read	Low	Low	High	Low	Data out	Active
Write	Low	Low	Low	X	Data in	Active
Output disable	Low	Low	High	High	High Z	Active

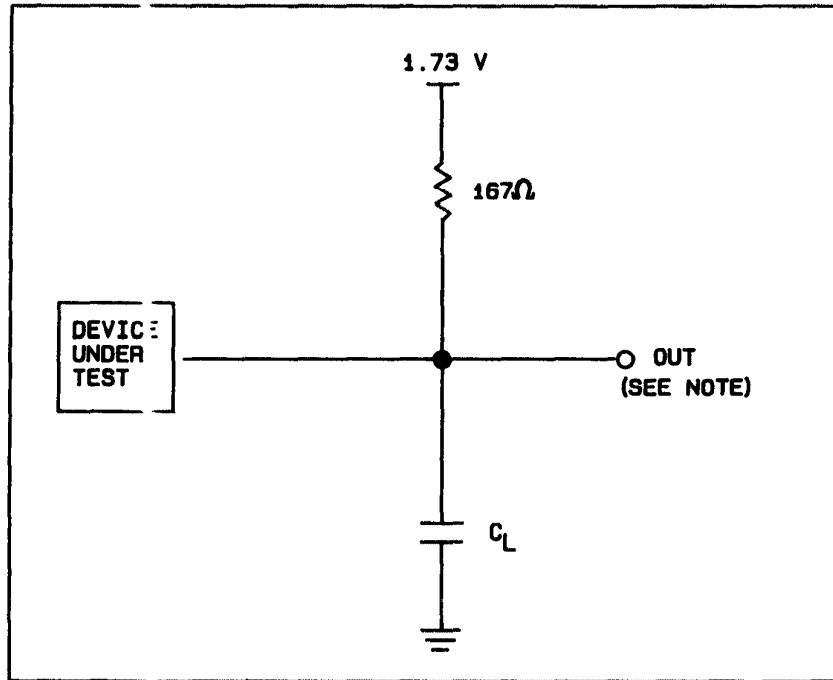
Device types 07, 08, 09, 12, 13, 14, 15, 17, 20-28

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/ outputs	Power
Not selected	High	X	X	High Z	Standby
Read	Low	High	Low	Data out	Active
Write	Low	Low	X	Data in	Active
Output disable	Low	High	High	High Z	Active

NOTES:

1. X = Don't care
2. High Z = High-impedance state

FIGURE 2. Truth tables.



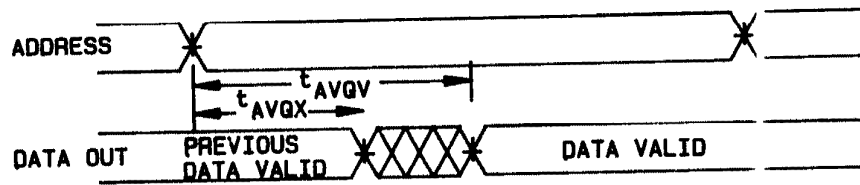
NOTE: $C_L = 30$ pF minimum, including jig and probe capacitance, t_{OHQZ} , t_{EHQZ} , and t_{WLQZ} are specified with $C_L = 5$ pF.

AC test conditions

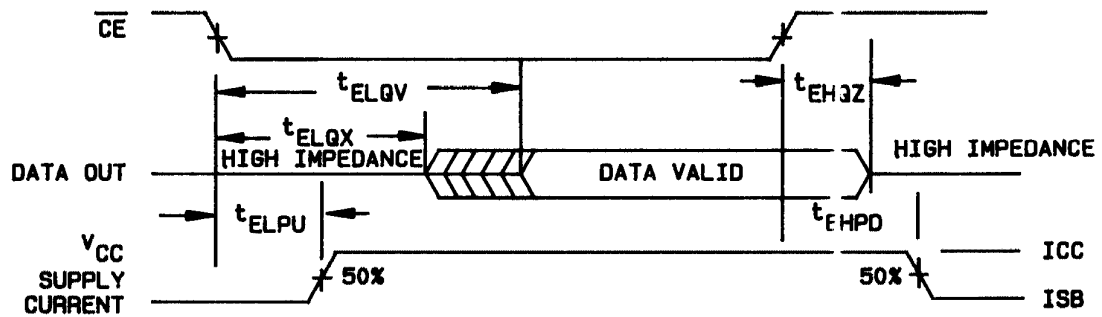
Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and test conditions.

Read cycle no. 1 for all device types



Read cycle no. 2 for device types 01, 02, 03, 04, 10, and 11



Read cycle no. 2 for device types 05, 06, and 16

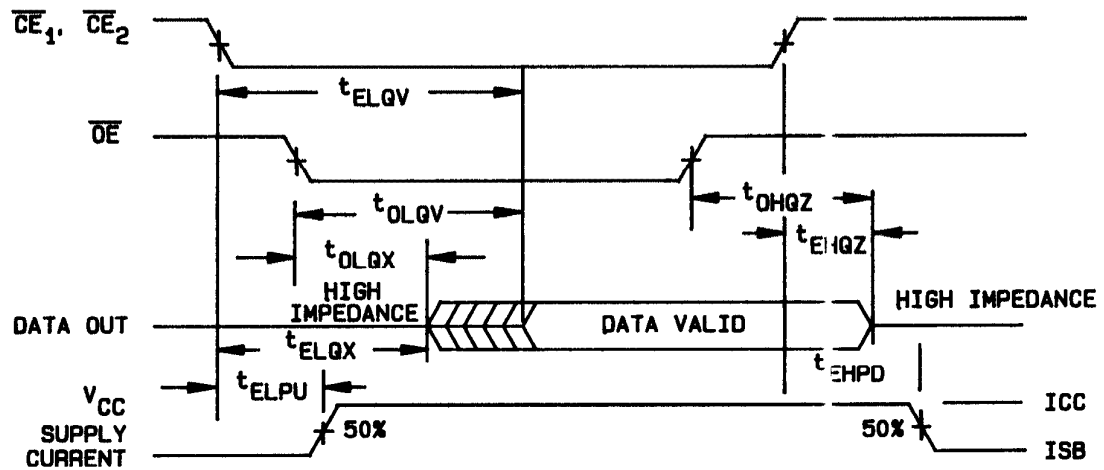
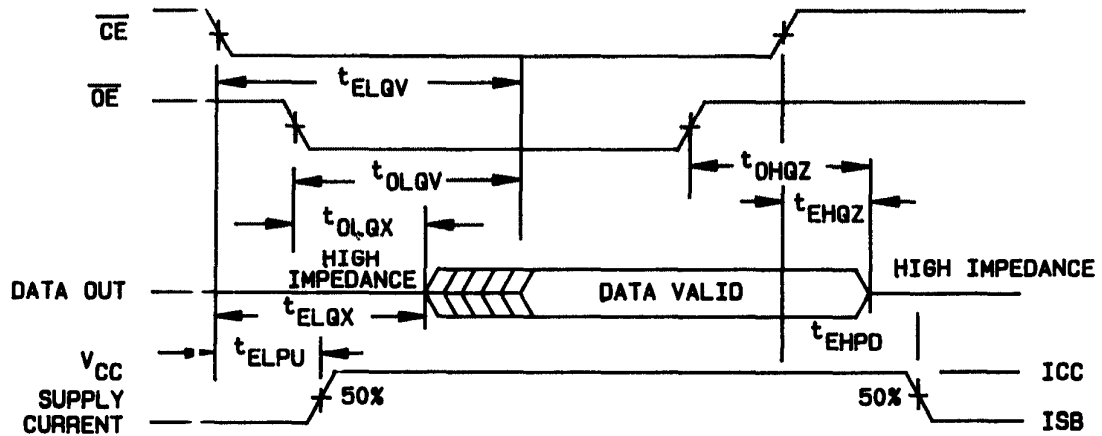


FIGURE 4. Switching time waveforms.

Read cycle no. 2 for device types 07, 08, 09, 12, 13, 14, and 15



Write cycle no. 1 ($\overline{WE}$ controlled) for device types 01, 02, 03, 04, 07, 08, 09, 10, 11, 12, 13, 14, and 15

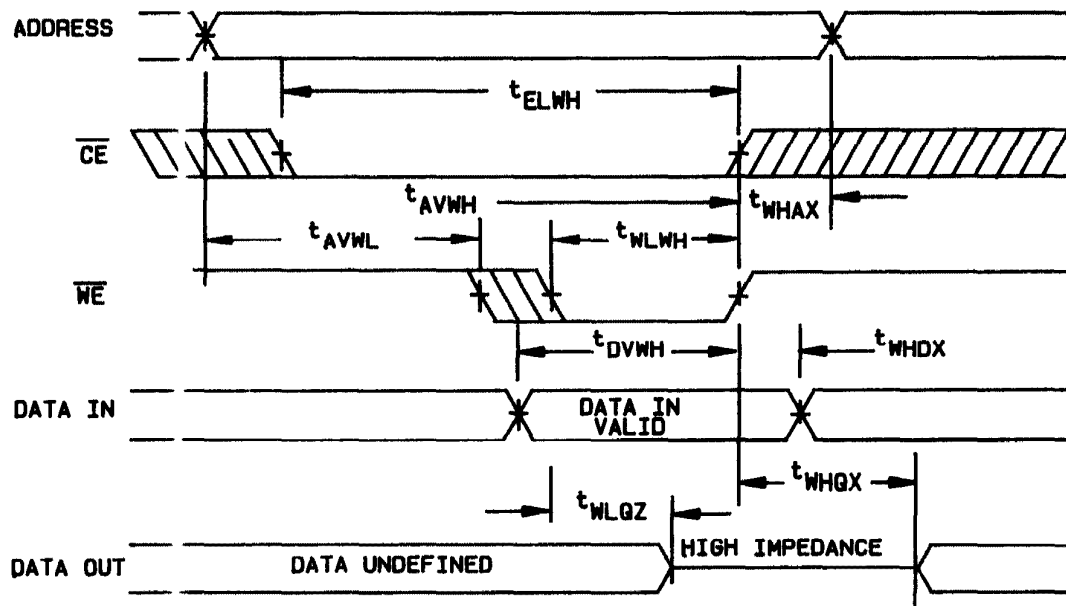
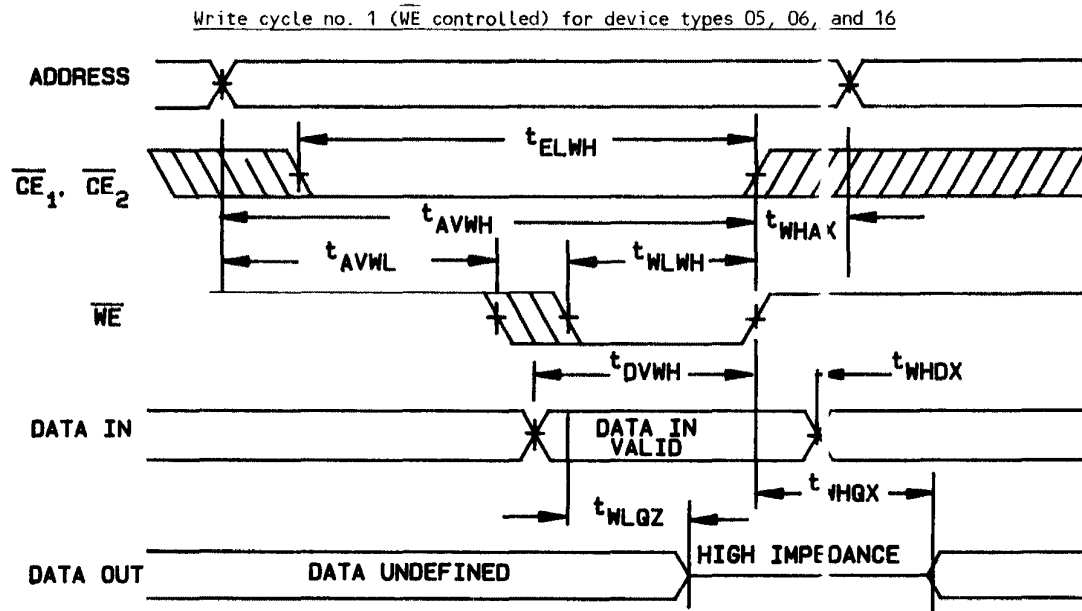


FIGURE 4. Switching time waveforms - Continued.



Write cycle no. 2 ($\overline{CE}$ controlled) for device types 01, 02, 13, 04, 07, 08, 09, 10, 11, 12, 13, 14, and 15

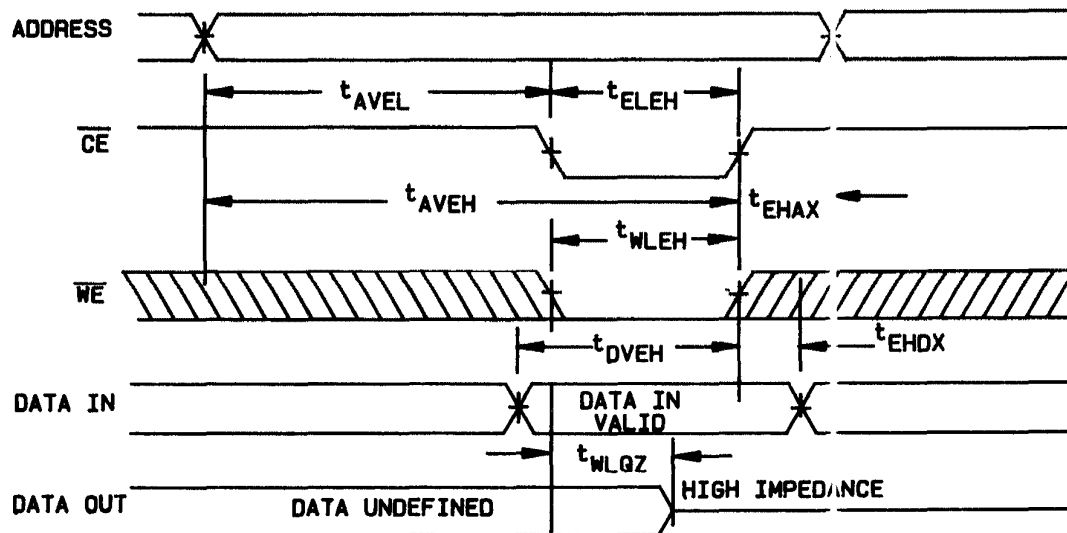
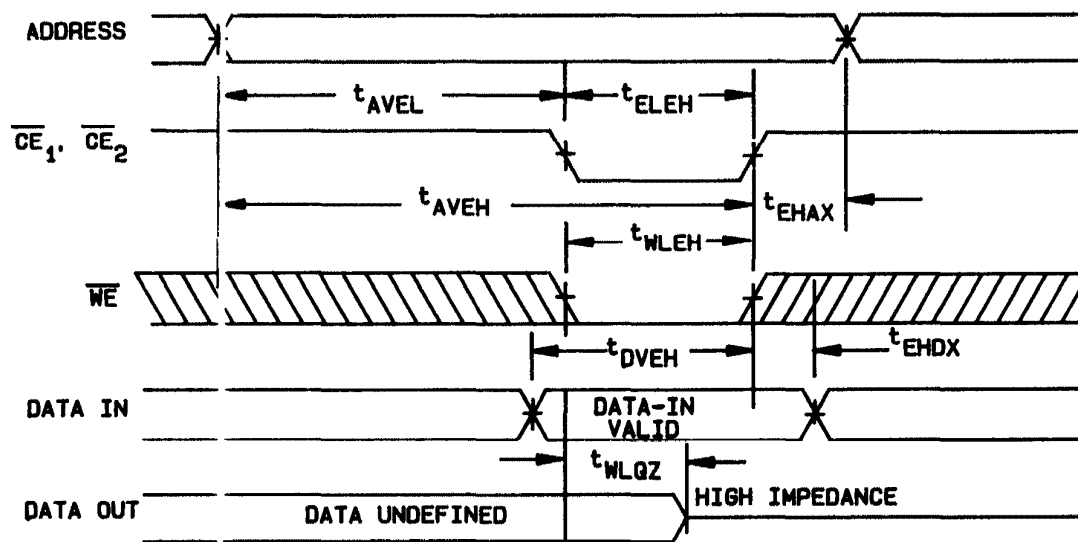


FIGURE 4. Switching time waveforms - Continued.

Write cycle no. 2 ($\overline{CE}$ controlled) for device types 05, 06, and 16



NOTES ON READ OPERATION:

1. $\overline{WE}$ is high for read cycles.
2. For read cycle no. 1, device is continuously selected, $\overline{CE}$, $\overline{OE} = V_{IL}$.
3. For read cycle no. 2, addresses are valid prior to or coincident with $\overline{CE}$ transition low.
4. At any given temperature and voltage condition, t_{EHQZ} maximum is less than t_{ELQX} minimum.

NOTES ON WRITE OPERATION:

1. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CE}$ switches low coincident with or after $\overline{WE}$ switches low, the outputs will stay in a high impedance state.
3. If $\overline{CE}$ switches high coincident with or after $\overline{WE}$ switches high, the outputs will stay in a high impedance state.
4. A write occurs during the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

FIGURE 4. Switching time waveforms - Continued.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.5). Qualification data for subgroups 7 through 11 shall be attributes only.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection. If a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type of this specification, the slower device type may be part I qualified without further qualification testing. At the manufacturer's request, the slower device types will be added to the QPL.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be performed in accordance with table II herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_I , C_O measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. Procedures and circuits shall be submitted to DESC-ECS for class M devices. For classes B and S, the procedures and circuits shall be submitted to the qualifying activity. For classes Q and V, the procedures and circuits shall be submitted to DESC-ECS and shall be as indicated in the QM plan and will be under the control of the device manufacturer's technical review board (TRB). Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

- a. Class S steady-state life test circuits shall be conducted using test condition D and the circuit described in 4.2b herein, or equivalent as approved by the qualifying activity.
- b. Class S only, end-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 5 of group B inspection and shall consist of tests specified in table III herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table III herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) shall be conducted using test condition D and as specified in 4.5.2 herein using a circuit as described in 4.2c herein, or equivalent as approved by the qualifying activity.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Burn-in and life test cool down procedures. Procedures shall be in accordance with method 1015 of MIL-STD-883.

4.5.3 Delta measurements. Delta measurements, as specified in table II, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table III.

TABLE III. Delta limits at +25°C.

Parameter ^{1/}	Device types
	ALL
I_{CC2}	±1 mA

^{1/} The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ).

4.5.4 Quiescent supply current test. When performing quiescent supply current measurements, the meter shall be placed so that all currents flow through the meter.

4.6 Data reporting. When specified in the purchase order or contract, a copy of the following data, as applicable, shall be supplied.

- Attributes data for all screening tests (see 4.2) and variables data for all dynamic burn-in, and steady-state life tests.
- A copy of each radiograph.
- The quality conformance inspection data (see 4.4).
- Parameter distribution data on parameters evaluated during burn-in.
- Final electrical parameters data (see 4.2c).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents must specify the following:

- Part or Identifying Number (PIN) (see 6.6).
- Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- Requirement for certificate of compliance, if applicable.

- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths, or lead forming, if applicable. These requirements shall not affect the PIN. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- h. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

C_i	-----	Input, output terminal-to-GND capacitance.
C_o	-----	Ground zero voltage potential.
I_{CC}	-----	Quiescent supply current.
T_c	-----	Case temperature.
V_{CC}	-----	Positive supply voltage.

6.4 Logistic support. Lead materials and finishes (see 3.1.5) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class S for National Aeronautics and Space Administration or class B for Department of Defense (see 1.2.2), lead finish A. Longer length leads and lead forming shall not affect the PIN.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01,02,10,18,33,34,35,36	7C197; MT5C2561
03,04,11,19,29,30,31,32	7C194; MT5C2564
05,06,16	7C196
07,08,09,13,17,25-28	7C198, 7C199; MT5C2568
12,14,15,20-24	MT5C2565

6.6 Part or Identifying number (PIN). The PIN shall be in accordance with MIL-I-38510, and as specified herein.

6.7 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protective devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment, tools, and operator.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent, if practical.

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).30.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).30.2.1 March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially, for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

APPENDIX

30.3 Algorithm C (pattern 3).30.3.1 XY march

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially, for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
- Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
- Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

MIL-M-38510/293A

CONCLUDING MATERIAL

Custodians:

Army - ER
Navy - EC
Air Force - 17

Review activities:

Army - AR, MI
Navy - TD
Air Force - 19, 85 99
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC

Preparing activity:

Air Force - 17

Agent:

DLA - ES

(Project 5962-1233)