

INCH POUND

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SUPERSEDING
MIL-M-38510/291A
12 September 1988

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, CMOS 16,384 BIT STATIC RANDOM ACCESS MEMORY (RAM) MONOLITHIC SILICON

Inactive for new design after 28 July 1995.

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS, 16,384 bit static random access memory microcircuits. Two product assurance classes and a choice of case outlines, lead finishes, and radiation hardness assured (RHA) products are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The complete PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

<u>Device type</u>	<u>Circuit organization</u>	<u>Access time</u>
01	2,048 words / 8 bits	150 ns
02	2,048 words / 8 bits	210 ns (synchronous)
03	16,384 words / 1 bit	85 ns
04	2,048 words / 8 bits	90 ns
05	2,048 words / 8 bits	200 ns
06	16,384 words / 1 bit	45 ns
07 (RHA)	16,384 words / 1 bit	150 ns
08 (RHA)	16,384 words / 1 bit	175 ns
09	16,384 words / 1 bit	70 ns
10	2,048 words / 8 bits	70 ns

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
J	GDIP1-T24, CDIP2-T24	24	Dual in line package
R	GDIP1-T20, CDIP2-T20	20	Dual in line package
X	CQCC1-N32	32	Leadless chip carrier package
Y	CQCC3-N20	20	Leadless chip carrier package
Z	CDFP4-F24	24	Flat package

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to bipolar@dsccl.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil>.

1.2.4 RHA level. Radiation hardness levels will be as defined in MIL-PRF-38535.

1.3 Absolute maximum ratings (device types 01 through 10).

Supply voltage range ($V_{CC}-V_{SS}$).....	-0.3 V dc to +7.0 V dc
Input voltage range.....	$(V_{SS} - 0.3 \text{ V}) \leq V_I \leq (V_{CC} + 0.3 \text{ V})$
Storage temperature range	-65°C to +150°C
Maximum dc output current	50 mA
Maximum power dissipation (P_D)	1 W
Lead temperature (soldering, 5 seconds)	+270°C
Junction temperature (T_J) ^{1/}	+150°C
Thermal resistance, junction-to-case (θ_{JC}) :	
Case J, R, X, Y, and Z	(See MIL-STD-1835)

1.4 Recommended operating conditions.

Supply voltages:

V_{CCDR} (data retention supply voltage):

Device types 01 through 06 and device types

09 and 10 2.0 V dc

Device types 07 and 08 3.0 V dc

V_{CC} 4.5 V dc minimum to 5.5 V dc maximum

V_{SS} 0 V dc

High level input voltage (V_{IH}) (all inputs):

Device types 01, 03 through 06 and device

Types 09 and 10..... $V_{CC} - 2.3 \text{ V}$ to $V_{CC} + 0.3 \text{ V}$

Device type 02..... $V_{CC} - 2.1 \text{ V}$ to $V_{CC} + 0.3 \text{ V}$

Device type 07..... $V_{CC} - 1.5 \text{ V}$ to $V_{CC} + 0.3 \text{ V}$

Device type 08..... 2.3 V to $V_{CC} + 0.3 \text{ V}$

Low level input voltage (V_{IL}) (all inputs):

All device types $V_{SS} - 0.3 \text{ V}$ to +0.8 V

Case operating temperature range (T_C) -55°C to +125°C

2.0 APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and standards. The following specifications and standards form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

^{1/} Maximum junction temperature will not be exceeded except for allowable short duration burn in screening conditions in accordance with method 5004 of MIL-STD-883.

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein. Die bonding may be performed using conductive silver paste or other epoxy. All epoxies must be qualified to test method 5011 of MIL-STD-883. Laser scribing shall be allowed only for SOS technology product and only to the backside of the wafer.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Block diagrams. The block diagrams shall be as specified on figure 2.

3.3.3 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.

3.3.4 Truth tables. The truth tables shall be as specified on figure 3.

3.3.5 Functional tests. The functional tests used to test this device are contained in Appendix A. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be documented, maintained, and available to the acquiring activity and qualifying activity upon request.

3.3.5 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.5.1 Post irradiation performance characteristics. The electrical performance characteristics of the RHA devices at the RHA levels are as specified in table I and apply at an ambient temperature of $+25^{\circ}\text{C} \pm 5^{\circ}\text{C}$.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.7.1 Serialization. All class S devices shall be serialized in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics (device types 01 through 06 and device types 09 and 10).

Test	Symbol	Conditions V _{SS} = 0 V, V _{CC} = 5.5 V -55°C ≤ T _C ≤ +125°C unless otherwise specified		Device types	Limits		Unit	
					Min	Max		
Operating supply current	I _{CC1}	Addresses cycling f = 1 MHz CE = V _{IL} , I ₀ = 0 (outputs are open)		01,04,05, 10		70	mA	
				02		10		
				03,09		50		
				06		100		
Standby supply current	I _{CC2}	Addresses stable CE = V _{CC} - 0.3 V, I ₀ = 0		01,02,03, 04,05,09, 10		100	μA	
	I _{CC3}			Address stable CE = V _{IH} , I ₀ = 0		03,09		5
		01,04,05, 06,10				10		
	Data retention supply current	I _{CC4}	V _{CC} = 2.0 V, I ₀ = 0 CE = V _{CC} - 0.3 V		01,02,03, 04,05,09, 10		50	μA
Low level output voltage	V _{OL}	V _{CC} = 4.5 V	I _{OL} = 4.0 mA	01,04,05,06 10		0.4	V	
			I _{OL} = 3.2 mA	02		0.4		
			I _{OL} = 8.0 mA	03,09		0.4		
High level output voltage	V _{OH}	V _{CC} = 4.5 V	I _{OH} = -1.0 mA	01,02,04, 05,06,10	2.4		V	
			I _{OH} = -4.0 mA	03,09	2.4			
Input leakage current	I _{IL}	V _{IN} = GND		01,04,05, 10	-1	1	μA	
	I _{IH}	V _{IN} = 5.5 V		02,03,09	-1	1		
				06	-10	10		
High impedance output leakage current	I _{OLZ}	V _{OUT} = GND	CE = V _{IH}	01,03,04, 05,09,10	-1	1	μA	
	I _{OHZ}	V _{OUT} = 5.5 V		02	-1	1		
				06	-20	20		
Input capacitance	C _I	T _C = +25°C, V _{CC} = GND V _{IN} = GND, f = 1 MHz		01,03,04, 05,06,09,10		10	pF	
				02		12		

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device types 01 through 06 and device types 09 and 10).– Continued.

Test	Symbol	Conditions $V_{SS} = 0\text{ V}$, $V_{CC} = 5.5\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Output capacitance	C_O	$T_C = +25^{\circ}\text{C}$, $V_{CC} = \text{GND}$ $V_{IN} = \text{GND}$, $f = 1\text{ MHz}$	01,03,04, 05,06,09,10		12	pF
			02		14	
Read or write cycle time	t_{AVAV}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ See figure 4	01	150		ns
			03	85		
			04	90		
			05	200		
			06	45		
			09	70		
			10	70		
Address access time	t_{AVQV}		01		150	ns
			02		200	
			03		85	
			04		90	
			05		200	
			06		45	
			09		70	
			10		70	
Chip enable access time	t_{ELQV}		01		150	ns
			02		200	
			03		85	
			04		90	
			05		200	
			06		45	
			09		70	
			10		70	
Chip disable to output disable time	t_{EHQZ}		01,04		50	ns
			02		80	
			03		40	
			05		60	
			06		25	
			09		40	
			10		40	
Output hold after address change	t_{AVQX}		01,05	0		ns
			06	3		
			03,04, 09,10	5		
Chip enable to output active	t_{ELQX}		01,05	0		ns
			02	10		
			06	3		
			03,04, 09,10	5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device types 01 through 06 and device types 09 and 10).– Continued.

Test	Symbol	Conditions V _{SS} = 0 V, V _{CC} = 5.5 V -55°C ≤ T _C ≤ +125°C unless otherwise specified	Device types	Limits		Unit			
				Min	Max				
Write pulse width	t _{WLWH}	V _{CC} = 4.5 V to 5.5 V See figure 4	01	90		ns			
			02	200					
			03	45					
			04	55					
			05	120					
			06	30					
			09	40					
			10	40					
			Chip enable to end-of-write	t _{ELWH}	01		90		ns
					02		200		
03	65								
04	55								
05	120								
06	35								
09	55								
10	45								
Data setup to end-of-write	t _{DVWH}		01	50		ns			
			02	80					
			03	35					
			04	30					
		05	70						
		06	25						
		09	30						
		10	30						
Data hold after end-of-write	t _{WHDX}	01,04,05	15		ns				
		02	10						
		03,09	0						
		06	5						
		10	10						
Address setup before write low	t _{AVWL}	01,04,05, 10	10		ns				
		06	5						
		03,09	0						
Address setup to end-of-write	t _{AVWH}	01	120		ns				
		03	65						
		04	80						
		05	140						
		06	35						
		09	55						
		10	50						
Write recovery time	t _{WHAX}	01,04,05, 10	10		ns				
		06	5						
		03,09	0						

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device types 01 through 06 and device types 09 and 10).– Continued.

Test	Symbol	Conditions V _{SS} = 0 V, V _{CC} = 5.5 V -55°C ≤ T _C ≤ +125°C unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Output enable access time	t _{OLQV}	V _{CC} = 4.5 V to 5.5 V See figure 4	01		75	ns
			02		80	
			04		65	
			05		100	
			10		50	
Output enable to output active	t _{OLQX}		01,04,05	0		ns
			02	10		
			10	5		
Output enable to output active	t _{OHQZ}		01,05		60	ns
			02		80	
			04		40	
			10		35	
Address to chip enable setup time	t _{AVEL}		02	0		ns
Address to chip enable hold time	t _{ELAX}	02	50		ns	
Chip enable pulse negative width	t _{ELEH}	02	200		ns	
Chip enable pulse positive width	t _{EHEL}	02	80		ns	
Write enable pulse setup time	t _{WLEH}	02	200		ns	
Read or write cycle time	t _{ELEL}	02	280		ns	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device types 07 and 08).

Test	Symbol	Conditions $V_{SS} = 0\text{ V}$, $V_{CC} = 5.5\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Low level output voltage	V_{OL}	$V_{CC} = 4.5\text{ V}$; $I_{OL} = 5.0\text{ mA}$	07 08		0.4 0.4	V
High level output voltage	V_{OH}	$V_{CC} = 4.5\text{ V}$; $I_{OH} = -5.0\text{ mA}$	07 08	4.0 4.0		V
Input leakage current	I_{IH}	$V_{CC} = 5.5\text{ V}$; $V_{IN} = 5.5\text{ V}$	07 08		1.0 1.0	μA
Input leakage current	I_{IL}	$V_{CC} = 5.5\text{ V}$; $V_{IN} = \text{GND}$	07 08		-1.0 -1.0	μA
High impedance output leakage	I_{OHZ}	$V_{CC} = 5.5\text{ V}$	07 08		10.0 10.0	μA
High impedance	I_{OLZ}	$V_{CC} = 5.5\text{ V}$	07 08		-10.0 -10.0	μA
Standby supply	I_{CC}	$V_{CC} = 5.5\text{ V}$	07 08		200 5	μA mA
Data retention supply voltage	V_{CCDR}	$V_{CC} = 3.0\text{ V}$ minimum (see power down test in table III)	07 08	3.0 3.0		V
Operating current	I_{CCOP}	$T_C = +25^{\circ}\text{C}$, $V_{CC} = 5.5\text{ V}$ $f = 1\text{ MHz}$	07 08		6 6	mA
Data retention quiescent supply current	I_{CCDR}	$V_{CC} = 3.0\text{ V}$; $I_O = 0$; $V_I = V_{CC}$ or GND	07 08		100 100	μA
Input capacitance	C_I	$V_{CC} = 5.5\text{ V}$; $V_{IN} = V_{CC}$ or GND $f = 1\text{ MHz}$	07 08		8 8	pF
Address access time	t_{AVQV}	See table III	07 08		150 175	ns
Chip enable access	t_{ELQV}		07 08		150 175	ns
Read cycle time	t_{AVAV}		07 08	150 175		ns
Chip enable output time	t_{ELQX}		07 08	20 40		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device types 07 and 08) – Continued.

Test	Symbol	Conditions $V_{SS} = 0\text{ V}$, $V_{CC} = 5.5\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Chip enable output disable	t_{EHQZ} 1/	See table III	07 08		25 50	ns
Chip enable pulse negative width	t_{ELEH}		07 08	100 125		ns
Chip disable output hold time	t_{EHQX} 1/		07 08	20 40		ns
Address setup time	t_{AVEL}		07 08	0 0		ns
Address invalid output hold time	t_{AXQX} 1/		07 08	40 60		ns
Write enable pulse width	t_{WLWH}		07 08	75 100		ns
Write enable pulse setup time	t_{WLEH}		07 08	100 125		ns
Address setup time	t_{AVWL}		07 08	10 10		ns
Chip enable to end-of-write	t_{ELWH}	See table III $I_O = 0$; $V_I = V_{CC}$ or GND	07 08	100 125		ns
Write disable output enable time	t_{WHQX} 1/	See table III	07 08	0 0		ns
Address valid to end-of-write	t_{AVWH}		07 08	100 125		ns
Address hold time	t_{WHAX}		07 08	20 25		ns
Address hold time	t_{EHAX}		07 08	0 0		ns
Address valid to end-of-write	t_{AVEH}		07 08	100 125		ns
Write enable output disable time	t_{WLQZ} 1/		07 08		25 50	ns
Data setup time	t_{DVWH}		07 08	75 100		ns
Data hold time	t_{WHDX}		07 08	20 20		ns
Data setup time	t_{DVEH}		07 08	75 100		ns
Data hold time	t_{EHDX}		07 08	0 0		ns

1/ This parameter is guaranteed but not tested.

TABLE II. Electrical test requirements

Line No.	MIL-PRF-38535 Test requirements	Class S devices <u>1/</u> <u>2/</u>					Class B devices <u>1/</u> <u>2/</u>				
		Reference paragraph	Table III <u>3/</u> subgroups	Table IV <u>4/</u> delta limits	Test circuit figure	Table V <u>5/</u> subgroups	Reference paragraph	Table III <u>3/</u> subgroups	Table IV <u>4/</u> delta limits	Test circuit figure	Table V <u>5/</u> subgroups
1	Interim electrical parameters		1					2, 8* (hot only) 10			
2	Static burn in	4.3b									
3	Same as <u>6/</u> line 1		1*	Δ							
4	Dynamic burn in	4.3b	<u>7/</u>				4.3b	<u>7/</u>			
5	Same as line 1	4.3d	1*	Δ			4.3d	1*	Δ		
6	Final electrical parameters		1*, 2, 3, 8, 9, 10, 11					1*, 2, 3, 7, 8, 9, 10, 11,			
7	Group A test requirements	4.4.1	1, 2, 3, 4, 8, 9, 10, 11, 12				4.4.1	1, 2, 3, 4, 7, 8, 9, 10, 11			
8	Group B end-point electrical test parameters when using the method 5005 QCI option.	4.4.2	1, 2, 4, 8, 9, 10, 11	Δ			4.4.2 4.5.2	1 <u>8/</u>			
9	Group C end point electrical test parameters		1, 2, 4, 8, 9, 10, 11				4.4.3	1, 7, 9	Δ		
10	Group D end point electrical test parameters,	4.4.4	1, 2, 3				4.4.4	1, 7, 9			
11	Group E end point electrical test parameters,	4.5.4			Table V	1, 2	4.5.4				1, 2

1/ Blank spaces indicate tests are not applicable.

2/ For subgroups 9, 10, and 11, only the worst value measured per device need be recorded when variables data is required (e.g., during qualification).

3/ (*) indicates PDA applies to subgroup 1.

4/ (Δ) indicates delta limit shall be required, and delta values shall be computed with reference to the previous interim electrical parameters (see 4.5.2).

5/ As applicable in group E of MIL-STD-883.

6/ The device manufacturer may, at his option, delete line number 3.

7/ The device manufacturer may, at his option, either perform delta measurements, or within 24 hours after burn in (removal of temperature or bias), perform the final electrical parameter measurements, subgroup A1.

8/ Applies to electrostatic discharge sensitivity tests.

TABLE III. Group A inspection for device types 01 and 05. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20	21	22	23	24	25	26	28	29	32	Measured terminal	Test limits		Unit					
			Case J	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		Min	Max						
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	DQ0	DQ1	DQ2	V _{SS}	DQ3	DQ4	DQ5	DQ6	DQ7	CE	A10	OE	WE	A9	A8	V _{CC}									
1 T _C =+25°C	I _{CC1}	3005	1	2/	2/	2/	2/	2/	2/	2/	2/	3/	3/	3/	GND	3/	3/	3/	3/	3/	2/	2/	2/	2/	2/	2/	5.5 V	V _{CC}			mA					
	I _{CC2}		2	4/	4/	4/	4/	4/	4/	4/	4/	4/	"	"	"	"	"	"	"	"	4/	4/	4/	4/	4/	4/	"	"			100					
	I _{CC3}		3	5/	5/	5/	5/	5/	5/	5/	5/	5/	"	"	"	"	"	"	"	"	5/	5/	5/	5/	5/	5/	"	"			10					
	I _{CC4}		4	6/	6/	6/	6/	6/	6/	6/	6/	6/	"	"	"	"	"	"	"	"	6/	6/	6/	6/	6/	6/	2.0 V	"	90	100	μA					
	I _{IL}	3009	5	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	A7	-2		μA					
	6		5.5 V	GND	5.5 V	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A6								
	7		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A5								
	8		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A4								
	9		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A3								
	10		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A2								
	11		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A1								
	12		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A0								
	13		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ0								
	14		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ1								
	15		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ2								
	16		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ3								
	17		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ4								
	18		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ5								
	19		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ6								
	20		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ7								
	21		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CE								
	22		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A10								
	23		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	OE								
	24		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	WE								
	25		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				A9				
	26		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				A8				
	28		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
	29		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
	32		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			I _{IH}	3010	27	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	"	GND	GND	GND	GND	GND	GND	GND	GND	GND	"	"				"	A7	2		
28		GND	5.5 V		GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A6								
29		"	GND		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A5								
30		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A4								
31		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A3								
32		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A2								
33		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A1								
34		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A0								
35		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ0								
36		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ1								
37		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ2								
38		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ3								
39		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ4								
40		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ5								
41		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ6								
42		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ7								
43		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CE								
44		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A10								
45		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	OE								
46		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	WE							
47		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A9							
48		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A8							

See footnotes at end of device types 01 and 05.

TABLE III. Group A inspection for device types 01 and 05 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20	21	22	23	24	25	26	28	29	32	Measured terminal	Test limits		Unit	
			Case J	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		Min	Max		
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	DQ0	DQ1	DQ2	V _{SS}	DQ3	DQ4	DQ5	DQ6	DQ7	$\overline{\text{CE}}$	A10	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	A8	V _{CC}					
1 T _C =+25°C	I _{OLZ}	3020	49									GND	5.5 V	5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	2.2 V		2.2 V	5.5 V		5.5 V	DQ0		-10	μA		
			50										5.5 V	GND	5.5 V												DQ1					
			51										5.5 V	GND	5.5 V												DQ2					
			52												5.5 V	GND											DQ3					
			53													5.5 V	GND											DQ4				
			54														5.5 V	GND										DQ5				
			55															5.5 V	GND									DQ6				
			56																5.5 V	GND								DQ7				
	I _{OHZ}	3021	57										GND	GND	GND		GND	GND	GND	GND								DQ0		10		
			58										5.5 V	GND	5.5 V													DQ1				
			59										GND	5.5 V	GND													DQ2				
			60												5.5 V	GND												DQ3				
			61													5.5 V	GND											DQ4				
			62														5.5 V	GND										DQ5				
			63															5.5 V	GND									DQ6				
			64																5.5 V	GND	5.5 V	5.5 V						DQ7				
	V _{OL} Z/	3007	65	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/		8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	4.5 V	DQ0		0.4	V
			66																									DQ1				
			67																									DQ2				
			68																									DQ3				
			69																									DQ4				
			70																									DQ5				
			71																									DQ6				
			72																									DQ7				
	V _{OH} Z/	3006	73	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/		9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/		DQ0		2.4	
			74																									DQ1				
			75																									DQ2				
			76																									DQ3				
			77																									DQ4				
			78																									DQ5				
			79																									DQ6				
			80																									DQ7				
2	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = +125°C.																															
3	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = -55°C.																															
4 T _C =+25°C	C _I C _O	3012	81 82	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	GND	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	All inputs All outputs		10	pF pF	
9 T _C =+25°C	NOT	See	83	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/		11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	All	11/	11/	ns	
	WRITE/	fig. 7	84	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/		11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	5.5 V	outputs	11/	11/	ns	
	WRITE/	fig. 8	85	12/	12/	12/	12/	12/	12/	12/	12/	12/	12/	12/		12/	12/	12/	12/	12/	12/	12/	12/	12/	12/	12/	4.5 V	All	12/	12/	ns	
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = +125°C.																															
11	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = -55°C.																															

See footnotes at end of device types 01 and 05.

- 1/ Pins not designated may be "high" level logic, or "low" level logic. Exceptions are the input/output terminals, in the output condition, may be open.
- 2/ All inputs levels and timing edges are set to table I limits with read cycle timing; $V_{IL} = 0.4$ V and $V_{IH} = 2.2$ V for device types 01 and 05.
- 3/ Outputs loaded with load as specified on figure 5.
- 4/ Test is done with addresses held stable, and all inputs held at $V_{IL} = 0.4$ V and $V_{IH} = 2.2$ V for device types 01 and 05.
- 5/ Test is done with addresses held stable, and all inputs held at $V_{IL} = 0.4$ V and $V_{IH} = V_{CC} - 0.3$ V.
- 6/ Test is done with addresses held stable, $V_{CC} = 2.0$ V, and all other inputs held at V_{CC} . The data retention test condition shall be held for 250 milliseconds before measurements. The data must remain valid after power is returned to device.
- 7/ For V_{OL} or V_{OH} , testing all terminals, only the worst case variables data shall be recorded, and variables data for each failed terminal. Attributes data otherwise.
- 8/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels and forcing current during measurement shall be $V_{IL} = 0.8$ V, $I_{OL} = 2.0$ mA.
- 9/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels and forcing current during measurement shall be $V_{IH} = 2.2$ V, $I_{OH} = -1.0$ mA.
- 10/ See 4.4.1c.
- 11/ Since the object of the NOT WRITE pattern (see figure 7) is to verify that the device may not be written into when it is disabled, the waveforms shown on figure 4 may be applied using nominal timing. The outputs shall be loaded with the load specified on figure 5.
- 12/ Timing waveforms shown on figure 4 shall be applied while performing a WRITE/WRITE address complement pattern (see figure 8). This procedure ensures that the following parameters meet the specified limits:

Parameter		Limits				Unit
		Device type 01		Device type 05		
		Min	Max	Min	Max	
t _{AVAV}		150	---	200	---	ns
t _{AVQV}		---	150	---	200	"
t _{AVQX}		0	---	0	---	"
t _{OLQX}		0	---	0	---	"
t _{OLQV}		---	75	100	---	"
t _{OHQZ}		---	60	---	60	"
t _{ELQV}		150	---	---	200	"
t _{ELQX}		0	---	0	---	"
t _{EHQZ}		---	50	---	60	"
t _{AVEL}		---	---	---	---	"
t _{ELAX}		---	---	---	---	"
t _{ELEH}		---	---	---	---	"
V _{IL}		0.0		0.0		V
V _{IH}		2.2		2.2		"
Output compare level	V _{OL}	0.4		0.4		"
	V _{OH}	2.4		2.4		"
Read cycle timing						

Parameter		Limits				Unit
		Device type 01		Device type 05		
		Min	Max	Min	Max	
t _{WHAV}		10	---	10	---	ns
t _{ELWH}		90	---	120	---	"
t _{AVWH}		120	---	140	---	"
t _{AWWL}		10	---	10	---	"
t _{WLWH}		90	---	120	---	"
t _{DVWH}		50	---	70	---	"
t _{WHDX}		15	---	15	---	"
t _{WLEH}		---	---	---	---	"
V _{IL}		0.0		0.0		V
V _{IH}		2.2		2.2		"
Output compare level	V _{OL}	0.4		0.4		"
	V _{OH}	2.4		2.4		"
Write cycle timing						

The output shall be loaded with the load specified on figure 5. If the test equipment limitations prevent the simultaneous application or verification of all the specified parameters, multiple executions of the algorithm may be required to effect the measurement of all dynamic parameters.

TABLE III. Group A inspection for device type 02. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20	21	22	23	24	25	26	28	29	32	Algorithm	Measured terminal	Test limits		Unit		
			Case J	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24			Min	Max			
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	DQ0	DQ1	DQ2	V _{SS}	DQ3	DQ4	DQ5	DQ6	DQ7	$\overline{\text{CE}}$	A10	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	A8	V _{CC}							
1 T _C =+25°C	I _{CC1}	3005	1	2/ GND	2/ GND	2/ GND	2/ GND	2/ GND	2/ GND	2/ GND	2/ GND	3/ "	3/ "	3/ "	GND	3/ "	3/ "	3/ "	3/ "	3/ "	2/ 5.2 V	2/ GND	2/ GND	2/ GND	2/ GND	2/ GND	5.5 V	1 MHz	V _{CC}			mA		
	I _{CC2}		2	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1.7 V	"	"	"	"	5.5 V		"			μA			
	I _{CC4}		3	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2.0 V		"			"				
	I _{IL}	3009	4	"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}				"						V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	5.5 V	A7	A6	-1	1	"	
			5	"	GND	GND	GND	"	"	"	"	"	"				"					"	"	"	"	"	"	"		A5	"	"	"	
			6	"	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"				"					"	"	"	"	"	"	"		A4	"	"	"	
			7	"	"	GND	GND	GND	"	"	"	"	"				"					"	"	"	"	"	"	"		A3	"	"	"	
			8	"	"	"	"	V _{CC}	"	"	"	"	"				"					"	"	"	"	"	"	"		A2	"	"	"	
			9	"	"	"	"	"	GND	"	"	"	"				"					"	"	"	"	"	"	"		A1	"	"	"	
			10	"	"	"	"	"	"	V _{CC}	"	"	"				"					"	"	"	"	"	"	"		A0	"	"	"	
			11	"	"	"	"	"	"	"	"	GND	"				"					"	"	"	"	"	"	"		CE	"	"	"	
			12	"	"	"	"	"	"	"	"	V _{CC}	"				"					"	"	"	"	"	"	"		"	A10	"	"	"
			13	"	"	"	"	"	"	"	"	"	GND				"					"	"	"	"	"	"	"		"	OE	"	"	"
			14	"	"	"	"	"	"	"	"	"	"				"					"	"	"	"	"	"	"		"	WE	"	"	"
			15	"	"	"	"	"	"	"	"	"	"				"					"	"	"	"	"	"	"		"	A9	"	"	"
			16	"	"	"	"	"	"	"	"	"	"				"					"	"	"	"	"	"	"		"	A8	"	"	"
17	"	"	"	"	"	"	"	"	"	"				"					"	"	"	"	"	"	"	"		"	"	"				
I _{IH}	3010	18	"	GND	GND	GND	GND	GND	GND	GND	GND				"						GND	GND	GND	GND	GND	"	A7	A6	"	"	"			
		19	"	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"				"					"	"	"	"	"	"		"	A5	"	"	"		
		20	"	GND	GND	GND	"	"	"	"	"	"				"					"	"	"	"	"	"		"	A4	"	"	"		
		21	"	"	"	"	V _{CC}	"	"	"	"	"				"					"	"	"	"	"	"		"	"	A3	"	"	"	
		22	"	"	"	"	"	"	"	"	"	"				"					"	"	"	"	"	"		"	"	A2	"	"	"	
		23	"	"	"	"	"	"	"	"	"	"				"					"	"	"	"	"	"		"	"	A1	"	"	"	
		24	"	"	"	"	"	"	GND	"	"	"				"					"	"	"	"	"	"		"	"	A0	"	"	"	
		25	"	"	"	"	"	"	"	V _{CC}	"	"				"					"	"	"	"	"	"		"	"	CE	"	"	"	
26	"	"	"	"	"	"	"	"	"	GND				"					"	"	"	"	"	"	"	"	A10	"	"	"				
27	"	"	"	"	"	"	"	"	"	"				"					"	"	"	"	"	"	"	"	OE	"	"	"				
28	"	"	"	"	"	"	"	"	"	"				"					"	"	"	"	"	"	"	"	WE	"	"	"				
29	"	"	"	"	"	"	"	"	"	"				"					"	"	"	"	"	"	"	"	"	A9	"	"	"			
30	"	"	"	"	"	"	"	"	"	"				"					"	"	"	"	"	"	"	"	"	A8	"	"	"			
I _{OLZ}	3020	32										GND	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	2.2 V		2.2 V					DQ0	"	"	"			
		33										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ1	"	"	"		
		34										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ2	"	"	"		
		35										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ3	"	"	"		
		36										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ4	"	"	"		
		37										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ5	"	"	"		
		38										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ6	"	"	"		
39										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ7	"	"	"				
I _{OHZ}	3021	40										"	GND	GND	GND	"	GND	GND	GND	"	"	"	"	"	"	"			DQ0	"	"	"		
		41										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ1	"	"	"		
		42										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ2	"	"	"		
		43										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ3	"	"	"		
		44										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ4	"	"	"		
		45										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ5	"	"	"		
		46										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ6	"	"	"		
		47										"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	DQ7	"	"	"		
V _{OL} V _{OH}	3007	48-55	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	"	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4/ 5/	4.5 V		DQ0-DQ7		0.4	V			
	3006	56-63	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	4.5 V		DQ0-DQ7	2.4		V			

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20	21	22	23	24	25	26	28	29	32	Algorithm	Measured terminal	Test limits		Unit																													
			Case J	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24			Min	Max																														
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	DQ0	DQ1	DQ2	V _{SS}	DQ3	DQ4	DQ5	DQ6	DQ7	$\overline{\text{CE}}$	A10	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	A8	V _{CC}																																		
2	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = +125°C.																																																												
3	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = -55°C.																																																												
4	T _C =+25°C	C _{IN}	3012	64	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/																																			
		C _{OUT}	65	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	"	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/																																			
7	T _C =+25°C	I/O	Function tests	66	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	4.5 V	Pattern 5 Pattern 4	Input Output		12 14	pF pF																													
		V _{DR}	67	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	2.0 V																																			
8	Same tests, terminal conditions, and limits as for subgroup 7, except T _C = +125°C and -55°C.																																																												
9	T _C =+25°C	Functional tests		69	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	GND	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	4.5 V	Patterns 1,3,5 Patterns 1,3,5	DQ DQ																															
				70													"											5.5 V																																	
			t _{ELQV}	68	71												"											4.5 V	Pattern 3	DQ		200	ns																												
				71												"											5.5 V	Pattern 3	DQ		200	ns																													
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = +125°C.																																																												
11	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = -55°C.																																																												

See footnotes at end of device type 02.

- 1/ Pins not designated may be "high" level logic, or "low" level logic. Exceptions are the input/output terminals, in the output condition, may be open.
- 2/ All input levels and timing edges are set to table I limits with read cycle timing: For device type 02, outputs are open. $I_0 = 0$ mA. Device type 02 inputs = GND and V_{CC} .
- 3/ Outputs loaded with load as specified on figure 5.
- 4/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels and forcing current during measurement shall be $V_{IL} = 0.8$ V, $I_{OL} = 3.2$ mA.
- 5/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels and forcing current during measurement shall be $V_{IH} = 2.4$ V, $I_{OH} = -1.0$ mA.
- 6/ See 4.4.1c.
- 7/ Tested as follows: $f = 2$ MHz, $V_{IL} = 0.4$ V, $V_{IH} = 2.4$ V, $I_{OL} = -4$ mA, $I_{OH} = +4.0$ μ A, $V_{OH} \geq 1.5$ V and $V_{OL} \leq 1.5$ V.
- 8/ Test is done with addresses held stable, $V_{CC} = 2.0$ V, and all other inputs held at V_{CC} . The data retention test condition shall be held for 250 milliseconds before measurements. The data must remain valid after power is returned to device.
- 9/ Timing waveforms shown on figure 4 shall be applied while performing a WRITE/WRITE address complement pattern (see figure 8). Device type 02 uses patterns 1, 3, 5 (see Appendix A). A combination of test patterns is used to verify all of the ac parameters. Each pattern does not test all ac parameters inclusive. This procedure ensures that the following parameters meet the specified limits:

Parameter		Limits		Unit
		Device type 02		
		Min	Max	
t _{AVAV}		210	---	ns
t _{AVQV}		---	210	"
t _{AVQX}		---	---	"
t _{OLQX}		---	---	"
t _{OLQV}		---	---	"
t _{OHQZ}		---	---	"
t _{ELQV}		210	---	"
t _{ELQX}		---	---	"
t _{EHQZ}		---	---	"
t _{AVEL}		10	---	"
t _{ELAX}		50	---	"
t _{ELEH}		200	---	"
V _{IL}		0.0		V
V _{IH}		3.0		"
Output compare level	V _{OL}	1.5		"
	V _{OH}	1.5		"
Read cycle timing				

Parameter		Limits		Unit
		Device type 02		
		Min	Max	
t _{WHAV}		---	---	ns
t _{ELWH}		200	---	ns
t _{AVWH}		---	---	ns
t _{AVWL}		---	---	ns
t _{WLWH}		200	---	ns
t _{DVWH}		80	---	ns
t _{WHDX}		10	---	ns
t _{WLEH}		200	---	ns
V _{IL}		0.0		V
V _{IH}		3.0		ns
Output compare level	V _{OL}	1.5		ns
	V _{OH}	1.5		ns
Write cycle timing				

The output shall be loaded with the load specified on figure 5. If the test equipment limitations prevent the simultaneous application or verification of all the specified parameters, multiple executions of the algorithm may be required to effect the measurement of all dynamic parameters.

TABLE III. Group A inspection for device types 03 and 09. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R,Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Algorithm	Measured terminal	Test limits		Unit						
			Test no.	A0	A1	A2	A3	A4	A5	A6	DQ	$\overline{WE}$	V _{SS}	$\overline{CE}$	D _{IN}	A7	A8	A9	A10	A11	A12	A13	V _{CC}			Min	Max							
1 T _C =+25°C	I _{CC1}	3005	1	2/	2/	2/	2/	2/	2/	2/	3/	2/	GND	0.8 V	2/	2/	2/	2/	2/	2/	2/	2/	5.5 V	1 MHz	V _{CC}			mA						
	I _{CC2}		2	GND	GND	GND	GND	GND	GND	GND	"	GND	"	5.2 V	GND	GND	GND	GND	GND	GND	GND	GND	"		"			μA						
I _{CC3}	3		"	"	"	"	"	"	"	"	"	"	"	2.2 V	"	"	"	"	"	"	"	"	"		"	"			mA					
I _{CC4}	4		"	"	"	"	"	"	"	"	"	"	"	1.7 V	"	"	"	"	"	"	"	"	2.0 V		"	"			μA					
	I _{IL}	3009	5	GND	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	5.5 V	A0	A1	-1	1	"						
	6		V _{CC}	GND	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}		V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}		"	A2	"	"	"					
	7		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	A3	"	"	"			
	8		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	A4	"	"	"		
	9		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	A5	"	"	"		
	10		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	A6	"	"	"		
	11		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	WE	"	"	"		
	12		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	CE	"	"	"		
	13		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	D _{IN}	"	"	"		
	14		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	A7	"	"	"		
	15		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	A8	"	"	"		
	16		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	A9	"	"	"		
	17		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	A10	"	"	"		
	18		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	A11	"	"	"		
	19		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	A12	"	"	"		
	20		"	"	"	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	"	A13	"	"	"		
			I _{IH}	3010	22	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"	A0	A1	"	"	"		
			23		GND	V _{CC}	GND	"	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"		"	A2	"	"	"	
			24		"	GND	V _{CC}	V _{CC}	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"		"	"	A3	"	"	"
			25		"	"	"	V _{CC}	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"		"	"	A4	"	"	"
			26		"	"	"	GND	"	"		"	"	"	"	"	"	"	"	"	"	"	"		"	"	"		"	"	A5	"	"	"
27		"	"		"	V _{CC}	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A6		"	"	"			
28		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	WE	"		"	"				
29		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CE	"		"	"				
30		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	D _{IN}	"		"	"				
31		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A7		"	"	"			
32		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A8		"	"	"			
33		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A9		"	"	"			
34		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A10		"	"	"			
35		"	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A11		"	"	"			
36	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A12	"	"	"						
37	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A13	"	"	"						
38	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"										
	I _{OLZ}	3020	39								GND		"	2.2 V											D _Q	"	"	"	"					
	I _{OHZ}	3021	40								V _{CC}		"	2.2 V												D _Q	"	"	"	"				
	V _{OL}	3007	41	4/	4/	4/	4/	4/	4/	4/	4/	4/	"	4/	4/	4/	4/	4/	4/	4/	4/	4/	4.5 V		D _Q		0.4	V						
	V _{OH}	3006	42	5/	5/	5/	5/	5/	5/	5/	5/	5/	"	5/	5/	5/	5/	5/	5/	5/	5/	5/	4.5 V		D _Q	2.4		V						
2	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = +125°C.																																	
3	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = -55°C.																																	

See footnotes at end of device type 03.

TABLE III. Group A inspection for device types 03 and 09 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R,Y Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Algorithm	Measured terminal	Test limits		Unit	
				A0	A1	A2	A3	A4	A5	A6	DQ	WE	V _{SS}	CE	D _{IN}	A7	A8	A9	A10	A11	A12	A13	V _{CC}			Min	Max		
4 T _C =+25°C	C _{IN} C _{OUT}	3012	43 44	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	Pattern 5 Pattern 4	Input Output		10 12	pF pF	
7 T _C =+25°C	I/O V _{DR}	Function tests	45 46	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	"	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	7/ 8/	5.5 V 2.0 V						
8	Same tests, terminal conditions, and limits as for subgroup 7, except T _C = +125°C and -55°C.																												
9 T _C =+25°C	Functional tests		48	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	GND	"	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	9/ 9/	4.5 V 5.5 V	Patterns 1,3,5 Patterns 1,3,5	D _O D _O			
	t _{ELQV} t _{ELQV} t _{AVQV} t _{AVQV}	47	49 50 51 52										" " " "										4.5 V 5.5 V 4.5 V 5.5 V	Pattern 3 Pattern 3 Pattern 3 Pattern 3	D _O D _O D _O D _O	85 " " "	ns " " "		
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = +125°C.																												
11	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = -55°C.																												

- 1/ Pins not designated may be "high" level logic, or "low" level logic. Exceptions are the input/output terminals, in the output condition, may be open.
- 2/ All input levels and timing edges are set to table I limits with read cycle timing: Inputs = GND and V_{CC}, outputs = open, I_O = 0 mA.
- 3/ Outputs loaded with load as specified on figure 5.
- 4/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels and forcing current during measurement shall be: V_{IL} = 0.8 V, I_{OL} = 8.0 mA.
- 5/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels and forcing current during measurement shall be: V_{IH} = 2.2 V, I_{OH} = -4.0 mA.
- 6/ See 4.4.1c.
- 7/ Tested as follows: f = 2 MHz, V_{IL} = 0.4 V, V_{IH} = 2.2 V, I_{OL} = -4 mA, I_{OH} = +4.0 μA, V_{OH} ≥ 1.5 V and V_{OL} ≤ 1.5 V.
- 8/ Test is done with addresses held stable, V_{CC} = 2.0 V, and all other inputs held at V_{CC}. The data retention test condition shall be held for 250 milliseconds before measurements. The data must remain valid after power is returned to device.

- 9/ Timing waveforms shown on figure 4 shall be applied while performing a WRITE/WRITE address complement pattern (see figure 8). This procedure ensures that the following parameters meet the specified limits:

Parameter		Limits				Unit
		Device type 03		Device type 09		
		Min	Max	Min	Max	
t _{AVAV}		85	---	70	---	ns
t _{AVQV}		---	85	---	70	"
t _{ELQV}		---	85	---	70	"
V _{IL}		0.0		0.0		V
V _{IH}		3.0		3.0		"
Output compare level	V _{OL}	1.5		1.5		"
	V _{OH}	1.5		1.5		
Read cycle timing						

Parameter		Limits				Unit
		Device type 03		Device type 09		
		Min	Max	Min	Max	
t _{AWWH}		65	---	55	---	ns
t _{WHAV}		0	---	0	---	"
t _{ELWH}		65	---	55	---	"
t _{AWWL}		0	---	0	---	"
t _{WLWH}		45	---	40	---	"
t _{WHDX}		0	---	0	---	"
t _{DVWH}		35	---	30	---	"
t _{ELQX}		---	---	---	---	"
t _{WHQZ}		---	---	---	---	"
V _{IL}		0.0		0.0		V
V _{IH}		3.0		3.0		"
Output compare level	V _{OL}	1.5		1.5		"
	V _{OH}	1.5		1.5		"
Write cycle timing						

The output shall be loaded with the load specified on figure 5. If the test equipment limitations prevent the simultaneous application or verification of all the specified parameters, multiple executions of the algorithm may be required to effect the measurement of all dynamic parameters.

- 10/ When testing subgroup 9, device type 09 will have the same test conditions as device type 03, except for the following:

- t_{ELQV} = 70 ns maximum.
- t_{ELQV} = 70 ns maximum.
- t_{AVQV} = 70 ns maximum.
- t_{AVQV} = 70 ns maximum.

TABLE III. Group A inspection for device types 04 and 10. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20	21	22	23	24	25	26	28	29	32	Algorithm	Measured terminal	Test limits		Unit
			Case J	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24			Min	Max	
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	DQ0	DQ1	DQ2	V _{SS}	DQ3	DQ4	DQ5	DQ6	DQ7	$\overline{\text{CE}}$	A10	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	A8	V _{CC}					
1 T _C =+25°C	I _{CC1}	3005	1	2/	2/	2/	2/	2/	2/	2/	2/	3/	3/	3/	GND	3/	3/	3/	3/	3/	0.8 V	2/	2/	2/	2/	2/	5.5 V	1 MHz	V _{CC}			mA
	I _{CC2}		2	GND	GND	GND	GND	GND	GND	GND	GND	"	"	"	"	"	"	"	"	"	5.2 V	GND	GND	GND	GND	GND	"	"	"	100	μA	
	I _{CC3}		3	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2.2 V	"	"	"	"	"	2.0 V	"	"	8	mA	
	I _{CC4}		4	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1.7 V	"	"	"	"	"	"	"	"	50	μA		
	I _{IL}	3009	5	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}									V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	5.5 V	A7	A6	-1	1	"	
		6	"	GND	GND	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}									"	"	"	"	"	"	"		"	A5	"	"	"
		7	"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}									"	"	"	"	"	"	"		"	A4	"	"	"
		8	"	"	"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}									"	"	"	"	"	"	"		"	A3	"	"	"
		9	"	"	"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}									"	"	"	"	"	"	"		"	A2	"	"	"
		10	"	"	"	"	GND	V _{CC}	GND	V _{CC}	V _{CC}									"	"	"	"	"	"	"		"	A1	"	"	"
		11	"	"	"	"	V _{CC}	V _{CC}	GND	V _{CC}	V _{CC}									"	"	"	"	"	"	"		"	A0	"	"	"
		12	"	"	"	"	"	"	"	"	"									GND	"	"	"	"	"	"		"	CE	"	"	"
		13	"	"	"	"	"	"	"	"	"									V _{CC}	"	"	"	"	"	"		"	A10	"	"	"
		14	"	"	"	"	"	"	"	"	"									V _{CC}	GND	"	"	"	"	"		"	OE	"	"	"
		15	"	"	"	"	"	"	"	"	"									"	"	GND	"	"	"	"		"	WE	"	"	"
		16	"	"	"	"	"	"	"	"	"									"	"	V _{CC}	"	"	"	"		"	A9	"	"	"
		17	"	"	"	"	"	"	"	"	"									"	"	V _{CC}	GND	"	"	"		"	A8	"	"	"
		18	"	"	"	"	"	"	"	"	"									"	"	V _{CC}	GND	"	"	"		"		"	"	"
	I _{IH}	3010	19	GND	GND	GND	GND	GND	GND	GND	GND									GND	GND	GND	GND	GND	GND	"		A7	A6	"	"	"
		20	"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}									"	"	"	"	"	"	"			"	A5	"	"
		21	"	GND	GND	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}									"	"	"	"	"	"	"	"		A4	"	"	"
		22	"	"	"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}									"	"	"	"	"	"	"	"		A3	"	"	"
		23	"	"	"	"	"	"	"	"	"									"	"	"	"	"	"	"	"		A2	"	"	"
		24	"	"	"	"	"	"	"	"	"									"	"	"	"	"	"	"	"		A1	"	"	"
		25	"	"	"	"	"	"	"	"	"									"	"	"	"	"	"	"	"		A0	"	"	"
		26	"	"	"	"	"	"	"	"	"									"	"	"	"	"	"	"	"		CE	"	"	"
		27	"	"	"	"	"	"	"	"	"									V _{CC}	GND	"	"	"	"	"	"		A10	"	"	"
		28	"	"	"	"	"	"	"	"	"									"	"	V _{CC}	"	"	"	"	"		OE	"	"	"
		29	"	"	"	"	"	"	"	"	"									"	"	V _{CC}	GND	"	"	"	"		WE	"	"	"
		30	"	"	"	"	"	"	"	"	"									"	"	V _{CC}	GND	"	"	"	"		A9	"	"	"
		31	"	"	"	"	"	"	"	"	"									"	"	V _{CC}	GND	"	"	"	"		A8	"	"	"
		32	"	"	"	"	"	"	"	"	"									"	"	V _{CC}	GND	"	"	"	"			"	"	"
	I _{OLZ}	3009	33									GND	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	2.2 V		2.2 V			5.5 V		DQ0	"	"	"	
			34									"	GND	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ1	"	"	"
			35									"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ2	"	"	"
			36									"	"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ3	"	"	"
			37									"	"	"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ4	"	"	"
			38									"	"	"	"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ5	"	"	"
			39									"	"	"	"	"	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ6	"	"	"
			40									"	"	"	"	"	"	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ7	"	"	"
	I _{OHZ}	3010	41									V _{CC}	GND	GND	GND	GND	GND	GND	GND	"	"	"	"	"	"	"			DQ0	"	"	"
			42									"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ1	"	"	"
			43									"	"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ2	"	"	"
			44									"	"	"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ3	"	"	"
			45									"	"	"	"	V _{CC}	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ4	"	"	"
			46									"	"	"	"	"	V _{CC}	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ5	"	"	"
			47									"	"	"	"	"	"	V _{CC}	V _{CC}	"	"	"	"	"	"	"	"		DQ6	"	"	"
			48									"	"	"	"	"	"	"	V _{CC}	V _{CC}	"	"	"	"	"	"	"		DQ7	"	"	"
	V _{OL}	3007	49-56	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	"	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4.5 V		DQ0-DQ7		0.4	V	
	V _{OH}	3006	57-64	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	"	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	4.5 V		DQ0-DQ7	2.4		V	

See footnotes at end of device type 04.

TABLE III. Group A inspection for device types 04 and 10 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20	21	22	23	24	25	26	28	29	32	Algorithm	Measured terminal	Test limits		Unit															
			Case J	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24			Min	Max																
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	DQ0	DQ1	DQ2	V _{SS}	DQ3	DQ4	DQ5	DQ6	DQ7	$\overline{\text{CE}}$	A10	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	A8	V _{CC}																				
2	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = +125°C.																																														
3	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = -55°C.																																														
4	T _C =+25°C	C _{IN} C _{OUT}	3012	65	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	"	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/			Input Output		10	pF														
7	T _C =+25°C	I/O V _{DR}	Function tests	66	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	"	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	4.5 V	Pattern 5			12	pF														
				68	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	"	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	2.0 V	Pattern 4																			
8	Same tests, terminal conditions, and limits as for subgroup 7, except T _C = +125°C and -55°C.																																														
9	T _C =+25°C	Functional tests		70	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	GND	"	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	4.5 V	Patterns 1,3,5	D _O																	
																											5.5 V	Patterns 1,3,5	D _O																		
		t _{ELOW}	69	71											"												4.5 V	Pattern 3	D _O		90	ns															
		t _{ELOW}		72											"												5.5 V	Pattern 3	D _O		"	"															
		t _{AVOV}		73											"												4.5 V	Pattern 3	D _O		"	"															
		t _{AVOV}		74											"												5.5 V	Pattern 3	D _O		"	"															
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = +125°C.																																														
11	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = -55°C.																																														

See footnotes at end of device type 04.

- 1/ Pins not designated may be "high" level logic, or "low" level logic. Exceptions are the input/output terminals, in the output condition, may be open.
- 2/ All input levels and timing edges are set to table I limits with read cycle timing: Inputs = GND and V_{CC} , outputs = open, $I_o = 0$ mA.
- 3/ Outputs loaded with load as specified on figure 5.
- 4/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels and forcing current during measurement shall be: $V_{IL} = 0.8$ V, $I_{OL} = 2.0$ mA.
- 5/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels and forcing current during measurement shall be: $V_{IH} = 2.2$ V, $I_{OH} = -1.0$ mA.
- 6/ See 4.4.1c.
- 7/ Tested as follows: $f = 2$ MHz, $V_{IL} = 0.4$ V, $V_{IH} = 2.2$ V, $I_{OL} = -4$ mA, $I_{OH} = +4.0$ μ A, $V_{OH} \geq 1.5$ V and $V_{OL} \leq 1.5$ V.
- 8/ Test is done with addresses held stable, $V_{CC} = 2.0$ V, and all other inputs held at V_{CC} . The data retention test condition shall be held for 250 milliseconds before measurements. The data must remain valid after power is returned to device.
- 9/ Timing waveforms shown on figure 4 shall be applied while performing a WRITE/WRITE address complement pattern (see figure 8). Device types 04 and 10 use patterns 1, 3, 5 (see Appendix A). A combination of test patterns is used to verify all of the ac parameters. Each pattern does not test all ac parameters inclusive. This procedure ensures that the following parameters meet the specified limits:

Parameter		Limits				Unit
		Device type 04		Device type 10		
		Min	Max	Min	Max	
t _{AVAV}		90	---	70	---	ns
t _{AVQV}		---	90	---	70	"
t _{AVQX}		0	---	5	---	"
t _{OLQX}		---	---	---	---	"
t _{OLQV}		65	---	---	---	"
t _{OHQZ}		---	---	---	50	"
t _{ELQV}		90	---	70	---	"
t _{ELQX}		---	---	---	---	"
t _{EHQZ}		---	---	---	---	"
t _{AVEL}		---	---	---	---	"
t _{ELAX}		---	---	---	---	"
t _{ELEH}		---	---	---	---	"
V _{IL}		0.0		0.0		V
V _{IH}		3.0		3.0		"
Output compare level	V _{OL}	1.5		1.5		"
	V _{OH}	1.5		1.5		"
Read cycle timing						

Parameter		Limits				Unit
		Device type 04		Device type 10		
		Min	Max	Min	Max	
t _{WHAV}		10	---	10	---	ns
t _{ELWH}		55	---	45	---	"
t _{AVWH}		80	---	50	---	"
t _{AVWL}		10	---	10	---	"
t _{WLWH}		55	---	40	---	"
t _{DVWH}		30	---	30	---	"
t _{WHDX}		15	---	10	---	"
t _{WLEH}		---	---	40	---	"
V _{IL}		0.0		0.0		V
V _{IH}		3.0		3.0		"
Output compare level	V _{OL}	1.5		1.5		"
	V _{OH}	1.5		1.5		"
Write cycle timing						

The output shall be loaded with the load specified on figure 5. If the test equipment limitations prevent the simultaneous application or verification of all the specified parameters, multiple executions of the algorithm may be required to effect the measurement of all dynamic parameters.

- 10/ When testing subgroup 9, device type 10 will have the same test conditions as device type 04, except for the following:
 - a. $t_{ELQV} = 70$ ns maximum.
 - b. $t_{ELQV} = 70$ ns maximum.
 - c. $t_{AVQV} = 70$ ns maximum.
 - d. $t_{AVQV} = 70$ ns maximum.

TABLE III. Group A inspection for device type 06. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R,Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits		Unit
				Test no.	A0	A1	A2	A3	A4	A5	A6	DQ	WE	V _{SS}	CE	D _{IN}	A7	A8	A9	A10	A11	A12	A13	V _{CC}	Min	Max	
1 T _c =+25°C	I _{CC1}	3005	1	2/	2/	2/	2/	2/	2/	2/	3/	2/	GND	2/	2/	2/	2/	2/	2/	2/	2/	2/	5.5 V	V _{CC}			mA
	I _{CC2}		2	4/	4/	4/	4/	4/	4/	4/	"	4/	"	"	4/	4/	4/	4/	4/	4/	4/	4/	"	"			mA
	I _{CC3}		3	5/	5/	5/	5/	5/	5/	5/	"	5/	"	"	5/	5/	5/	5/	5/	5/	5/	5/	"	"			
	I _{CC4}		4	6/	6/	6/	6/	6/	6/	6/	"	6/	"	"	6/	6/	6/	6/	6/	6/	6/	6/	"	"	100		
	I _{IL}	3009	5	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"	5.5 V	"	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A0	A1			μA
			6	5.5 V	GND	5.5 V	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A2			
			7	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A3			
			8	"	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A4			
			9	"	"	"	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A5			
			10	"	"	"	"	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A6			
			11	"	"	"	"	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"		WE			
			12	"	"	"	"	"	GND	"	"	"	"	"	"	"	"	"	"	"	"	"		CE			
			13	"	"	"	"	"	"	GND	"	"	"	"	"	"	"	"	"	"	"	"		D _{IN}			
			14	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A7			
			15	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A8			
			16	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A9			
			17	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A10			
			18	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A11			
			19	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A12			
			20	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A13			
			21	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A13			
	I _{IH}	3010	22	"	GND	GND	GND	GND	GND	GND	"	GND	"	GND	GND	GND	GND	GND	GND	GND	"	"	A0	A1			
			23	"	5.5 V	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A2			
			24	"	"	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A3			
			25	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A4			
			26	"	"	"	"	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A5			
			27	"	"	"	"	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A6			
			28	"	"	"	"	"	5.5 V	"	"	"	"	"	"	"	"	"	"	"	"	"		WE			
			29	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		CE			
			30	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		D _{IN}			
			31	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A7			
			32	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A8			
			33	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A9			
			34	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A10			
			35	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A11			
			36	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A12			
			37	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A13			
			38	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		A13			
	I _{OLZ}	3020	39								GND	"	"	2.2 V								"	0			-20	"
	I _{OHZ}	3021	40								5.5 V	"	"	2.2 V								"	0			+20	"
	V _{OL}	3007	41	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	4.5 V	0			0.4	V
	V _{OH}	3006	42	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	4.5 V	0	2.4			V
2	Same tests, terminal conditions, and limits as for subgroup 1, except T _c = +125°C.																										
3	Same tests, terminal conditions, and limits as for subgroup 1, except T _c = -55°C.																										

See footnotes at end of device type 06.

TABLE III. Group A inspection for device type 06 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases R,Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits		Unit
			Test no.	A0	A1	A2	A3	A4	A5	A6	D _Q	$\overline{WE}$	V _{SS}	$\overline{CE}$	D _{IN}	A7	A8	A9	A10	A11	A12	A13	V _{CC}		Min	Max	
4	C _{IN}	3012	43	9/	9/	9/	9/	9/	9/	9/	9/		9/	9/	9/	9/	9/	9/	9/	9/	9/		Each input Each output		8	pF	
T _C =+25°C	C _{OUT}		44								9/															10	pF
9	NOT	See fig. 7	45	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	4.5 V	D _N	10/	10/	ns
T _C =+25°C	WRITE		46	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	5.5 V	D _N	10/	10/	"
	WRITE/	See fig. 8	47	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	D _N	11/	11/	"
	WRITE		48	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	5.5 V	D _N	11/	11/	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = +125°C.																										
11	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = -55°C.																										

- 1/ Pins not designated may be “high” level logic, or “low” level logic. Exceptions are the input/output terminals, in the output condition, may be open.
- 2/ All input levels and timing edges are set to table I limits with read cycle timing: V_{IL} = 0.4 V and V_{IH} = 2.2 V for device type 06.
- 3/ Outputs loaded with load as specified on figure 5.
- 4/ Test is done with addresses held stable, and all inputs held at V_{IL} = 0.4 V and V_{IH} = 2.2 V for device type 06.
- 5/ Test is done with addresses held stable, and all inputs held at V_{IL} = 0.4 V and V_{IH} = V_{CC} – 0.3 V.
- 6/ Test is done with addresses held stable, V_{CC} = 2.0 V, and all other inputs held at V_{CC}. The data retention test condition shall be held for 250 milliseconds before measurements. The data must remain valid after power is returned to device.
- 7/ An input preconditioning logic sequence shall be applied that results in a logic “0” at the output to be measured. Logic input levels and forcing current during measurement shall be: V_{IL} = 0.8 V, I_{OL} = 8.0 mA.
- 8/ An input preconditioning logic sequence shall be applied that results in a logic “1” at the output to be measured. Logic input levels and forcing current during measurement shall be: V_{IH} = 2.2 V, I_{OH} = -4.0 mA.
- 9/ See 4.4.1c.
- 10/ Since the object of the NOT WRITE pattern (see figure 7) is to verify that the device may not be written into when it is disabled, the waveforms shown on figure 4 may be applied using normal timing. The outputs shall be loaded with the load specified on figure 5.

- 11/ Timing waveforms shown on figure 4 shall be applied while performing a WRITE/WRITE address complement pattern (see figure 8). This procedure ensures that the following parameters meet the specified limits:

Parameter		Limits		Unit
		Device type 06		
		Min	Max	
t _{AVAV}		45	---	ns
t _{AVQV}		---	45	"
t _{ELQV}		---	45	"
V _{IL}		0.0		V
V _{IH}		2.2		"
Output compare level	V _{OL}	0.4		"
	V _{OH}	2.4		"
Read cycle timing				

Parameter		Limits		Unit
		Device type 06		
		Min	Max	
t _{AVWH}		35	---	ns
t _{WHAV}		5	---	"
t _{ELWH}		35	---	"
t _{AVWL}		5	---	"
t _{WLWH}		30	---	"
t _{WHDX}		5	---	"
t _{DVWH}		25	---	"
t _{ELQX}		3	---	"
t _{WHQZ}		---	25	"
V _{IL}		0.0		V
V _{IH}		2.2		"
Output compare level	V _{OL}	0.4		"
	V _{OH}	2.4		"
Write cycle timing				

The output shall be loaded with the load specified on figure 5. If the test equipment limitations prevent the simultaneous application or verification of all the specified parameters, multiple executions of the algorithm may be required to effect the measurement of all dynamic parameters.

TABLE III. Group A inspection for device type 07. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R Case Z Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits		Unit
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		Min	Max	
				A0	A1	A2	A3	A4	A5	A6	D _Q	WE	V _{SS}	CE	D _{IN}	A7	A8	A9	A10	A11	A12	A13	V _{CC}				
1 T _C =+25°C	V _{IC} (pos)	3022	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17	50 μA	50 μA	50 μA	50 μA	50 μA	50 μA	50 μA													GND	A0 A1 A2 A3 A4 A5 A6 WE CE D _{IN} A7 A8 A9 A10 A11 A12 A13	0.1 " " " " " " " " " " " " " "	2.0 " " " " " " " " " " " " " "	V " " " " " " " " " " " " " "
	V _{IC} (neg)	3022	18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34	-50 μA	-50 μA	-50 μA	-50 μA	-50 μA	-50 μA	-50 μA			GND										A0	A1 A2 A3 A4 A5 A6 WE CE D _{IN} A7 A8 A9 A10 A11 A12 A13	-0.1 " " " " " " " " " " " " " "	-2.0 " " " " " " " " " " " " " "	" " " " " " " " " " " " " " "
	V _{ON} 2/	3007	35	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	3/	4.5 V	"	GND	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	D _Q		0.4	"
V _{OH} 4/ I _{IH} 6/	V _{OH} 4/	3006	36	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	5/	4.5 V	"	"	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	D _Q	4.0		"
	I _{IH} 6/	3010	37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53	5.5 V GND	GND 5.5 V GND	GND GND 5.5 V GND	GND "	GND "	GND "	GND "		GND "	"	"	GND "	GND "	GND "	GND "	GND "	GND "	GND "	GND "	5.5 V	A0 A1 A2 A3 A4 A5 A6 WE CE D _{IN} A7 A8 A9 A10 A11 A12 A13		1.0 " " " " " " " " " " " " " "	μA " " " " " " " " " " " " " "
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"

See footnotes at end of device type 07.

TABLE III. Group A inspection for device type 07 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits		Unit			
			Case Z Test no.	A0	A1	A2	A3	A4	A5	A6	D _Q	$\overline{WE}$	V _{SS}	$\overline{CE}$	D _{IN}	A7	A8	A9	A10	A11	A12	A13	V _{CC}		Min	Max				
1 T _C =+25°C	I _L 6/	3009	54	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A0		-1.0	μA			
			55	5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A1					
			56		5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A2				
			57			5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A3			
			58				GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A4			
			59					GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A5			
			60						5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A6			
			61							5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	$\overline{WE}$			
			62								5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	CE		
			63									5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	D _{IN}		
			64										5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A7		
			65											5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A8		
			66												5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A9		
			67													5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A10		
			68														5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A11		
			69															5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A12		
			70																5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A13		
	I _{OHZ}	3021	71	GND	GND	GND	GND	GND	GND	GND	GND	5.5 V	5.5 V	GND	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	D _Q		10			
	I _{OHZ}	3021	72	GND	GND	GND	GND	GND	GND	GND	GND	5.5 V	GND		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	D _Q		10			
	I _{OLZ}	3020	73	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	5.5 V		5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	D _Q		-10			
	I _{OLZ}	3020	74	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	GND		GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	D _Q		-10			
	I _{CC1}	3005	75	GND	GND	GND	GND	GND	GND	GND	GND			5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V _{CC} 7/		200			
	I _{CC2}		76																						V _{CC} 8/					
	I _{CC3}		77																							V _{CC} 9/				
	I _{CC4}		78																							V _{CC} 2/				
2	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = +125°C and V _{IC} tests are omitted.																													
3	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = -55°C and V _{IC} tests are omitted.																													
4 T _C =+25°C	C _{IN}	3012	79	10/	10/	10/	10/	10/	10/	10/		10/	GND	10/	10/	10/	10/	10/	10/	10/	10/	10/	5.5 V	All inputs		8	pF			
8 T _C =+125°C	Power down			11/	11/	11/	11/	11/	11/	11/		11/	"	11/	11/	11/	11/	11/	11/	11/	11/	11/	V _{CC}		3.0	V				
	Functional tests	80		12/	12/	12/	12/	12/	12/	12/		12/	"	12/	12/	12/	12/	12/	12/	12/	12/	12/	D _Q	12/	12/	V				

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See footnotes at end of device type 07.

TABLE III. Group A inspection for device type 07 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits		Unit
			Case Z	Test no.	A0	A1	A2	A3	A4	A5	A6	DQ	$\overline{WE}$	V_{SS}	$\overline{CE}$	D_{IN}	A7	A8	A9	A10	A11	A12	A13		V_{CC}	Min	
9 $T_C=+25^{\circ}\text{C}$	t_{AVDQ}	See fig. 7	82	13/	13/	13/	13/	13/	13/	13/	13/	13/	GND	13/	13/	13/	13/	13/	13/	13/	13/	13/	4.5 V	D_O		150	ns
10	Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = +125^{\circ}\text{C}$.																										
11	Same tests, terminal conditions, and limits as for subgroup 9, except $T_C = -55^{\circ}\text{C}$.																										
12 $T_C=+25^{\circ}\text{C}$	I_{CCOP}		83	14/	14/	14/	14/	14/	14/	14/	14/	GND	14/	14/	14/	14/	14/	14/	14/	14/	14/	14/	5.5 V	V_{CC}		6	mA

1_/ Pins not designated may be “high” level logic, or “low” level logic. Exceptions are as follows: V_{IC} (pos) tests, the V_{SS} terminals shall be open; V_{IC} (neg) tests, the V_{CC} terminal shall be open; I_{SS} tests, the output terminal shall be open.

2_/ $V_{IL} = 0.8\text{ V}$, $V_{IH} = 4.0\text{ V}$.

3_/ Contents of addressed cell shall be = data “0”, $I_{OL} = 5\text{ mA}$.

4_/ $V_{IL} = 0.8\text{ V}$; $V_{IH} = 3.0\text{ V}$.

5_/ Contents of addressed cell shall be = data “1”, $I_{OH} = -5\text{ mA}$.

6_/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at $+25^\circ\text{C}$ for each individual input or measure all inputs together.

7_/ Random data pattern (data in memory established by power turn-on).

8_/ All data are “1’s” in memory.

9_/ All data are “0’s” in memory.

10_/ See 4.4.1c.

11/ Power down test (PWRDWN) terminal conditions shall be as follows:

- a. Use timing parameters and limits specified on figure 4.
- b. $V_{OL} < V_{CC} / 2$; $V_{OH} > V_{CC} / 2$.
- c. Use load specified on figure 5.
- d. $V_{IL} = 0 \text{ V}$; $V_{IH} = 4.5 \text{ V}$.
- e. The power down test shall be performed as follows:
 - (1) Power up RAM to $V_{CC} = 4.5 \text{ V}$.
 - (2) Write topologically true checkerboard pattern into RAM memory array (see Appendix A).
 - (3) Reduce V_{CC} to 3.0 V . All device inputs shall be reduced along with V_{CC} exercising special care to avoid latch-up.
 - (4) Maintain RAM at reduced voltage for 500 ms (0.5 second) minimum.
 - (5) Raise V_{CC} to 4.5 V .
 - (6) Verify RAM contents to be unchanged from pattern written in (2) above.
 - (7) Repeat steps (1) through (6), except use the complement of the first checkerboard pattern.

12/ Functional test terminal conditions shall be as follows:

- a. Use timing parameter and limits specified on figure 4.
- b. The output voltages shall be: $V_{OL} < V_{CC} / 2$; $V_{OH} > V_{CC} / 2$.
- c. Use CK, $\overline{\text{CK}}$, butterfly, spiral complement patterns.
- d. Use load specified on figure 5.
- e. $V_{CC} = 4.5 \text{ V}$; $V_{IL} = 0.8 \text{ V}$; $V_{IH} = V_{CC} - 1.5 \text{ V}$.

13/ Timing test terminal conditions shall be as follows:

- a. Use timing parameter and limits specified on figure 4.
- b. $V_{OL} < V_{CC} / 2$; $V_{OH} > V_{CC} / 2$
- c. Use CK, $\overline{\text{CK}}$, patterns.
- d. Use load specified on figure 5.
- e. $V_{CC} = 4.5 \text{ V}$; $V_{IL} = 0.8 \text{ V}$; $V_{IH} = V_{CC} - 1.5 \text{ V}$.

14/ Operating current test (I_{CCOP}) terminal conditions shall be as follows:

- a. Use timing parameters and limits specified on figure 4.
- b. Use topologically true checkerboard pattern (see Appendix A).
- c. Use load specified on figure 5.
- d. $V_{IL} = 0 \text{ V}$; $V_{IH} = 5.5 \text{ V}$.

TABLE III. Group A inspection for device type 08. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits		Unit			
			Case Z	1	2	3	4	5	8	9	10	11	12	13	14	15	16	17	20	21	22	23	24		Min	Max				
			Test no.	A0	A1	A2	A3	A4	A5	A6	D _Q	$\overline{WE}$	V _{SS}	$\overline{CE}$	D _{IN}	A7	A8	A9	A10	A11	A12	A13	V _{CC}							
1 T _C =+25°C	V _{IC} (pos)	3022	1	50 μA	50 μA	50 μA	50 μA	50 μA	50 μA	50 μA													GND	A0	0.1	2.0	V			
			2																					"	A1	"	"	"		
			3																					"	A2	"	"	"		
			4																					"	A3	"	"	"		
			5																					"	A4	"	"	"		
			6																					"	A5	"	"	"		
			7																					"	A6	"	"	"		
			8																					"	$\overline{WE}$	"	"	"		
			9																					"	CE	"	"	"		
			10																					"	D _{IN}	"	"	"		
			11																					"	A7	"	"	"		
			12																					"	A8	"	"	"		
			13																					"	A9	"	"	"		
			14																					"	A10	"	"	"		
			15																					"	A11	"	"	"		
			16																					"	A12	"	"	"		
			17																					"	A13	"	"	"		
	V _{IC} (neg)	3022	18	-50 μA	-50 μA	-50 μA	-50 μA	-50 μA	-50 μA	-50 μA			GND											A1	-0.1	-2.0	"			
			19																					"	A2	"	"	"		
			20																					"	A3	"	"	"		
			21																					"	A4	"	"	"		
			22																					"	A5	"	"	"		
			23																					"	A6	"	"	"		
			24																					"	$\overline{WE}$	"	"	"		
			25																					"	CE	"	"	"		
			26																					"	D _{IN}	"	"	"		
			27																					"	A7	"	"	"		
			28																					"	A8	"	"	"		
			29																					"	A9	"	"	"		
			30																					"	A10	"	"	"		
			31																					"	A11	"	"	"		
			32																					"	A12	"	"	"		
			33																					"	A13	"	"	"		
			34																					"						
	V _{OL} 2/	3007	35	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	3/	4.5 V	"	GND	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	D _Q		0.4	"			
	V _{OH} 4/	3006	36	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	5/	4.5 V	"	"	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	D _Q			"			
	I _{IH} 6/	3010	37	5.5 V	GND	GND	GND	GND	GND	GND		GND				GND	GND	GND	GND	GND	GND	GND	5.5 V	A0		1.0	μA			
			38	GND	5.5 V	GND	GND	GND	GND	GND	GND					GND	GND	GND	GND	GND	GND	GND	GND	"	A1		"	"		
			39	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	A2		"	"	
			40	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	A3		"	"	
			41	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	A4		"	"
			42	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	A5		"	"
			43	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	A6		"	"
			44	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	$\overline{WE}$		"	"
			45	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	CE		"	"
			46	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	D _{IN}		"	"
			47	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	A7		"	"
			48	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	A8		"	"
			49	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	A9		"	"
			50	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	A10		"	"
			51	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	A11		"	"
			52	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	A12		"	"
			53	"	"	"	"	"	"	"	"					"	"	"	"	"	"	"	"	"	"	"	A13		"	"

See footnotes at end of device type 08.

TABLE III. Group A inspection for device type 08 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R Case Z Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits		Unit			
				A0	A1	A2	A3	A4	A5	A6	D _Q	WE	V _{SS}	CE	D _{IN}	A7	A8	A9	A10	A11	A12	A13	V _{CC}		Min	Max				
1 T _C =+25°C	I _{IL} 6/	3009	54	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A0		-1.0	μA			
			55	5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V													A1					
			56		5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V														A2				
			57			5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V															A3			
			58				5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V															A4			
			59					5.5 V	GND	5.5 V	5.5 V	5.5 V															A5			
			60						5.5 V	GND	5.5 V	5.5 V															A6			
			61							5.5 V	GND	5.5 V															WE			
			62								5.5 V	GND	5.5 V														CE			
			63									5.5 V	GND	5.5 V	GND	5.5 V											D _{IN}			
			64													5.5 V	GND	5.5 V									A7			
			65														5.5 V	GND	5.5 V								A8			
			66															5.5 V	GND	5.5 V							A9			
			67																5.5 V	GND	5.5 V						A10			
			68																	5.5 V	GND	5.5 V					A11			
			69																		5.5 V	GND	5.5 V				A12			
			70																			GND						A13		
I _{OHZ}	3021	71	GND	GND	GND	GND	GND	GND	GND	GND	5.5 V	5.5 V	GND	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	D _Q		10				
		72	GND	GND	GND	GND	GND	GND	GND	GND	5.5 V	GND		GND	GND	GND	GND	GND	GND	GND	GND	GND	D _Q		10					
		73	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	5.5 V		5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	D _Q		-10					
		74	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	GND		GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	D _Q		-10					
		75	GND	GND	GND	GND	GND	GND	GND	GND				5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	V _{CC} 7/		200					
		76																					V _{CC} 8/							
		77																					V _{CC} 9/							
		78																					V _{CC} 10/							
2	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = +125°C and V _{IC} tests are omitted.																													
3	Same tests, terminal conditions, and limits as for subgroup 1, except T _C = -55°C and V _{IC} tests are omitted.																													
4	C _{IN}	3012	79	10/	10/	10/	10/	10/	10/	10/		10/	GND	10/	10/	10/	10/	10/	10/	10/	10/	10/	5.5 V	All inputs		8	pF			
8 T _C =+125°C	Power down			11/	11/	11/	11/	11/	11/	11/		11/	"	11/	11/	11/	11/	11/	11/	11/	11/	11/	V _{CC}		3.0	V				
	Functional tests	80		12/	12/	12/	12/	12/	12/	12/		12/	"	12/	12/	12/	12/	12/	12/	12/	12/	12/	D _Q	12/	12/	V				

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See footnotes at end of device type 08.

TABLE III. Group A inspection for device type 08 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case R	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits		Unit
			Case Z	1	2	3	4	5	8	9	10	11	12	13	14	15	16	17	20	21	22	23	24		Min	Max	
			Test no.	A0	A1	A2	A3	A4	A5	A6	D _Q	$\overline{WE}$	V _{SS}	$\overline{CE}$	D _{IN}	A7	A8	A9	A10	A11	A12	A13	V _{CC}				
9 T _C =+25°C	t _{AVQV}	See fig. 7	82	13/	13/	13/	13/	13/	13/	13/	13/	13/	GND	13/	13/	13/	13/	13/	13/	13/	13/	13/	4.5 V	D _Q		175	ns
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = +125°C.																										
11	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = -55°C.																										
12 T _C =+25°C	I _{CCDP}		83	14/	14/	14/	14/	14/	14/	14/	14/	14/	GND	14/	14/	14/	14/	14/	14/	14/	14/	14/	5.5 V	V _{CC}		6	mA

1_/ Pins not designated may be “high” level logic, or “low” level logic. Exceptions are as follows: V_{IC} (pos) tests, the V_{SS} terminals shall be open; V_{IC} (neg) tests, the V_{CC} terminal shall be open; I_{SS} tests, the output terminal shall be open.

2_/ V_{IL} = 0.8 V, V_{IH} = 3.0 V.

3_/ Contents of addressed cell shall be = data “0”, I_{OL} = 5 mA.

4_/ V_{IL} = 0.8 V; V_{IH} = 2.3 V.

5_/ Contents of addressed cell shall be = data “1”, I_{OH} = -5 mA.

6_/ The device manufacturer may, at his option, measure I_{IL} and I_{IH} at +25°C for each individual input or measure all inputs together.

7_/ Random data pattern (data in memory established by power turn-on).

8_/ All data are “1’s” in memory.

9_/ All data are “0’s” in memory.

10_/ See 4.4.1c.

11/ Power down test (PWRDWN) terminal conditions shall be as follows:

- a. Use timing parameters and limits specified on figure 4.
- b. $V_{OL} \leq 0.45 \text{ V}$; $V_{OH} \geq 2.4 \text{ V}$.
- c. Use load specified on figure 5.
- d. $V_{IL} = 0 \text{ V}$; $V_{IH} = 4.5 \text{ V}$.
- e. The power down test shall be performed as follows:
 - (1) Power up RAM to $V_{CC} = 4.5 \text{ V}$.
 - (2) Write topologically true checkerboard pattern into RAM memory array (see Appendix A).
 - (3) Reduce V_{CC} to 2.0 V . All device inputs shall be reduced along with V_{CC} exercising special care to avoid latch-up. (See 4.5)
 - (4) Maintain RAM at reduced voltage for 500 ms (0.5 second) minimum.
 - (5) Raise V_{CC} to 4.5 V .
 - (6) Verify RAM contents to be unchanged from pattern written in (2) above.
 - (7) Repeat steps (1) through (6), except use the complement of the first checkerboard pattern

12/ ADDCOMP (Functional) test terminal conditions shall be as follows:

- a. Use timing parameter and limits specified on figure 4.
- b. The output voltages shall be: $V_{OL} \leq 0.45 \text{ V}$; $V_{OH} \geq 2.4 \text{ V}$.
- c. Use ADDCOMP pattern (see Appendix A).
- d. Use load specified on figure 5.
- e. $V_{CC} = 4.5 \text{ V}$; $V_{IL} = 0.8 \text{ V}$; $V_{IH} = 2.3 \text{ V}$.

13/ Timing test terminal conditions shall be as follows:

- a. Use timing parameter and limits specified on figure 4.
- b. $V_{OL} \leq 0.45 \text{ V}$; $V_{OH} \geq 2.4 \text{ V}$.
- c. Use MARCH pattern (see Appendix A).
- d. Use load specified on figure 5.
- e. $V_{CC} = 4.5 \text{ V}$; $V_{IL} = 0.8 \text{ V}$; $V_{IH} = 2.3 \text{ V}$.

14/ Operating current test (I_{CCOP}) terminal conditions shall be as follows:

- a. Use timing parameters and limits specified on figure 4.
- b. Use topologically true checkerboard pattern (see Appendix A).
- c. Use load specified on figure 5.
- d. $V_{IL} = 0.8 \text{ V}$; $V_{IH} = 5.5 \text{ V}$.

Pin Number Case J	Device Type 01, 02, 04, 05, and 10
1	A ₇
2	A ₆
3	A ₅
4	A ₄
5	A ₃
6	A ₂
7	A ₁
8	A ₀
9	DQ ₀
10	DQ ₁
11	DQ ₂
12	V _{SS}
13	DQ ₃
14	DQ ₄
15	DQ ₅
16	DQ ₆
17	DQ ₇
18	$\overline{\text{CE}}$
19	A ₁₀
20	$\overline{\text{OE}}$
21	$\overline{\text{WE}}$
22	A ₉
23	A ₈
24	V _{CC}

Pin Number Case X	Device Type 01, 02, 04, 05, and 10
1	NC
2	NC
3	NC
4	A ₇
5	A ₆
6	A ₅
7	A ₄
8	A ₃
9	A ₂
10	A ₁
11	A ₀
12	NC
13	DQ ₀
14	DQ ₁
15	DQ ₂
16	V _{SS}
17	NC
18	DQ ₃
19	DQ ₄
20	DQ ₅
21	DQ ₆
22	DQ ₇
23	$\overline{\text{CE}}$
24	A ₁₀
25	$\overline{\text{OE}}$
26	$\overline{\text{WE}}$
27	NC
28	A ₉
29	A ₈
30	NC
31	NC
32	V _{CC}

FIGURE 1. Terminal connections.

Pin Number Case R	Device Type 03, 06, 07, 08, and 9
1	A ₀
2	A ₁
3	A ₂
4	A ₃
5	A ₄
6	A ₅
7	A ₆
8	D _{OUT}
9	WE
10	GND
11	CE
12	D _{IN}
13	A ₇
14	A ₈
15	A ₉
16	A ₁₀
17	A ₁₁
18	A ₁₂
19	A ₁₃
20	V _{CC}

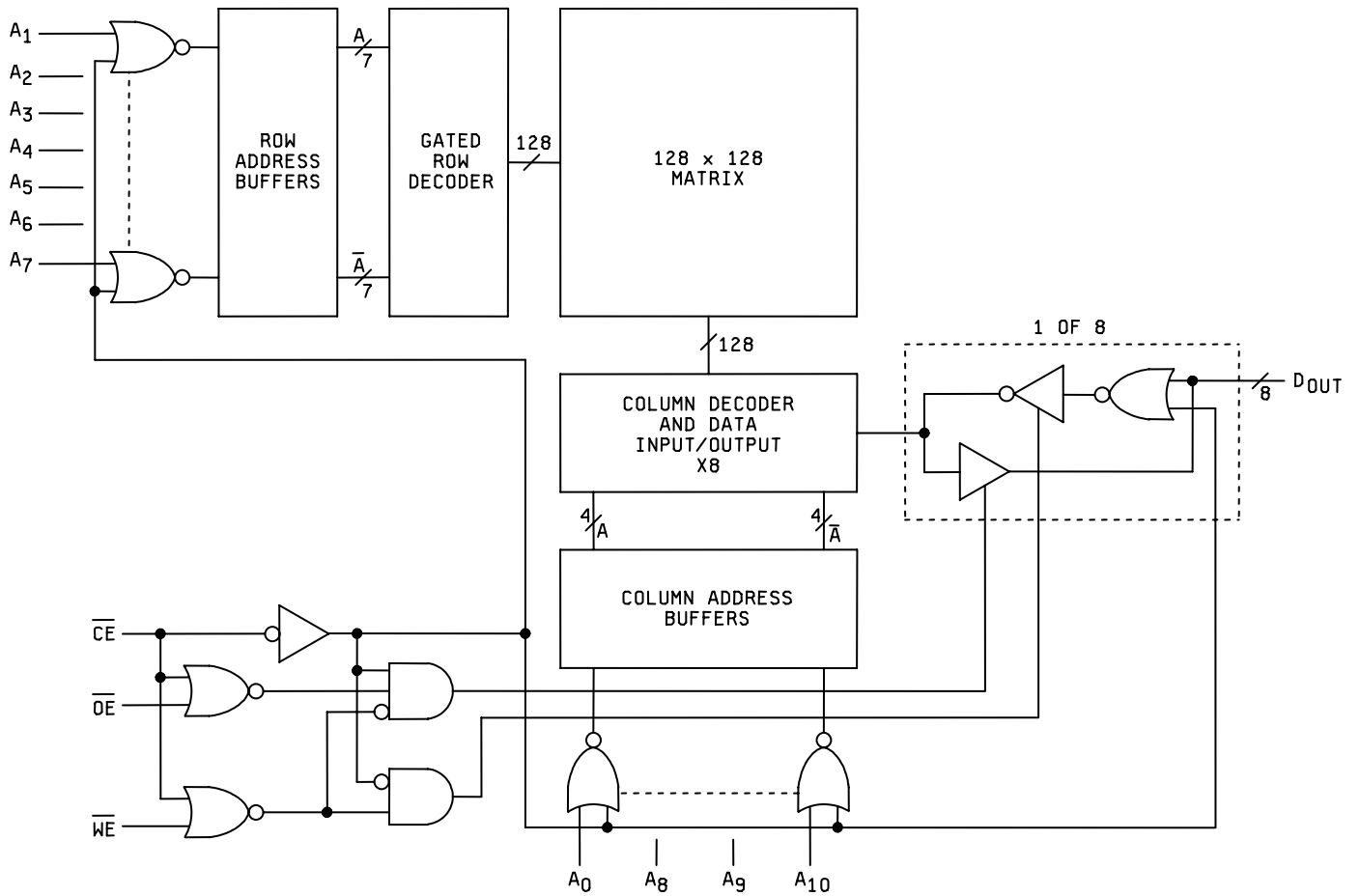
Pin Number Case Y	Device Type 03, 06, and 9
1	A ₀
2	A ₁
3	A ₂
4	A ₃
5	A ₄
6	A ₅
7	A ₆
8	D _{OUT}
9	WE
10	GND
11	CE
12	D _{IN}
13	A ₇
14	A ₈
15	A ₉
16	A ₁₀
17	A ₁₁
18	A ₁₂
19	A ₁₃
20	V _{CC}

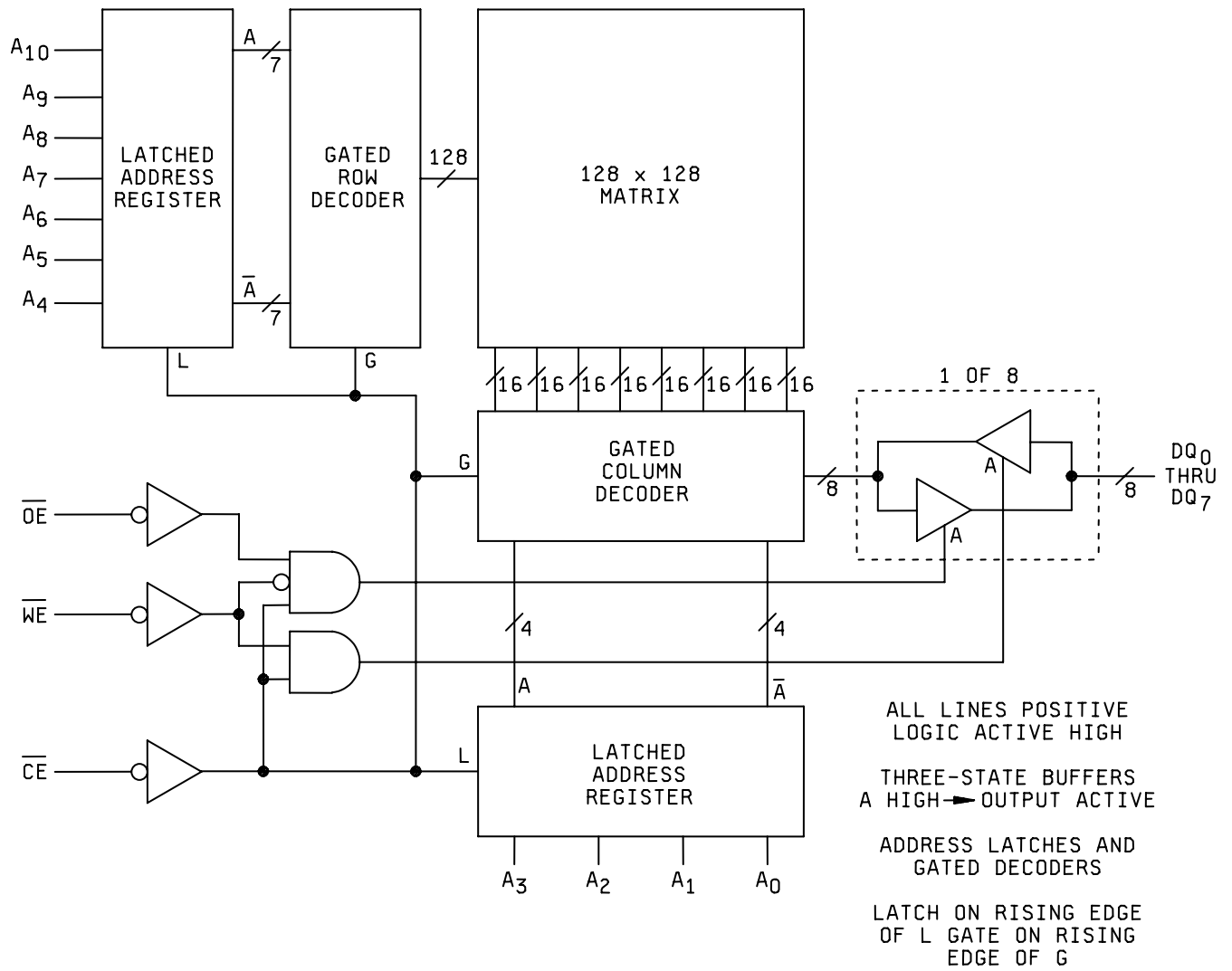
FIGURE 1. Terminal connections - Continued.

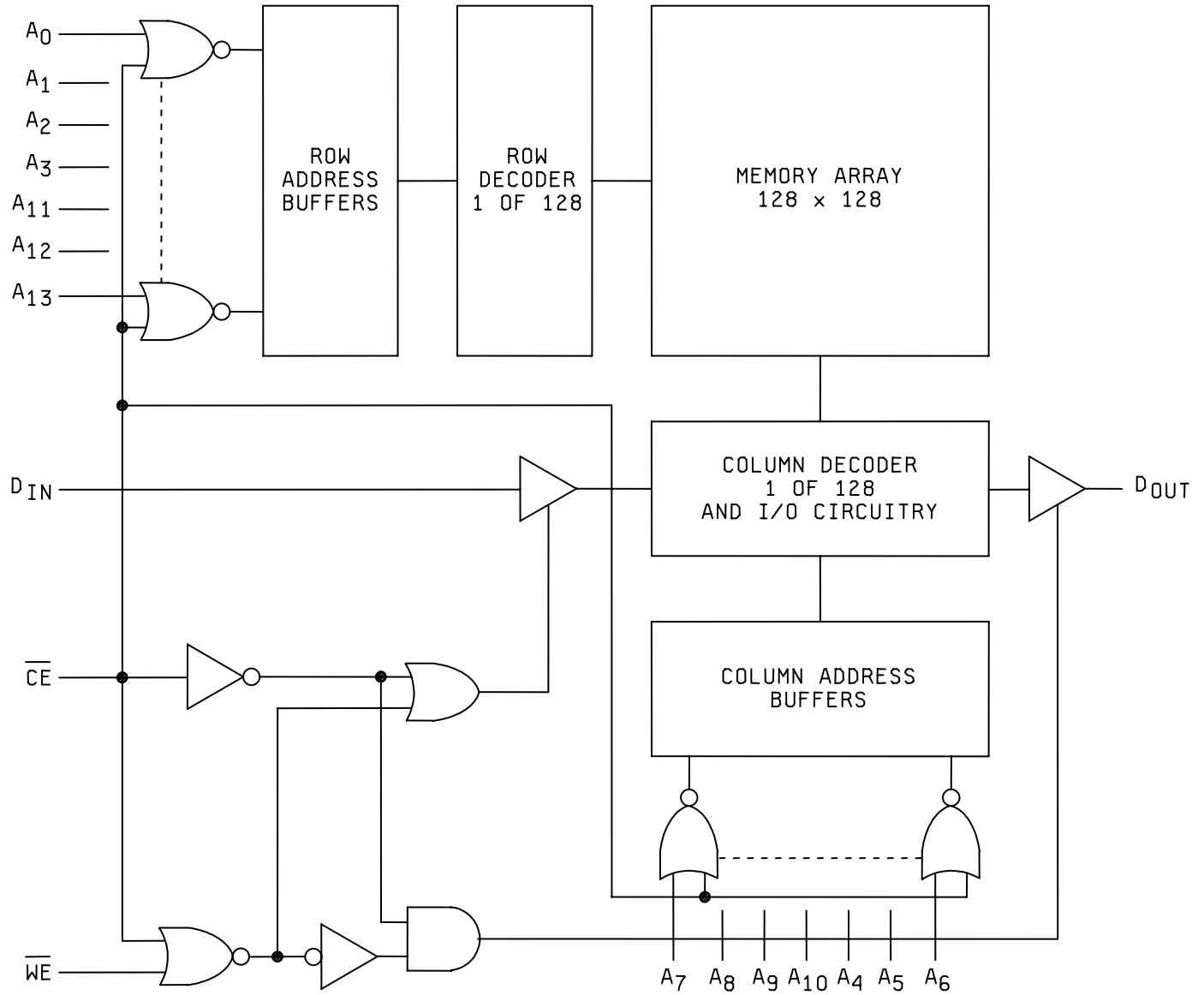
Pin Number Case Z	Device Type 07 and 08
1	A ₀
2	A ₁
3	A ₂
4	A ₃
5	A ₄
6	NC
7	NC
8	A ₅
9	A ₆
10	D _{OUT}
11	WE
12	GND
13	CE
14	D _{IN}
15	A ₇
16	A ₈
17	A ₉
18	NC
19	NC
20	A ₁₀
21	A ₁₁
22	A ₁₂
23	A ₁₃
24	V _{CC}

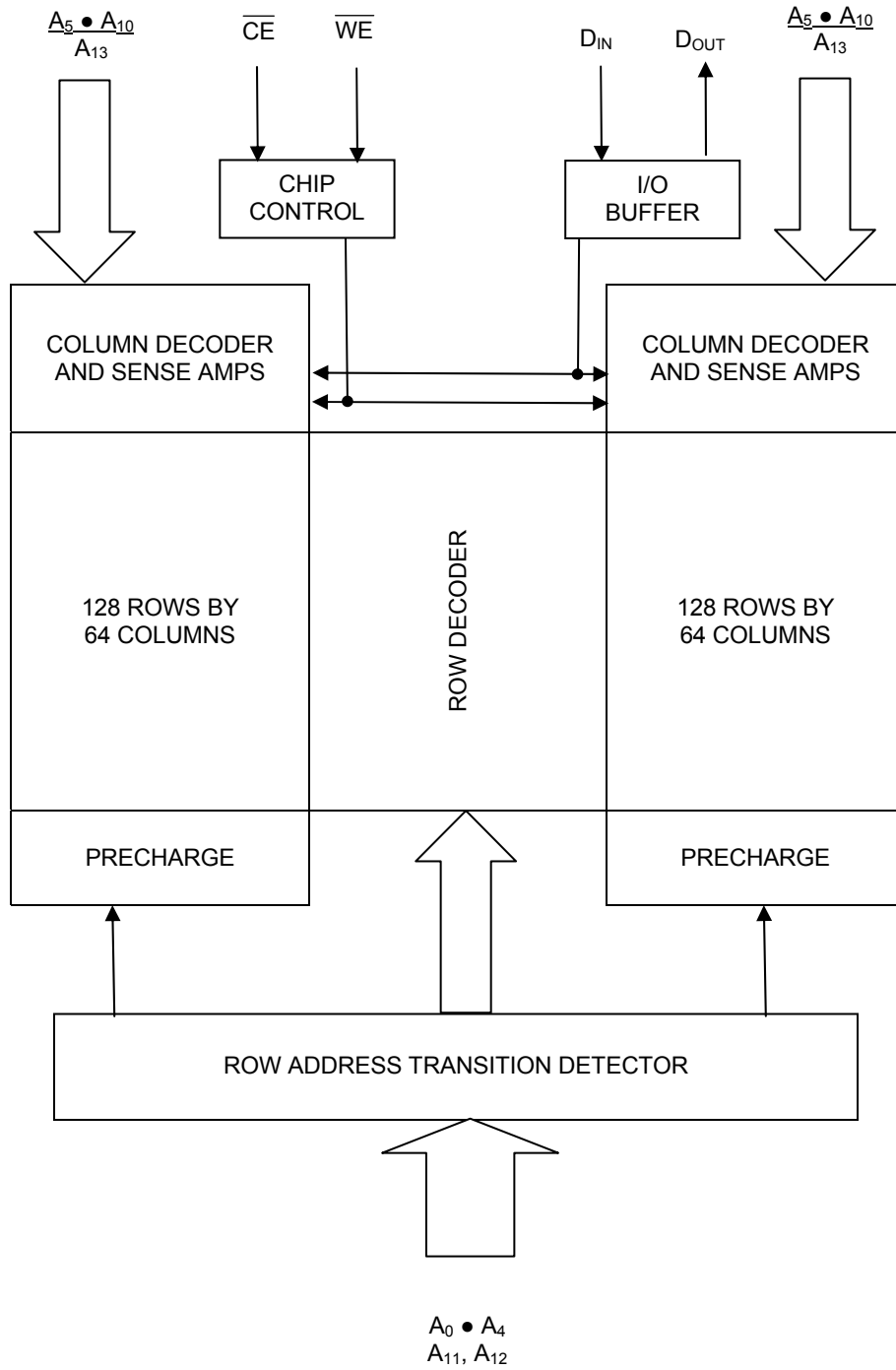
FIGURE 1. Terminal connections - Continued.

DEVICE TYPES 01,04,05 AND 10

FIGURE 2. Block Diagrams.

DEVICE TYPE 02FIGURE 2. Block Diagrams - Continued.

DEVICE TYPES 03,06 AND 09FIGURE 2. Block Diagrams - Continued.

Device types 07 and 08FIGURE 2. Block Diagrams - Continued.

Device types 01, 04, 05 and 10

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O operation
Standby	H	X	X	High Z
Read	L	L	H	D _{out}
Read	L	H	H	High Z
Write	L	X	L	D _{in}

Read Cycle
Device type 02

Inputs					Function
$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	A	DQ	
H	X	X	X	Z	Memory disable
	H	X	V	Z	Cycle begins, addresses are latched
L	H	L	X	X	Output enable
L	H	L	X	V	Output valid
	H	X	X	V	Read accomplished
H	X	X	X	Z	Prepare for next cycle
	H	X	V	Z	Cycle ends, next cycle begins

Write Cycle
Device type 02

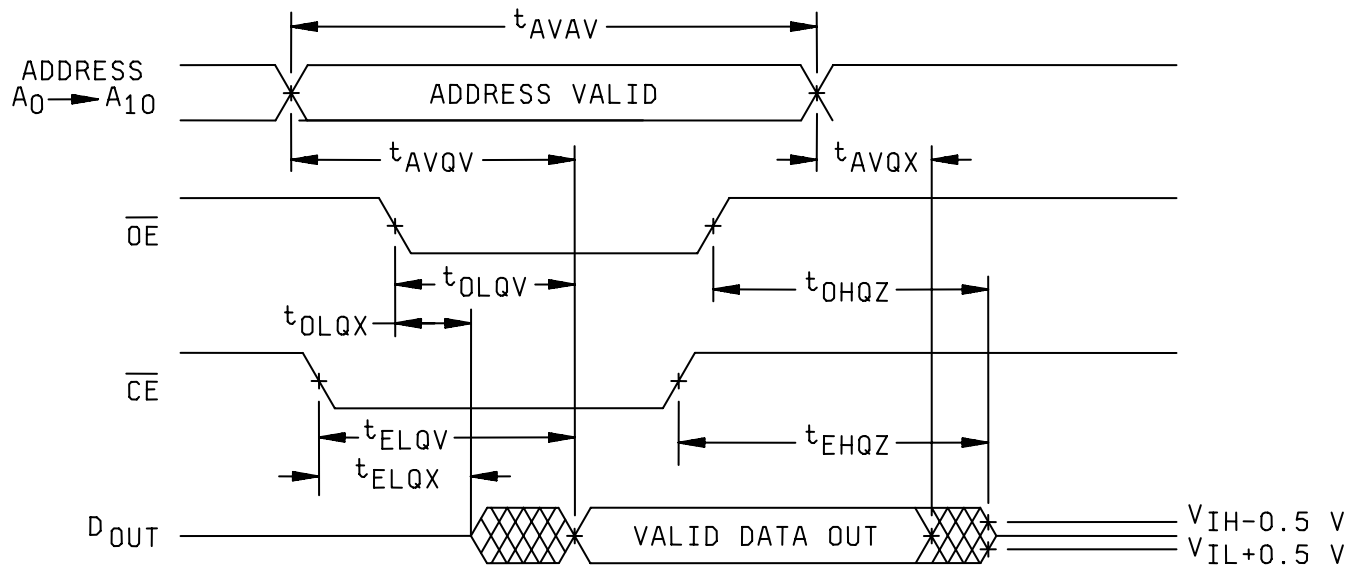
Inputs					Function
$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	A	DQ	
H	X	H	X	X	Memory disable
	X	H	V	X	Cycle begins, addresses are latched
L	L	H	X	X	Write period begins
L		H	X	V	Data in is written
	H	H	X	X	Write completed
H	X	H	X	X	Prepare for next cycle
	X	H	V	X	Cycle ends, next cycle begins

Device types 03, 06, 07, 08, and 09

Mode	$\overline{\text{CE}}$	$\overline{\text{WE}}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	D _{out}	Active
Write	L	L	High Z	Active

FIGURE 3. Truth Table.

READ CYCLE TIMING FOR DEVICE TYPES 01,04,05 AND 10



WRITE CYCLE TIMING FOR DEVICE TYPES 01,04,05 AND 10

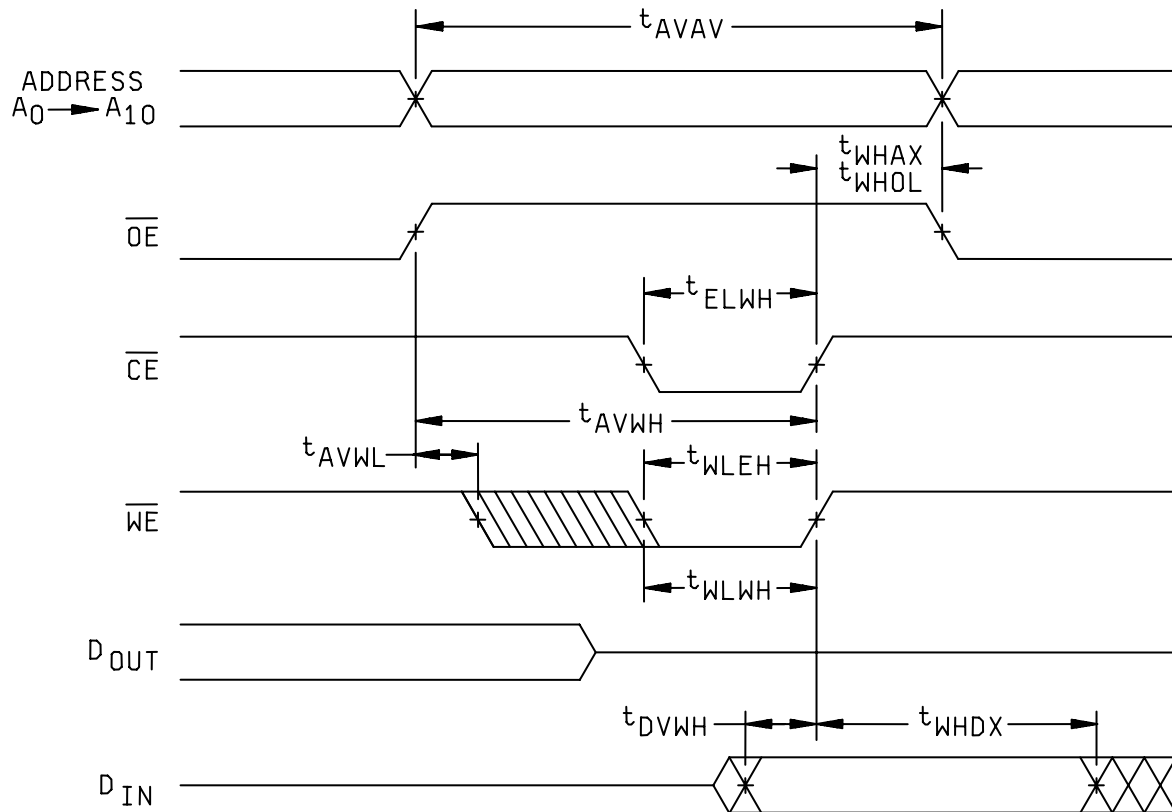
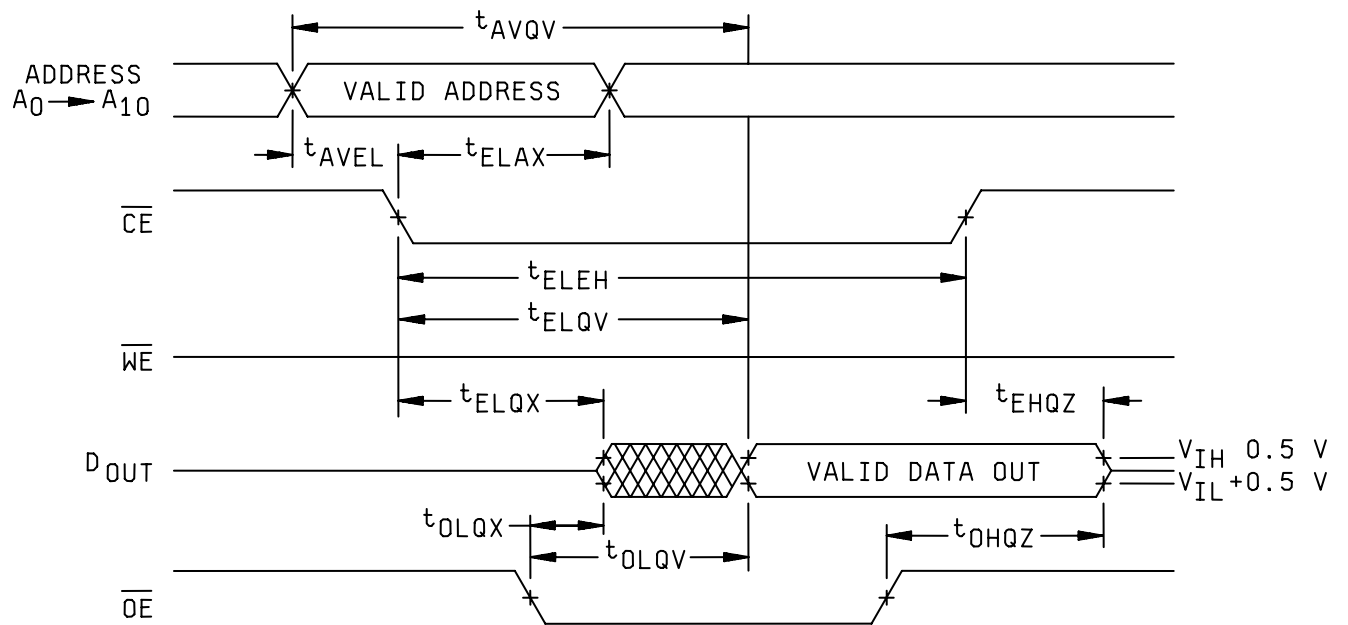
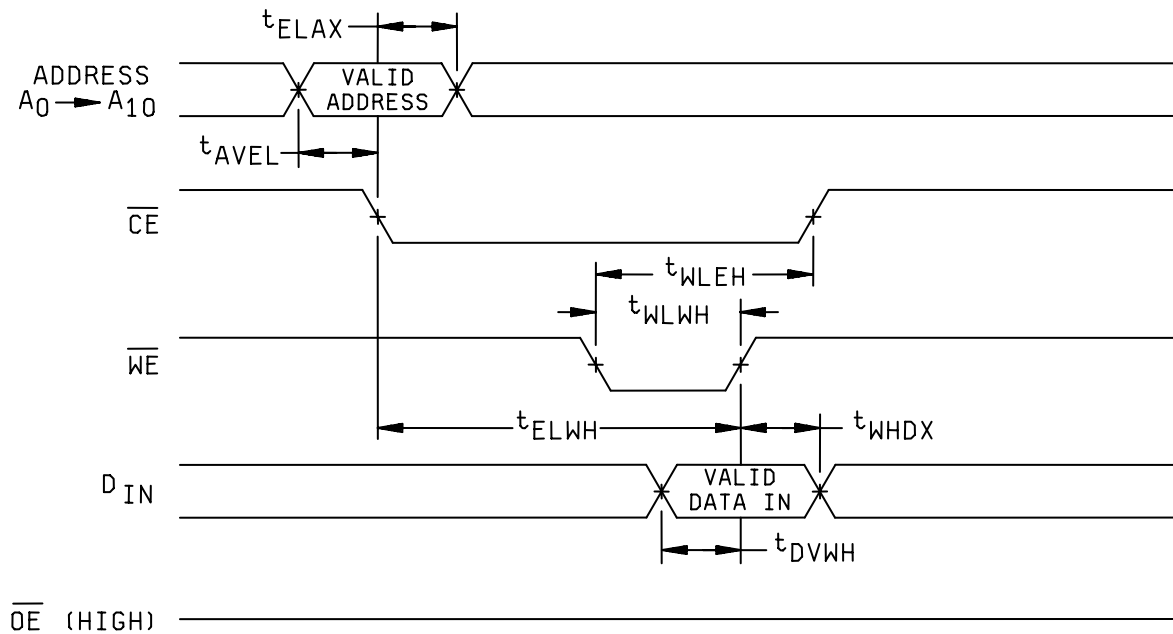


FIGURE 4. Timing diagrams.

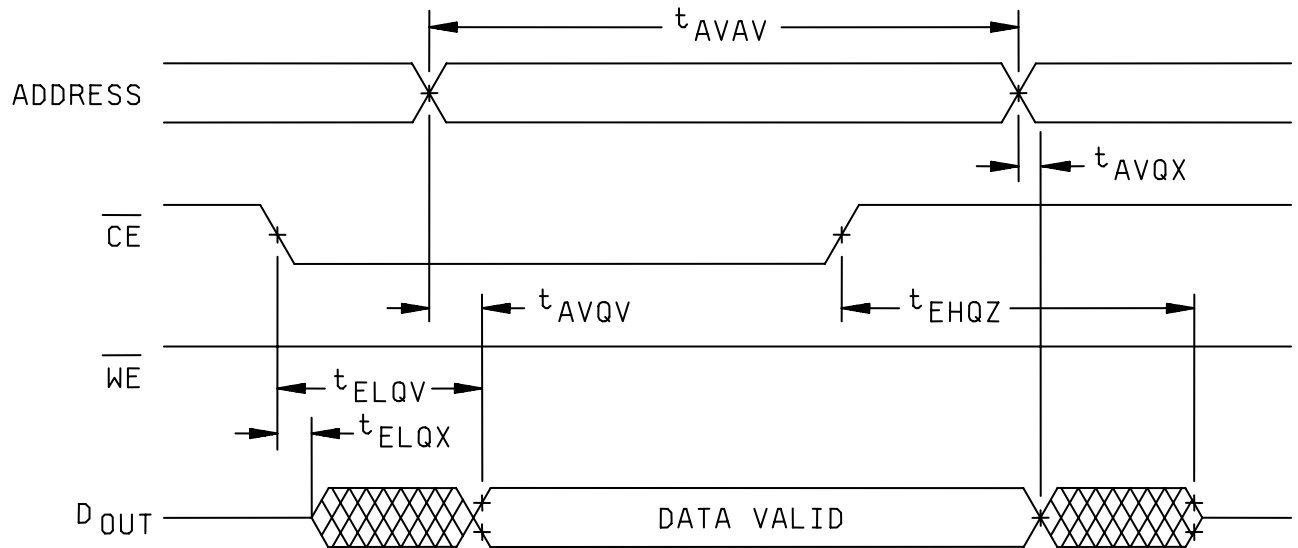
READ CYCLE TIMING FOR DEVICE TYPE 02



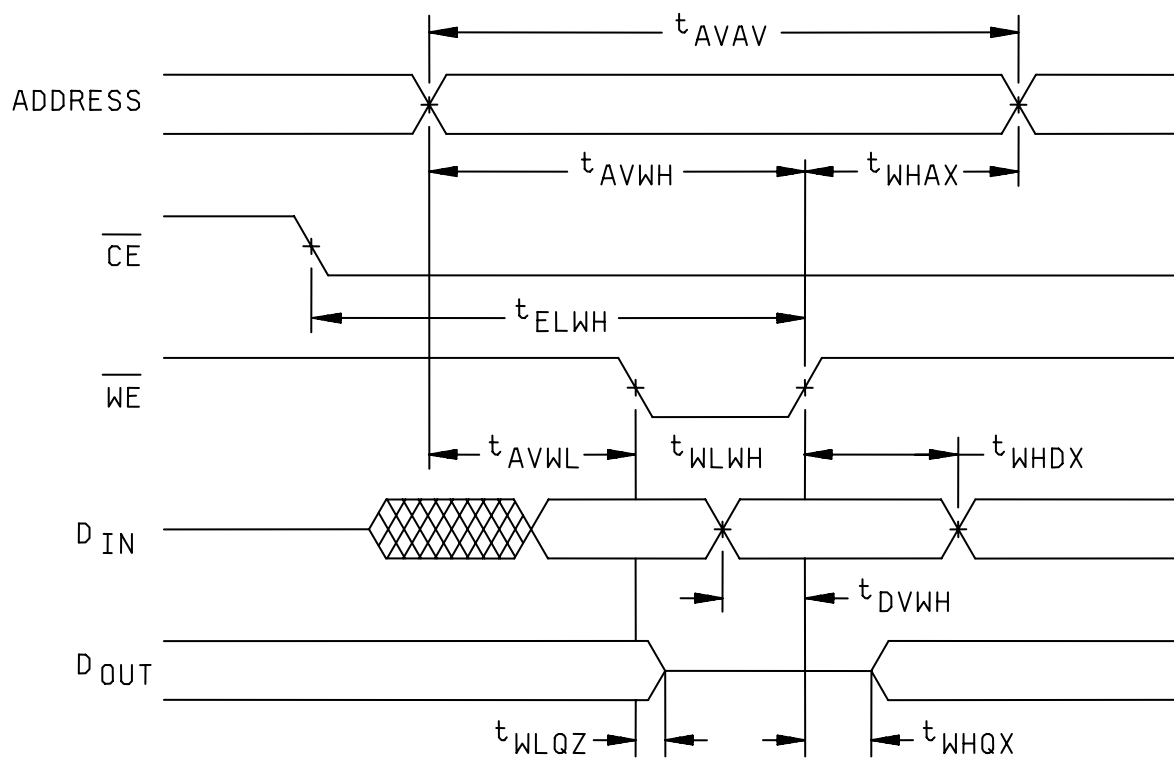
WRITE CYCLE TIMING FOR DEVICE TYPE 02

FIGURE 4. Timing diagrams - Continued.

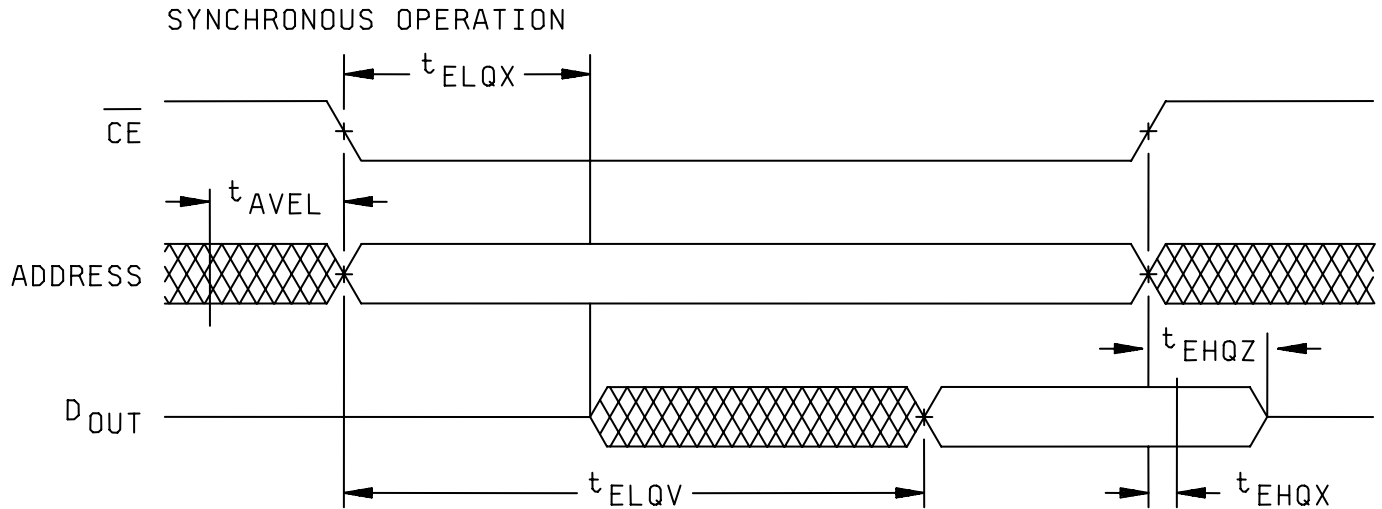
READ CYCLE TIMING FOR DEVICE TYPES 03,06 AND 09



WRITE CYCLE TIMING FOR DEVICE TYPES 03,06 AND 09

FIGURE 4. Timing diagrams - Continued.

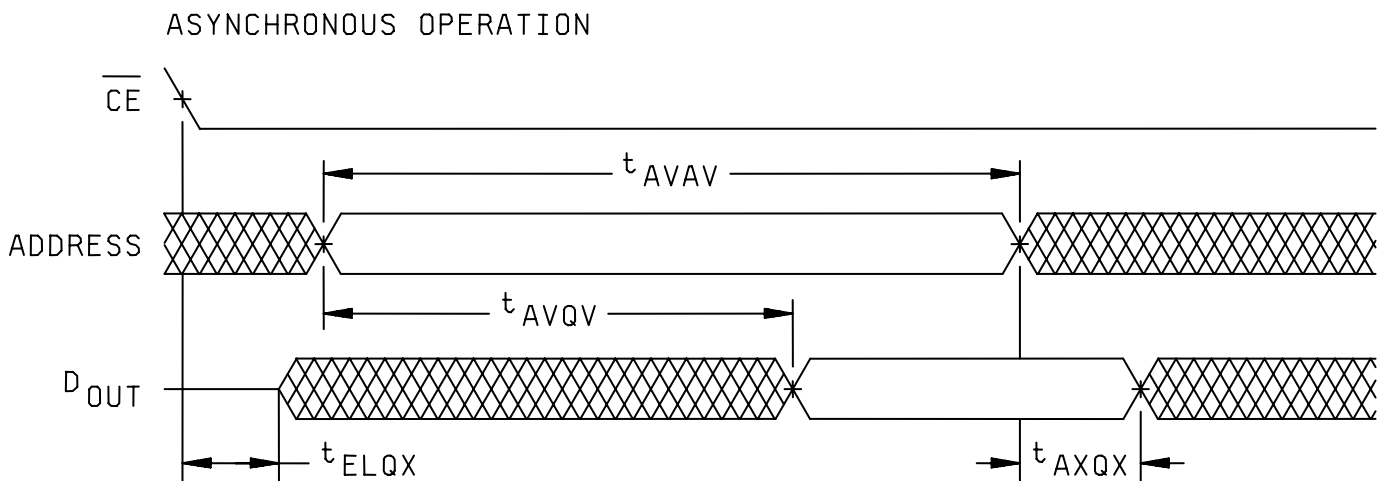
READ CYCLE TIMING FOR DEVICE TYPES 07 AND 08



NOTES:

1. $\overline{WE}$ is held high for entire cycle and D_{OUT} is ignored. Address is stable by the time $\overline{CE}$ goes low and remains valid until $\overline{CE}$ goes high.
2. See figure 6 for test conditions.

READ CYCLE TIMING FOR DEVICE TYPES 07 AND 08



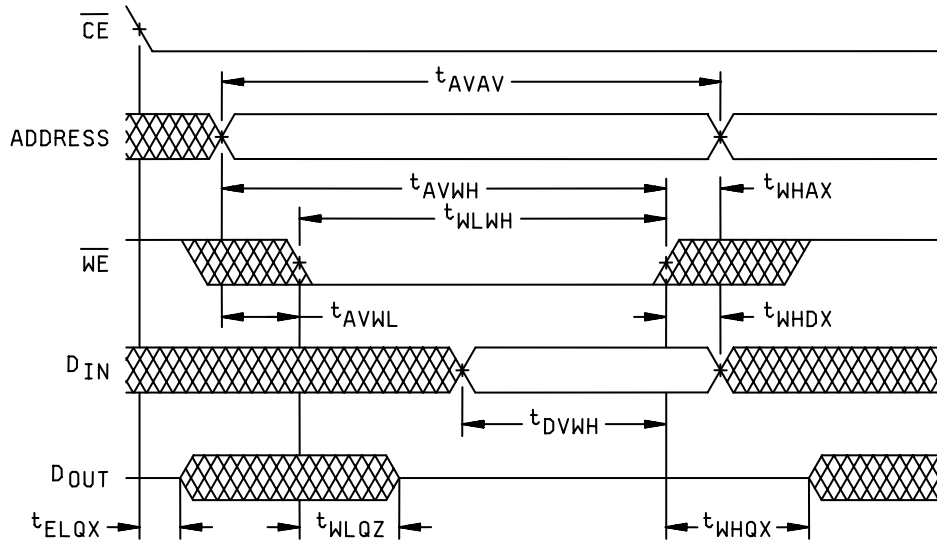
NOTES:

1. $\overline{WE}$ is high for entire cycle and D_{OUT} is ignored. $\overline{CE}$ is stable prior to address becoming valid and after address becomes invalid.
2. See figure 6 for test conditions.

FIGURE 4. Timing diagrams - Continued.

WRITE CYCLE TIMING FOR DEVICE TYPES 07 OR 08

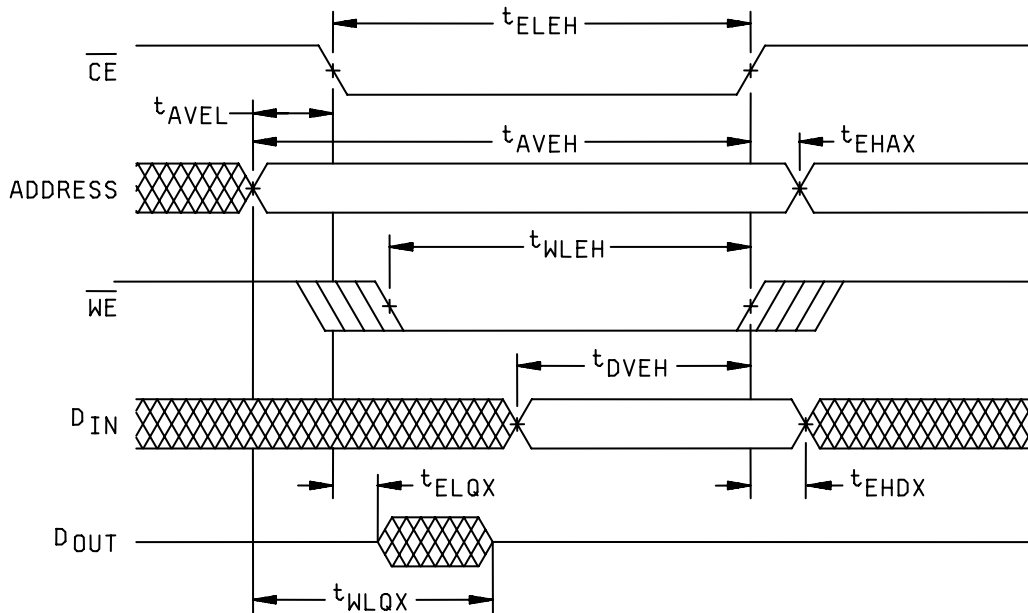
ASYNCHRONOUS OPERATION



NOTES:

1. In this mode, $\overline{CE}$ rises after $\overline{WE}$. The address must remain stable whenever both $\overline{CE}$ and $\overline{WE}$ are low.
2. See figure 6 for test conditions.

SYNCHRONOUS OPERATION

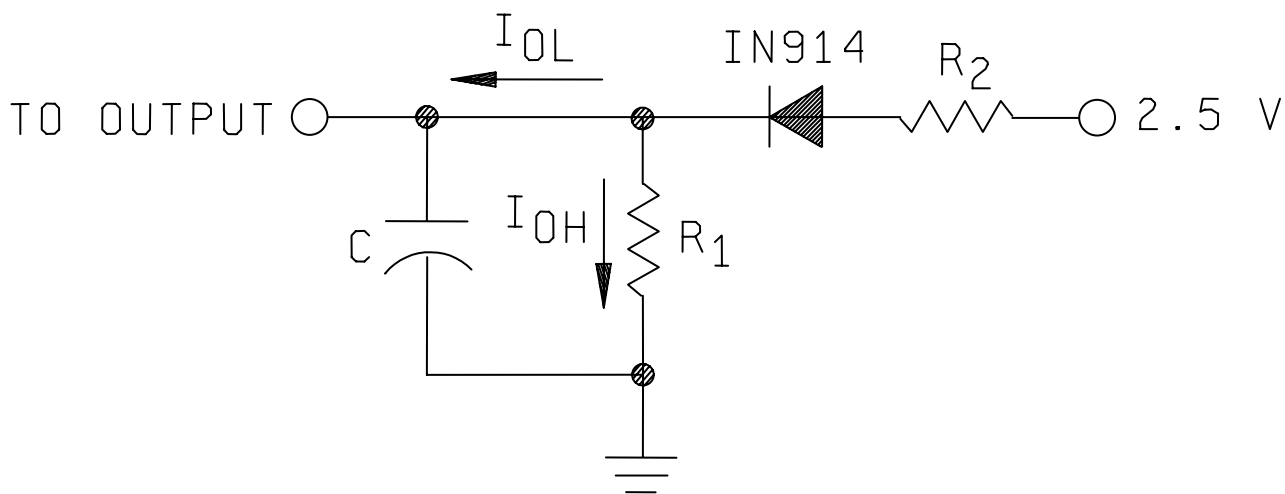


NOTES:

1. In this mode, $\overline{WE}$ rises after $\overline{CE}$. If $t_{WLEL} \neq 0$ ($\overline{WE}$ low before $\overline{CE}$) then D_{OUT} will remain in the high impedance state throughout the cycle. The address must remain stable whenever $\overline{CE}$ and $\overline{WE}$ are both low.
2. See figure 6 for test conditions.

FIGURE 4. Timing diagrams - Continued.

Device types 01, 05, and 06



Device types 01 and 05

NOTE:

$R_1 = 2.4 \text{ k}\Omega \pm 5\%$

$R_2 = 140 \text{ }\Omega \pm 5\%$

$C = 34 \text{ pF}$ including jig and probe capacitance

Device type 06

NOTE:

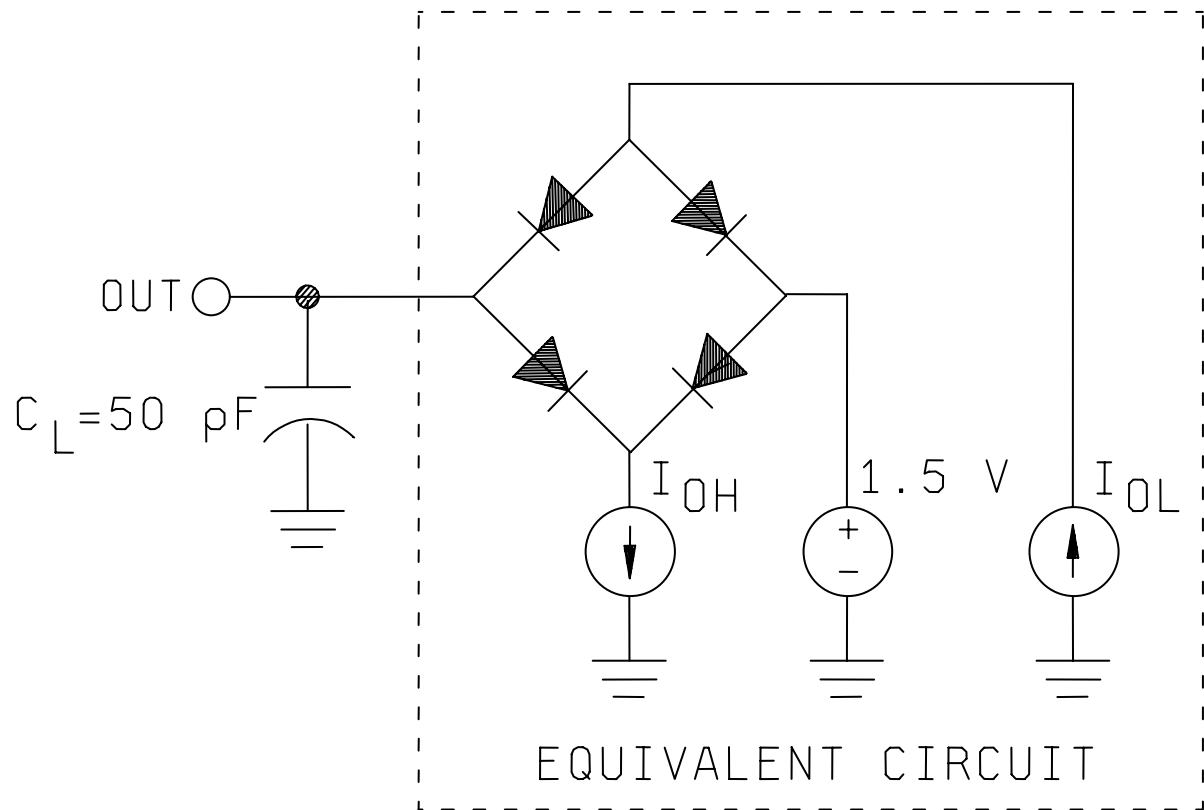
$R_1 = 620 \text{ }\Omega \pm 5\%$

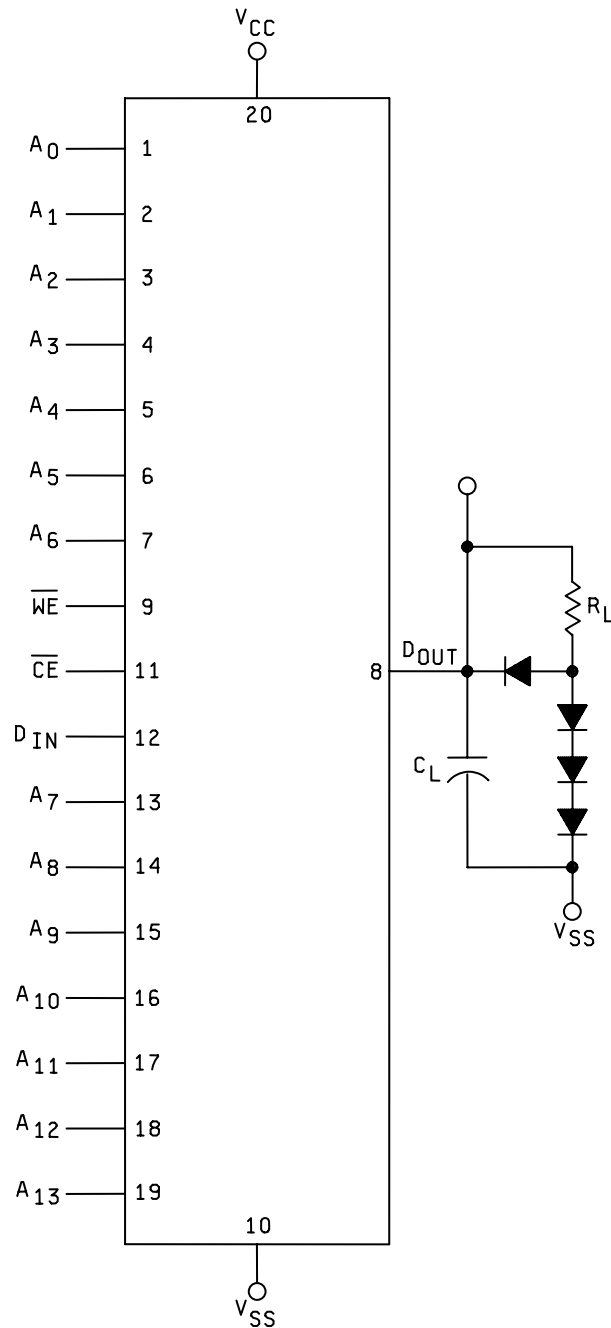
$R_2 = 180 \text{ }\Omega \pm 5\%$

$C = 30 \text{ pF}$ including jig and probe capacitance

Output load circuit

FIGURE 5. Output load and switching time test circuits.

Device types 02, 03, 04, 09, and 10FIGURE 5. Output load and switching time test circuits - Continued.

Device types 07 and 08

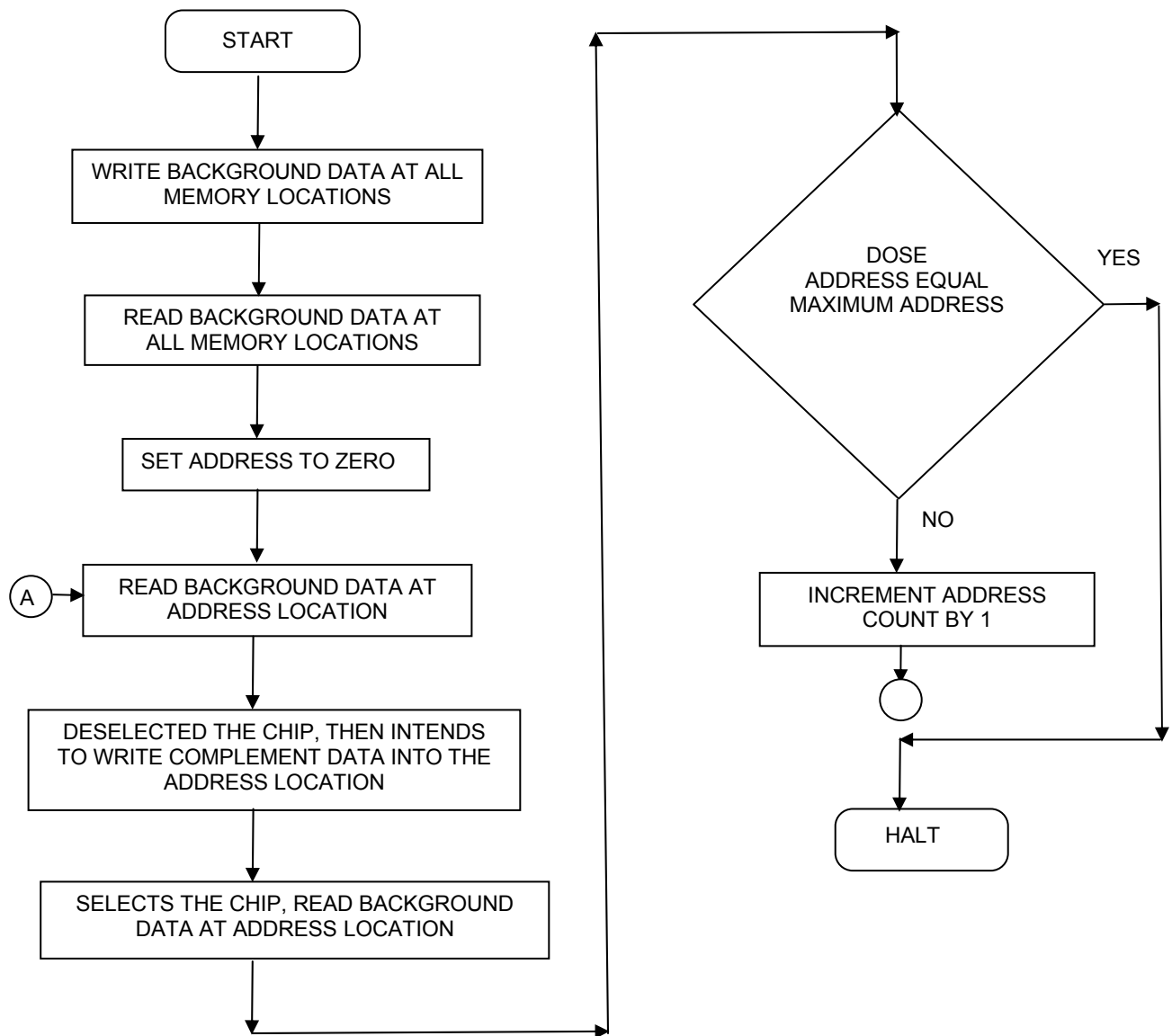
NOTES:

1. $C_L = 50 \text{ pF} \pm 10\%$ nominal.
2. $R_L = 2.2 \text{ k}\Omega \pm 10\%$.
3. Diodes are 1N914 or equivalent.
4. All t_{TLH} and $t_{THL} \leq 20 \text{ ns}$.
5. All generator output impedance = 50 ohms nominal.
6. All voltages measured with respect to V_{SS} terminal.
7. See figure 5 for waveforms and figure 7 for timing conditions.

FIGURE 5. Output load and switching time test circuits - Continued.

Timing parameter	Description	Device Type 07		Device Type 07		Unit
		Min	Max	Min	Max	
t _{AVAV}	Read cycle time	150	-----	175	-----	ns
t _{AVEL}	Address setup time	0	-----	0	-----	ns
t _{AVQV}	Address access time	-----	150	-----	175	ns
t _{ELQV}	Chip enable access time	-----	150	-----	175	ns
t _{ELQX}	Chip enable output enable time	20	-----	40	-----	ns
t _{EHQX}	Chip disable output hold time	20	-----	40	-----	ns
t _{AXQX}	Address invalid output hold time	40	-----	60	-----	ns
t _{EHQZ}	Chip disable output disable time	-----	25	-----	50	ns
t _{AVAV}	Write cycle time	150	-----	175	-----	ns
t _{ELWH}	Chip enable to end of write	100	-----	125	-----	ns
t _{WLWH}	Write enable pulse width	75	-----	100	-----	ns
t _{AVWL}	Address setup time	0	-----	0	-----	ns
t _{WHAX}	Address hold time	20	-----	25	-----	ns
t _{DVWH}	Data setup time	75	-----	100	-----	ns
t _{WHDX}	Data hold time	0	-----	0	-----	ns
t _{WLQZ}	Write enable output disable time	-----	25	-----	50	ns
t _{WHQX}	Write disable output enable time	0	-----	-----	-----	ns
t _{AVWH}	Address valid to end of write	100	-----	125	-----	ns
t _{AVEL}	Address setup time	0	-----	0	-----	ns
t _{EHAX}	Address hold time	0	-----	0	-----	ns
t _{AVEH}	Address valid to end of write	100	-----	125	-----	ns
t _{ELEH}	Enable pulse width	100	-----	125	-----	ns
t _{WLEH}	Write to end of write	100	-----	125	-----	ns
t _{DVEH}	Data setup time	75	-----	100	-----	ns
t _{EHDX}	Data hold time	0	-----	0	-----	ns

FIGURE 6. Timing test conditions over operating temperature range.



Step 1. Write the array with background data.

Step 2. Read the array for background data.

Step 3. Read address location zero for background data.

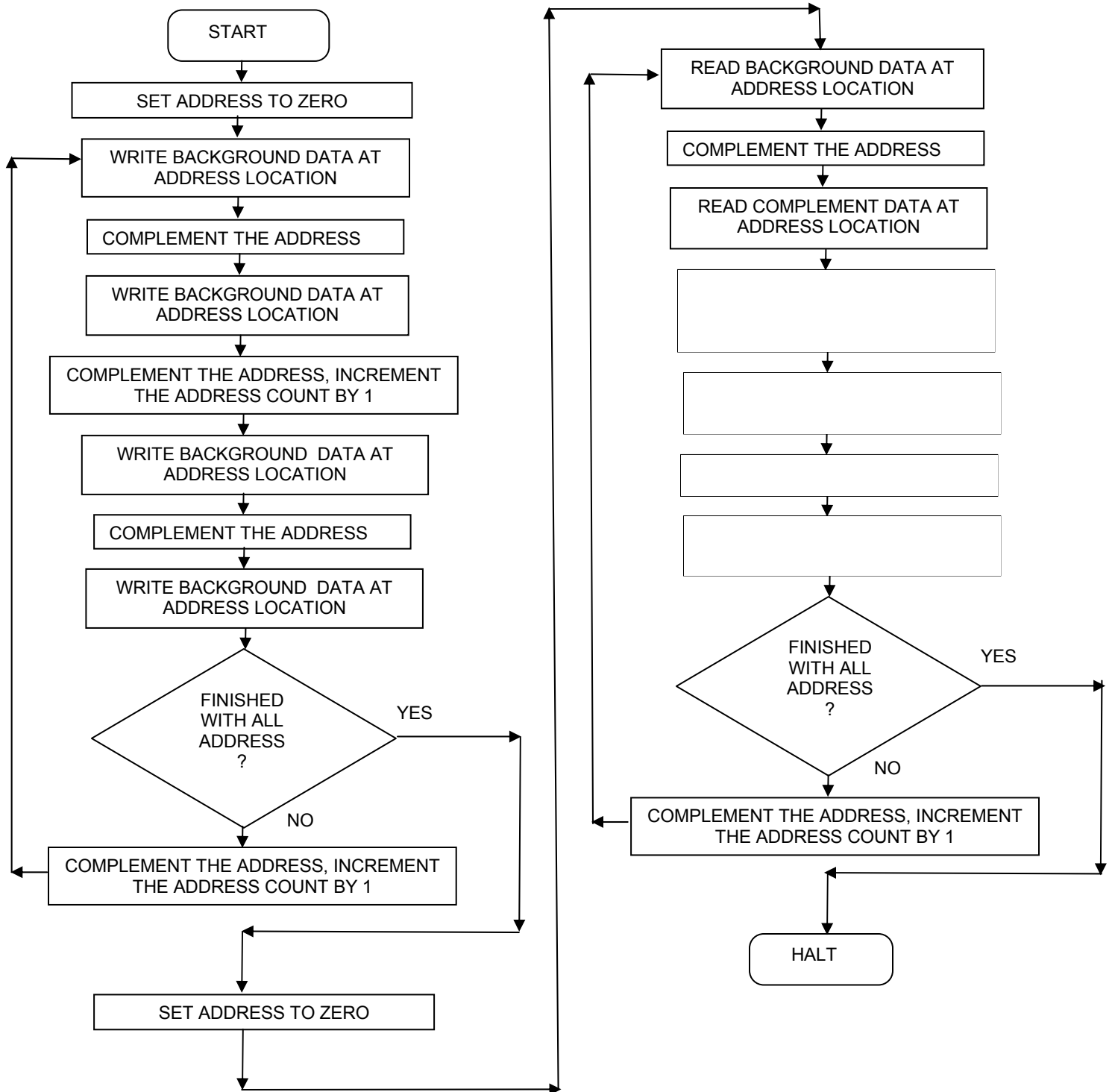
Step 4. Apply a Write cycle while deselecting the device (verifies that a Write operation cannot be performed while the device is disabled).

Step 5. Select the chip, and read address location zero for background data.

Step 6. Repeat steps 3 through 5 for each address location (sequentially).

Step 7. Repeat steps 1 through 6 with complement background data.

FIGURE 7. Not write pattern flow chart.



DATA = 1 COMPLEMENT DATA = 0 FOR DEVICE TYPE 01

DATA = 10101010 FOR DEVICE TYPE 02

COMPLEMENT DATA = 01010101

FIGURE 8. Write / write address complement flow chart.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.1.1 Step coverage acceptance criteria. The step coverage acceptance criteria (class S microcircuits) of 3.7.1 of method 2018 should read, "Oxide steps". All four directional edges of every type of oxide step (contact window or other type of oxide step) shall be examined (refer to 3.4.2). A directional edge shall be unacceptable if any defect or combination of defects, excluding thinning, reduces the cross section area on either side of the directional edge. The metal shall not be thinned to less than 4,000 Å. For an oxide step (contact window or other type of oxide step) to be acceptable, all four directional edges must be covered with metallization (in accordance with 3.4.2) and be acceptable (in accordance with the preceding sentence) except in the cases described in 3.7.1a and 3.7.1b. Where all contact cuts are completely covered by metal, the metallization viewed from the normal viewing angle (refer to 3.4.1) will show evidence of contoured metal flow into the contact area. Verification of the actual step coverage shall be determined by cross sectioning an additional die from the same wafer or using a test die to show contact step coverage of 4,000 Å or more.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.3 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted prior to qualification, and conformance inspection. The following additional criteria shall apply:

- a. Delete the sequence specified in 3.1.9 through 3.1.13 of method 5004 and substitute lines 1 through 5 of table II herein.
- b. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- c. Interim and final electrical parameters shall be as specified in table II, herein
- d. Post dynamic burn in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter measurements.
- e. The manufacturers of SOS devices shall use a high temperature stress test prior to the static burn in. Conditions shall be static II, +125°C, supply voltage at 7 V $\pm$ 0.5 V, and a duration of 48 hours minimum. A PDA of 15 percent shall be imposed. Devices need not be serialized prior to stress testing.
- f. At the manufacturer's option, class S visual inspection is to be performed in accordance with MIL-STD-883, method 2010, condition A, except as follows:
 - (1) High magnification inspection is performed at 100X to 300X on the high current area of the chip.
 - (2) Condition A criteria 3.1.1.1 and 3.1.1.2 shall be replaced by condition B criteria, respectively, however, the 75 percent of the original metal width over passivation step requirements shall be reduced to 50 percent, and underlying oxide must also be exposed.
 - (3) Criteria 3.1.1.7 shall apply to three areas, two opposite corners and one area in the center of sufficient complexity to assure general alignment and contact coverage, and shall consist only of the area in the immediate field of view.
 - (4) Condition A criteria 3.1.3c shall be replaced by condition B criteria. Cracks greater than 5 mils are rejected only if they point to or cross the scribe grid line.
 - (5) Burn in testing shall be performed at an operating voltage of 7 V $\pm$ 0.5 V, if this option is chosen.

g. At the manufacturer's option, the class B visual inspection is to be performed in accordance with MIL-STD-883, method 2010, condition B, except as follows:

- (1) Criteria 3.1.1 and 3.1.2 metallization scratches and voids, the 75 percent of the original metal width over passivation step requirements shall be reduced to 50 percent, and underlying oxide must also be exposed.
- (2) Criteria 3.1.7 shall apply to three areas, two opposite corners and one area in the center of sufficient complexity to assure general alignment and contact coverage, and consist only of the area in the immediate field of view.
- (3) Criteria 3.3c. Cracks greater than 5 mils are rejected only if they point or cross the scribe grid line.
- (4) Burn in testing shall be performed at an operating voltage of 7 ± 0.5 V, if this option is chosen.

4.3.1 Additional screening for space level product shall be as specified in MIL-PRF-38535.

4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- a. Tests shall be performed in accordance with table II herein.
- b. The following subgroups of table III of MIL-PRF-38535 shall be omitted:
 - (1) Class S devices: Subgroups 5, 6, and 7.
 - (2) Class B devices: Subgroups 5, 6, and 8.
- c. Subgroup 4 (C_i , C_o measurements) shall be measured only for initial qualification and after process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz and a signal amplitude not to exceed 50 mV rms. This test shall be performed using a fixed sample size of 25 devices and an acceptance number of zero.
- d. Subgroup 12 shall be added to the group A inspection requirements using a sample size series of 15 and shall consist of the procedures, test conditions, and limits specified in table III herein.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535 and as follows:

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- c. The devices selected for testing shall be programmed with a minimum of 50 percent of the total number of cells programmed. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for the RHA devices and shall be performed in accordance with MIL-PRF-38535, 4.5.4, and table VI herein.

4.5 Methods of Inspection. Methods of inspection shall be specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Delta measurements. Delta measurements, as specified in table II, shall be made and recorded before and after the required burn in screens and steady state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IV herein.

TABLE IV. Delta limits at +25°C

Parameters 1/	Limits		
	02, 03, 04, 09, 10	07, 08	01, 05, 06
I_{CC}	+30 μA	$\pm 30 \mu A$	
V_{OL}	+60 mV	± 40 mV	+60 mV
V_{OH}	-400 mV	± 340 mV	-200 mV
I_{IL}	-500 nA	± 100 nA	-50 nA
I_{IH}	+500 nA	± 100 nA	+50 nA

1/ Conditions and mechanization of measurements shall be as specified in table III, subgroup 1.

4.5.3 Quiescent supply current tests. When performing quiescent supply current measurements, the meter shall be placed so that all currents flow through the meter.

4.5.4 RHA testing. The RHA testing shall be performed in accordance with procedures and sampling specified in MIL-PRF-38535 and herein:

a. Before irradiation, selected samples shall be assembled in qualified packages and pass the governing electrical parameters (group A, subgroup 1 at +25°C).

b. Radiation exposure shall be performed according to method 1019 of MIL-STD-883 with the devices biased in accordance with table V, and meet the group E end point electrical parameters as defined in table I at +25°C $\pm 5^\circ C$ after exposure. The ionizing radiation exposure shall be 200 KRads (Si).

4.6 Data reporting. When specified in the contract or purchase order, a copy of the following data, as applicable, shall be supplied:

- Attributes data for all screening tests (see 4.3) and variables data for all static burn in, dynamic burn in, and steady state life tests.
- A copy of each radiograph.
- The quality conformance inspection data (see 4.4).
- Parameter distribution data on parameters evaluated during burn in.
- Final electrical parameters data.

TABLE V. Bias during exposure to radiation.

Device type	Pin connections	$V_{SS} = \text{GND}$	$V_{CC} = 5 \text{ V dc}$
	V_{CC} (through a 1 k Ω to 60 k Ω resistor)		
07	1, 2, 3, 4, 5, 6, 7, 8*, 9, 11, 12, 13, 14, 15, 16, 17, 18, 19	10	20
08	1, 2, 3, 4, 5, 6, 7, 8*, 9, 11, 12, 13, 14, 15, 16, 17, 18, 19	10	20

* Output pins connected to voltage divider.

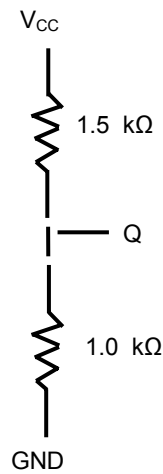


TABLE VI. Group E end-point electrical parameter limits for devices 07 and 08.

Test	Symbol	Conditions 1/ $V_{SS} = 0\text{ V}$, $V_{CC} = 5.5\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ Unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Low level output voltage	V_{OL}	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 5.0\text{ mA}$	07 08		0.4 0.4	V V
High level output voltage	V_{OH}	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -5\text{ mA}$	07 08	4.0 4.0		V V
Input leakage current	I_{IH}	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 5.5\text{ V}$	07 08		1.0 1.0	μA μA
Input leakage current	I_{IL}	$V_{CC} = 5.5\text{ V}$ $V_{IN} = \text{GND}$	07 08		-1.0 -1.0	μA μA
High impedance output leakage	I_{OHZ}	$V_{CC} = 5.5\text{ V}$	07 08		10.0 10.0	μA μA
High impedance	I_{OLZ}	$V_{CC} = 5.5\text{ V}$	07 08		-10.0 -10.0	μA μA
Standby supply	I_{CC}	$V_{CC} = 5.5\text{ V}$	07 08		200 5	μA mA
Data retention supply voltage	V_{CCDR}	$V_{CC} = 3.0\text{ V}$ minimum (see power down test in table III)	07 08	3.0 3.0		V V
Operating current	I_{CCOP}	$T_C = +25^{\circ}\text{C}$, $V_{CC} = 5.5\text{ V}$ $f = 1\text{ MHz}$	07 08		6 6	mA mA
Data retention quiescent supply current	I_{CCDR}	$V_{CC} = 3.0\text{ V}$, $I_O = 0$ $V_I = V_{CC}$ or GND	07 08		100 100	μA μA
Input capacitance	C_i	$V_{CC} = 5.5\text{ V}$, $V_{IN} = V_{CC}$ or GND $f = 1\text{ MHz}$	07 08		8 8	pF pF
Address access time	t_{AVQV}	See table III	07 08	150 175		ns ns
Chip enable access	t_{ELQV}		07 08	150 175		ns ns
Read cycle time	t_{AVAV}		07 08	150 175		ns ns
Chip enable output time	t_{ELQX}		07 08	20 40		ns ns
Chip enable output disable	t_{EHQZ} 1/		07 08		25 50	ns ns
Chip enable pulse negative width	t_{ELEH}		07 08	100 125		ns ns
Chip disable output hold time	t_{EHQX}		07 08	20 40		ns ns
Address setup time	t_{AVEL}		07 08	0 0		ns ns
Address invalid output hold time	t_{AXQX}		07 08	40 60		ns ns
Write enable pulse width	t_{WLWH}		07 08	75 100		ns ns
Write enable pulse setup time	t_{WLEH}		07 08	100 125		ns ns
Address setup time	t_{AVWL}		07 08	0 0		ns ns
Chip enable to end of write	t_{ELWH}		07 08	100 125		ns ns

See footnote at end of table.

TABLE VI. Group E end-point electrical parameter limits for devices 07 and 08 - Continued.

Test	Symbol	Conditions ^{1/} $V_{SS} = 0\text{ V}$, $V_{CC} = 5.5\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ Unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Write disable output enable time	t_{WHQX}	See table III	07 08	0 0		ns ns
Address valid to end of write	t_{AVWH}		07 08	100 125		ns ns
Address hold time	t_{WHAX}		07 08	15 25		ns ns
Address hold time	t_{EHAX}		07 08	0 0		ns ns
Address valid to end of write	t_{AVEH}		07 08	100 125		ns ns
Write enable output disable time	t_{WLQZ}		07 08		25 50	ns ns
Data setup time	t_{DVWH}		07 08	75 100		ns ns
Data hold time	t_{WHDX}		07 08	0 0		ns ns
Data setup time	t_{DVEH}		07 08	75 100		ns ns
Data hold time	t_{EHDX}		07 08	0 0		ns ns

^{1/} This parameter is guaranteed, but not tested.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but it is not mandatory)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. The acquisition document should specify the following:

- a. Title, number, and date of the specification.
- b. PIN and compliance identifier, if applicable (see 1.2).
- c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirement for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to the acquiring activity in addition to notification to the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for special lead lengths or lead forming, if applicable. These requirements will not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by, or direct shipment to the Government.
- i. Requirements for "JAN" marking.
- k. Packaging requirements (see 5.1).

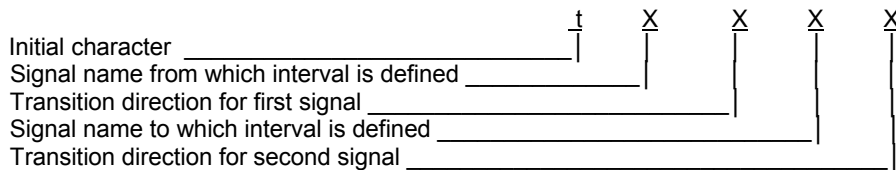
6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

V_{SS}	Common or reference voltage mode.
V_{CC}	Supply voltage.
A0 - A13	Address inputs, used to address 1 of 16, 384/1 bit locations in static storage array.
$\overline{CE}$	Chip enable, used along with the write enable ($\overline{WE}$) signal to control the states of the data in (D_{IN}) and data out (D_{OUT} / D_Q) buses.
D_{OUT} / D_Q	Data output.
D_{IN}	Data input through which data is stored.
$\overline{WE}$	Write enable, used to select the Read or Write mode.
I_{CC}	Supply current.
I_{IH}, I_{IL}	Input leakage current.
I_{OHZ}, I_{OLZ}	High impedance output leakage current.
V_{IL}	Logical low input voltage.
V_{IH}	Logical high input voltage.
V_{OL}	Logical low output voltage.
V_{OH}	Logical high output voltage.
C_i	Input capacitance.
C_o	Output capacitance.
t_{ELQV}	Chip enable access time.
t_{AVQV}	Address access time.
t_{EHQZ}	Chip enable to output disable.
t_{AVAV}	Read cycle time.
t_{AVQX}	Output hold after address change.
t_{ELQX}	Chip enable to output active.
t_{WLWH}	Write pulse width.
t_{ELWH}	Chip enable to end of write.
t_{DVWH}	Data setup to end of write.
t_{WHDX}	Data hold after end of write.
t_{AVWL}	Address setup before write enable low.
t_{AVWH}	Address setup up to end of write.
t_{WHAV}	Write recovery time
t_{OLQV}	Output enable access time.
t_{OLQX}	Output enable to output active.
t_{OHQX}	Output enable to output disable time.
t_{AVEL}	Address to chip enable setup time.
t_{ELAX}	Address to chip enable hold time.
t_{ELEH}	Chip enable pulse negative width.
t_{EHEL}	Chip enable pulse positive width.
t_{WLEH}	Write enable pulse setup time.
t_{ELEL}	Read or write cycle time.

6.5.1 Timing parameter abbreviations. All timing abbreviations used lower case characters with upper case character subscripts. The initial character is always t and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transition. Thus, the format is:



Signal definitions:

A = Address

 D_{IN} = Data in D_{OUT}/D_Q = Data out $\overline{WE}$ = Write enable $\overline{CE}$ = Chip enable

O = Output enable

Transition definitions:

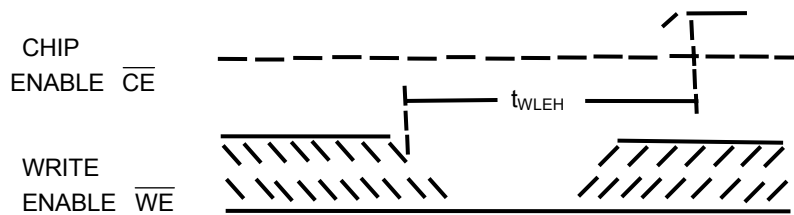
H = Transition to high

L = Transition to low

V = transition to valid

X = Transition to invalid or don't care

Z = Transition to off (high impedance)



The example shows Write pulse setup time defined as t_{WLEH} -time from Write Enable to Low Chip Enable High.

Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of views. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Waveforms:

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming will not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic industry type. Generic industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

<u>Device type</u>	<u>Commercial type</u>
01, 04, 05	6116
02	6516
03, 09	65262
04, 10	65162
06	61C16
07	65C262RH
08	65T262RH

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extent of the changes..

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of the events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This Appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS.

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Address complement, data background = all "0's".

This pattern produces maximum address line noise. It is performed in the following manner:

- Step 1. Load memory with background data.
- Step 2. Read minimum address location.
- Step 3. Load minimum address location with "1".
- Step 4. Read maximum address location.
- Step 5. Load maximum address location with "1".
- Step 6. Read minimum address location +1.
- Step 7. Load minimum address location +1 with "1".
- Step 8. Read maximum address location -1.
- Step 9. Load maximum address location -1 with "1".
- Step 10. Repeat steps 2 through 9 until all address locations have been read and loaded with "1's".
- Step 11. Repeat steps 2 through 10 reading "1's" and loading "0's".
- Step 12. Read memory, all "0's".

A.3.2 Algorithm B (pattern 2).

A.3.2.1 GALPAT (ping pong) data background = "0".

This pattern tests for performance sensitivities by testing all possible combinations of address and data out transitions. It is performed in the following manner:

- Step 1. Load memory with data background.
- Step 2. Write data complement in location 0 (test bit).
- Step 3. Alternately read test bit and each location in the array.
- Step 4. Write the test bit back to background data.
- Step 5. Repeat steps 2 through 4 with each location in the array.
- Step 6. Repeat steps 1 through 5 with complemented background data.

APPENDIX A

A.3.3 Algorithm C (pattern 3).A.3.3.1 March data, data background = all "0's".

This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

- Step 1. Load memory with background data.
- Step 2. Read location 0.
- Step 3. Write data complement in location 0.
- Step 4. Read data complement in location 0.
- Step 5. Repeat steps 2 through 4 for all other locations in memory (sequentially).
- Step 6. Read data complement at location 0.
- Step 7. Write data at location 0.
- Step 8. Read data at location 0.
- Step 9. Repeat steps 6 through 8 for all other locations in the memory (sequentially).
- Step 10. Repeat steps 1 through 9 with data background of all "1's".

A.3.4 Algorithm D (pattern 4).A.3.4.1 Data retention, data background = checkerboard.

This algorithm tests for data retention mode functionality. It is performed in the following manner:

- Step 1. Load memory with background data.
- Step 2. Set chip enable = V_{CC} .
- Step 3. Reduce V_{CC} and chip enable to minimum V_{DR} .
- Step 4. Pause for 200 ms.
- Step 5. Bring V_{CC} and chip enable back up and test for background data.
- Step 6. Repeat steps 1 through 5 with complemented background data.

A.3.5 Algorithm E (pattern 5).A.3.5.1 Checkerboard, checkerboard.

- Step 1. Load memory with a checkerboard pattern.
- Step 2. Read the memory, verifying the checkerboard pattern.
- Step 3. Load the memory with a checkerboard pattern.
- Step 4. Read the memory, verifying the checkerboard pattern.

A.3.6 Algorithm F (pattern 6).A.3.6.1 Butterfly.

- Step 1. Write a background pattern of "0's" throughout the memory.
- Step 2. Write a "1" (test bit) at the first location.
- Step 3. Read the test cell and the next sequential cell in the same row, then the test cell and the next sequential cell in the same column, until all cells have been tested in the same row and column as the test cell.
- Step 4. Rewrite the test cell to "0", write a "1" into the next cell which will become the test cell, then repeat the ping-pong row column march.
- Step 5. After all cells have been used as test cells, repeat the test with complement data.

A.3.7 Algorithm G (pattern 7).A.3.7.1 Spiral complement.

- Step 1. Write a background pattern of "0's" in all cells.
- Step 2. Beginning at cell "0", write and read a diagonal of "1's" on the field "0's".
- Step 3. Shift the diagonal one increment in the x direction until each row has been used as a starting point of the diagonal and all cells within the diagonal have been tested.
- Step 4. Repeat the test with complement data.

Custodians:

Army – CR
Navy - EC
Air Force – 11
DLA-CC

Preparing activity:

DLA - CC

Review activities:

Army – MI, SM
Navy – AS, CG, MC, SH TD
Air Force – 03, 19, 99

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NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://assist.daps.dla.mil>.