

MILITARY SPECIFICATION

MICROCIRCUITS, MEMORY, DIGITAL, CMOS
32K X 8-BIT, ELECTRICALLY ERASABLE PROGRAMMABLE
READ-ONLY MEMORY (EEPROM), MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS, 32K words/8-bit, 5.0-volt, electrically erasable programmable read-only memory microcircuits. Two product assurance classes (B and S), a choice of lead finish and three package types are provided for each device and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device types. The device types shall be as shown in the following:

Device type	Circuit organization	Access time	Write speed	Write mode	Endurance	Software data protect
01	32K words/8-bit	350 ns	10 ms	Byte/page	10,000 cy	No
02	32K words/8-bit	300 ns	10 ms	Byte/page	10,000 cy	No
03	32K words/8-bit	250 ns	10 ms	Byte/page	10,000 cy	No
04	32K words/8-bit	200 ns	10 ms	Byte/page	10,000 cy	No
05	32K words/8-bit	150 ns	10 ms	Byte/page	10,000 cy	No
06	32K words/8-bit	250 ns	10 ms	Byte/page	100,000 cy	No
07	32K words/8-bit	350 ns	10 ms	Byte/page	10,000 cy	Yes
08	32K words/8-bit	300 ns	10 ms	Byte/page	10,000 cy	Yes
09	32K words/8-bit	250 ns	10 ms	Byte/page	10,000 cy	Yes
10	32K words/8-bit	200 ns	10 ms	Byte/page	10,000 cy	Yes
11	32K words/8-bit	150 ns	10 ms	Byte/page	10,000 cy	Yes
12	32K words/8-bit	250 ns	10 ms	Byte/page	100,000 cy	Yes

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
U	Figure 1 (28-lead, .660" x .560" x .100"), pin grid array
X	D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package
Y	C-12 (32-terminal, .560" x .458" x .120"), rectangular chip carrier package
Z	F-12 (28-lead, .740" x .420" x .130"), flat package

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RBE-2, Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.
--

MIL-M-38510/261

1.3 Absolute maximum ratings.

All input and output voltages (including V_{CC})	1/-	-	-0.5 V dc to +6.0 V dc
Voltage for chip clear (V_h)	-	-	+15.0 V dc
Operating case temperature range	-	-	-55°C to +125°C
Storage temperature range	-	-	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	-	-	+300°C
Thermal resistance, junction-to-case (θ_{JC})	-	-	See MIL-M-38510, appendix C
Maximum power dissipation (P_D)	2/-	-	1.0 W
Junction temperature (T_J)	3/-	-	+175°C
Endurance:			
Device types 01-05 and 07-11	-	-	10,000 cycles/byte, minimum
Device types 06 and 12	-	-	100,000 cycles/byte, minimum
Data retention	-	-	10 years, minimum

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	-	-	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-	-	-55°C to +125°C
Input voltage, low range (V_{IL})	-	-	-0.1 V dc to +0.8 V dc
Input voltage, high range (V_{IH})	-	-	+2.0 V dc to $V_{CC}+0.3$ V dc
High level chip erase voltage (V_h)	-	-	12 V dc to 13 V dc

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for Microelectronics.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099.)

- 1/ Voltages are with respect to ground. Pin voltages will be stated in this manner throughout the remainder of this specification unless otherwise noted.
- 2/ Under worse case operating conditions.
- 3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications, specification sheets, or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 3.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this specification.

3.2.3 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and shall apply over the full case operating temperature range specified. Test conditions for the specified electronic performance characteristics are as specified in table I. A pin for pin conditions and testing sequence for table I parameters shall be maintained and available upon request from the qualifying activity, on qualified devices.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups of table II. The electrical tests for each subgroup are described in table I.

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, the country of origin may be omitted from the body of the microcircuit but shall be retained on the initial container.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

3.8 Processing of EEPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.8.1 Conditions of the supplied devices. Devices will be supplied in an unprogrammed or cleared state. No provision will be made for supplying programmed devices.

3.8.2 Erase of EEPROMs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.6.4.

3.8.3 Programming of EEPROMs. When specified, devices shall be programmed in accordance with the procedures and characteristics specified in 4.6.3.

3.8.4 Verification of state of EEPROMs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and the device shall be removed from the lot or sample.

3.8.5 Power supply sequence of EEPROMs. In order to reduce the probability of inadvertent writes, the following power supply sequences shall be observed:

- a. A logic high state shall be applied to $\overline{WE}$ and $\overline{CE}$, or both at the same time or before the application of V_{CC} .
- b. A logic high state shall be applied to $\overline{WE}$ and $\overline{CE}$, or both at the same time or before the removal of V_{CC} .

4. QUALITY ASSURANCE PROVISION

4.1 Sampling and inspection. Inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D, E, or F using the circuits shown on figure 4 (or equivalent).
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Prior to burn-in, the devices shall be programmed (see 3.8.3) with the data pattern shown on figure 5. The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation (see 4.2c).
- b. Interim and final electrical test parameters shall be as specified in table II. Interim electrical test parameters prior to burn-in shall be performed by the manufacturer. The following data patterns shall be included in group A, subgroups 7 or 8 (high and low temperature): All 0's, all 1's, checkerboard, and checkerboard complement. Each temperature shall include, at a minimum, the programming of one data pattern. Subgroups 9, 10, and 11 shall be performed on devices containing a checkerboard and a checkerboard complement data patterns or equivalent alternating bit and complementary data patterns.
- c. Percent defective allowable (PDA): The PDA for class S and B devices shall be as specified in MIL-M-38510. The PDA is specified as 5 percent for class B devices based on failures from group A, subgroups 1 and 7 after cooldown, at final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. All screening failures of group A, subgroups 1 and 7 after burn-in divided by the total number of devices submitted to burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA.

- d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.
- e. An endurance test including a data retention bake, in accordance with method 1033 of MIL-STD-883, prior to burn-in (e.g., may be performed at wafer sort) shall be included as part of the screening procedure, with the following conditions:
 - (1) Cycling may be block, byte, or page at equipment room ambient temperature and shall cycle all bytes for a minimum of 10,000 cycles for device types 01 through 05 and 07 through 11, and a minimum of 50,000 cycles for device types 06 and 12.
 - (2) After cycling, perform a high temperature unbiased bake for 48 hours at +150°C, minimum. The storage time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship:

$$A_F = e^{-\frac{E_A}{K} \left[\frac{1}{T_1} - \frac{1}{T_2} \right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2
 T = temperature in Kelvin (i.e., $t_1 + 273$)
 t_1 = time (hours) at temperature T_1
 t_2 = time (hours) at temperature T_2
 K = Boltzmann's constant = $8.62 \times 10^{-5} \text{ eV/}^\circ\text{K}$ using an apparent activation energy (E_A) of 0.6 volt

The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices. All devices shall be programmed with a charge opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern).
 - (3) Read the data retention pattern and test using subgroups 1, 7, and 9 (minimum, e.g., high temperature equivalent subgroups 2, 8A, and 10 may be used) after cycling and bake, prior to burn-in. Devices having bits not in the proper state after storage shall constitute a device failure and shall be removed from the lot.
- f. After the completion of all screening, the devices shall be erased and verified prior to delivery.

4.3 Qualification inspection. Qualification inspection shall be those in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type on this specification, the slower device type may be part I qualified without further qualification testing. At the manufacturer's request, the slower device types will be added to the QPL.

4.4 Quality conformance inspections. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V 1/ 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
Supply current (active)	I _{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/O's = open, inputs = V _{CC} = 5.5 V	1, 2, 3 (3005)	A11		80	mA
Supply current (TTL standby)	I _{CC2}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$, all I/O's = open, inputs = V _{CC} - 0.3 V	1, 2, 3 (3005)	A11		3	mA
Supply current (CMOS standby)	I _{CC3}	$\overline{CE} = V_{CC} - 0.3$ V, all I/O's = open, inputs = V _{IL} or V _{CC} - 0.3 V	1, 2, 3 (3005)	A11		350	μA
Input leakage (high)	I _{IH}	V _{IN} = 5.5 V	1 (3010)	A11	-100	+100	nA
			2, 3 (3010)		-1	+1	μA
Input leakage (low)	I _{IL}	V _{IN} = 0.1 V	1 (3009)	A11	-100	+100	nA
			2, 3 (3009)		-1	+1	μA
Output leakage (high)	I _{OZH} 2/	V _{OUT} = 5.5 V CE = V _{IH}	1 (3021)	A11	-500	+500	nA
			2, 3 (3021)		-10	+10	μA
Output leakage (low)	I _{OLZ} 2/	V _{OUT} = 0.1 V CE = V _{IH}	1 (3020)	A11	-500	+500	nA
			2, 3 (3020)		-10	+10	μA
Input voltage low	V _{IL} 3/		1, 2, 3 (3008)	A11		0.8	V
Input voltage high	V _{IH} 3/		1, 2, 3 (3008)	A11	2.0		V
Output voltage low	V _{OL}	I _{OL} = 2.1 mA, V _{IH} = 2.0 V, V _{CC} = 4.5 V, V _{IL} = 0.8 V	1, 2, 3 (3007)	A11		0.45	V
Output voltage high	V _{OH}	I _{OL} = -400 μA, V _{IH} = 2.0 V, V _{CC} = 4.5 V, V _{IL} = 0.8 V	1, 2, 3 (3006)	A11	2.4		V
$\overline{OE}$ high leakage (chip erase)	I _{OE}	V _H = 13 V	1, 2, 3	A11	-10	100	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V 1/ 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
Input capacitance	C _I 4/ 5/	V _I = 0 V, V _{CC} = 5.0 V, T _A = +25°C, f = 1 MHz (see 4.4.1c)	4 (3012)	A11		10	pF
Output capacitance	C _O 4/ 5/	V _O = 0 V, V _{CC} = 5.0 V, T _A = +25°C, f = 1 MHz (see 4.4.1c)	4 (3012)	A11		10	pF
Read cycle time	t _{AVAY} 6/	See figure 6 (as applicable) 7/	9, 10, 11 (3003)	01	350		ns
				02	300		
				03, 06	250		
				04	200		
				05	150		
Address access time	t _{AVQV} 6/		9, 10, 11 (3003)	01		350	ns
				02		300	
				03, 06		250	
				04		200	
				05		150	
Chip enable access time	t _{ELQV} 6/		9, 10, 11 (3003)	01		350	ns
				02		300	
				03, 06		250	
				04		200	
				05		150	
Output enable access time	t _{OLQV} 6/		9, 10, 11 (3003)	01-03, 06		100	ns
				04, 05		80	
Chip enable to output in low Z	t _{ELQX} 5/		9, 10, 11 (3003)	A11	0		ns
Chip disable to output in high Z	t _{EHQZ} 5/		9, 10, 11 (3003)	01, 02		80	ns
				03-06		60	
Output enable to output in low Z	t _{OLQX} 5/		9, 10, 11 (3003)	A11	0		ns
Output disable to output in high Z	t _{OHQZ} 5/		9, 10, 11 (3003)	01, 02		80	ns
				03-06		60	
Output hold from address change	t _{AXQX} 6/		9, 10, 11 (3003)	A11	0		ns
Write cycle time	t _{WHWL1} t _{EHFL1} 6/ 8/	See figure 6 (as applicable)	9, 10, 11 (3003)	A11		10	ms

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{SS} = 0 V 1/ 4.5 V < V _{CC} < 5.5 V unless otherwise specified	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
Address setup time	t _{AVEL} t _{AVWL} 6/	See figure 6 (as applicable) 8/	9, 10, 11 (3003)	A11	20		ns
Address hold time	t _{ELAX} t _{WLAX} 6/		9, 10, 11 (3003)	A11	150		ns
Write setup time	t _{WLEL} t _{ELWL} 6/		9, 10, 11 (3003)	A11	0		ns
Write hold time	t _{EHWH} t _{WHEH} 6/		9, 10, 11 (3003)	A11	0		ns
OE setup time	t _{OHLEL} t _{OHWL} 6/		9, 10, 11 (3003)	A11	20		ns
OE hold time	t _{EHOL} t _{WHOL} 6/ 9/		9, 10, 11 (3003)	A11	20		ns
WE pulse width (page or byte write)	t _{ELEH} t _{WLWH1} 6/ 10/ 11/		9, 10, 11 (3003)	A11	.150	1	μs
Data setup time	t _{DVEH} t _{DVWH} 6/		9, 10, 11 (3003)	A11	50		ns
Delay to next write	t _{DVWL} t _{DVEL} 6/		9, 10, 11 (3003)	A11		10	μs
Data hold time	t _{EHDX} t _{WHDX} 6/		9, 10, 11 (3003)	A11	10		ns
Byte load cycle	t _{WHWL2} 6/ 9/ 11/	See figure 6 (as applicable)	9, 10, 11 (3003)	A11	.20	149	μs
Last byte loaded to data polling	t _{WHEL} t _{EHEL} 6/ 8/		9, 10, 11 (3003)	A11		650	μs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

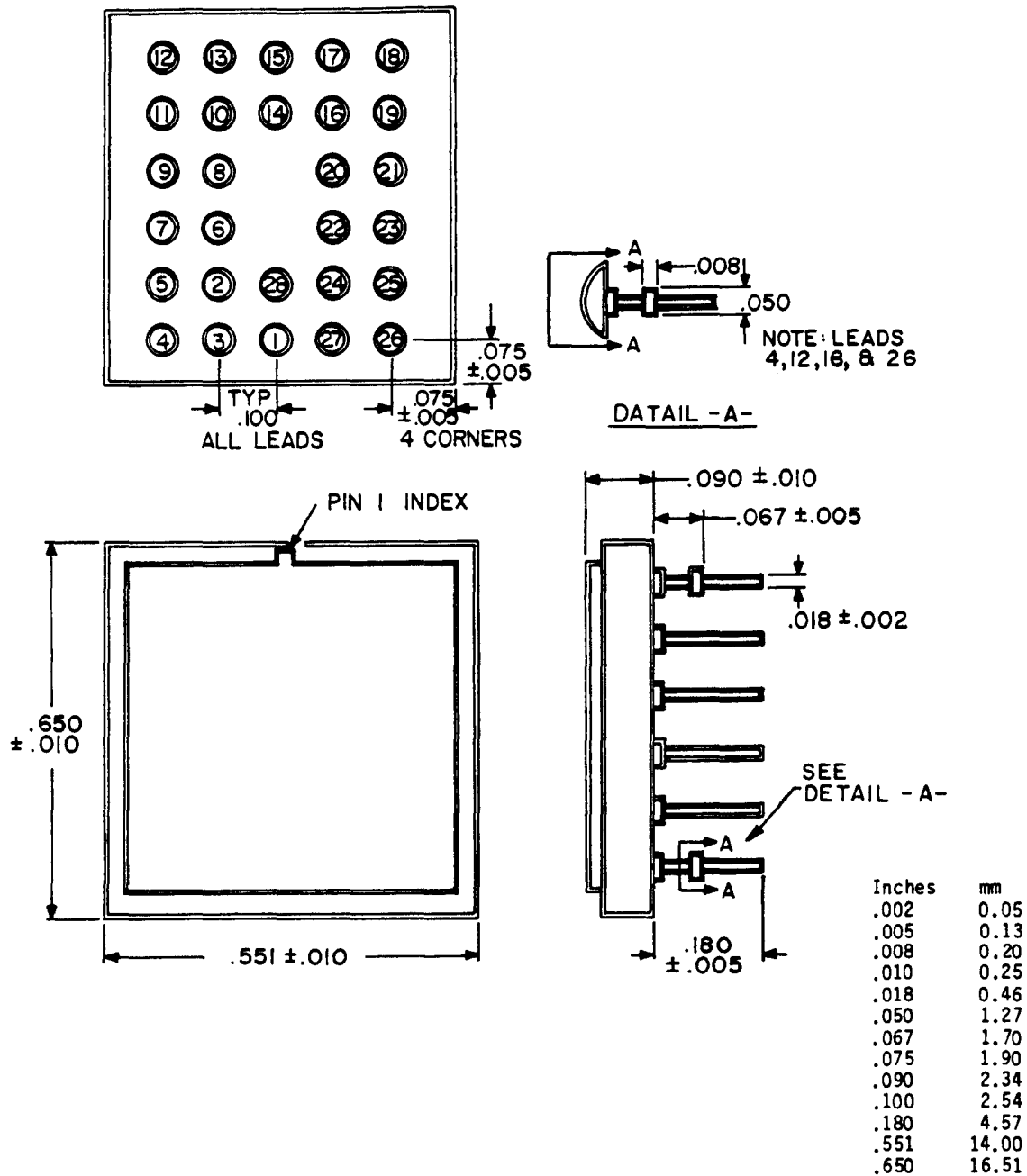
Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V 1/ 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups (test method)	Device types	Limits		Unit
					Min	Max	
CE setup time	t _{ELWL} 6/	See figure 6 (as applicable) 10/	9, 10, 11 (3003)	A11	5		μs
Output setup time	t _{OVHHL} 6/		9, 10, 11 (3003)	A11	5		μs
CE hold time	t _{EHWH} t _{WHEH} 6/		9, 10, 11 (3003)	A11	5		μs
OE hold time	t _{WHOH} 6/		9, 10, 11 (3003)	A11	5		μs
High voltage	V _H 6/		9, 10, 11	A11	12	13	V
WE pulse width (chip erase)	t _{WLWH2} 6/	See figure 6 (as applicable)	9, 10, 11	A11	150		ns
Data in high	t _{DHHL}		9, 10, 11	A11	5		μs
Data high hold	t _{WHDX} 10/		9, 10, 11	A11	5		μs
Erase recovery	t _{OHEL}		9, 10, 11	A11		50	ms

1/ DC and read mode.

2/ Connect all address inputs and OE to V_{IH} and measure I_{OLZ} and I_{OHZ} with the output under test connected to V_{OUT}. Terminal conditions for the output leakage current test shall be as follows:

- a. V_{IH} = 2.0 V; V_{IL} = 0.8 V.
- b. For I_{OLZ}: Select an appropriate address to acquire a logic 1, on the designated output apply V_{IH} to CE. Measure the leakage current while applying the specified voltage.
- c. For I_{OHZ}: Select an appropriate address to acquire a logic 0 on the designated output. Apply V_{IH} to CE. Measure the leakage current while applying the specified voltage.

- 3/ A functional test shall verify the DC input and output levels and applicable patterns as appropriate. All address locations shall be tested. Terminal conditions are as follows:
 - a. Inputs: $H = 2.0\text{ V}$; $L = 0.8\text{ V}$.
 - b. Outputs: $H = 2.4\text{ V}$ minimum and $L = 0.4\text{ V}$ maximum.
 - c. The functional tests shall be performed with $V_{CC} = 4.5\text{ V}$ and $V_{CC} = 5.5\text{ V}$.
- 4/ All pins not being tested are to be open.
- 5/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
- 6/ Tested by application of specified timing signals and conditions, including:
 - a. Output load: 1 TTL gate and $C_1 = 100\text{ pF}$ (minimum) or equivalent circuit (see figure 7).
 - b. Input rise and fall times $\leq 10\text{ ns}$.
 - c. Input pulse levels: 0.4 V and 2.4 V .
 - d. Timing measurements reference levels:
 - (1) Inputs: 1 V and 2 V .
 - (2) Outputs: 0.8 V and 2 V .
- 7/ Timing diagrams appear on figure 6 as applicable. Subgroups 9, 10, and 11 shall be performed with $V_{CC} = 4.5\text{ V}$ and $V_{CC} = 5.5\text{ V}$. The manufacture shall define a worse addressing algorithm, e.g., column galpat, diagonal incrementing, address complement, that shall be approved by the qualifying activity.
- 8/ These tests in subgroups 9, 10, and 11 are the byte write cycle limits. These parameters shall be verified during functional testing, subgroups 7 and 8 by application of the timing limits in table I. Timing diagrams appear on figure 6 (as applicable). Subgroups 7, 8, 9, 10, and 11 shall be performed with $V_{CC} = 4.5\text{ V}$ and $V_{CC} = 5.5\text{ V}$. $\overline{WE}$ and $\overline{CE}$ both must be active to initiate a write cycle; therefore, the sequence of $\overline{WE}$ or $\overline{CE}$ (e.g., for $\overline{WE}$ or $\overline{CE}$ controlled write) is verified interchangeable without duplicate testing.
- 9/ These tests in subgroups 9, 10, and 11 are the page mode write cycle limits. These parameters shall be verified during the functional testing, subgroups 7 and 8 by application of the timing limits in table I. Timing diagrams appear on figure 6 (as applicable). Subgroups 7, 8, 9, 10, and 11 shall be performed with $V_{CC} = 4.5\text{ V}$ and $V_{CC} = 5.5\text{ V}$.
- 10/ These tests in subgroups 9, 10, and 11 are the chip erase cycle limits. These parameters shall be verified during functional testing, subgroups 7 and 8, by application of the timing limits and signal levels in table I. Timing diagrams appear on figure 6 (as applicable). Subgroups 7, 8, 9, 10, and 11 shall be performed with $V_{CC} = 4.5\text{ V}$ and $V_{CC} = 5.5\text{ V}$.
- 11/ During a page write operation, the cycle time defined by t_{WLWH} and t_{WHWL2} shall not be less than $1\text{ }\mu\text{s}$.



NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 1. Case outline.

Device types	01 and 02	
Case outlines	X, Z, and U	Y
Terminal number	Terminal symbol	
1	A14	NC
2	A12	A14
3	A7	A12
4	A6	A7
5	A5	A6
6	A4	A5
7	A3	A4
8	A2	A3
9	A1	A2
10	A0	A1
11	I/O0	A0
12	I/O1	NC
13	I/O2	I/O0
14	GND	I/O1
15	I/O3	I/O2
16	I/O4	GND
17	I/O5	NC
18	I/O6	I/O3
19	I/O7	I/O4
20	CE	I/O5
21	A10	I/O6
22	OE	I/O7
23	A11	CE
24	A9	A10
25	A8	OE
26	A13	NC
27	WE	A11
28	VCC	A9
29	---	A8
30	---	A13
31	---	WE
32	---	VCC

FIGURE 2. Terminal connections.

Mode <u>1</u> /	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Device type
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A11
Standby	V_{IH}	X	X	High Z	A11
Chip clear	V_{IL}	V_H	V_{IL}	$D_{IN} = V_{IH}$	A11
Byte write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A11
Write inhibit	X	V_{IL}	X	High Z/ D_{OUT}	A11
Write inhibit	X	X	V_{IH}	High Z/ D_{OUT}	A11

Table definitions:

V_{IH} = High logic level

V_{IL} = Low logic level

V_H = Chip clear voltage (15)

X = Do not care

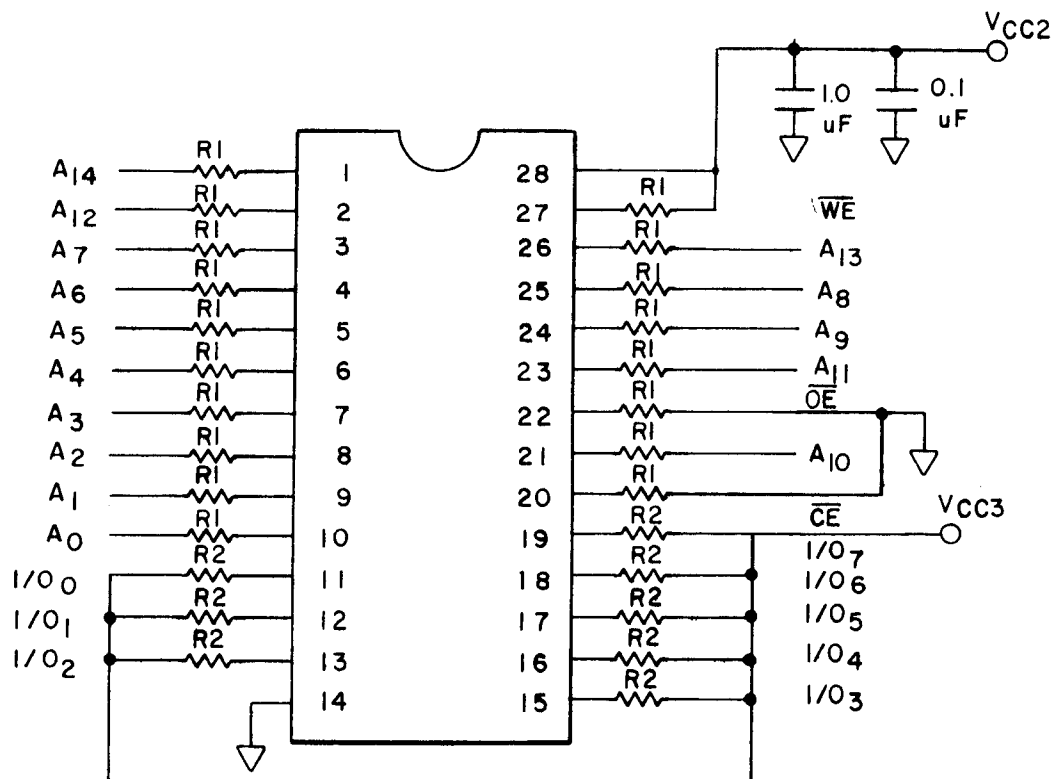
High Z = High impedance state

D_{IN} = Data input

D_{OUT} = Data output

FIGURE 3. Truth table for unprogrammed devices.

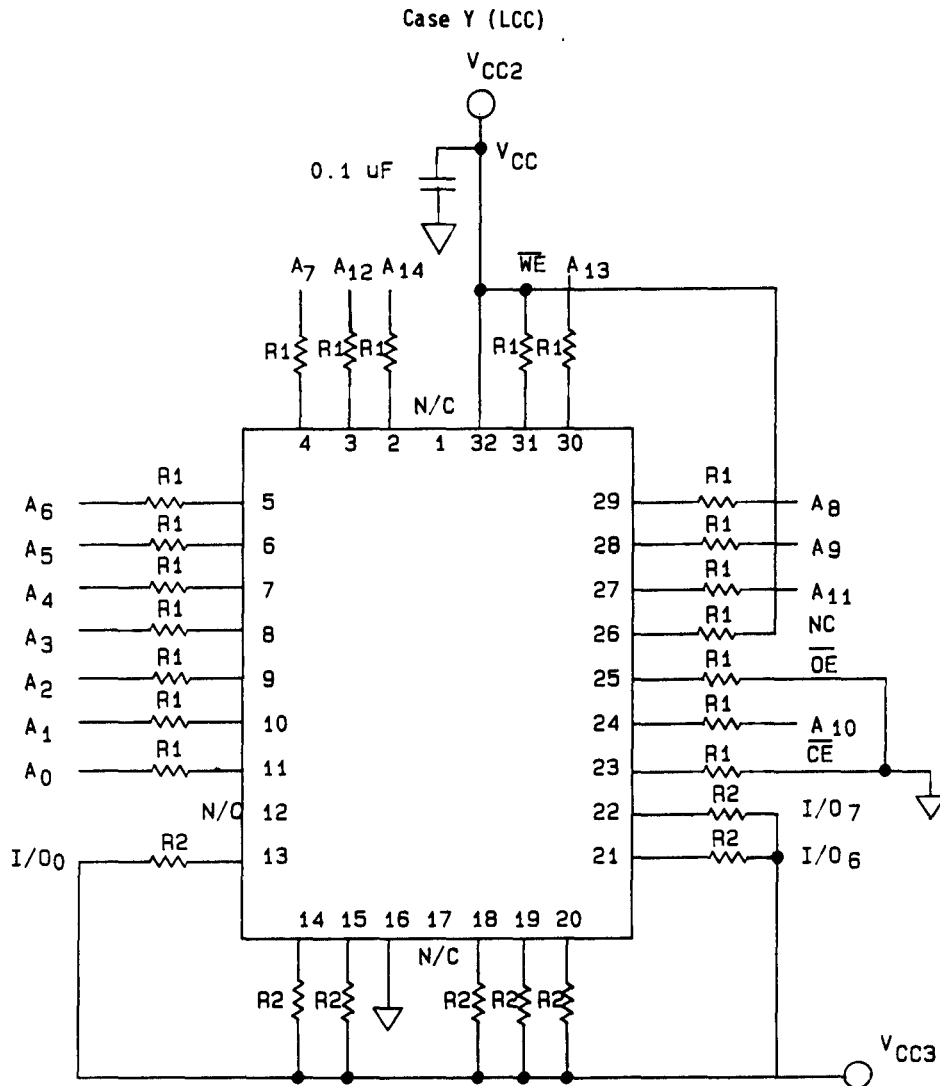
Case X (CERDIP) and case Z (flat pack)



NOTES:

1. All resistors labeled R1 are 3.3 k Ω , .25 W, 5% metal film, at every socket.
2. All resistors labeled R2 are 2.3 k Ω , .25 W, 5% metal film, at every socket.
3. There is a 1.0 μ F decoupling capacitor between pin 27 and GND at every socket.
4. There is a 0.1 μ F decoupling capacitor between V_{CC} and GND at every socket.
5. V_{CC1} = V_{CC2} = 5.25 V, V_{CC3} = 2.25 V. All voltage levels are ± 0.25 V.
6. Power up sequence: V_{CC1}, V_{CC2}, addresses, V_{CC3}.
7. Power down sequence: V_{CC3} addresses, V_{CC2}, V_{CC1}.
8. F₀ (A₀) = 125 kHz (minimum).
9. F₁ (A₁) = F₀ divided by 2, F₂ = F₁ divided by 2 ... F₁₂ (A₁₂) = F₁₁ divided by 2.

FIGURE 4. Burn-in and operating life test circuit.



NOTES:

1. All resistors labeled R1 are 3.3 k Ω , .25 W, 5% carbon film, at every socket.
2. All resistors labeled R2 are 2.2 k Ω , .25 W, 5% carbon film, at every socket.
3. There is a 0.1 μF decoupling capacitor between V_{CC} and GND at every socket.
4. $V_{CC1} = V_{CC2} = 5.25$ V, $V_{CC3} = 2.5$ V. All voltage levels are ± 0.25 V.
5. Power up sequence: V_{CC1} , V_{CC2} , addresses, V_{CC3} .
6. Power down sequence: V_{CC3} addresses, V_{CC2} , V_{CC1} .
7. Resistor at pin 2 can be 200 Ω as an alternative.
8. F_0 (A_0) = 125 kHz (minimum).
9. F_1 (A_1) = F_0 divided by 2, F_2 (A_2) = F_1 divided by 2 ... F_{12} (A_{12}) = F_{11} divided by 2.

FIGURE 4. Burn-in and operating life test circuit - Continued.

Column address (see notes)

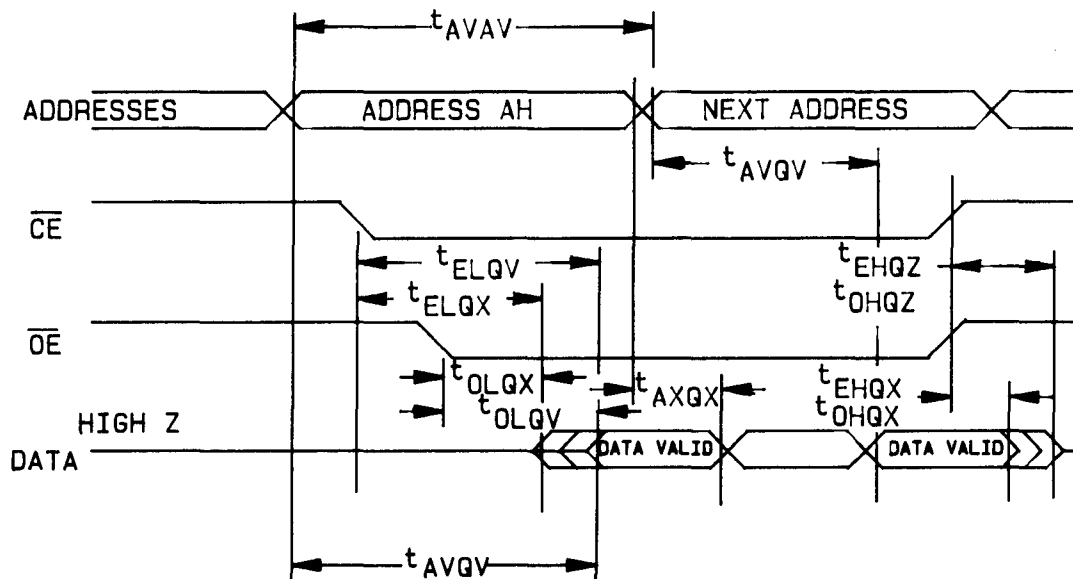
		0	1	2	3	4	5	6	. . .	57	58	59	60	61	62	63
	0	AA	AA	AA	AA	AA	AA	AA	. . .	AA	AA	AA	AA	AA	AA	AA
	1	55	55	55	55	55	55	55	. . .	55	55	55	55	55	55	55
	2	AA	AA	AA	AA	AA	AA	AA	. . .	AA	AA	AA	AA	AA	AA	AA
	3	55	55	55	55	55	55	55	. . .	55	55	55	55	55	55	55
R	.								. . .							
O	.								. . .							
W	.								. . .							
	124	AA	AA	AA	AA	AA	AA	AA	. . .	AA	AA	AA	AA	AA	AA	AA
A	125	55	55	55	55	55	55	55	. . .	55	55	55	55	55	55	55
D	126	AA	AA	AA	AA	AA	AA	AA	. . .	AA	AA	AA	AA	AA	AA	AA
D	127	55	55	55	55	55	55	55	. . .	55	55	55	55	55	55	55
R	.								. . .							
E	.								. . .							
S	.								. . .							
S	508	AA	AA	AA	AA	AA	AA	AA	. . .	AA	AA	AA	AA	AA	AA	AA
	509	55	55	55	55	55	55	55	. . .	55	55	55	55	55	55	55
See note 1	510	AA	AA	AA	AA	AA	AA	AA	. . .	AA	AA	AA	AA	AA	AA	AA
See note 2	511	55	55	55	55	55	55	55	. . .	55	55	55	55	55	55	55

NOTES:

1. All address numbers shown in decimal.
2. Each column/row address location corresponds to one byte.
3. All data numbers shown in hexadecimal.
AA = 10101010 55 = 01010101
4. Manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern.

FIGURE 5. Data pattern.

Read mode



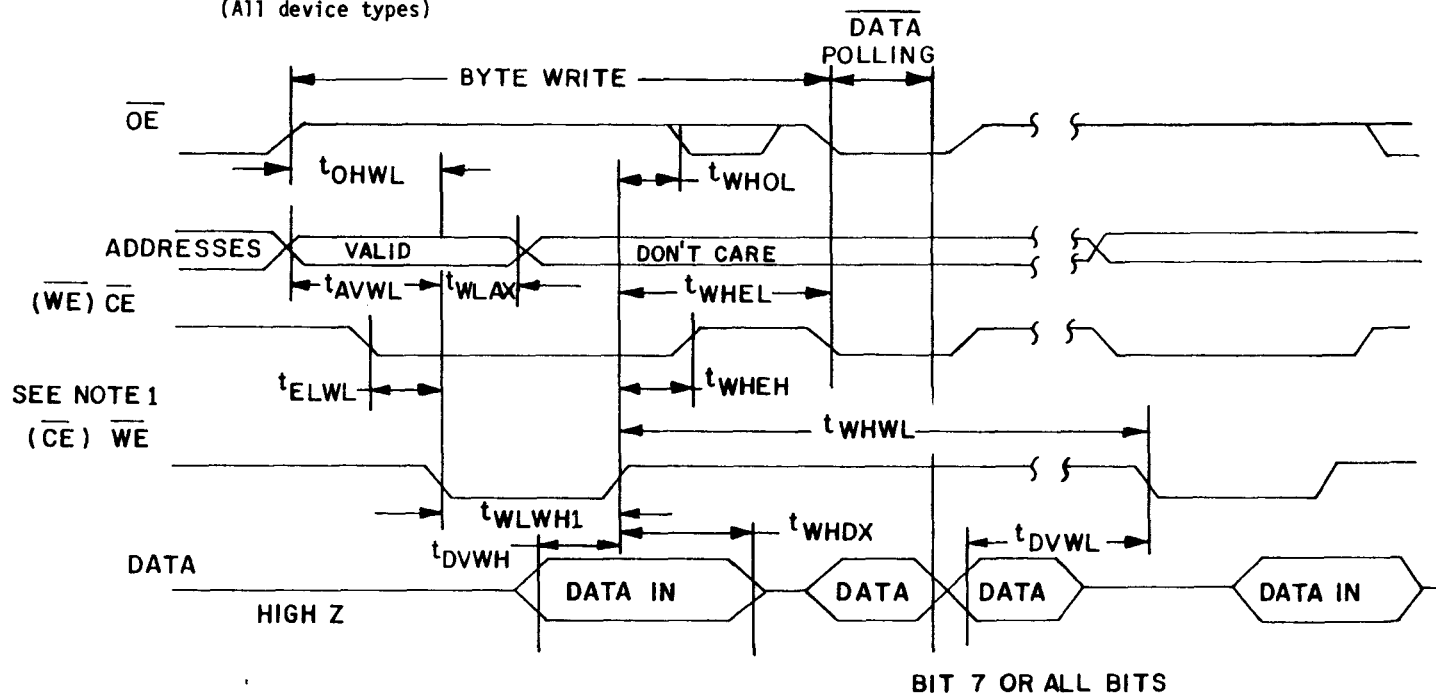
NOTES:

1. V_{CC} shall be applied simultaneously or after $\overline{WE}$ and removed simultaneously or before $\overline{WE}$.
2. Output load is a TTL gate and 100 pF including jig or probe capacitance.
3. Input rise and fall time < 20 ns.
4. Input pulse levels of 0.4 V and 2.4 V.
5. Timing measurement reference levels:
Inputs 1.0 V and 2.0 V.
Outputs 0.8 V and 2.0 V.

FIGURE 6. Waveforms.

Byte write waveforms ($\overline{WE}$ and $\overline{CE}$ controlled)

(All device types)

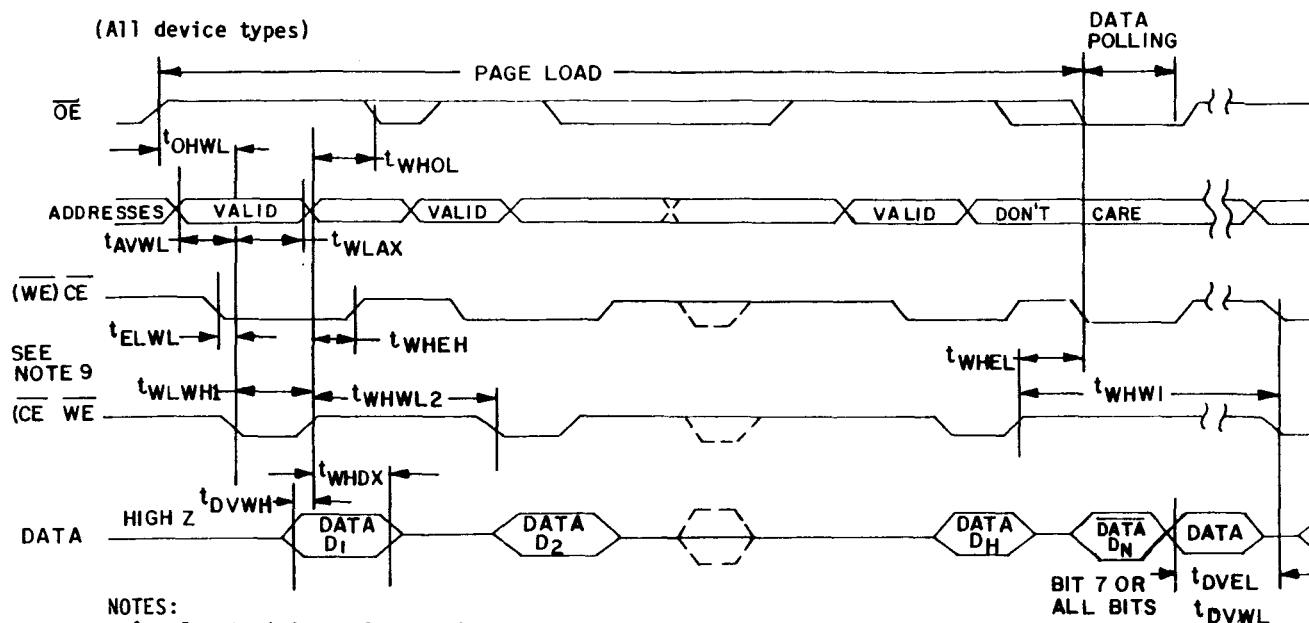


NOTES:

1. Input timing reference levels are 1.0 V and 2.0 V.
2. Output timing reference levels are 0.8 V and 2.0 V.
3. Input pulse rise and fall times (10% and 90%) ≤ 20 ns.
4. Input pulse levels of 0.4 V and 2.4 V.
5. Program verify equivalent to the read mode.
6. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
7. $\overline{WE}$ and $\overline{CE}$ both must be active to initiate a write cycle; therefore, the sequence of $\overline{WE}$ or $\overline{CE}$ (e.g., for $\overline{WE}$ or $\overline{CE}$ controlled write) is verified interchangeable without duplicate testing.

FIGURE 6. Waveforms - Continued.

Page mode write cycle waveforms



NOTES:

1. Input timing reference levels are 1.0 V and 2.0 V.
2. Output timing reference levels are 0.8 V and 2.0 V.
3. Input pulse rise and fall times (10% and 90%) ≤ 20 ns.
4. Input pulse levels are 0.4 V and 2.4 V.
5. Program verify equivalent to the read mode.
6. Page load is 1 to 64 bytes of data.
7. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
8. $\overline{WE}$ and $\overline{CE}$ both must be active to initiate a write cycle; therefore, the sequence of $\overline{WE}$ or $\overline{CE}$ (e.g., for $\overline{WE}$ or $\overline{CE}$ controlled write) is verified interchangeable without duplicate testing.
9. Page write cycle timings are referenced to the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go low, and $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
10. Bytes may be loaded and reloaded at random within a page load cycle. The page addresses must remain the same for each successive write operation throughout the page load cycle. Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed low; e.g., this can be done for the next write; or with $\overline{WE}$ high and $\overline{CE}$ low effectively performing a polling operation.

FIGURE 6. Waveforms - Continued.

Chip erase mode waveforms
(All device types)

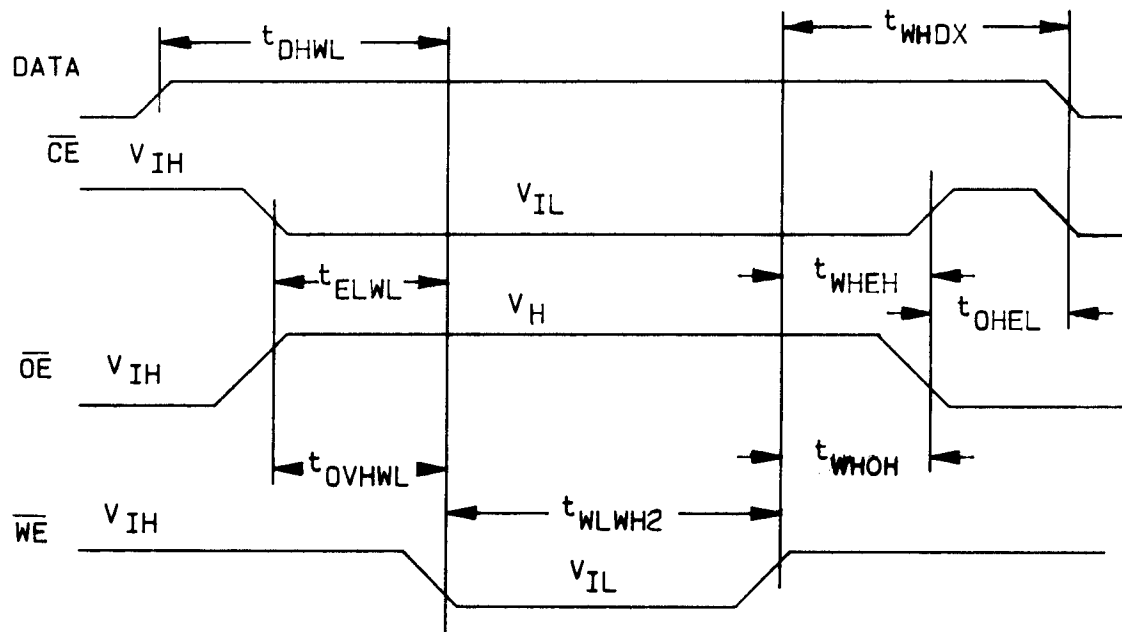
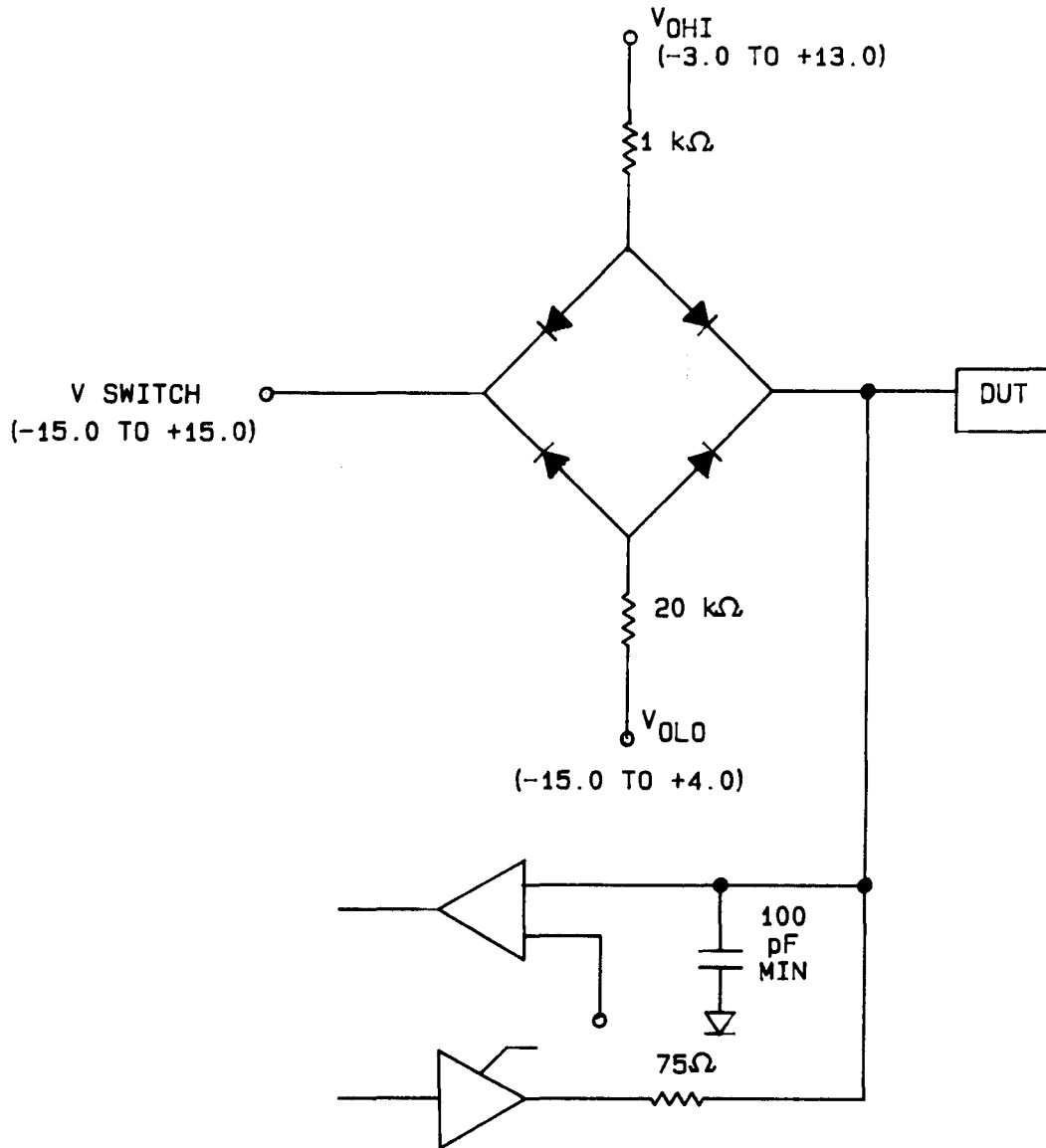


FIGURE 6. Waveforms - Continued.



NOTE: V_{OHI} and V_{OLO} will be adjusted to meet load conditions of table I.

FIGURE 7. Switching load circuit.

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_I and C_O measurements) shall be measured for initial qualification and after process or design changes which may affect capacitance. Sample size is 15 devices, all input and output terminals tested, and no failures.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. All class S devices selected for testing shall be programmed (see 3.8.3) with pattern shown on figure 5.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. All devices requiring end-point electrical testing shall be programmed with the pattern shown on figure 5.
- c. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition D, E, or F as specified in 4.6.2 and figure 6 (as applicable).
 - (2) Ambient temperature = +125°C, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
 - (4) Read the pattern after burn-in and perform end-point electrical tests in accordance with table II herein for group C.
- d. An endurance test, in accordance with method 1033 of MIL-STD-883, shall be added to group C inspection (see 4.4.3c(1)) prior to performing the steady-state life test (see 4.4.3c) and extended data retention (see 4.4.3e). After the completion of the requirements of 4.2 herein, cycling may be block, byte, or page from devices passing group A. Initially, two groups (cell 1 and cell 2) of devices shall be formed. The following conditions shall be met:
 - (1) Cell 1 shall be cycled at -55°C and cell 2 shall be cycled at +125°C for a minimum of 10,000 cycles for device types 01 through 05 and 07 through 11, and 50,000 cycles for device types 06 and 12 (see 1.2.1) per device type.
 - (2) Perform group A subgroups 1, 7, and 9 after cycling. Form new cells (cell 3 and cell 4) for steady-state life and extended data retention. Cell 3 for steady-state life test consists of one-half of the devices from cell 1 and one-half of the devices from cell 2. Cell 4 for extended data retention consists of the remaining devices from cell 1 and cell 2.
 - (3) The sample plans for cell 1, cell 2, cell 3, and cell 4 shall individually be the same as for group C (see 4.4.3c(1)), as specified in method 5005 of MIL-STD-883.

e. Extended data retention shall consist of the following:

- (1) All devices shall be programmed with a charge on all memory cells in each device, such that the cell will read opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern).
- (2) Unbiased bake for 1000 hours (minimum) at +150°C (minimum). The unbiased bake time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship.

$$A_F = e^{-\frac{E_A}{K} \left[\frac{1}{T_1} - \frac{1}{T_2} \right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2

T = temperature in Kelvin (i.e., $t_1 + 273$)

t_1 = time (hours) at temperature T_1

t_2 = time (hours) at temperature T_2

K = Boltzmann's constant = $8.62 \times 10^{-5} \text{ eV/}^\circ\text{K}$ using an apparent activation energy (E_A) of 0.6 volt

The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

- (3) Read the pattern after bake and perform end-point electrical tests for table II herein for group C.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. All devices selected for electrical testing shall be programmed with the pattern shown on figure 5. After completion of all testing, the devices shall have the programmed pattern read, then be erased and verified. When the use of electrical rejects is permitted, no programming or erasure or verification is required.

4.5 Electrostatic discharge sensitivity (ESDS). Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with method 3015 of MIL-STD-883 and MIL-M-38510 for initial testing and after any design or process changes which may affect input or output protection circuitry. The option to categorize devices as ESD sensitive without performing the test is not allowed. Only those device types that pass ESDS testing at 1000 volts or greater shall be considered as conforming to the requirements of this specification.

4.6 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.6.1 Voltages and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6.2 Life test, burn-in, cooldown, and electrical test procedure. When devices are measured at +25°C following application of the steady-state life or burn-in test condition, all devices shall be cooled to +35°C or within +10°C of power stable condition prior to removal of bias voltages/signals. Any electrical tests required shall first be performed at -55°C or +25°C prior to any required tests at +125°C.

4.6.3 Programming procedure. The waveforms and timing relationships shown on figure 6 (as applicable) and the conditions specified in table I shall be adhered to. Initially and after each chip erasure (see 4.6.4), all bits are in the high state (output at V_{OH}).

4.6.3.1 Byte write operation. Information is introduced by selectively programming L (logic 0 level) or H (logic 1 level) into the desired bit locations. A programmed L can be changed to an H by programming an H. No erasure is necessary (see 4.6.4).

4.6.3.2 Page Write operation. The page write operation can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional 1 to 63 bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ ($\overline{CE}$) high to low transition, must begin within 150 μ s of the falling edge of the preceding $\overline{WE}$ ($\overline{CE}$) high to low transition, $t_{w1wh1}+t_{whw12\infty}$ or $t_{te1eh}+t_{ehel2\infty}$. If a subsequent $\overline{WE}$ high to low transition is not detected within 149 μ s, the internal automatic programming cycle will commence. The successive writes need not be sequential; however, the page address (A_6 through A_{14}) for each write during a page write operation shall be the same.

4.6.3.3 Data polling operation. During the internal programming cycle after a byte or page write operation, an attempt to read the last byte written will produce the complement of that data on all I/O or I/O7 (i.e., write data - 0xxx xxx and read data - 1xxx xxx). Once the programming cycle has completed, all I/O or I/O 7 will reflect true data (i.e., write data - 0xxx xxx read data - 0xxx xxx, applies to all toggle bit device types).

4.6.4 Erasing procedure. The waveforms and timing relationship shown on figure 6 (as applicable) and the conditions specified in tables I and III shall be adhered to. Initially and after each chip erasure, all bits are in the high state (output at V_{OH}).

4.6.4.1 Byte erasure. A byte is erased by simultaneously programming an H state into each bit at the selected address (see 4.6.3). This can be done via a byte write cycle or a page mode write cycle (see figure 6, as applicable).

4.6.4.2 Chip erase. The device is erased by setting the $\overline{OE}$ output enable pin to V_H (see figure 6, as applicable), while all other inputs are set in the normal byte erase mode (see 4.6.4.1). After chip erasure, all bits are in the H state (applies to all device types).

TABLE II. Burn-in and electrical test requirements.

Line no.	Applicable tests and MIL-STD-883 test method	Class S device <u>1/</u>			Class B device <u>1/</u>		
		Reference paragraph	Table I subgroups <u>2/3/4/5/6/</u>	Table III delta limits <u>7/</u>	Reference paragraph	Table I subgroups <u>2/3/4/5/6/</u>	Table III delta limits <u>7/</u>
1	Interim electrical parameters (method 5004)		1,7,9 or 2,8(+125°C), 10			1,7,9 or 2,8(+125°C), 10	
2	Static burn-in I (method 1015)		Not required			Not required	
3	Same as line 1						
4	Static burn-in II (method 1015)		Not required			Not required	
5	Same as line 1						
6	Dynamic burn-in (method 1015)	4.2a 4.6.2	Required		4.2a 4.6.2	Required	
7	Final electrical parameters (method 5004)		1*,2,3,7*, 8,9,10,11	Δ		1*,2,3,7*, 8,9,10,11 <u>8/</u>	
8	Group A test requirements (method 5005)	4.4.1	1,2,3,4**, 7,8,9,10,11		4.4.1	1,2,3,4**, 7,8,9,10,11	
9	Group B end-point electrical parameters (method 5005)	4.4.2	1,2,3,7,8, 9,10,11	Δ			
10	Group C end-point electrical parameters (method 5005)	4.4.3			4.4.3	1,2,3,7,8, 9,10,11	Δ <u>9/</u>
11	Group D end-point electrical parameters (method 5005)	4.4.4	1,2,3,7,8, 9,10,11		4.4.4	1,2,3,7,8, 9,10,11	

See footnotes at top of next page.

- 1/ Blank spaces indicate tests are not applicable.
- 2/ * indicates PDA applies to subgroup .
- 3/ ** See 4.4.1c.
- 4/ For all electrical tests, the device shall be programmed to the data pattern specified.
- 5/ Any or all subgroups at the same temperature may be combined when using a multifunction tester.
- 6/ Subgroups 7 and 8 shall consist of writing and reading the data patterns specified in accordance with the limits of table I, subgroups 9, 10, and 11.
- 7/ Δ indicates delta limits shall be required, and delta values shall be computed with reference to the previous interim electrical parameters (line 1). Refer to table III for required parameters and limits to be tested.
- 8/ The device manufacturer may at his option either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).
- 9/ Delta limits required for initial qualification and after any design or process changes.

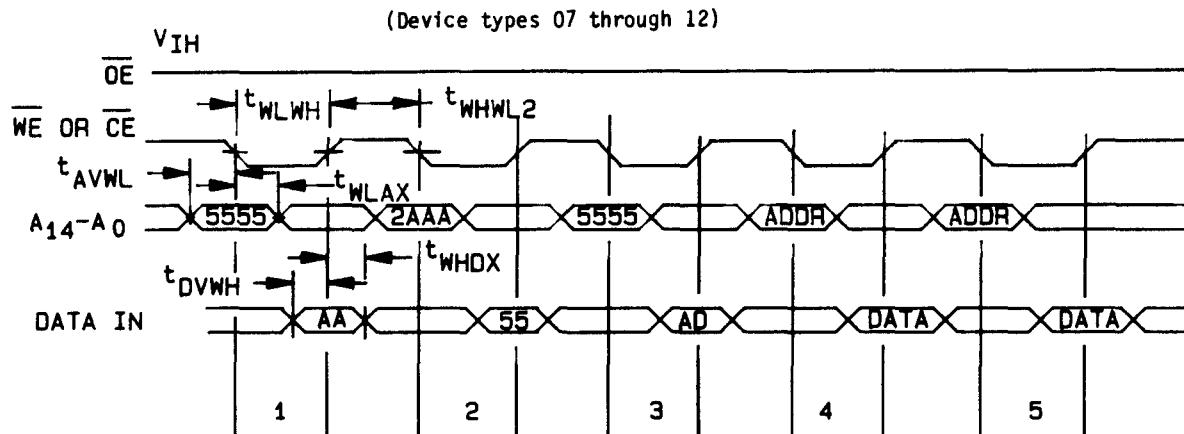
TABLE III. Delta limits at +25°C (subgroup 1).

Parameter <u>1/</u>	Device types
	All
I _{CC3}	±10% of specified value
I _{OHZ}	±10% of specified value
I _{OLZ}	±10% of specified value

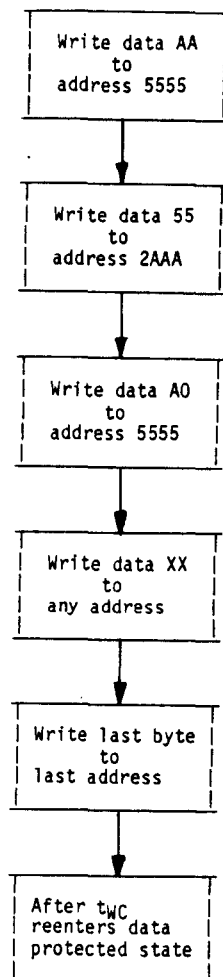
- 1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine deltas.

4.6.5 Read mode operation. The device is in the read mode whenever the $\overline{CE}$ and $\overline{OE}$ pins are at V_{IL} and the $\overline{WE}$ pin is at V_{IH} . The waveforms and timing relationships shown on figure 6 (as applicable) and the test conditions and limits specified in table I shall be applied.

4.6.6 Software data protection. Device types 07 through 12 software data protection offers the host a method of protecting the data written in array from inadvertent writes without the use of external protection circuits. The waveforms and timing relationships shown on figures 6 and 8 and the conditions specified in table I shall apply.



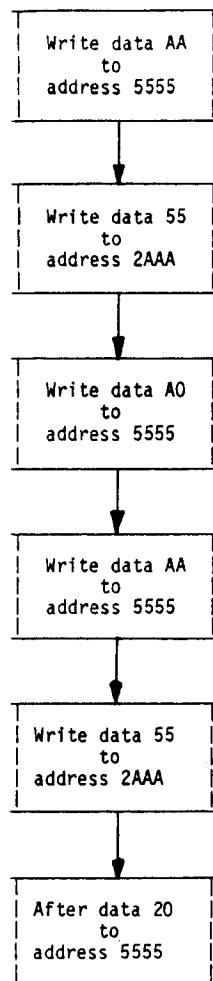
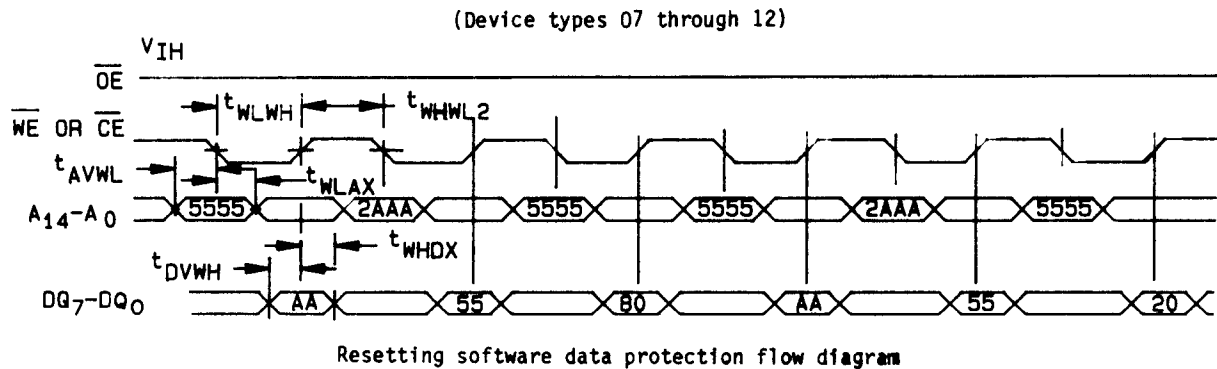
Setting software data protection flow diagrams



NOTES:

1. Software data protection timings are referenced to the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go low, and the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
2. A minimum of one valid byte write must follow the first three bytes of the command sequence.
3. The command sequence and subsequent data must conform to the page write timing.

FIGURE 8. Software data protection waveforms.



NOTES:

1. Reset software data protection timings are referenced to the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go low, and the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
2. The command sequence must conform to the page write timing.

FIGURE 8. Software data protection waveforms - Continued.

4.6.6.1 Set software protection. Device types 07 through 12 or placed in protected state by writing a series of instructions (see figure 8) to the device. Once protected, writing to the device may only be preformed by executing the same sequence of instructions appended with either a byte write operation or page write operation. The waveforms and timing relationship shown on figure 8 and the test conditions and limits specified in table I apply.

4.6.6.2 Reset software data protection. Device types 07 through 12 protection feature is reset by writing a series of instructions (see figure 8) to the device. The waveforms and timing relationships shown on figures 6 and 8 and the test conditions and limits specified in table I apply.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.3 Ordering data. The contract of purchase order should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to procuring activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of MIL-STD-883, method 5003), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths or lead forming if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase or direct shipment to the Government.
- h. Requirements for JAN marking.

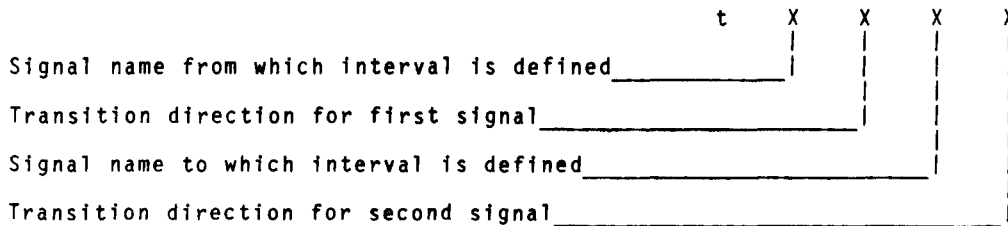
6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331 (including terms and symbols for device terminals) and as follows:

V_{SS}	Common or reference voltage mode.
V_{CC}	Supply voltage.
V_h	Output enable and write enable voltage during chip erase.
A_0-A_{14}	Address inputs used to address 1 of 32K/8-bit locations in static storage array.
$\overline{CE}$	Chip enable used with the output enable ($\overline{OE}$) signal to control the state of the 8 data I/O signals.
$\overline{OE}$	Output enable used to control the I/O terminals.
$I/O_0-I/O_7$	Data I/O, 8-bit wide data bus.
$\overline{WE}$	Write enable input used to select a write mode.
I_{CC1}	Supply current (standby and active).
I_{CC2}	Supply current (TTL standby).
I_{CC3}	Supply current (CMOS standby).
I_{OE}	Output enable high voltage current.
I_{IH}, I_{IL}	Input leakage currents.
I_{OHZ}, I_{OLZ}	High impedance output leakage current.
V_{IL}	Logical low input voltage.
V_{IH}	Logical high input voltage.
V_{OL}	Logical low output voltage.
V_{OH}	Logical high output voltage.
C_I	Input capacitance.
C_O	Output capacitance.
t_{AVAV}	Cycle time from one read to next read.
t_{ELQV}	Chip enable access time.
t_{AVQV}	Address access time.
t_{OLQV}	Output enable access time.
t_{ELQX}	Chip enable to output in low Z.
t_{EHQZ}	Chip enable to output in high Z.

tOLOX	Output enable to output in low Z.
tOHQZ	Output enable to output in high Z.
tAXQX	Output hold from address change.
tWHWL1	Cycle time during $\overline{WE}$ write operation.
tEHEL1	Cycle time during $\overline{CE}$ write operation.
tAVWL	Address to $\overline{WE}$ setup time.
tAVEL	Address to $\overline{CE}$ setup time.
tWLAX	Address hold time after $\overline{WE}$ low.
tELAX	Address hold time after $\overline{CE}$ low.
tELWL	Chip enable to $\overline{WE}$ setup time.
tWLEL	Write enable to $\overline{CE}$ setup time.
tWHEH	Chip enable hold time after $\overline{WE}$ high.
tEHWH	Write enable hold time after $\overline{CE}$ high.
tELEH	Chip enable pulse width during write.
tOHWL	Output enable to $\overline{WE}$ setup time.
tOHEL	Output enable to $\overline{CE}$ setup time.
tWHOL	Output enable hold time after $\overline{WE}$ high.
tEHOL	Output enable hold time after $\overline{CE}$ high.
tWLWH	Write enable pulse width during write.
tWHWL2	Minimum write enable high time.
tEHEL2	Minimum chip enable high time after write.
tDVWH	Data in setup time before $\overline{WE}$ high.
tDVEH	Data in setup time before $\overline{CE}$ high.
tWHDX	Data hold time after $\overline{WE}$ high.
tEHDX	Data hold time after $\overline{CE}$ high.
tDVWL	Minimum time from valid data out to next write.
tDVEL	Minimum time from valid data out of next write.
tVDEHWL	V_{OE} setup time to $\overline{WE}$ low (chip erase).
tWHVOEL	V_{OE} hold time after $\overline{WE}$ high (chip erase).

t_{WLWL}	Cycle time during chip erase operation.
t_{DVWL}	Data to $\overline{WE}$ setup time (chip erase).
t_{ELWL}	$\overline{CE}$ setup time (chip erase).
t_{OVHWL}	Output setup time (chip erase).
t_{WLWH}	$\overline{WE}$ pulse width (chip erase).
t_{WHOH}	$\overline{OE}$ hold time (chip erase).
t_{OHEL}	Erase recovery (chip erase).
t_{DHWL}	Data setup time.
t_{WHDx}	Data hold time.

6.4.1 Timing parameter abbreviations. All timing abbreviations use lower case character with upper case character subscripts. The initial character is always t and is followed by four descriptors. These characters specify two signal points arranged by from-to sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Note: There are exceptions for undefined signals.



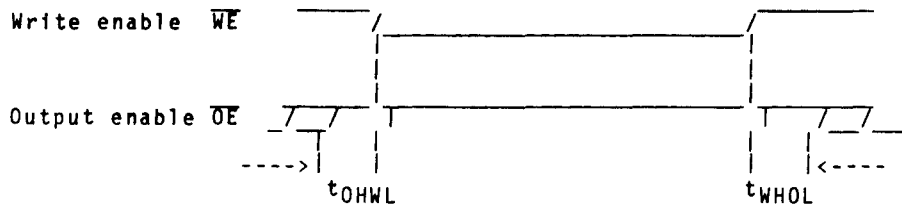
a. Signal definitions:

A = Address	D = Data in	Q = Data out
W = Write enable	E = Chip enable	O = Output enable
P = VCC	R = Ready/busy	

b. Transition definitions:

H = Transition to high	L = Transition to low
V = Transition to valid	X = Transition to invalid
Z = Transition to high impedance	

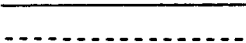
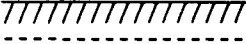
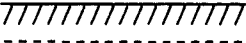
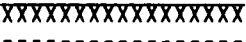
Example:



The example shows $\overline{OE}$ to $\overline{WE}$ setup time defined as t_{OHWL} and $\overline{OE}$ hold time after $\overline{WE}$ high defined as t_{WHOL} .

- c. **Timing limits:** The table of timing values show either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device will never provide data later than that time (even though most devices will supply data much sooner).

- d. **Waveforms:**

Waveform Symbol	Input	Output
	Must be valid	Will be valid
	Change from low to high	Will change from low to high
	Change from high to low	Will change from high to low
	Do not care: Any change permitted	Changing state unknown
	Not applicable	Change to high impedance

6.5 **Lead materials and finishes.** Logistic support lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer length and lead forming shall not affect the part number.

6.6 **Handling.** MOS devices shall be handled with certain precautions to avoid damage due to accumulation of static charge. Input protective devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

- Devices should be handled on benches with conductive and grounded surface.
- Ground test equipment and tools.
- Handling of devices by the leads should be avoided.
- Store devices in conductive foam or carriers.

- e. The use of plastic, rubber, or silk in the MOS area should be avoided.
- f. Relative humidity should be maintained above 50 percent, if practical.
- g. Operator should be grounded when handling devices.

6.7 Testing by inference. Testing by inference is the validation of the performance of a parameter by measurement of the correct performance of a dependent parameter or function.

6.8 Substitutability.

<u>Device type</u>	<u>Similar generic part number</u>
01, 07	28C256-350
02, 08	28C256-300
03, 09	28C256-250
04, 10	28C256-200
05, 11	28C256-150
06, 12	28C256-250

CONCLUDING MATERIAL

Custodians:

Army - ER
Navy - EC
Air Force - 17
NASA - NA

Preparing activity:
Air Force - 17

Agent:
DLA - ES

Review activities:

Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

(Project 5962-1153)

User activities:

Army - SM
Navy - AS, CG, MC