

MILITARY SPECIFICATION
 MICROCIRCUIT, DIGITAL, BIPOLAR
 256 BIT RANDOM ACCESS MEMORY (RAM)
 MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic, silicon, bipolar static 256-bit random access memories. One product assurance class and a choice of case outlines lead finishes are provided for each type and reflected in the complete part number.

1.2 Part number. The complete part number shall be in accordance with MIL-M-38510. The "JAN" or "J" certification mark shall not be used.

1.2.1 Device type. The device type shall be as follows:

<u>Device type</u>	<u>Circuit organization package</u>
01	256 words/1 bit per word RAM with open collector output and three chip select inputs.
02	256 words/1 bit per word RAM with three-state output, three chip select inputs, and inverted data output.
03	256 words/1 bit per word RAM with open collector output, three chip select inputs, and inverted data output.
04	256 words/1 bit per word low power RAM with three-state output, three chip selects, and inverted data out.

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Outline letter</u>	<u>Case outline, (MIL-M-38510, appendix C)</u>
E	D-2 (16-lead, 1/4" x 7/8"), dual-in-line package
F	F-5 (16-lead, 1/4" x 3/8"), Flat-package

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RADC (RBRD), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.
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1.3 Absolute maximum ratings.

Supply voltage range - - - - -	-0.5 V dc to 7.0 V dc
Input voltage range - - - - -	-1.2 V dc at -10 mA to 5.5 V dc
Storage temperature range - - - - -	-65°C to 150°C
Lead temperature (soldering, 10 seconds) - - - - -	300°C
Thermal resistance, junction-to-case <u>1/</u> :	
Case E - - - - -	50°C/W
Case F - - - - -	70°C/W
Output supply voltage - - - - -	-0.5 V dc to 5.5 V dc
Output sink current - - - - -	+20 mA
Maximum power dissipation, P_D <u>2/</u> - - - - -	(01, 02, 03) 798 mWdc (145 mA)
	(04) 413 mWdc (75 mA)
Maximum junction temperature - - - - -	175°C

1.4 Recommended operating conditions.

Supply voltage - - - - -	4.50 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage - - - - -	2.0 V dc
Maximum low level input voltage - - - - -	0.80 V dc
Normalized fanout (each output) - - - - -	40 maximum
Ambient operating temperature range - - - - -	-55°C to 125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagrams. The logic diagrams shall be as specified on figure 2.

1/ Heat sinking is recommended to reduce the junction-to-case temperature.

2/ Must withstand the added P_D due to short circuit (e.g., I_{OS}) test.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $\frac{1}{-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}}$	Device type	Limits		Unit
				Min	Max	
High-level output voltage	V_{OH}	$V_{IN} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $I_{OH} = -5.2 \text{ mA}$	02 04	2.4	---	V
Low-level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}$ $V_{IN} = 0.8 \text{ V}$ $I_{OL} = 16 \text{ mA}$	A11	---	0.45	V
Input clamp voltage	V_{IC}	$V_{CC} = 5.5 \text{ V}$ $T_A = 25^{\circ}\text{C}$ $I_{IN} = -10 \text{ mA}$	A11	---	-1.5	V
Output leakage current	I_{CEX}	$V_{CC} = 5.5 \text{ V}$ $V_{OH} = 5.5 \text{ V}$	01 03	---	100	μA
High-impedance (off-state) output high current	I_{OHZ}	$V_{CC} = 5.5 \text{ V}$ $V_O = 2.4 \text{ V}$	02 04	---	50	μA
High-impedance (off-state) output low current	I_{OLZ}	$V_{CC} = 5.5 \text{ V}$ $V_O = 0.5 \text{ V}$	02 04	---	-50	μA
High-level input current	I_{IH1}	$V_{CC} = 5.5 \text{ V}$ $V_{IN} = 4.5 \text{ V}$	A11	---	25	μA
High-level input current	I_{IH2}	$V_{CC} = 5.5 \text{ V}$ $V_{IN} = 5.5 \text{ V}$	A11	---	1	mA
Low-level input current	I_{IL}	$V_{CC} = 5.5 \text{ V}$ $V_{IN} = 0.4 \text{ V}$	A11	---	-800	μA
Short circuit output current	I_{OS}	$V_{CC} = 5.5 \text{ V}$ $V_O = 0.0 \text{ V}$	02 04	-20	-100	mA
Supply current	I_{CC}	$V_{CC} = 5.5 \text{ V}$ $\overline{WE} = \text{GND}$ All other inputs = 4.5 V	01,02 03		145	mA
			04		75	mA
Address access time	t_{AA}	$V_{CC} = 4.5 \text{ and } 5.5 \text{ V}$ $C_L = 30 \text{ pF}$ see figure 6	A11	---	65	ns
Chip select access time	t_{ACS}		A11	---	40	ns
Chip select recovery time	t_{RCS}		01,03	---	35	ns
Chip select to high impedance	t_{ZRCS}		02,04	---	35	ns
Minimum write pulse width	t_{WP}		A11	50	---	ns
Write disable time	t_{WS}		01,03	---	50	ns

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{1/} $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
Write disable to high impedance	t_{ZWS}	$V_{CC} = 4.5 \text{ and } 5.5 \text{ V}$ $C_L = 30 \text{ pF}$ see figure 6	02,04	---	50	ns
Write recovery time	t_{WR}		A11	---	50	ns
Address setup prior to write	t_{WSA}		A11	10	---	ns
Address hold after write time	t_{WHA}		A11	5	---	ns
Data setup prior to write time	t_{WSD}		A11	10	---	ns
Data hold after write time	t_{WHD}		A11	5	---	ns
Chip select setup prior to write	t_{WSCS}		A11	10	---	ns
Chip select hold after write time	t_{WHCS}		A11	5	---	ns

1/ Complete terminal conditions shall be as specified in table III.

3.2.3 Schematic circuits. The schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in this specification and shall be submitted to the qualifying activity as a prerequisite for qualification. All manufacturers' schematics shall be maintained and available upon request.

3.2.4 Bit address map. The bit address map shall be as specified on figure 3.

3.2.5 Truth table. The truth table shall be as specified on figure 4.

3.2.6 Case outline. The case outline shall be in accordance with 1.2.3.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. The "JAN" or "J" certification mark shall not be used.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 6 (see MIL-M-38510, appendix E).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III) Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7,9
Group A test requirements (method 5005)	1,2,3,7,9, 10,11
Group C end-point electrical parameters (method 5005)	1,2,3
Additional electrical subgroups for group C periodic inspections	None
Group D end-point electrical parameters (method 5005)	1,2,3

*PDA applies to subgroup 1 (see 4.2c)

3.8 Manufacturer eligibility. To be eligible to supply microcircuits to this specification a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line, not necessarily the line producing the device type described herein.

3.9 Certification. Certification in accordance with MIL-M-38510 is not required for this device.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 and 5007 of MIL-STD-883 except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
 1. Test condition D, using the circuit shown on figure 5 or equivalent.
 2. $T_A = 125^\circ\text{C}$ minimum.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

4.3 Qualification inspection. Qualification inspection is not required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Generic test data may be used to satisfy the requirements for group C and D inspections (see 6.7).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II.
- b. Subgroups 4, 5, 6, and 8 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

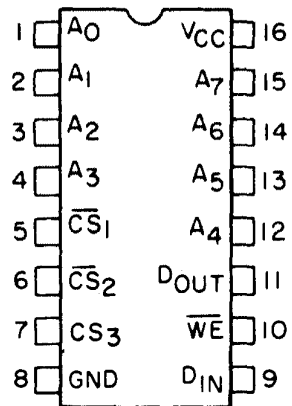
4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883.

- a. End-point electrical parameters shall be as specified in table II.
- b. Subgroups 3 and 4 shall be added to the group C inspection requirements for class C devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.
- c. Steady state life test (method 1005 of MIL-STD-883) conditions:
 1. Test condition D, using the circuit shown on figure 5 or equivalent.
 2. $T_A = 125^\circ\text{C}$ minimum.
 3. Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 end-point electricals parameters shall be as specified in table III.

Device type 01

Cases E or F



Device type 02, 03 and 04

Cases E or F

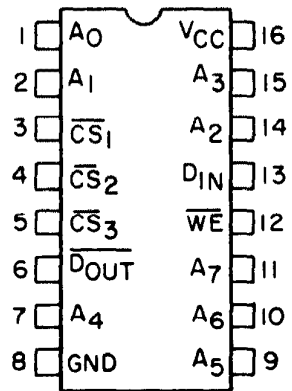
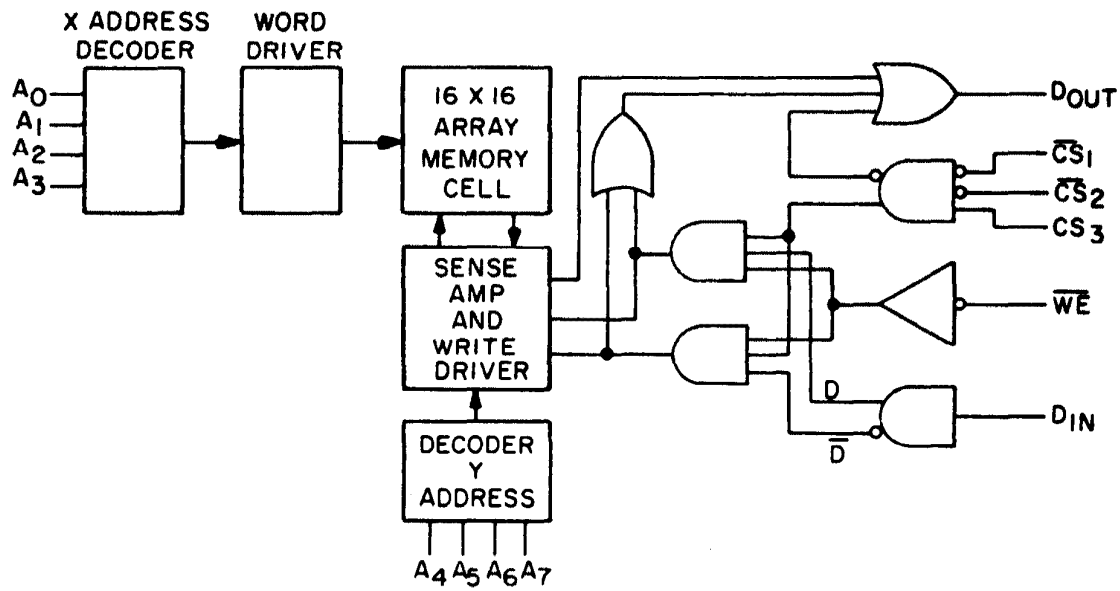
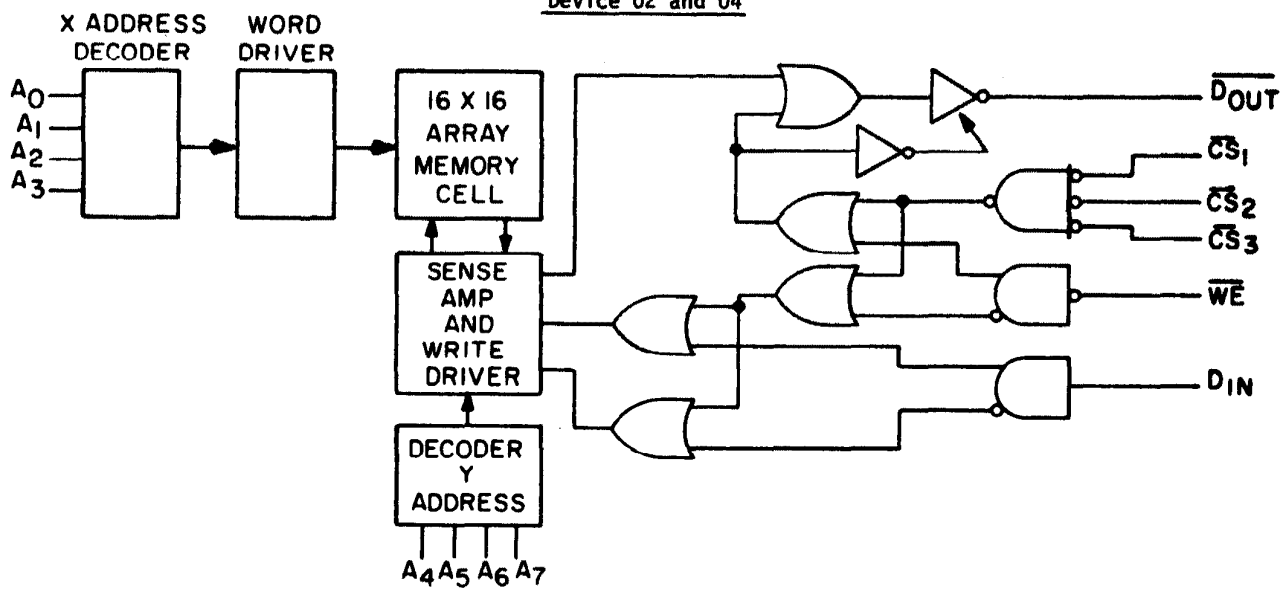
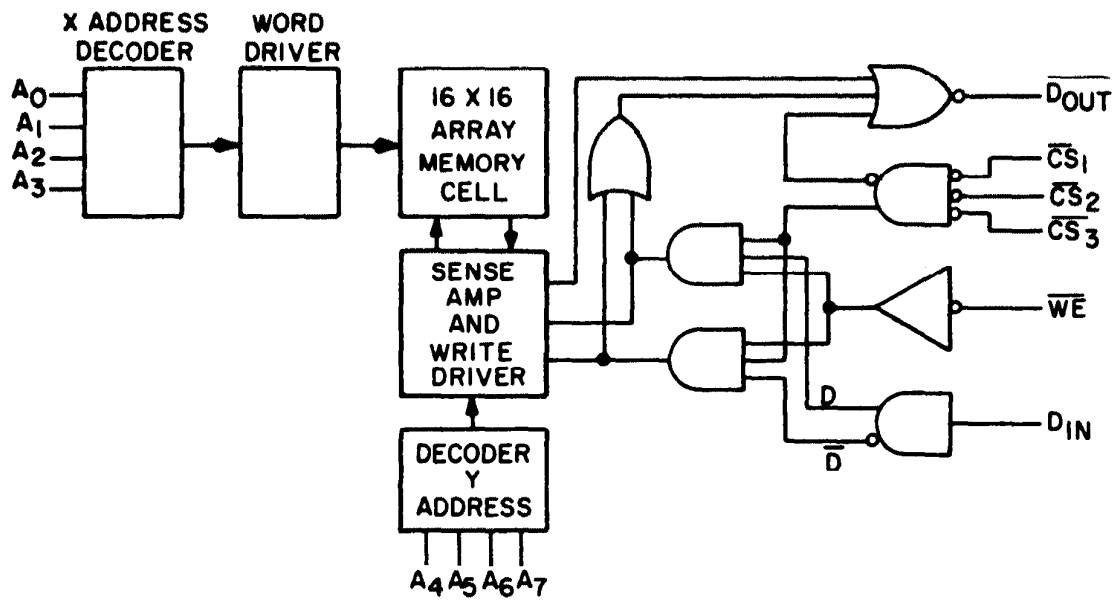


FIGURE 1. Terminal connection.

Device 01Device 02 and 04FIGURE 2. Block diagram.

Device 03FIGURE 2. Block diagram - Continued.

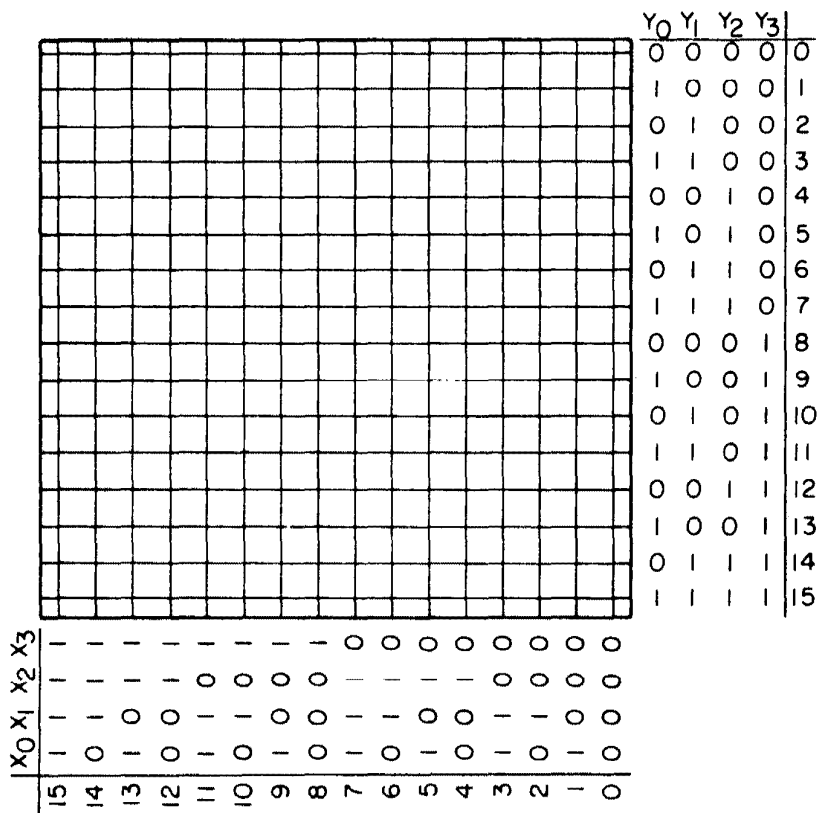


FIGURE 3. Bit address map.

Inputs					Output	Mode
$\overline{CS}_1$	$\overline{CS}_2$	CS_3	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	X	X	H	Not selected
X	H	X	X	X	H	Not selected
X	X	L	X	X	H	Not selected
L	L	H	L	L	H	Write "0"
L	L	H	L	H	H	Write "1"
L	L	H	H	X	D_{OUT}	Read data from addressed location

Device 01

Inputs					Output	Mode
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
H	X	X	X	X	High Z	Not selected
X	H	X	X	X	High Z	Not selected
X	X	H	X	X	High Z	Not selected
L	L	L	L	L	High Z	Write "0"
L	L	L	L	H	High Z	Write "1"
L	L	L	H	X	D_{OUT}	Read inverted data from addressed location

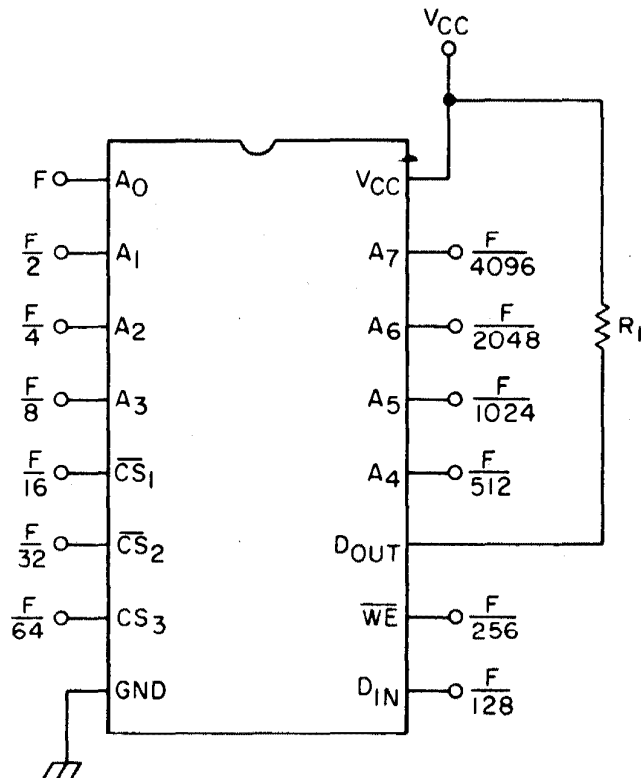
Device 02 & 04

Inputs					Output	Mode
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
H	X	X	X	X	H	Not selected
X	H	X	X	X	H	Not selected
X	X	H	X	X	H	Not selected
L	L	L	L	L	H	Write "0"
L	L	L	L	H	H	Write "1"
L	L	L	H	X	D_{OUT}	Read inverted data from addressed location

H = High voltage level
 L = Low voltage level
 X = Don't care (high or low)

Device 03

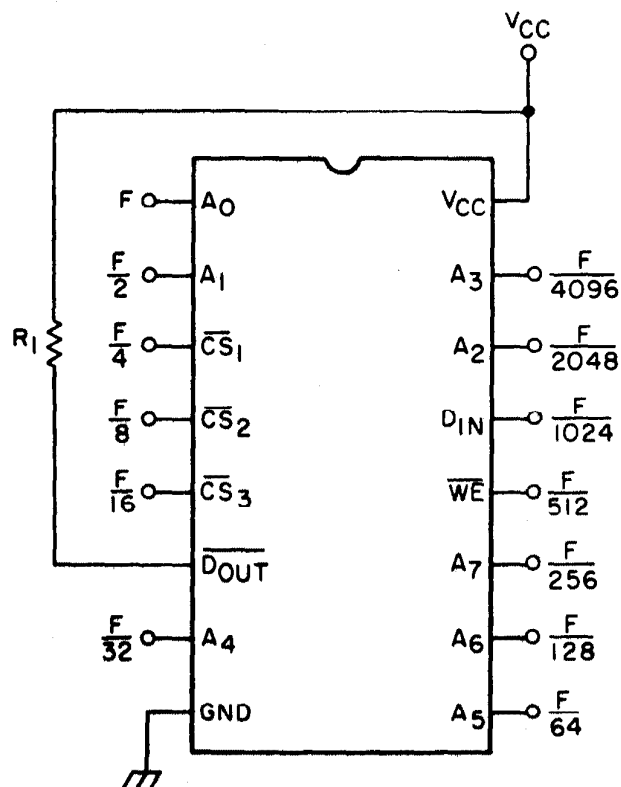
FIGURE 4. Truth tables.

Device type 01

NOTES:

1. $R_1 = 330\Omega \pm 5\%$.
2. All pulse generators have the following characteristics: $V_{IL} = -1.5$ V minimum to 0.8 V maximum; $V_{IH} = 2.0$ V minimum to 5.5 V maximum; 50% $\pm 15\%$ duty cycle and $F = 100$ kHz minimum.
3. V_{CC} shall be high enough to insure 5.0 V at the device V_{CC} terminal.

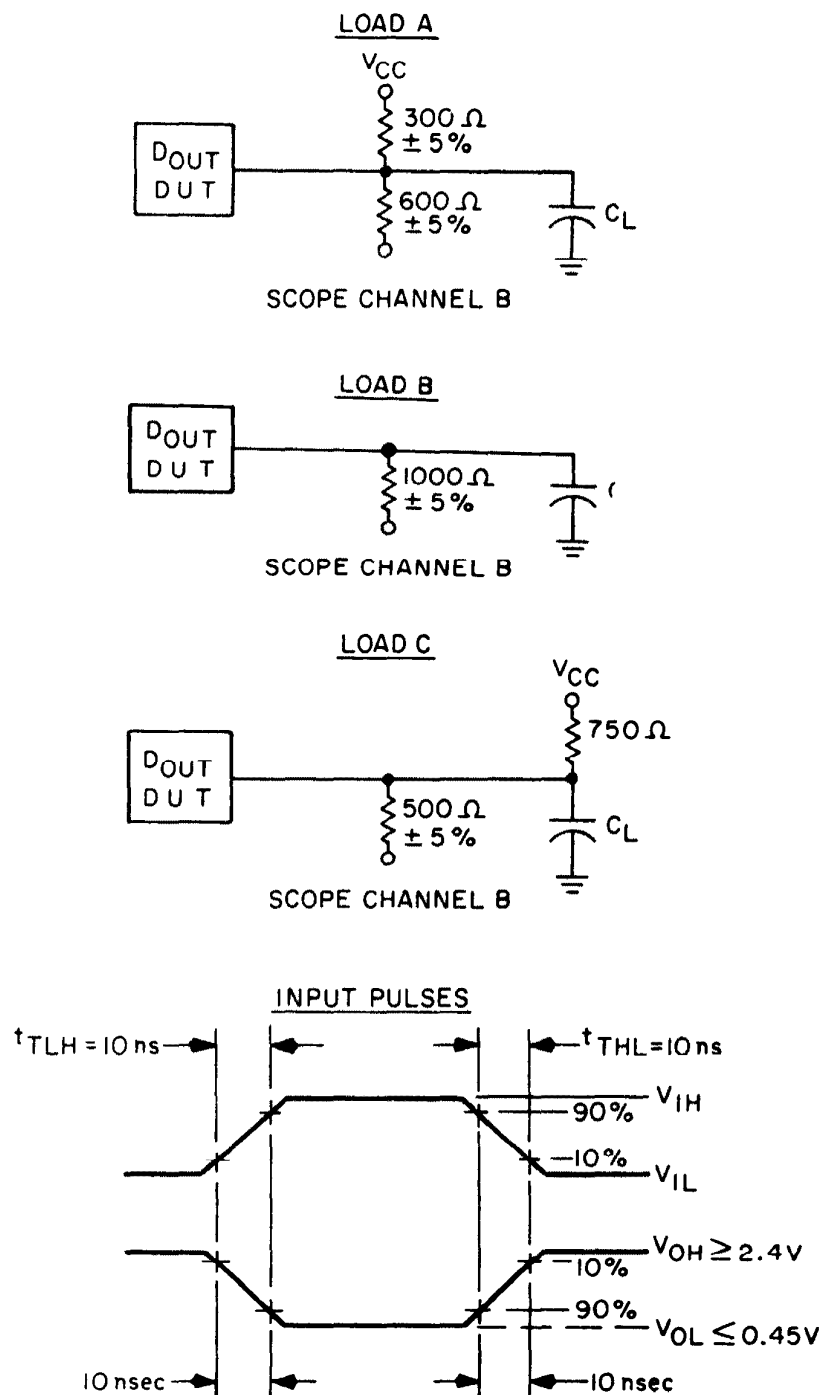
FIGURE 5. Burn-in and life test circuits.

Device types 02, 03 and 04

NOTES:

1. $R_1 = 330\Omega \pm 5\%$.
2. All pulse generators have the following characteristics $V_{IL} = -1.5$ V min. to 0.8 V max; $V_{IH} = 2.0$ V min to 5.5 V max; 50% $\pm 15\%$ duty cycle and $F = 100$ kHz minimum.
3. V_{CC} shall be high enough to insure 5.0 V at the device V_{CC} terminal.

FIGURE 5. Burn-in and life test circuits - Continued.

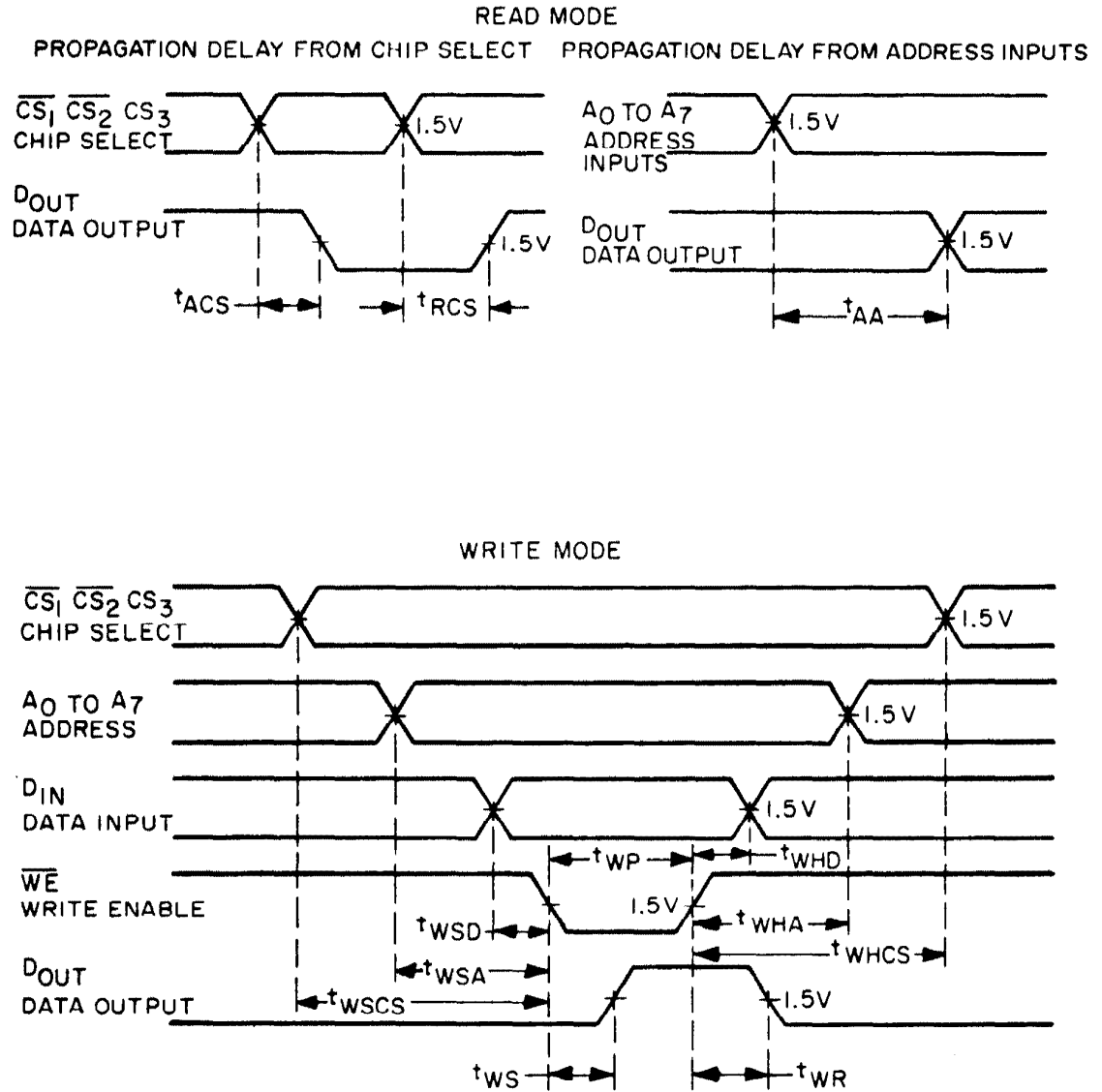


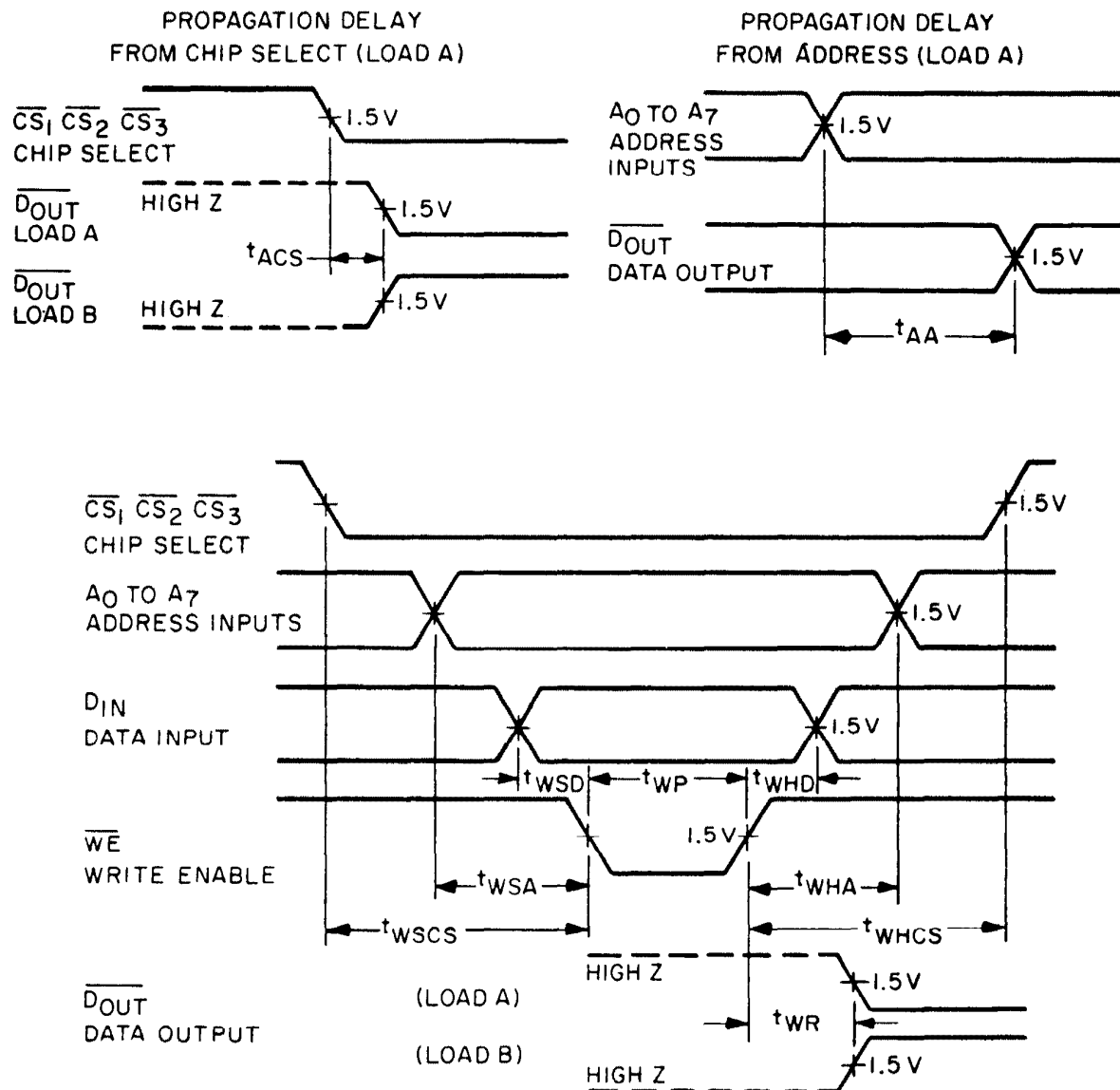
NOTES:

1. Use load circuit A in transitions between logic levels and from high Z state to a logic low state.
2. Use load circuit B in transitions from high Z state to logic high state.
3. Use load circuit C in transitions from a logic level to the high Z state.
4. $C_L = 30 \text{ pF} \pm 5\%$ including wiring and probe capacitance.

FIGURE 6. Switching time load circuits, test conditions and waveforms.

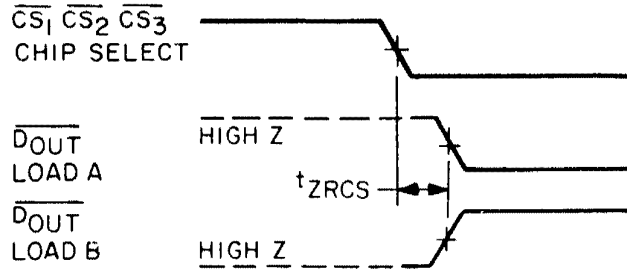
Device type 01

FIGURE 6. Switching time test circuit and waveforms - Continued.

Device type 02 and 04FIGURE 6. Switching time test circuit and waveforms - Continued.

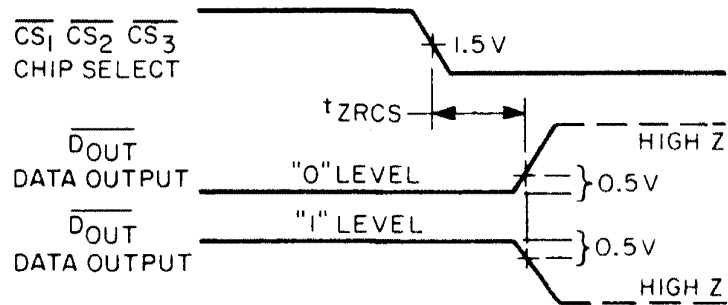
Device type 02

PROPAGATION DELAY
FROM CHIP SELECT TO HIGH Z



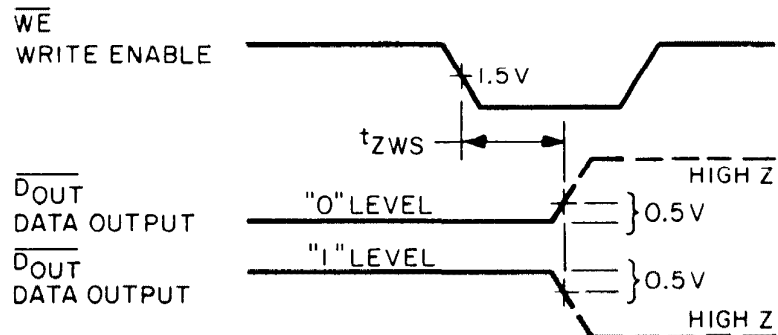
Device type 04

PROPAGATION DELAY
FROM CHIP SELECT TO HIGH Z



Device type 02 and 04

WRITE ENABLE TO HIGH Z DELAY



(ALL t_{ZXXX} PARAMETERS ARE MEASURED AT A DELTA OF 0.5V
FROM THE LOGIC LEVEL AND USING LOAD C)

FIGURE 6. Switching time test circuit and waveforms - Continued.

Device type 03

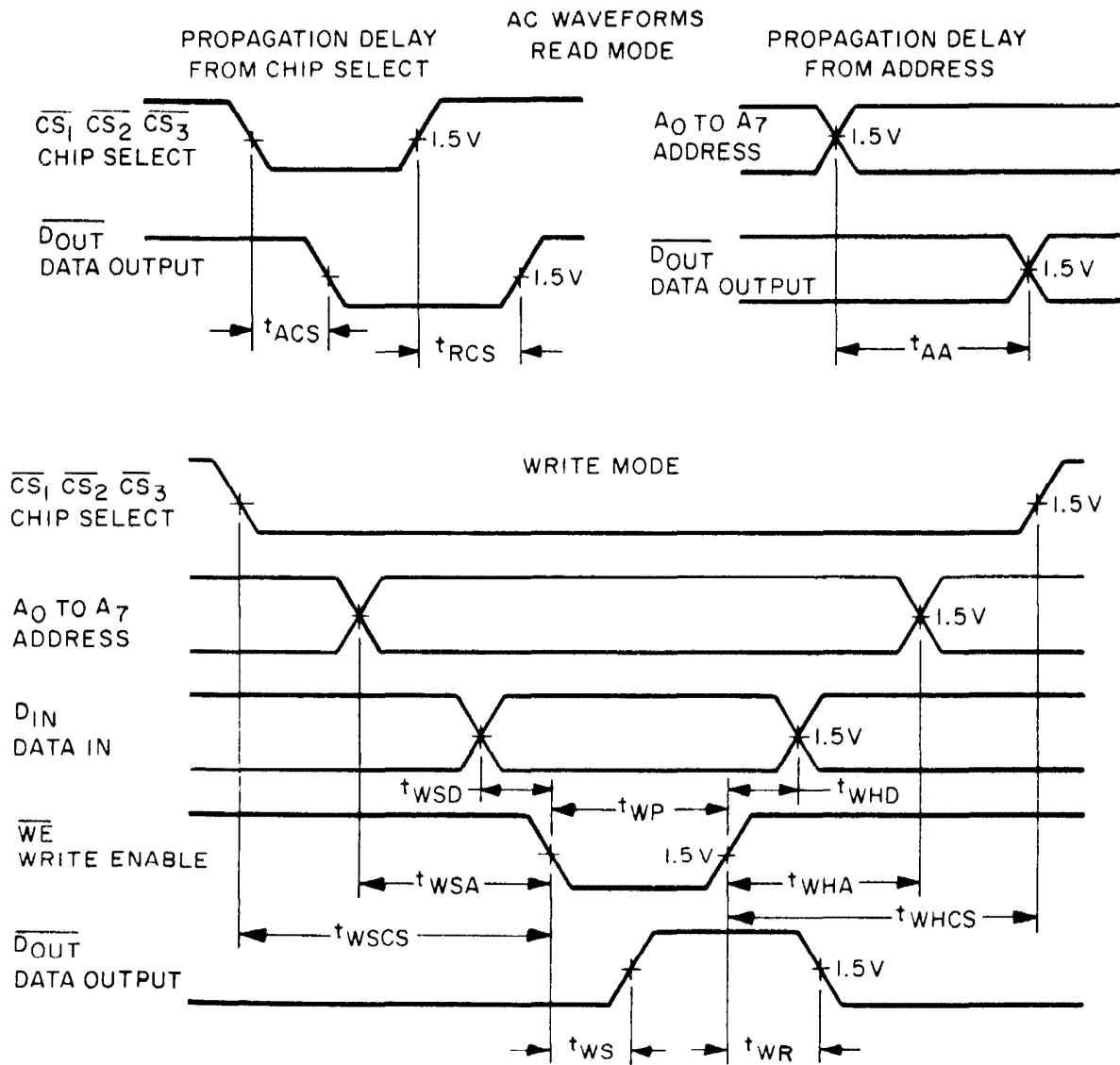


FIGURE 6. Switching time test circuit and waveforms - Continued.

Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F Test No.	1 A0	2 A1	3 A2	4 A3	5 CST	6 CS2	7 CS3	8 GND	9 DIN	10 WE	11 DOU	12 A4	13 A5	14 A6	15 A7	16 VCC	Meas. terminal	Test limits		
																					Min	Max	Unit
$T_A = 25^\circ\text{C}$	V_{IC} 																						

TABLE III. Group A inspection for device type 01 - Continued.

Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
				A0	A1	A2	A3	CS1	CS2	CS3	GND	DIN	WE	DOUT	A4	A5	A6	A7	VCC		Min	Max	Unit
$T_A = 25^\circ\text{C}$	I_{IH1}	3010	30				4.5 V				GND								5.5 V	A3		25	μA
			31					4.5 V												CS1			
			32						4.5 V											CS2			
			33							4.5 V										CS3			
			34									4.5 V								DIN			
			35										4.5 V							WE			
			36												4.5 V					A4			
			37													4.5 V				A5			
			38														4.5 V			A6			
			39															4.5 V		A7			
	I_{IH2}		40	5.5 V																A0	1		mA
			41		5.5 V															A1			
			42			5.5 V														A2			
			43				5.5 V													A3			
			44					5.5 V												CS1			
			45						5.5 V											CS2			
			46							5.5 V										CS3			
			47								5.5 V									DIN			
			48									5.5 V								WE			
			49										5.5 V							A4			
	I_{CEX} I_{CC} V_{OL} V_{IL} V_{IH}	3005 3007 1/	50												5.5 V					A5			
			51													5.5 V				A6			
			52														5.5 V			A7			
			53											5.5 V						DOUT	100		μA
			54	GND	GND	GND	GND	GND	GND	GND		GND	GND		GND	GND	GND	GND		VCC	145		mA
			55	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V		0.8 V	2/	16 mA	0.8 V	0.8 V	0.8 V	0.8 V	4.5 V	DOUT	.45		V
			56	.8 V 2.0 V	.8 V 2.0 V	.8 V 2.0 V	.8 V 2.0 V	.8 V 2.0 V	.8 V 2.0 V	.8 V 2.0 V		.8 V 2.0 V	.8 V 2.0 V		.8 V 2.0 V	.8 V 2.0 V	.8 V 2.0 V	.8 V 2.0 V	4.5 V	DOUT	2/		

See footnotes at end of table.

Terminal conditions (pins not designated are open)

See footnotes at end of table.

TABLE III. Group A inspection for device types 02 and 04.

Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
				A0	A1	$\overline{\text{CS1}}$	$\overline{\text{CS2}}$	$\overline{\text{CS3}}$	$\overline{\text{DOUT}}$	A4	GND	A5	A6	A7	$\overline{\text{WE}}$	DIN	A2	A3	VCC		Min	Max	Unit
$T_A = 25^\circ\text{C}$	V_{IC}		1	-10 mA							GND								5.5 V	A0		-1.5	V
			2		-10 mA															A1			
			3			-10 mA														$\overline{\text{CS1}}$			
			4				-10 mA													$\overline{\text{CS2}}$			
			5					-10 mA												$\overline{\text{CS3}}$			
			6							-10 mA										A4			
			7									-10 mA								A5			
			8										-10 mA							A6			
			9											-10 mA						A7			
			10												-10 mA					$\overline{\text{WE}}$			
			11													-10 mA				DIN			
			12														-10 mA			A2			
			13															-10 mA		A3			
$T_A = 25^\circ\text{C}$	I_{IL}	3009	14	0.4 V																A0	-800		μA
			15		0.4 V															A1			
			16			0.4 V														$\overline{\text{CS1}}$			
			17				0.4 V													$\overline{\text{CS2}}$			
			18					0.4 V												$\overline{\text{CS3}}$			
			19						0.4 V											A4			
			20							0.4 V										A5			
			21								0.4 V									A6			
			22									0.4 V								A7			
			23										0.4 V							$\overline{\text{WE}}$			
			24											0.4 V						DIN			
			25												0.4 V					A2			
			26													0.4 V				A3			
			27	4.5 V														0.4 V		A0		25	
			28		4.5 V															A1		25	
			29			4.5 V														$\overline{\text{CS1}}$		25	

MIL-M-38510/230A

TABLE III. Group A inspection for device types 02 and 04 - Continued.

Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
				A0	A1	CST	CS2	CS3	DOUT	A4	GND	A5	A6	A7	WE	DIN	A2	A3	VCC		Min	Max	Unit
$T_A = 25^\circ\text{C}$	I_{IH1}	3010	30				4.5 V				GND								5.5 V	CS2		25	μA
			31					4.5 V												CS3			
			32							4.5 V										A4			
			33									4.5 V								A5			
			34										4.5 V							A6			
			35											4.5 V						A7			
			36												4.5 V					WE			
			37													4.5 V				DIN			
			38														4.5 V			A2			
			39															4.5 V		A3			
			40	5.5 V																A0	1		mA
			41		5.5 V															A1			
			42			5.5 V														CST			
			43				5.5 V													CS2			
			44					5.5 V												CS3			
			45							5.5 V										A4			
			46									5.5 V								A5			
			47										5.5 V							A6			
			48											5.5 V						A7			
			49												5.5 V					WE			
			50													5.5 V				DIN			
			51														5.5 V			A2			
			52															5.5 V		A3			
	I_{OS}	3011	53						GND											DOUT	-20	-100	mA
			54	GND	GND	GND	GND	GND		GND		GND	GND	GND	GND	GND	GND	GND		VCC		7/	μA
			55	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	2.4 V	0.4 V		0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V		DOUT		50	μA
			56	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	.5 V	0.4 V		0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V		DOUT		-50	μA
			57	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	16 mA	0.8 V		0.8 V	0.8 V	0.8 V	8/	0.8 V	0.8 V	0.8 V	4.5 V	DOUT		.45	V
			58	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	-5.2 mA	0.8 V		0.8 V	0.8 V	0.8 V	8/	0.8 V	0.8 V	0.8 V	4.5 V	DOUT	2.4		V
	I_{IH2}																						
	I_{OLZ}	3009																					
	V_{OL}	3007																					
	V_{OH}	3006																					

See footnotes at end of table.

MIL-M-38510/230A

24

[illegible]

TABLE III. Group A inspection for device type 03.

Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
				A0	A1	CST	CS2	CS3	DOOT	A4	GND	A5	A6	A7	WE	DIN	A2	A3	YCC		Min	Max	Unit
$T_A = 25^\circ\text{C}$ I_{IL} I_{IH1} I_{IH2}	I_{IL} I_{IH1} I_{IH2}	3009 3010	1	.4 V							GND								5.5 V	A0	-800		μA
			2		.4 V																		
			3			.4 V																	
			4				.4 V																
			5					.4 V															
			6							.4 V													
			7									.4 V											
			8										.4 V										
			9											.4 V									
			10												.4 V								
			11													.4 V							
			12														.4 V						
			13															.4 V					
			14	4.5 V															.4 V				
			15		4.5 V																		
			16			4.5 V																	
			17				4.5 V																
			18					4.5 V															
			19						4.5 V														
			20							4.5 V													
			21								4.5 V												
			22									4.5 V											
			23										4.5 V										
			24											4.5 V									
			25												4.5 V								
			26													4.5 V							
			27	5.5 V														4.5 V					
			28		5.5 V																1		mA
			29			5.5 V															1		mA

MIL-M-38510/230A

TABLE III. Group A inspection for device type 03 - Continued.

Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
				A0	A1	CS1	CS2	CS3	DOUT	A4	GND	A5	A6	A7	WE	DIN	A2	A3	VCC		Min	Max	Unit
$T_A = 25^\circ\text{C}$	I_{IH2}	3010	30				5.5 V				GND								5.5 V	CS2		1	mA
			31					5.5 V												CS3			
			32							5.5 V										A4			
			33									5.5 V								A5			
			34										5.5 V							A6			
			35											5.5 V						A7			
			36												5.5 V					WE			
			37													5.5 V				DIN			
			38														5.5 V			A2			
			39															5.5 V		A3			
	V_{IC}		40	-10 mA																A0	-1.5	V	
			41		-10 mA															A1			
			42			-10 mA														CS1			
			43				-10 mA													CS2			
			44					-10 mA												CS3			
			45							-10 mA										A4			
			46									-10 mA								A5			
			47										-10 mA							A6			
			48											-10 mA						A7			
			49												-10 mA					WE			
			50													-10 mA				DIN			
			51														-10 mA			A2			
	I_{CEX}		52															-10 mA		A3			
	I_{CC}	3005	54						5.5 V											DOUT	100	μA	
	V_{IL}			.8 V	.8 V	.8 V	.8 V	.8 V		.8 V		.8 V	.8 V	.8 V	.8 V	.8 V	.8 V	.8 V		VCC	145	mA	
	V_{IH}	1/	55	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V		2.0 V		2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V		Output	2/		
	V_{OL}	3007	56	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	16 mA	0.8 V		0.8 V	0.8 V	0.8 V	8/	0.3 V	0.8 V	0.8 V	4.5 V	DOUT	.45	V	

MIL-M-38510/230A

TABLE III. Group A inspection for device type 03 - Continued.

Terminal conditions (pins not designated are open)																							
Subgroup	Symbol	MIL-STD-883 method	Cases E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
				A0	A1	CS1	CS2	CS3	DO0T	A4	GND	A5	A6	A7	WE	DIN	A2	A3	VCC		Min	Max	Unit
2	Same test terminal conditions and limits as subgroup 1, except $T_A = 125^{\circ}\text{C}$ and V_{IC} tests are omitted.																						
3	Same test terminal conditions and limits as subgroup 1, except $T_A = -55^{\circ}\text{C}$ and V_{IC} tests are omitted.																						
7	Functional	3014	57	3/	3/	3/	3/	3/	3/	3/	GND	3/	3/	3/	3/	3/	3/	3/	3/	Output		3/	
8	Same tests, terminal conditions and limits as subgroup 7, except $T_A = 125^{\circ}\text{C}$ and -55°C .																						
$T_A = 25^{\circ}\text{C}$	t_{AA}	GALPAT Figure 6 GG II Figure 6	58	4/	4/	4/	4/	4/	5/	4/	GND	4/	4/	4/	4/	4/	4/	4/	4/	Output		65	ns
	t_{ACS}		59	4/	4/	4/	4/	4/	5/	4/		4/	4/	4/	4/	4/	4/	4/	4/			40	
	t_{RCS}		60	4/	4/	4/	4/	4/	5/	4/		4/	4/	4/	4/	4/	4/	4/	4/			35	
	t_{WS}		61	4/	4/	4/	4/	4/	5/	4/		4/	4/	4/	4/	4/	4/	4/	4/			50	
	t_{WR}		62	4/	4/	4/	4/	4/	5/	4/		4/	4/	4/	4/	4/	4/	4/	4/			50	
	t_{WP}		63	6/	6/	6/	6/	6/	6/	6/		6/	6/	6/	6/	6/	6/	6/	5/		50		
	t_{WSA}		64	6/	6/	6/	6/	6/	6/	6/		6/	6/	6/	6/	6/	6/	6/	5/		10		
	t_{MHA}		65	6/	6/	6/	6/	6/	6/	6/		6/	6/	6/	6/	6/	6/	6/	5/		5		
	t_{WSD}		66	6/	6/	6/	6/	6/	6/	6/		6/	6/	6/	6/	6/	6/	6/	5/		10		
	t_{MHD}		67	6/	6/	6/	6/	6/	6/	6/		6/	6/	6/	6/	6/	6/	6/	5/		5		
	t_{WSCS}		68	6/	6/	6/	6/	6/	6/	6/		6/	6/	6/	6/	6/	6/	6/	5/		10		
	t_{MHCS}		69	6/	6/	6/	6/	6/	6/	6/		6/	6/	6/	6/	6/	6/	6/	5/		5		
10	Same test, terminal conditions and limits as subgroup 9, except $T_A = 125^{\circ}\text{C}$.																						
11	Same test, terminal conditions and limits as subgroup 9, except $T_A = -55^{\circ}\text{C}$.																						

27

MIL-M-38510/230A

- 1/ A field of ones and zeros is written into the memory and then read for correct contents.
 2/ Memory contents are checked at all locations at functional speeds.
 3/ The function tests shall verify the truth table of figure 4. All bits shall be tested. Terminal conditions shall be as follows:
- Inputs: $H = 2.0\text{ V}$, $L = 0.8\text{ V}$.
 - Outputs: Output voltage shall be either:
 - $H = 2.4\text{ V}$ minimum and $L = 0.45\text{ V}$ maximum, when using a high-speed checker double comparator, or
 - $H \geq 1.0\text{ V}$ and $L \leq 1.0\text{ V}$, using a high-speed checker single comparator.
 - The functional tests shall be performed with $V_{CC} = 4.5\text{ V}$ and $V_{CC} = 5.5\text{ V}$.
- 4/ GALPAT. This program will test all bits in the array, the addressing and interaction between bits for performance, t_{AA} , t_{ACS} , t_{RCS} , t_{WS} , and t_{WR} , the memory is initialized by writing a field of "H" and then a field of "L". Description:
- Write an "H" in word 0.
 - Word 0 is read.
 - Word 1 is read.
 - Word 0 is read.
 - Word 2 is read.
 - Word 0 is read.
 - The reading procedure continues back and forth between word 0 and the next higher numbered word until word 255 is reached then increments to the next word and reads back and forth as in steps a through

- h. Pass execution time = $(n^2 + n) \times \text{cycle time}$, $n = 256$.
 i. The GALPAT tests shall be performed with $V_{CC} = 4.5\text{ V}$ and 5.5 V .

- 5/ The test conditions of figure 6 shall apply.
 6/ Galloping Galwresh (with row column ping-pong read GG II). The Galloping Galwresh (GG) is started by first writing a field of zeros and then a field of ones into the memory under test (MUT). The following sequence is then performed.

Test bit



Background bit

The background bits are read in ping-pong fashion in the row/column of the test bit. The sequence is repeated for the next test bit (Y advancing X) until the test bit reaches X max Y max. The inverse pattern is then performed with $V_{CC} = 4.5\text{ V}$, then 5.5 V .

- 7/ I_{CC} limit for device type 02 is 145 mA, maximum.
 I_{CC} limit for device type 04 is 75 mA, maximum.
 8/ Toggle from 5.5 V to 0.4 V and return.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logistic support.

6.3 Ordering data. The contract should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirement for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to procuring activity in addition to notification to qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003), corrective action, and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements will not affect the part number.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	- - - - -	Electrical ground (common terminal)
V _{IN}	- - - - -	Voltage level at an input terminal
V _{IC}	- - - - -	Input clamp voltage
I _{OHZ}	- - - - -	High impedance (off-state) output high current
I _{OLZ}	- - - - -	High impedance (off-state) output low current
t _{AA}	- - - - -	Address access time.
t _{ACS}	- - - - -	Chip select time.
t _p	- - - - -	Write pulse width.
t _{RCS}	- - - - -	Chip select recovery time.
t _{WHA}	- - - - -	Address hold time after write.
t _{WHD}	- - - - -	Data hold time after write.
t _{WHCS}	- - - - -	Chip select hold time after write.
t _{WR}	- - - - -	Write recovery time.
t _{WS}	- - - - -	Write disable time.
t _{WSA}	- - - - -	Address setup time prior to write.
t _{WSCS}	- - - - -	Chip select setup time prior to write.
t _{WSD}	- - - - -	Data setup time prior to write.
t _{ZRCS}	- - - - -	Chip select disable time to high impedance.
t _{ZWS}	- - - - -	Write disable time to high impedance.

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits procured for Government logistic support will be procured to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer lengths leads and lead forming shall not affect the part number.

6.6 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes not more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process from the same plant as the die represented. Group D (see 4.4.4) generic data shall be on date codes no more than one year old and on the same package type (see terms, definitions, and symbols of MIL-M-38510) and from the same plant as the package represented. The vendor is required to retain generic data for a period of not less than 36 months from the date of shipment.

6.7 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

6.8 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	93410
02	93421
03	93411
04	93L420

6.9 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
 Army - ER
 Navy - EC
 Air Force - 17

Preparing activity:
 Air Force - 17
 (Project 5962-0708)

Review activities:
 Army - AR, MI
 Navy - SH, OS
 Air Force - 11, 19, 85, 99
 DLA - ES

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User activities:
 Army - SM
 Navy - AS, CG, MC

Agent:
 DLA - ES