

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, NMOS 8K X 8 BIT, ELECTRICALLY ERASABLE, PROGRAMMABLE READ-ONLY MEMORY (EEPROM) MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, N-channel MOS, 8192 words/8 bit, 5.0 volt, electrically erasable programmable read-only memory microcircuits. Two product assurance classes (S and B), a choice of lead finishes and two package types are provided for each device and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device types. The device types shall be as shown in the following. The circuit organization shall be 8192 words/8 bit.

Device type	Access time	Write speed	Write mode	End of write indicator	Endurance
01	450 ns	10 ms	Byte/page	Data poll	10,000 cy
02	350 ns	10 ms	Byte/page	Data poll	10,000 cy
03	300 ns	10 ms	Byte/page	Data poll	10,000 cy
04	250 ns	10 ms	Byte/page	Data poll	10,000 cy
05	350 ns	10 ms	Byte/page	Data poll	100,000 cy
06	250 ns	10 ms	Byte/page	Data poll	100,000 cy
07	350 ns	10 ms	Byte	RDY/BUSY	10,000 cy
08	250 ns	10 ms	Byte	RDY/BUSY	10,000 cy
09	250 ns	2 ms	Byte	RDY/BUSY	10,000 cy
10	250 ns	10 ms	Byte	RDY/BUSY	100,000 cy
11	250 ns	10 ms	Byte	RDY/BUSY	1,000,000 cy

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows.

Outline letter	Case outline (see MIL-M-38510, appendix C)
X	D-10 (28-lead, 1/2" x 1 3/8"), dual-in-line package
Y	C-12 (32-terminal, 0.450" x 0.550"), chip carrier package

1.3 Absolute maximum ratings.

All input and output voltages (including V_{CC})	1/	-0.5 V dc to +7.0 V dc
Voltage on OE and WE	- - - - -	-0.5 v dc to +18.0 V dc
Voltage for chip clear (V_h)	- - - - -	+18.0 V dc
Operating case temperature range (T_C)	- - - - -	-55°C to +125°C
Storage temperature range	- - - - -	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	- - - - -	+300°C

1/ Voltages are with respect to ground. Pin voltages will be stated in this manner throughout the remainder of this specification unless otherwise noted.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

Thermal resistance, junction-to-case (θ_{JC}):

Case X - - - - -	21°C/W (CERDIP)
Case Y - - - - -	18°C/W (LCC)
Maximum power dissipation (P_D) ^{2/-} - - - - -	1.0 W
Junction temperature (T_J) - - - - -	+175°C
Endurance - - - - -	10,000 cycles/byte, minimum (types 01-04, 07-09)
	100,000 cycles/byte, minimum (types 05-06, 10)
	1,000,000 cycles/byte, minimum (type 11)
Data retention - - - - -	10 years, minimum

1.4 Recommended operating conditions.

	Device types	Min	Max	Units
Supply voltages:				
V _{CC} - - - - -	All	4.5	5.5	V dc
V _{SS} - - - - -	All	0.0	0.0	V dc
High level input voltages:				
V _{IH} - - - - -	All	2.0	V _{CC} +1	V dc
Low level input voltages:				
V _{IL} - - - - -	All	-0.3	0.8	V dc
Operating case temperature (T_C) - - - - -	All	-55	+125	°C
High level chip erase voltage:				
V _{OE} on OE - - - - -	01-06	18	22	V dc
V _H on OE and WE - - - - -	07-11	14	16	V dc

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets, or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

^{2/-} Under worst case operating conditions.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram will be as specified on figure 3. Upon implementing design changes, the manufacturer must submit a new block diagram to the qualifying activity for inclusion in this specification. The block diagram shall clearly define row address inputs and the column address inputs.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, the country of origin may be omitted from the body of the microcircuit but shall be retained on the initial container.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 47 (see MIL-M-38510, appendix E).

3.8 Processing of EEPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.8.1 Condition of the supplied devices. Devices will be supplied in an unprogrammed or cleared state. No provision will be made for supplying programmed devices.

3.8.2 Erasure of EEPROMs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.4.

3.8.3 Programming of EEPROMs. When specified, devices shall be programmed in accordance with the procedures and characteristics specified in 4.5.3.

3.8.4 Verification of state of EEPROMs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and the device shall be removed from the lot or sample.

3.8.5 Power supply sequence of EEPROMs. In order to reduce the probability of inadvertent writes, the following power supply sequence shall be observed:

- a. A logic high state shall be applied to $\overline{WE}$ and $\overline{CE}$ or both at the same time or before the applications of V_{CC} .
- b. A logic high state shall be applied to $\overline{WE}$ and $\overline{CE}$ or both at the same time or before the removal of V_{CC} .

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $V_{CC} = +5 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V dc}$ $-55^\circ\text{C} < T_C < +125^\circ\text{C}$ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
V_{CC} supply current	ICC1 (A) active	$\overline{WE} = V_{IH}$, $\overline{CE} = \overline{OE} = V_{IL}$ Addresses = V_{CC} I/O open	A11		140	mA
	ICC2 (SB) standby	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ Addresses = V_{CC} I/O open	01-06 07-11		70 50	mA mA
Low level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V dc}$, $I_{OL} = 2.1 \text{ mA}$	A11		.4	V
High level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V dc}$, $I_{OH} = -400 \text{ } \mu\text{A}$	A11	2.4		V
Input leakage current	I_{IL}	$V_I = 0.1 \text{ V dc}$	A11	-10	10	μA
	I_{IH}	$V_I = 5.5 \text{ V dc}$	A11	-10	10	μA
High impedance output leakage	I_{OLZ}	$V_O = 0.0 \text{ V dc}$, $\overline{CE} = V_{IH}$	A11	-10	10	μA
	I_{OHZ}	$V_O = 5.5 \text{ V dc}$, $\overline{CE} = V_{IH}$	A11	-10	10	μA
Input capacitance	C_I	$V_I = 0 \text{ V}$, $V_{CC} = 5 \text{ V}$, $T_A = +25^\circ\text{C}$, $f = 1 \text{ MHz}$ (see 4.4.1c) 2/	A11		6	pF
Output capacitance	C_O	$V_O = 0 \text{ V}$, $V_{CC} = 5 \text{ V}$, $T_A = +25^\circ\text{C}$, $f = 1 \text{ MHz}$ (see 4.4.1c) 2/	A11		10	pF
Output enable		$\overline{WE} = V_{IH}$, $\overline{CE} = V_{IL}$				
High voltage input current	I_{OE}	$V_{OE} = 22 \text{ V dc}$	01-06		10	μA
	I_{WE} , I_{OE}	$V_h = 16 \text{ V dc}$	07-11		10	μA
High voltage (chip erase)	V_{OE}	$\overline{WE} = \overline{CE} = V_h$	01-06	18	22	V
	V_h		07-11	14	16	V
Input logic high voltage	V_{IH} 3/		A11	2.0	V_{CC+1}	V
Input logic low voltage	V_{IL} 3/		A11	-0.3	0.8	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions $V_{CC} = +5 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V dc}$ $-55^\circ \text{C} < T_C < +125^\circ \text{C}$ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
READ cycle time	t_{AVAV} 4/	(See figures 5-8)	01	450		ns
			02,05,07	350		ns
			03	300		ns
			04,06,08			
			09,10,11	250		ns
Chip enable access time	t_{ELQV} 4/		01		450	ns
			02,05,07		350	ns
			03		300	ns
			04,06,08			
			09,10,11		250	ns
Address access time	t_{AVQV} 4/		01		450	ns
			02,05,07		350	ns
			03		300	ns
			04,06,08			
			09,10,11		250	ns
Output enable access time	t_{OLQV} 4/		01-06		150	ns
			07-11		100	ns
Chip enable to output in low Z	t_{ELQX} 5/		All	10		ns
Chip enable to output in high Z	t_{EHQZ} 6/		01		100	ns
			02,03		80	ns
			05,07		80	ns
			04,06,08		60	ns
			09,10,11		60	ns
Output enable to output in low Z	t_{OLQX} 5/		All	10		ns
Output enable to output in high Z	t_{OHQZ} 6/		01		100	ns
			02,03		80	ns
			05,07		80	ns
			04,06,08		60	ns
			09,10,11		60	ns
Output hold from address change	t_{AXQX} 5/		01-06	10		ns
			07-11	0		ns
Write cycle time, $\overline{WE}$ write	t_{WLAV}		01-08		10	ms
			10,11		10	ms
			09		2	ms
Write cycle time, $\overline{CE}$ write	t_{ELAV}		01-08		10	ms
			10,11		10	ms
			09		2	ms
Address to $\overline{WE}$ setup time	t_{AVWL} 4/		All	10		ns
Address to $\overline{CE}$ setup time	t_{AVEL} 4/		All	10		ns
Address hold time after $\overline{WE}$ low	t_{WLAX} 4/		01-06	200		ns
			07-11	50		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions $V_{CC} = +5 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V dc}$ $-55^{\circ}\text{C} < T_C < +125^{\circ}\text{C}$ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Address hold time after CE low	t_{ELAX} 4/	(See figures 5-8)	01-06	200		ns
			07-11	50		ns
Chip-enable to WE setup time	t_{ELWL} 4/		All	0		ns
Write enable to CE setup time	t_{WLEL} 4/		All	0		ns
Chip enable hold time after WE high	t_{WHEH} 4/		All	0		ns
Write enable hold time after CE high	t_{EHWH} 4/		All	0		ns
Chip enable to end of write input	t_{ELEH} 3/4/7/		All	150		ns
Write pulse width	t_{WLWH} 3/4/7/		All	150		ns
Output enable setup time	t_{OHWL} , t_{OHEL} 4/		All	10		ns
Output enable hold time	t_{WHOL} , t_{EHOL} 4/		All	10		ns
Write control recovery time	t_{WHWL} , t_{EHEL} 4/		All	50		ns
Data valid time	t_{WLDV} 4/ 8/		01-06	300		ns
			07-11	1		μs
Data setup time	t_{DVWH} , t_{DVEH} 4/		01-06	100		ns
			07-11	50		ns
Data hold time	t_{WHDX} , t_{EHDX} 4/		All	20		ns
WE pulse high	t_{WHHL1}		01-06	50		ns
Byte load cycle	t_{WLWL1}		01-06	3	20	μs
Write cycle	t_{WHWL2}		01-06		10	ms
Time to device busy	t_{WHRL} , t_{EHRL} 4/		07-11		200	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions $V_{CC} = +5 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V dc}$ $-55^{\circ}\text{C} < T_C < +125^{\circ}\text{C}$ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Delay from ready to next write	t_{RHAV} 4/	(See figures 5-8)	07-11	10		μs
Data valid to next write (page mode)	t_{QVWL}		01-06	500		μs
Output enable hold time (page mode)	t_{WHOL}		01-06	10		ns
Output enable access time (page mode)	t_{OLQV}		01-06		150	ns
Chip enable access time (page mode)	t_{ELQV}		01		450	ns
			02,05		350	ns
			03		300	ns
			04,06		250	ns
Output enable hold time (page mode)	t_{OHWL1}		01-06	10		ns
Write cycle time	t_{WHWL2}	01-06		10	ms	

1/ DC and read and write modes.

2/ This parameter is measured only upon initial qualification and for redesigns, see 4.4.1c. All pins not being tested are to be grounded.

3/ Tested by inference for all input and control pins.

4/ Tested by applying specified timing signals and conditions, including:

Equivalent ac test conditions.

Output load: 1 TTL gate and $C_L = 100 \text{ pF}$.

Input rise and fall times $\leq 10 \text{ ns}$.

Input pulse levels: 0.4 V and 2.4 V.

Timing measurement reference levels: Inputs 1 V and 2 V.

Outputs 0.8 V and 2 V.

When using single level comparators, 1.5 V reference levels may be used for functional tests.

5/ Only performed for initial qualification and after a design change that could affect the high or low impedance state.

6/ Tested by inference only.

7/ $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 20 ns write pulse will not activate a write cycle.

8/ Data must be valid within 300 ns (device types 01-06) or 1 μs (device types 07-11) after the initiation of a write cycle.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1,7,9, or 2, 8 (hot), 10	1,7,9, or 2, 8 (hot), 10
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11 4/	1*,2,3,7*,8, 9,10,11 4/
Group A test requirements (method 5005)	1,2,3,4**,7, 8,9,10,11 5/	1,2,3,4**,7, 8,9,10,11 5/
Group B test requirements (method 5005) subgroup 5	1,2,3,7,8,9, 10,11	N/A
Group C end-point electrical parameters (method 5005)	N/A	1,2,3,7,8, 9,10,11
Group D end-point electrical parameters (method 5005)	1,2,3,7,8, 9,10,11	1,2,3,7,8, 9,10,11

- 1/ For all electrical tests, the device shall be programmed to the data pattern specified.
- 2/ Any subgroups at the same temperature may be combined when using a multifunction tester.
- 3/ Subgroups 7 and 8 shall consist of writing and reading the data pattern specified.
- 4/ * The PDA applies to subgroups 1 and 7 (see 4.2c):
- 5/** Subgroup 4 (capacitance) is measured only upon initial qualification and for redesign; see 4.4.1c.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in (method 1015 of MIL-STD-883).

- (1) Test condition D or E, using the circuit shown on figure 4 (or equivalent).
- (2) $T_A = +125^\circ\text{C}$ minimum.
- (3) Prior to burn-in the devices shall be programmed (see 3.8.3) with the data pattern shown on figure 8. The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation (see 4.2c).

b. Interim and final electrical test parameters shall be as specified in table II. Interim electrical test parameters prior to burn-in must be performed by the manufacturer. The following data patterns shall be included in group A subgroups 7 or 8 (high and low temperature): All "0's", all "1's", checkerboard and checkerboard complement. Each temperature shall include, at a minimum, the programming of one data pattern. Subgroups 9, 10, and 11, and 11 shall be performed on devices containing a checkerboard and a checkerboard complement data patterns or equivalent alternating bit and complementary data patterns.

- c. Percent defective allowable (PDA). The PDA for class B devices shall be as specified in MIL-M-38510. The PDA is specified as 5 percent for class B devices based on failures from group A, subgroups 1 and 7 after cooldown, at final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. All screening failures of group A, subgroups 1 and 7 after burn-in divided by the total number of devices submitted to burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA.
- d. An endurance test including a data retention bake in accordance with method 1003 of MIL-STD-883, prior to burn-in (e.g., may be performed at wafer sort) shall be included as part of the screening procedure, with the following conditions:
 - (1) Cycling may be block, byte or page at equipment room ambient and shall cycle all bytes a minimum 10,000 cycles for device types 01-04, 07-09, and 50,000 cycles for device types 05-06 and 10-11.
 - (2) After cycling, perform a high temperature unbiased storage for 2.5 hours at +250°C minimum, or 24 hours at +170°C minimum, or 72 hours at +150°C minimum. All devices shall be programmed with a charge opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern, see 3.8.3).
 - (3) Read the data retention pattern and test using subgroups 1, 7, and 9 (minimum, e.g., high temperature equivalent subgroups 2, 8, and 10 may be used) after cycling and bake, prior to burn-in. Devices having bits not in the proper state after storage shall constitute a device failure.
- e. After the completion of all screening, the devices shall be erased and verified prior to delivery.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type on this specification, then the slower device type may be part I qualified by conducting only group A electrical tests and any electricals specified as additional group C subgroups and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_1 and C_0 measurements) shall be measured for initial qualification and after process or design changes which affect capacitance. Sample size is 25 devices with an accept on zero.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows.

- a. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015 for initial qualification and after process or design changes which may affect input-output protection

circuitry. The option to categorize devices as ESD sensitive without performing the test is not allowed. Device types categorized as ESD sensitive shall be further tested using method 3015 modified as follows:

Only those device types that pass ESDS testing at 1,000 volts or greater shall be considered as conforming to the requirements of this specification.

- b. All class S devices selected for testing shall be programmed (see 3.8.3) with pattern shown on figure 8.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. All devices requiring endpoint electrical testing shall be programmed with the pattern shown on figure 8.
- c. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, as specified in 4.5.2 and using the circuit shown on figure 4 (or equivalent).
 - (2) Ambient temperature shall be +125°C minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
 - (4) Read the pattern after burn-in and perform endpoint electrical tests in accordance with table II herein for group C.
- d. An endurance test, in accordance with method 1033 of MIL-STD-883, shall be added to group C1 inspection prior to performing the steady-state life test (see 4.4.3c) and extended data retention (see 4.4.3e). Cycling may be block, byte or page from devices passing group A after the completion of the requirements of 4.2 herein. Initially, two groups of devices shall be formed, cell 1 and cell 2. The following conditions shall be met:
 - (1) Cell 1 shall be cycled at -55°C and cell 2 shall be cycled at +125°C for a minimum of 10,000 cycles for device types 01-04, 07-09; 100,000 for device types 05-06 and 10; or 1,000,000 cycles for device type 11 (see 1.2.1).
 - (2) Perform group A subgroups 1, 7, and 9 after cycling. Form two new cells (cell 3 and cell 4) for steady-state life and extended data retention. Cell 3 for steady-state life test consists of 1/2 of the devices from cell 1 and 1/2 of the devices from cell 2. Cell 4 for extended data retention consists of the remaining devices from cell 1 and cell 2.
 - (3) The sample plans for cell 1, cell 2, cell 3 and cell 4 shall individually be the same as for group C1, as specified in method 5005 of MIL-STD-883.
- e. Extended data retention shall consist of:
 - (1) Program all bits in each device with the data pattern representing the worst case data retention pattern (see 4.2d.2).
 - (2) Unbiased bake for 1,000 hours (minimum) at +150°C (minimum).
 - (3) Read the pattern after bake and perform endpoint electrical tests for table II herein for group C.
- f. Cell 1, cell 2, cell 3, and cell 4 must individually pass the specified sample plan.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows.

- a. Endpoint electrical tests shall be as specified in table II herein.
- b. All devices selected for electrical testing shall be programmed with the pattern shown on figure 8. After completion of all testing, the devices shall have the programmed pattern read, then be erased and verified. Where the use of electrical rejects are permitted, no programming or erasure or verification is required.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Voltages and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Life test, burn-in, cooldown and electrical test procedure. When devices are measured at +25°C following application of the steady-state life or burn-in test condition, all devices shall be cooled to +35°C or within +10°C of power stable condition prior to removal of bias voltages-signals. Any electrical tests required shall first be performed at -55°C or +25°C prior to any required tests at +125°C.

4.5.3 Programming procedure. The waveforms and timing relationships shown on figure 6 and the conditions specified in table I shall be adhered to. Initially and after each chip erasure (see 4.5.4), all bits are in the high state (output at V_{OH}).

4.5.3.1 Byte write operation. Information is introduced by selectively programming "L" (logic "0" level) or "H" (logic "1" level) into the desired bit locations. A programmed "L" can be changed to an "H" by programming an "H". No erasure is necessary (see 4.5.4).

4.5.3.2 Page mode write operation. During a page mode write cycle, the bits of the selected bytes can be "H" or "L", and addresses within the page that do not require data change should not be selected. Therefore, a page mode write cycle can be used to write data into two to sixteen address locations within the same page (i.e., it is not necessary to write all sixteen addresses in the page during a page mode write cycle) (applies to device types 01-06).

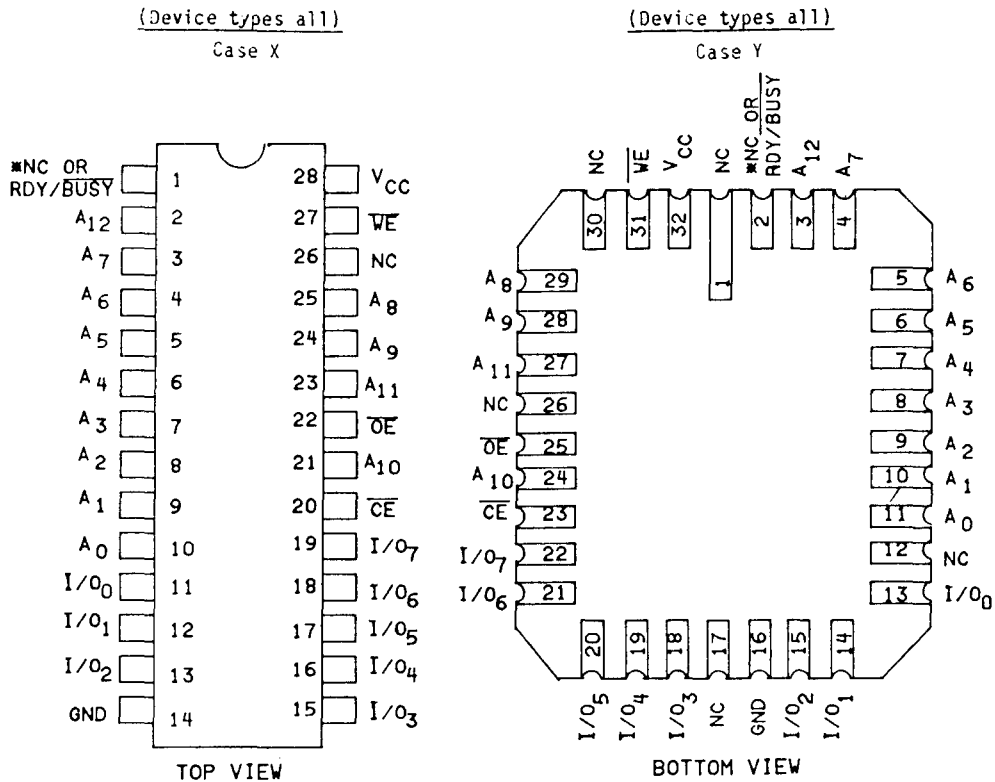
4.5.3.3 Data polling operation. During the internal programming cycle after a byte or page write operation, an attempt to read the last byte written will produce the complement of that data on I/O 7 (i.e., write data = 0xxx xxxx and read data = 1xxx xxxx). Once the programming cycle has completed, I/O 7 will reflect true data (i.e., write data = 0xxx xxxx read data = 0xxx xxxx) (applies to device types 01-06).

4.5.3.4 RDY/BUSY. While the write operation is in progress, the RDY/BUSY output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/BUSY pin to a TTL high. The RDY/BUSY pin is an open drain output and a typical 3 k Ω pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied RDY/BUSY pins (applies to device types 07-11).

4.5.4 Erasing procedure. The waveforms and timing relationships shown on figure 6 and figure 7 and the conditions specified in table I and table V shall be adhered to. Initially and after each chip erasure, all bits are in the high state (output at V_{OH}).

4.5.4.1 Byte erasure. A byte is erased by simultaneously programming an "H" state into each bit at the selected address (see 4.5.3). This can be done via a byte write cycle or a page mode write cycle (see figure 6). The page mode cycle allows for erasure of a maximum of sixteen bytes during one write cycle.

4.5.4.2 Chip erase. The device is erased by setting the $\overline{OE}$ output enable pin to 20.0 volts (see figure 7), while all other inputs are set in the normal byte erase mode (see 4.5.4.1). After chip erasure, all bits are in the "H" state (applies to device types 01-06).



Pin Names

A ₀₋₄	ADDRESSES - COLUMN (LOWER ORDER BITS)
A ₅₋₁₂	ADDRESSES - ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
RDY/BUSY	DEVICE READY/BUSY
N/C	NO CONNECT

*N/C for device types 01-06
RDY/BUSY for device types 07-11

FIGURE 1. Terminal connections.

MODE	INPUTS			I/O	PIN 1
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O ₀ - I/O ₇	RDY/BUSY (see note 1)
READ	V _{IL}	V _{IL}	V _{IH}	D _{OUT}	HI-Z
WRITE	V _{IL}	V _{IH}	V _{IL}	D _{IN}	V _{OL}
STANDBY AND	--	--	--	--	--
WRITE INHIBIT	V _{IH}	X	X	HI-Z	HI-Z
WRITE INHIBIT	X	V _{IL}	X	--	HI-Z
WRITE INHIBIT	X	X	V _{IH}	--	HI-Z
MASS ERASE	V _{IL}	V _{OE}	V _{IH}	D _{IN} = V _{IH}	N/A
CHIP CLEAR	V _{IL}	V _h	V _h	HI-Z	HI-Z
DATA POLLING (see note 2)	V _{IL}	V _{IL}	V _{IH}	D _{OUT} = -I/O ₇	N/A

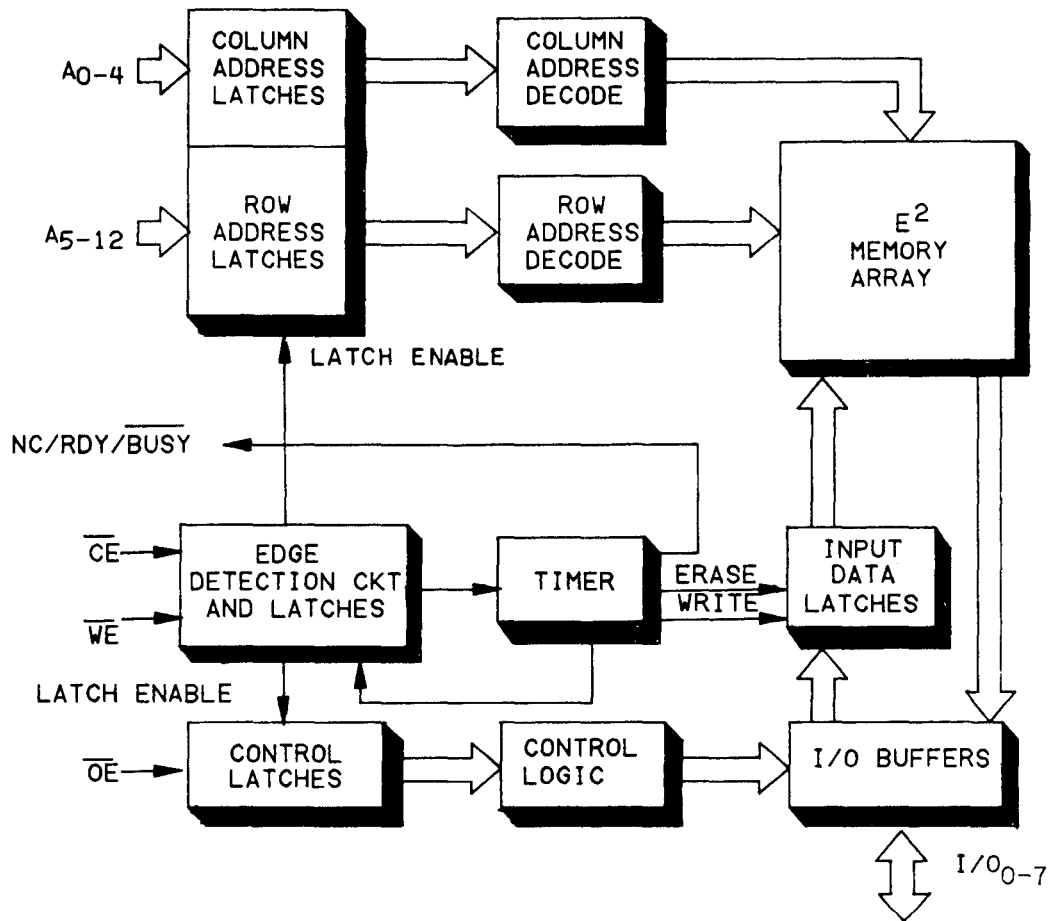
X = Don't care
HI-Z = High-impedance state

NOTES:

1. Applies to device types 07, 08, 09, 10 and 11 with the RDY/BUSY function. Pin 1 has an open drain output and requires an external 3 k Ω resistor to V_{CC}. This resistor value is dependent on the number of OR-tied RDY/BUSY pins.
2. Data polling is a technique used to decrease the byte write or page write cycle time. The device complements data bit seven during a read cycle of the last written address, while the internal write cycle is in process. Before the first data polling read cycle, a delay of t_{AVOY} (address access time) from $\overline{WE}$ high must occur. During data polling, data bits I/O₀ through I/O₆ are undefined. Five hundred microseconds (500 μ s) after I/O₇ reflects true data, a new-write cycle may be executed.
3. X = Input may be high, low, or open.

FIGURE 2. Truth table.

(Device types all)



*/ NC for device types 01-06
RDY/BUSY for device types 07-11

FIGURE 3. Functional block diagram.

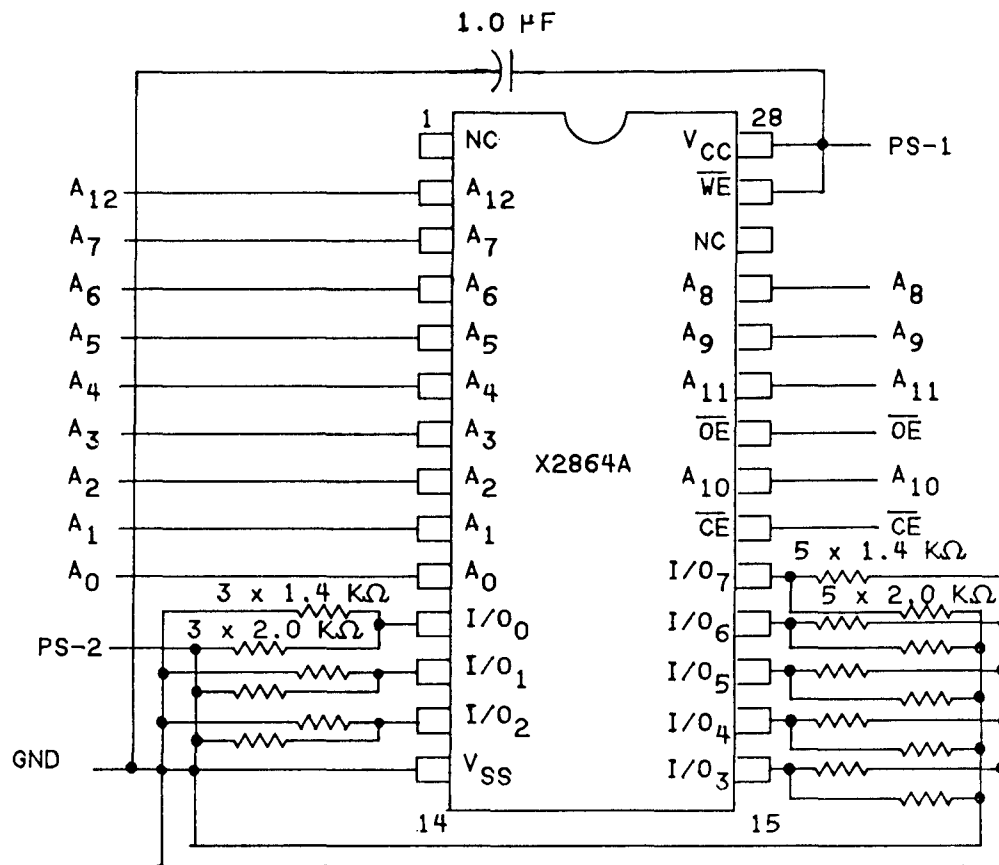
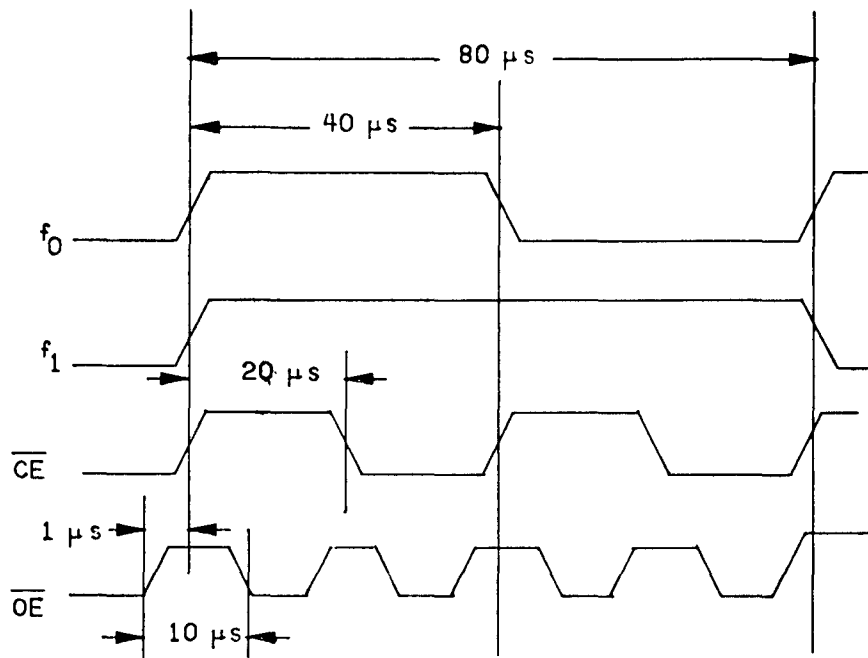


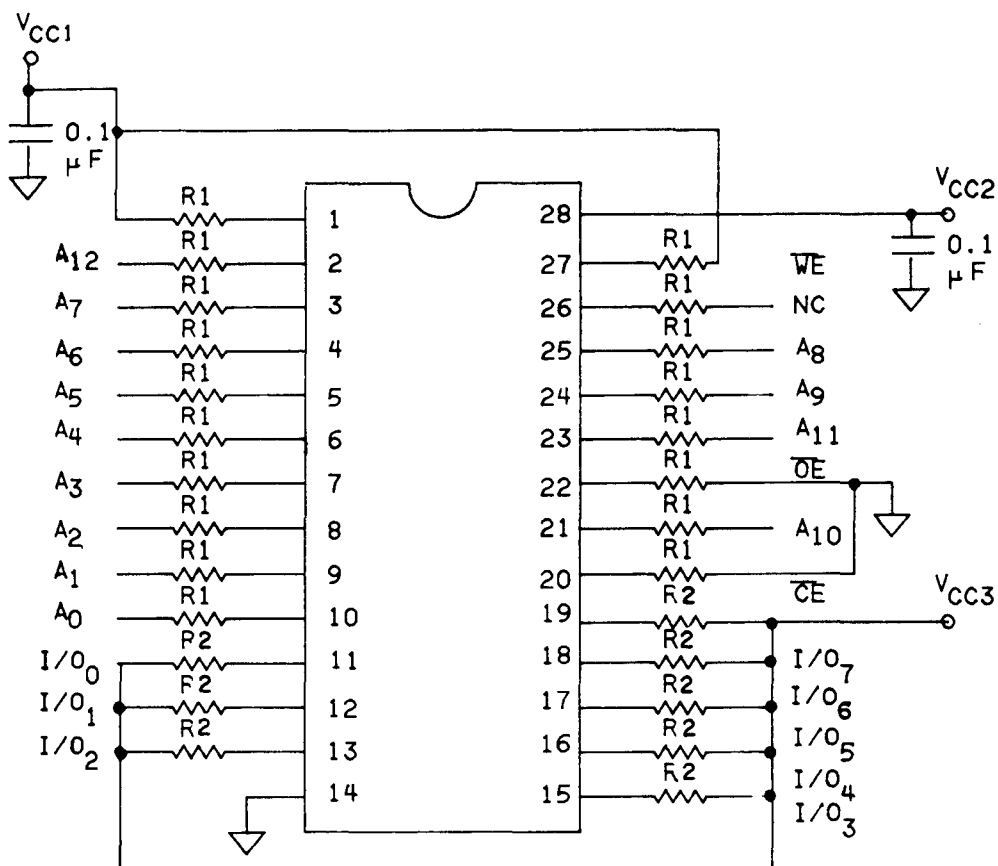
FIGURE 4. Burn-in and operating life test circuit (case X (CERDIP) device types 01-06).



NOTES:

1. $\overline{WE}$ must always be hardwired to V_{CC} (pin 28) at device as shown.
2. All resistors: 1 percent metal film, 1/4 watt.
3. I/O pullup: $2 k\Omega$.
I/O pulldown: $1.4 k\Omega$.
4. $V_{IH} = 2.0 V$ to V_{CC} , $V_{IL} = -0.1$ to $0.8 V$.
5. f_0 (A_0) = 12.5 kHz square wave.
6. f_1 (A_1) = f_0 divided by 2, f_2 (A_2) = f_1 divided by 2...
7. f_{12} (A_{12}) = f_{11} divided by 2.
 $PS-1 = 5.5 V$, $PS-2 = 5.0 V$.

FIGURE 4. Burn-in and operating life test circuit (case X (CERDIP) device types 01-06) - Continued.



NOTES:

1. All resistors labeled R1 are 3.3 k Ω , 1/4 W, 5 percent metal film, at every socket.
2. All resistors labeled R2 are 2.3 k Ω , 1/4 W, 5 percent metal film, at every socket.
3. There is a 0.1 μ F decoupling capacitor between pins 1/27 and GND at every socket.
4. There is a 0.1 μ F decoupling capacitor between VCC and GND at every socket.
5. VCC1 = VCC2 = 5.25 V, VCC3 = 2.25 V. All voltage levels are ± 0.25 V.
6. Power up sequence: VCC1, VCC2, addresses, VCC3.
7. Power down sequence: VCC3, addresses, VCC2, VCC1.
8. f_0 (A0) = 500 kHz.
9. f_1 (A1) = f_0 divided by 2, $f_2 = f_1$ divided by 2... f_{12} (A12) = f_{11} divided by 2.

FIGURE 4. Burn-in and operating life test circuit (case X (CERDIP) device types 07-11) - Continued.

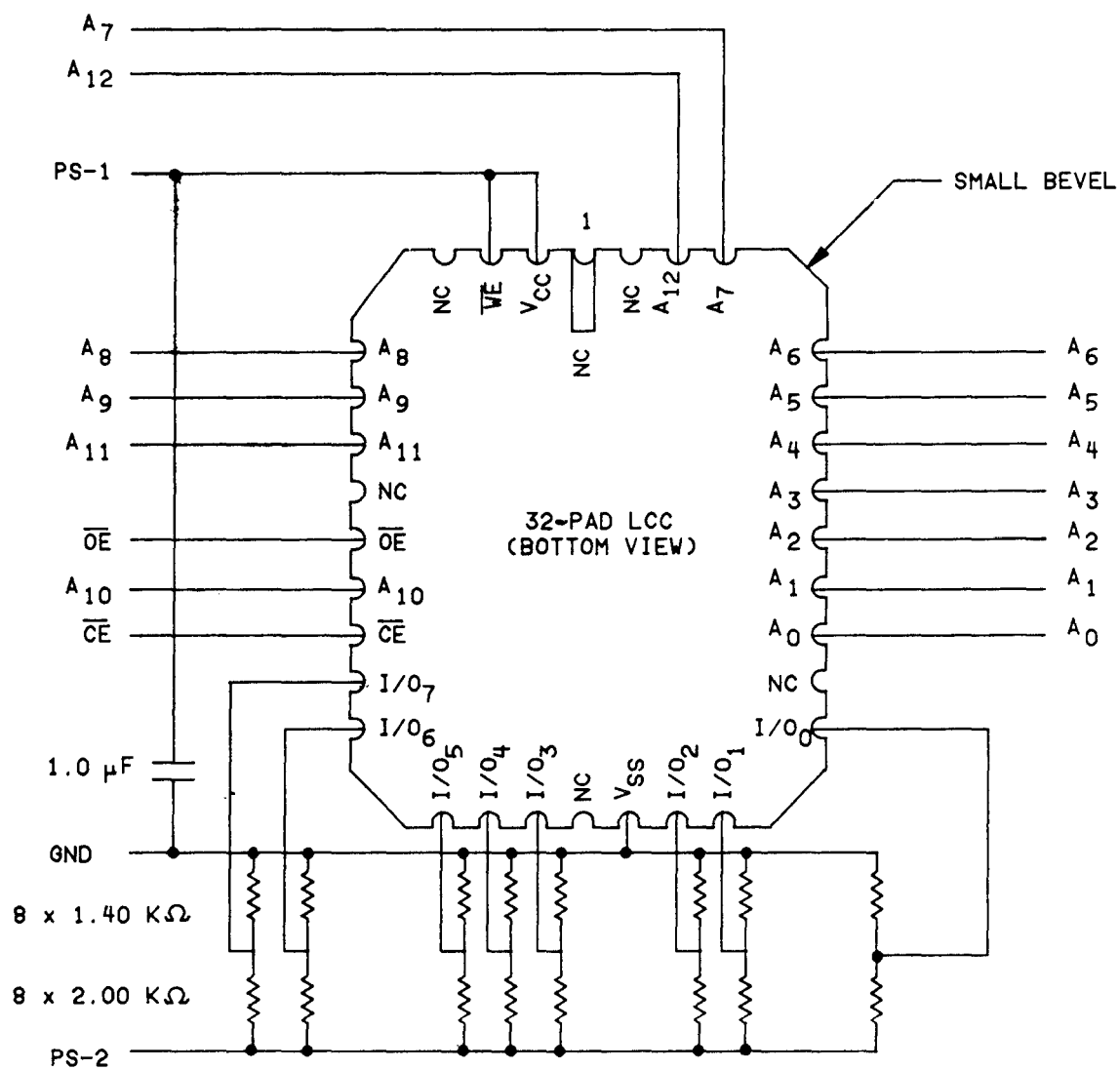
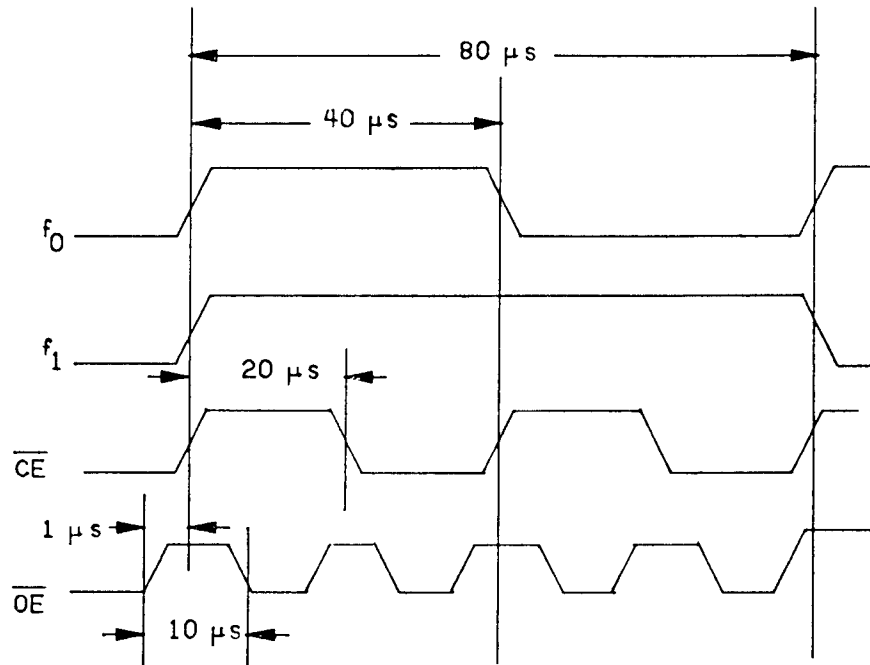


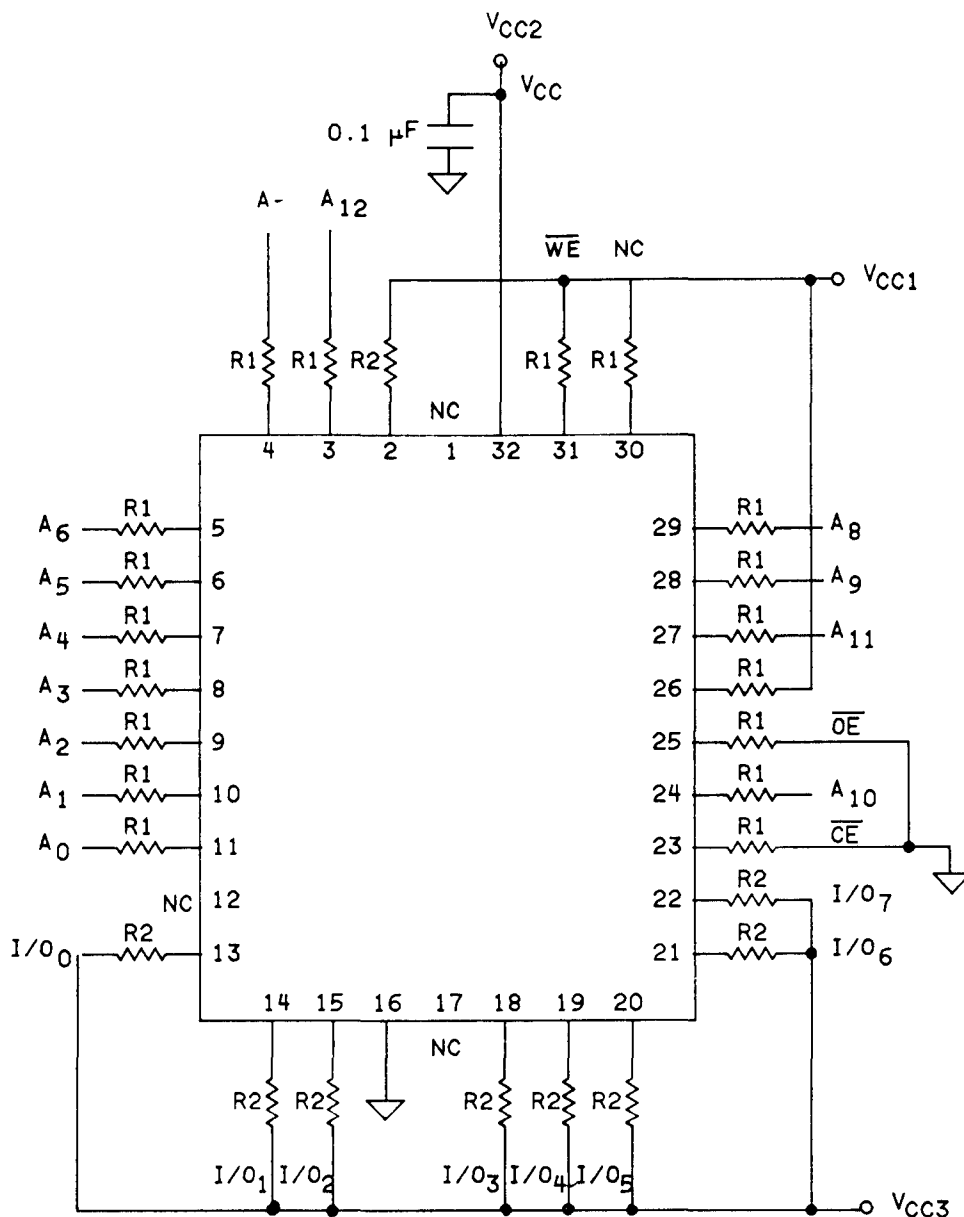
FIGURE 4. Burn-in and operating life test circuit (case Y (LCC) device types 01-06) - Continued.



NOTES:

1. WE must always be hardwired to V_{CC} (pad 31) at device as shown.
2. All resistors: 1 percent metal film, 1/4 watt.
3. I/O pullup: 2 k Ω .
I/O pulldown: 1.4 k Ω .
4. V_{IH} = 2.0 V to V_{CC} , V_{IL} = -0.1 to 0.8 V.
5. f_0 (A_0) = 12.5 kHz square wave.
6. f_1 (A_1) = f_0 divided by 2, f_2 (A_2) = f_1 divided by 2...
7. f_{12} (A_{12}) = f_{11} divided by 2.
7. PS-1 = 5.5 V, PS-2 = 5.0 V.

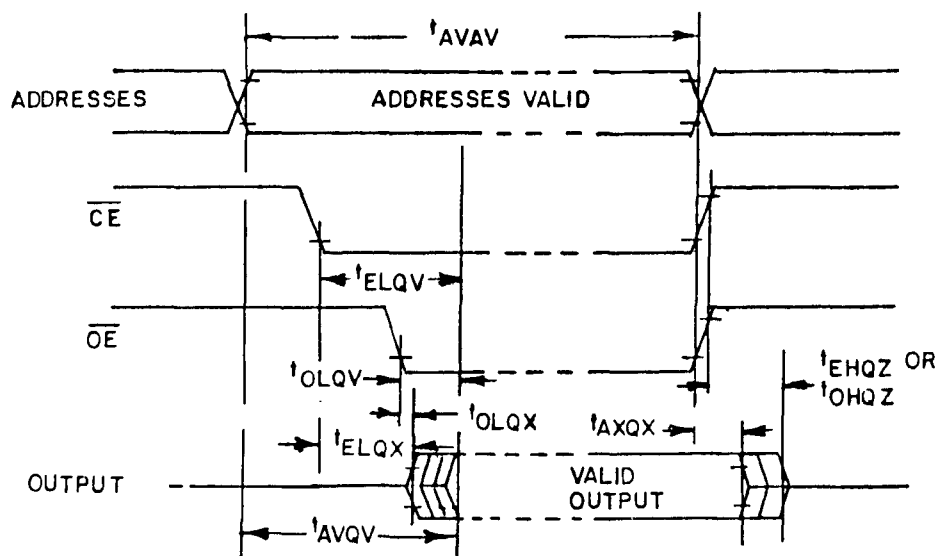
FIGURE 4. Burn-in and operating life test circuit (case Y (LCC) device types 01-06) - Continued.



NOTES:

1. All resistors labeled R1 are 3.3 k Ω , 1/4 W, 5 percent carbon film, at every socket.
2. All resistors labeled R2 are 2.2 k Ω , 1/4 W, 5 percent carbon film, at every socket.
3. There is a 0.1 μ F decoupling capacitor between VCC and GND at every socket.
4. VCC1 = VCC2 = 5.25 V, VCC3 = 2.5 V. All voltage levels are ± 0.25 V.
5. Power up sequence: VCC1, VCC2, addresses, VCC3.
6. Power down sequence: VCC3, addresses, VCC2, VCC1.
7. Resistor at pin 2 can be 200 Ω as an alternative.
8. f_0 (A₀) = 500 kHz.
9. f_1 (A₁) = f_0 divided by 2, f_2 (A₂) = f_1 divided by 2...
 f_{12} (A₁₂) = f_{11} divided by 2.

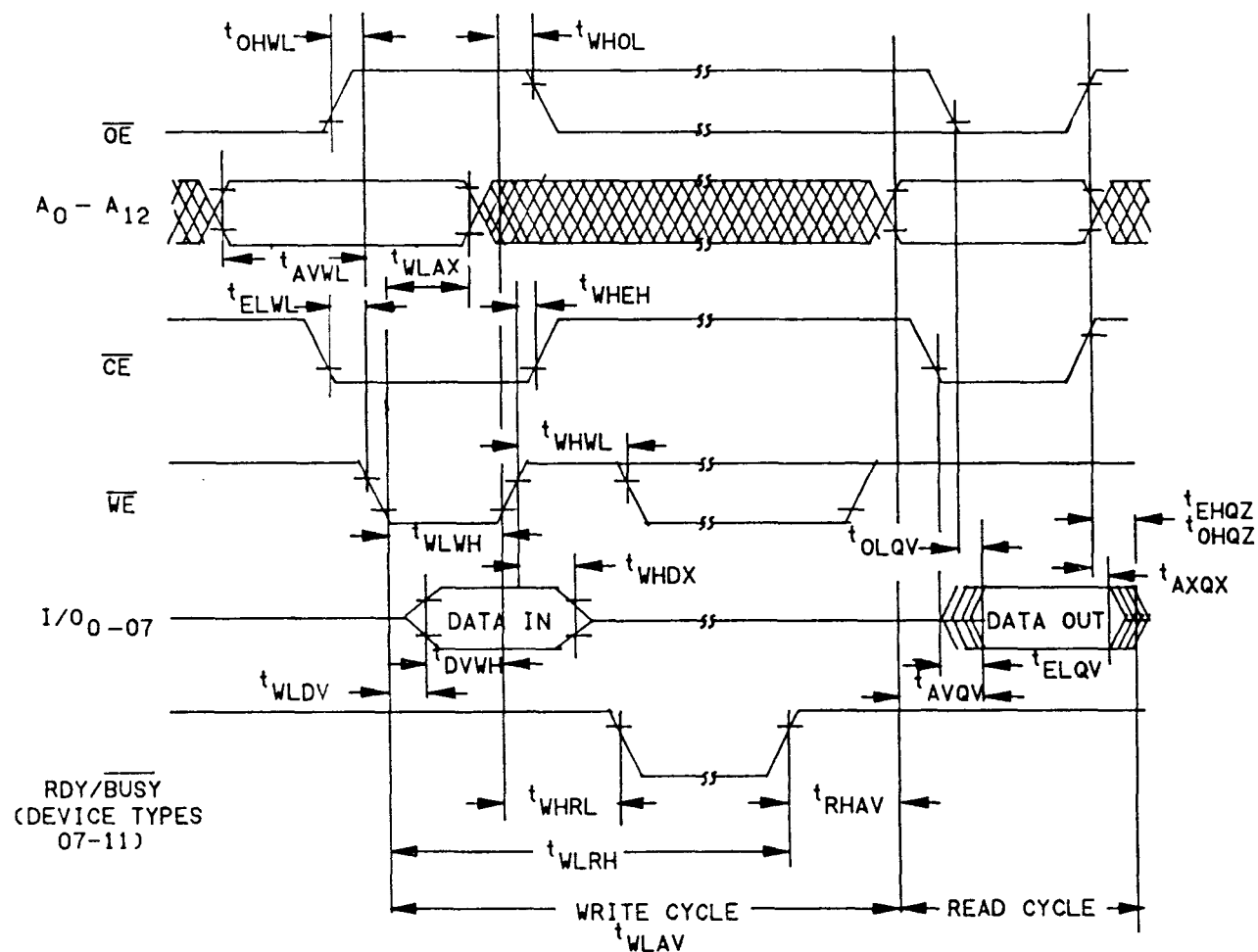
FIGURE 4. Burn-in and operating life test circuit (case Y (LCC) device types 07-11) - Continued.



NOTES:

1. V_{CC} shall be applied simultaneously or after $\overline{WE}$ and removed simultaneously or before $\overline{WE}$.
2. Output load is a TTL gate and 120 pF including jig or probe capacitance.
3. Input rise and fall time < 10 ns.
4. Input pulse levels of 0.4 V and 2.4 V.
5. Timing measurement reference levels:
Inputs 1.0 V and 2.0 V.
Outputs 0.8 V and 2.0 V.

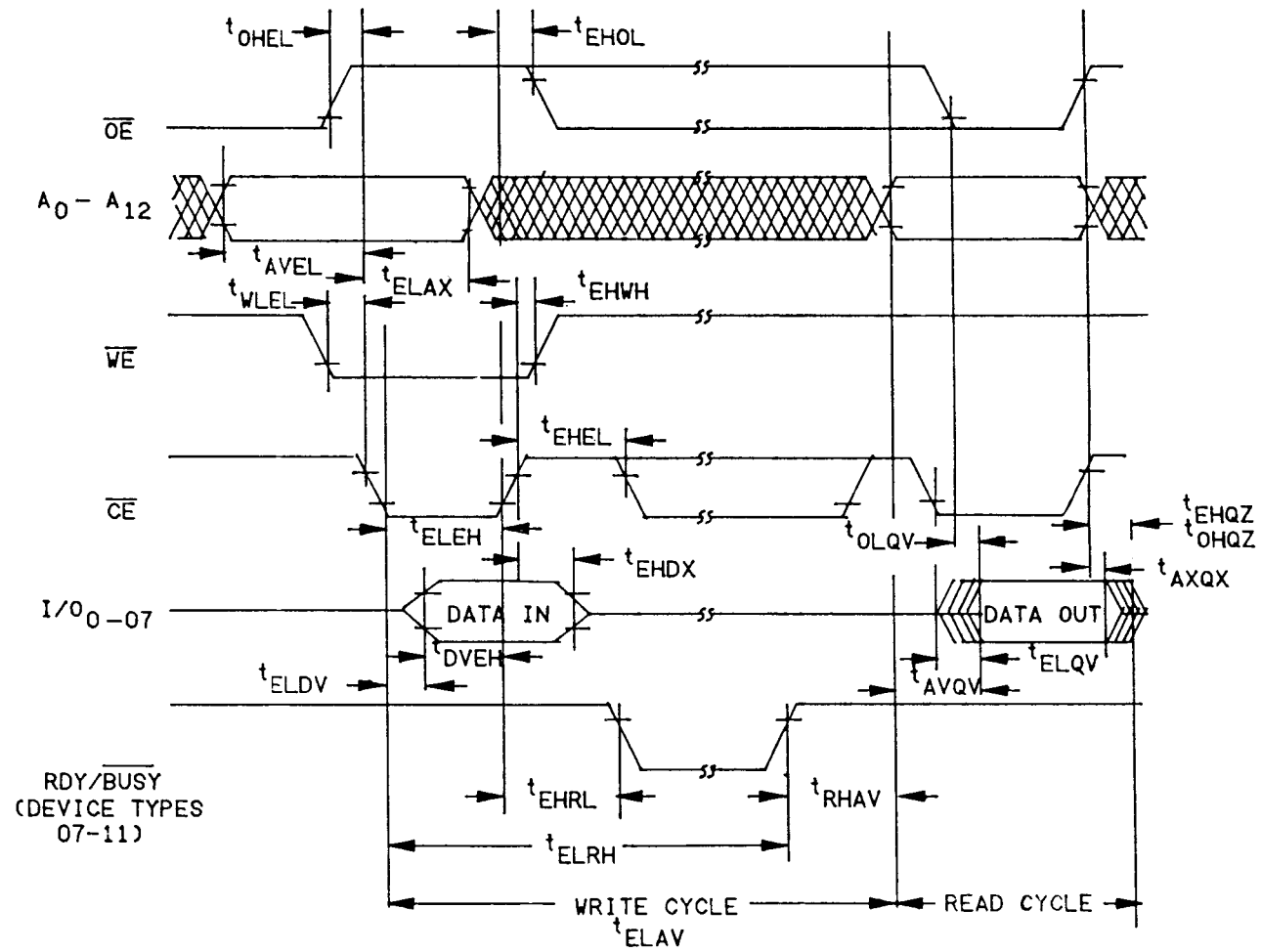
FIGURE 5. Read mode waveforms.



NOTES:

1. Input timing reference levels are 1.0 V and 2.0 V.
2. Output timing reference levels are 0.3 V and 2.0 V.
3. Input pulse rise and fall times (10 percent and 90 percent) ≤ 10 ns.
4. Input pulse levels are 0.4 V and 2.4 V.

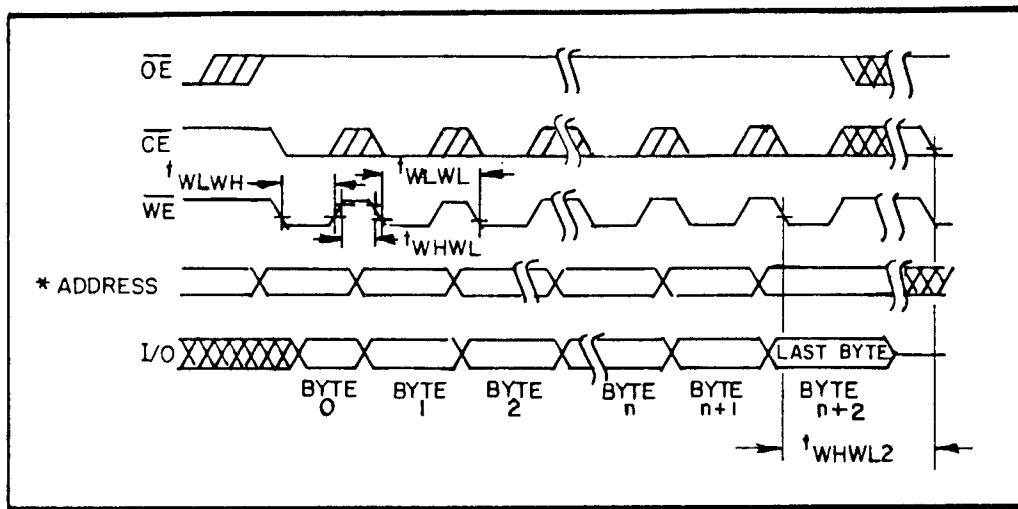
FIGURE 6. WE controlled byte write waveforms (all device types).



NOTES:

1. Input timing reference levels are 1.0 V and 2.0 V.
2. Output timing reference levels are 0.8 V and 2.0 V.
3. Input pulse rise and fall times (10 percent and 90 percent) ≤ 10 ns.
4. Input pulse levels are 0.4 V and 2.4 V.

FIGURE 6. $\overline{CE}$ controlled byte write waveforms (all device types) - Continued.



*For each successive write within the page write operation, A4-A12 should be the same or writes to an unknown address could occur.

FIGURE 6. Page mode write cycle waveforms (device types 01-06) - Continued.

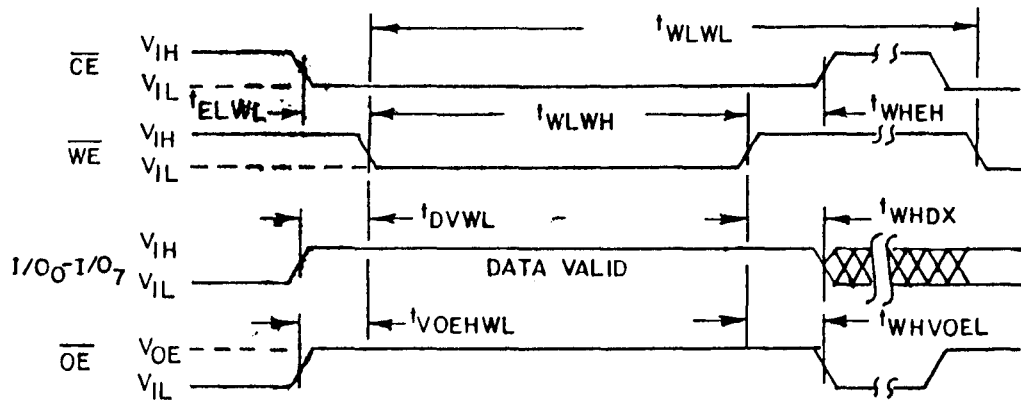
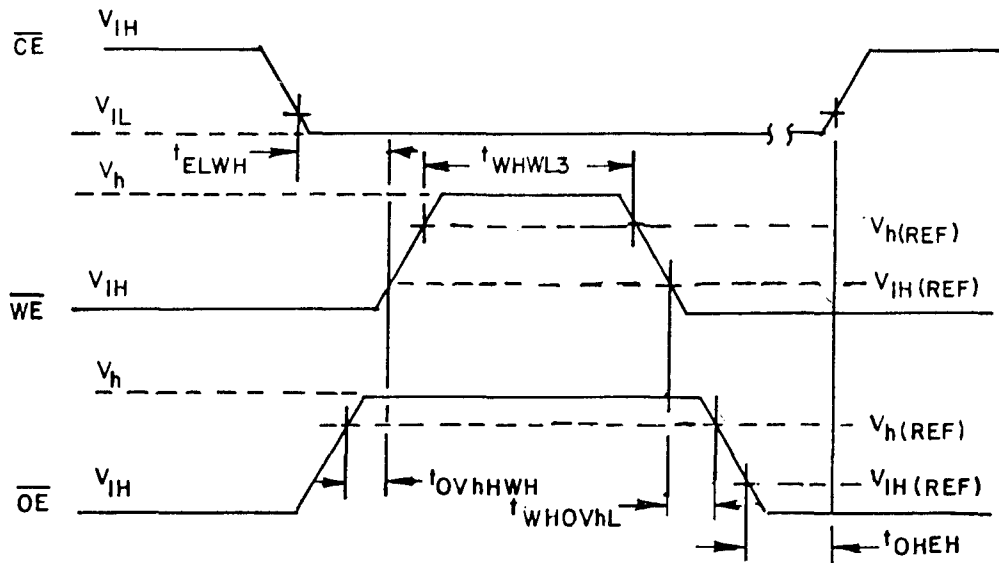


FIGURE 7. Chip erase mode waveforms (device types 01-06).

FIGURE 7. Chip erase mode waveforms (device types 07-11) - Continued.

Column address (see notes)

	0	1	2	3	4	5	6	.	.	.	25	26	27	28	29	30	31
0	AA	AA	AA	AA	AA	AA	AA	.	.	.	AA	AA	AA	AA	AA	AA	AA
1	55	55	55	55	55	55	55	.	.	.	55	55	55	55	55	55	55
2	AA	AA	AA	AA	AA	AA	AA	.	.	.	AA	AA	AA	AA	AA	AA	AA
3	55	55	55	55	55	55	55	.	.	.	55	55	55	55	55	55	55
R .								.	.	.							
O .								.	.	.							
W .								.	.	.							
124	AA	AA	AA	AA	AA	AA	AA	.	.	.	AA	AA	AA	AA	AA	AA	AA
A 125	55	55	55	55	55	55	55	.	.	.	55	55	55	55	55	55	55
D 126	AA	AA	AA	AA	AA	AA	AA	.	.	.	AA	AA	AA	AA	AA	AA	AA
D 127	55	55	55	55	55	55	55	.	.	.	55	55	55	55	55	55	55
R .								.	.	.							
E .								.	.	.							
S .								.	.	.							
S 252	AA	AA	AA	AA	AA	AA	AA	.	.	.	AA	AA	AA	AA	AA	AA	AA
253	55	55	55	55	55	55	55	.	.	.	55	55	55	55	55	55	55
See note 1 254	AA	AA	AA	AA	AA	AA	AA	.	.	.	AA	AA	AA	AA	AA	AA	AA
See note 2 255	55	55	55	55	55	55	55	.	.	.	55	55	55	55	55	55	55

NOTES:

1. All address numbers shown in decimal.
2. Each column/row address location corresponds to 1 byte.
3. Manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern.
4. All data numbers shown in hexadecimal.
AA = 10101010 55 = 01010101

FIGURE 8. Data pattern.

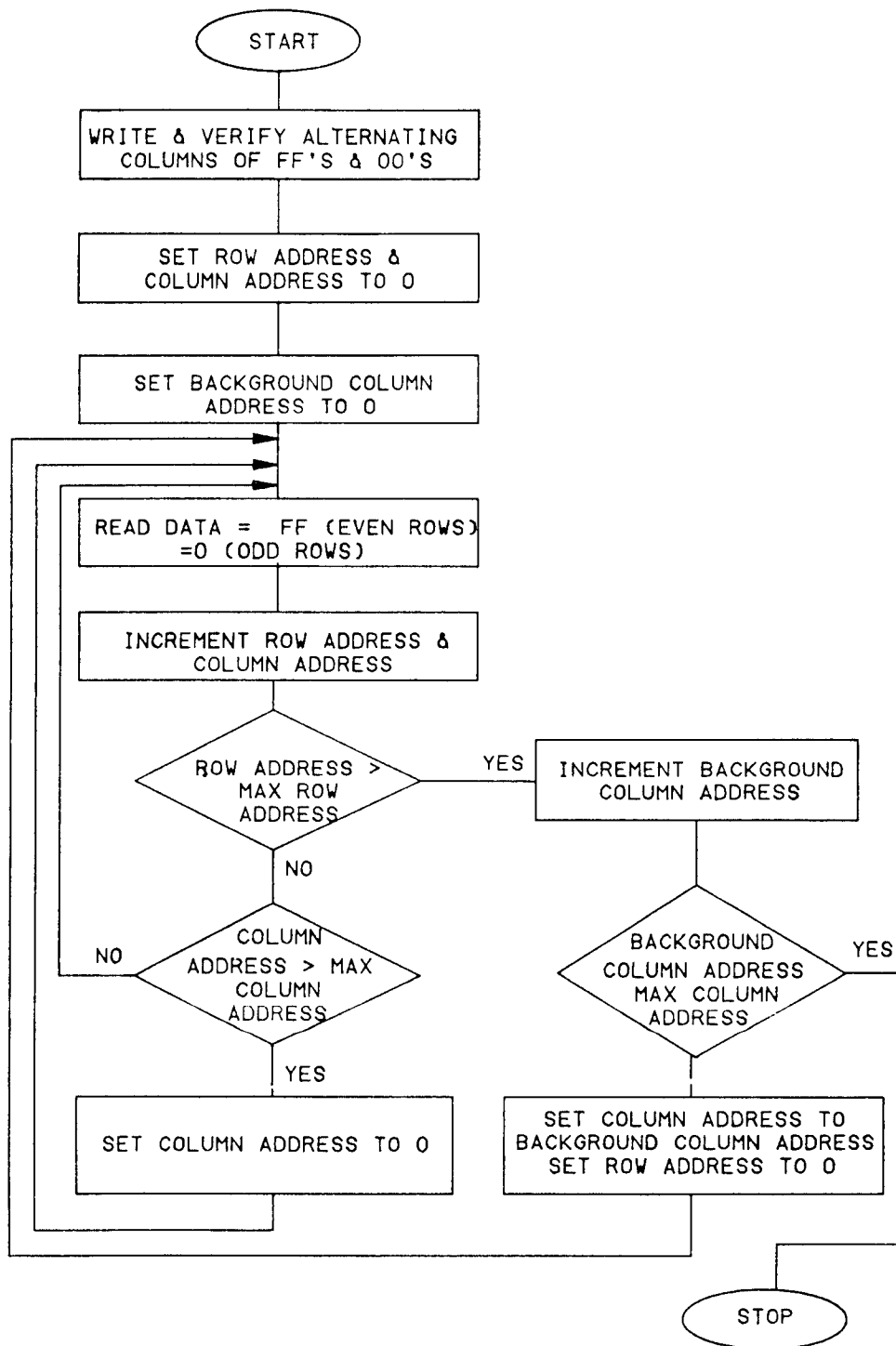


FIGURE 9. Addressing pattern 1 diagonal read.

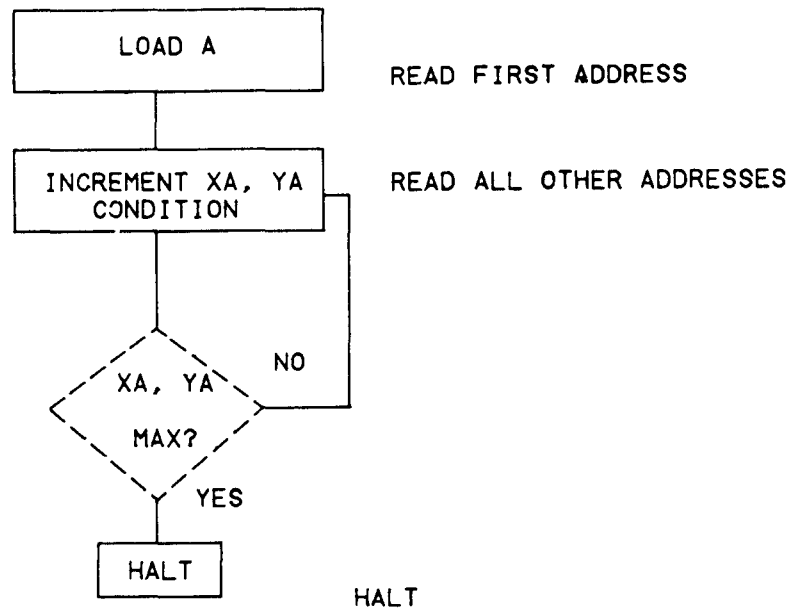


FIGURE 9. Addressing pattern 2 address increment.

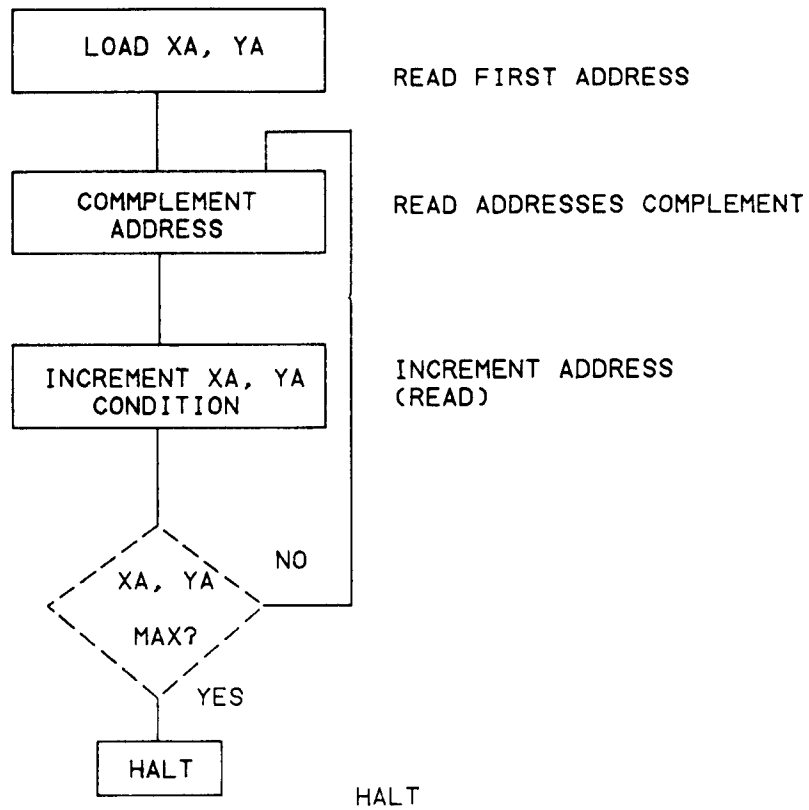


FIGURE 9. Addressing pattern 3 address/address complement.

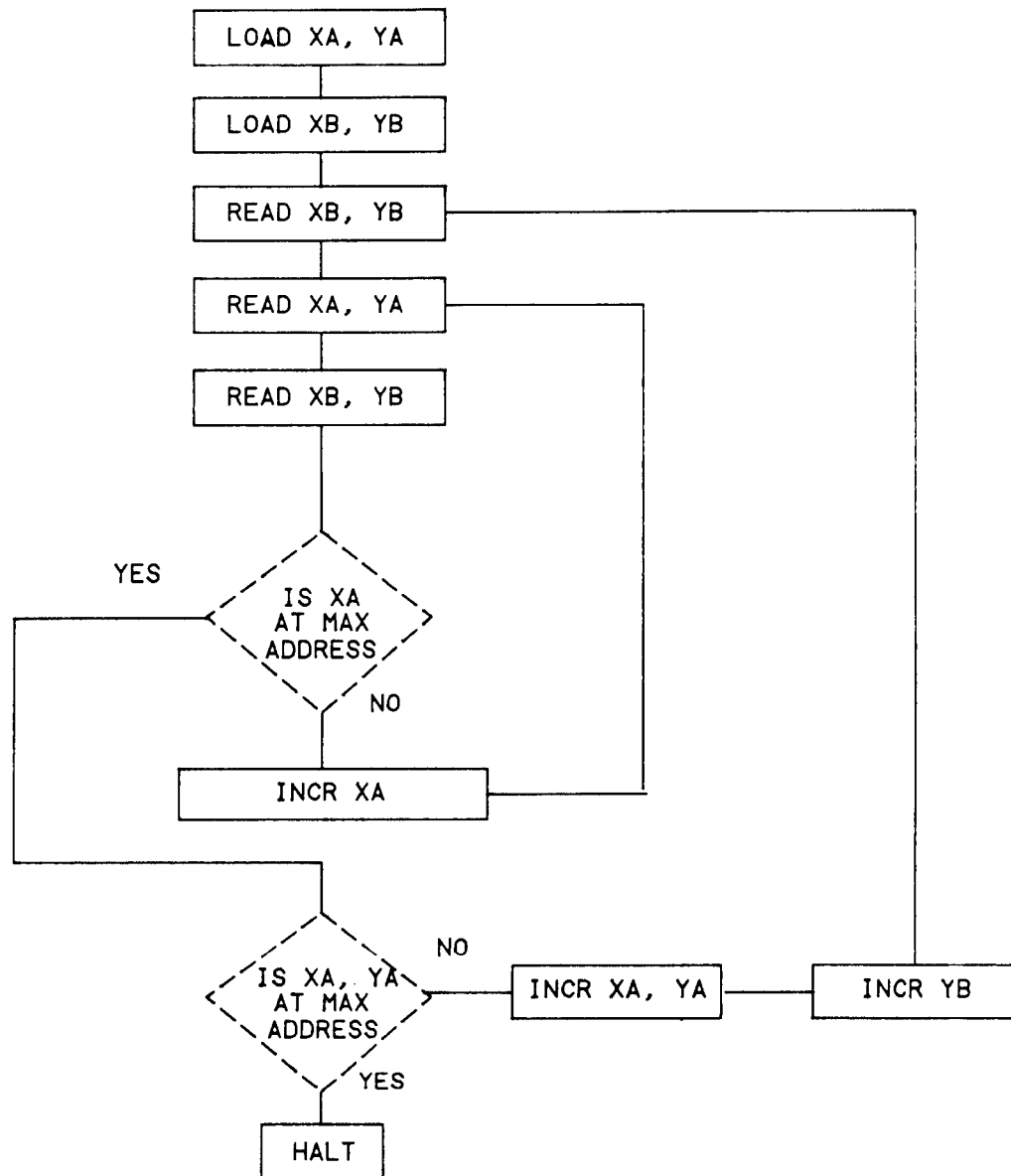
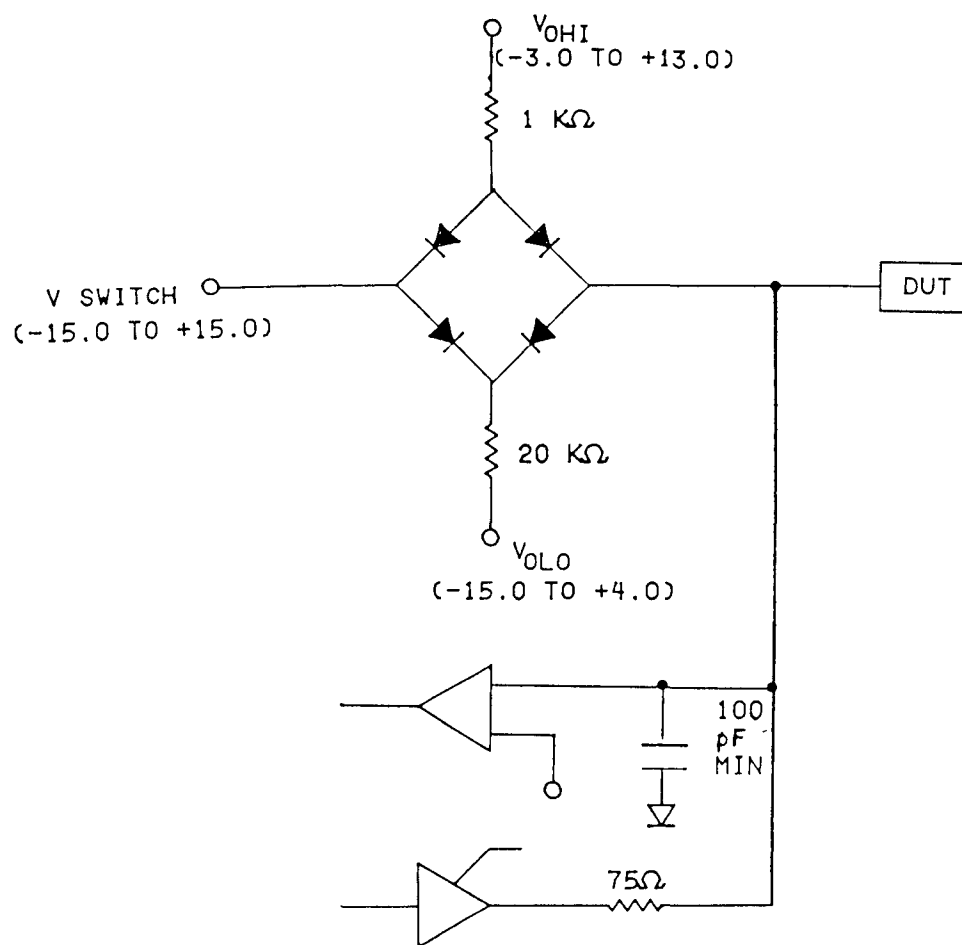


FIGURE 9. Addressing pattern 4 column galpat.



NOTE: V_{OHI} and V_{OLO} will be adjusted to meet load conditions of table I.

FIGURE 10. Switching load circuit.

TABLE III. Group A inspections - for device types 01 through 11.

Subgroup	Symbol	MIL-STD-883 method	Case Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
			Case X		1	2	3	4	5	6	7	8	9	10		11	12	13	14	
			Test no.	N/C	R/B	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	N/C	I/00	I/01	I/02	GND	N/C
A1, 2, 3	I _{CC1}	3005	1			V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}					GND	
A1, 2, 3	I _{CC2} 01-06 07-11	3005	2			.	.	.	.	.	.	.	.	.					.	
						.	.	.	.	.	.	.	.	.					.	
	V _{OL}	3007	3			1/	1/	1/	1/	1/	1/	1/	1/	1/		2.1 mA			.	
			4			.	.	.	.	.	.	.	.	.					.	
			5			.	.	.	.	.	.	.	.	.					.	
			6			.	.	.	.	.	.	.	.	.					.	
			7			.	.	.	.	.	.	.	.	.					.	
			8			.	.	.	.	.	.	.	.	.					.	
			9			.	.	.	.	.	.	.	.	.					.	
			10			.	.	.	.	.	.	.	.	.					.	
						.	.	.	.	.	.	.	.	.					.	
						.	.	.	.	.	.	.	.	.					.	
	V _{OH}	3006	11			2/	2/	2/	2/	2/	2/	2/	2/	2/		0.4 mA			.	
			12			.	.	.	.	.	.	.	.	.					.	
			13			.	.	.	.	.	.	.	.	.					.	
			14			.	.	.	.	.	.	.	.	.					.	
			15			.	.	.	.	.	.	.	.	.					.	
			16			.	.	.	.	.	.	.	.	.					.	
			17			.	.	.	.	.	.	.	.	.					.	
			18			.	.	.	.	.	.	.	.	.					.	
	I _{IL}	3009	19			0.1 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V					.	
			20			5.5 V	0.1 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V					.	
			21			.	5.5 V	0.1 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V					.	
			22			.	.	5.5 V	0.1 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V					.	
			23			.	.	.	5.5 V	0.1 V	5.5 V	5.5 V	5.5 V	5.5 V					.	
			24			.	.	.	.	0.1 V	5.5 V	5.5 V	5.5 V	5.5 V					.	
			25			.	.	.	.	5.5 V	0.1 V	5.5 V	5.5 V	5.5 V					.	
			26			.	.	.	.	.	5.5 V	0.1 V	5.5 V	5.5 V					.	
			27			.	.	.	.	.	.	5.5 V	0.1 V	5.5 V					.	
			28			.	.	.	.	.	.	.	5.5 V	0.1 V					.	
			29			.	.	.	.	.	.	.	.	5.5 V					.	
			30			.	.	.	.	.	.	.	.	.					.	
			31			.	.	.	.	.	.	.	.	.					.	
			32			.	.	.	.	.	.	.	.	.					.	
			33			.	.	.	.	.	.	.	.	.					.	
			34			.	.	.	.	.	.	.	.	.					.	
	I _{IH}	3010	35			5.5 V	0.1 V	0.1 V	0.1 V	0.1 V	0.1 V	0.1 V	0.1 V	0.1 V					.	
			36			0.1 V	5.5 V	0.1 V	0.1 V	0.1 V	0.1 V	0.1 V	0.1 V	0.1 V					.	
			37			.	0.1 V	5.5 V	0.1 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V					.	
			38			.	.	0.1 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V					.	
			39			.	.	.	0.1 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V					.	
			40			.	.	.	.	0.1 V	5.5 V	5.5 V	5.5 V	5.5 V					.	
			41			.	.	.	.	.	0.1 V	5.5 V	5.5 V	5.5 V					.	
			42			.	.	.	.	.	.	0.1 V	5.5 V	5.5 V					.	
			43			.	.	.	.	.	.	.	0.1 V	5.5 V					.	
			44			.	.	.	.	.	.	.	.	0.1 V					.	
			45			.	.	.	.	.	.	.	.	.					.	
			46			.	.	.	.	.	.	.	.	.					.	
			47			.	.	.	.	.	.	.	.	.					.	
			48			.	.	.	.	.	.	.	.	.					.	
			49			.	.	.	.	.	.	.	.	.					.	
			50			.	.	.	.	.	.	.	.	.					.	

See footnotes at end of table.

TABLE III. Group A inspections - for device types 01 through 11 - Continued.

Case Y	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	Measured terminal	Test limits		Unit
Case X	15	16	17	18	19	20	21	22		23	24	25	26	27	28		Min	Max	
Test no.	1/03	1/04	1/05	1/06	1/07	CE	A ₁₀	OE	N/C	A ₁₁	A ₉	A ₈	N/C	WE	V _{CC}				
1						0.1 V	V _{CC}	0.1 V		V _{CC}	V _{CC}	V _{CC}		V _{CC}	5.5 V	V _{CC}		140	mA
2						2.0 V	"	"		"	"	"		"	"	"		70	"
						2.0 V	"	"		"	"	"		"	"	"		50	"
3						1/	1/	1/		1/	1/	1/		1/	4.5 V	1/00		0.4	V
4						"	"	"		"	"	"		"	"	1/01		"	"
5						"	"	"		"	"	"		"	"	1/02		"	"
6	2.1 mA	2.1 mA				"	"	"		"	"	"		"	"	1/03		"	"
7			2.1 mA			"	"	"		"	"	"		"	"	1/04		"	"
8				2.1 mA		"	"	"		"	"	"		"	"	1/05		"	"
9					2.1 mA	"	"	"		"	"	"		"	"	1/06		"	"
10						"	"	"		"	"	"		"	"	1/07		"	"
11						2/	2/	2/		2/	2/	2/		2/	"	1/00	2.4		"
12						"	"	"		"	"	"		"	"	1/01	"		"
13						"	"	"		"	"	"		"	"	1/02	"		"
14	0.4 mA	0.4 mA				"	"	"		"	"	"		"	"	1/03	"		"
15			0.4 mA			"	"	"		"	"	"		"	"	1/04	"		"
16				0.4 mA		"	"	"		"	"	"		"	"	1/05	"		"
17					0.4 mA	"	"	"		"	"	"		"	"	1/06	"		"
18						"	"	"		"	"	"		"	"	1/07	"		"
19						5.5 V	5.5 V	5.5 V		5.5 V	5.5 V	5.5 V		5.5 V	5.5 V	A ₁₂	-10	+10	μA
20						"	"	"		"	"	"		"	"	A ₇	"	"	"
21						"	"	"		"	"	"		"	"	A ₆	"	"	"
22						"	"	"		"	"	"		"	"	A ₅	"	"	"
23						"	"	"		"	"	"		"	"	A ₄	"	"	"
24						"	"	"		"	"	"		"	"	A ₃	"	"	"
25						"	"	"		"	"	"		"	"	A ₂	"	"	"
26						"	"	"		"	"	"		"	"	A ₁	"	"	"
27						"	"	"		"	"	"		"	"	A ₀	"	"	"
28						0.1 V	"	"		"	"	"		"	"	CE	"	"	"
29						5.5 V	0.1 V	"		"	"	"		"	"	A ₁₀	"	"	"
30						"	5.5 V	0.1 V		"	"	"		"	"	OE	"	"	"
31						"	"	5.5 V		0.1 V	"	"		"	"	A ₁₁	"	"	"
32						"	"	"		5.5 V	0.1 V	"		"	"	A ₉	"	"	"
33						"	"	"		"	5.5 V	0.1 V		"	"	A ₈	"	"	"
34						"	"	"		"	"	5.5 V		0.1 V	"	WE	"	"	"
35						0.1 V	0.1 V	0.1 V		0.1 V	0.1 V	0.1 V		0.1 V	"	A ₁₂	"	"	"
36						"	"	"		"	"	"		"	"	A ₇	"	"	"
37						"	"	"		"	"	"		"	"	A ₆	"	"	"
38						"	"	"		"	"	"		"	"	A ₅	"	"	"
39						"	"	"		"	"	"		"	"	A ₄	"	"	"
40						"	"	"		"	"	"		"	"	A ₃	"	"	"
41						"	"	"		"	"	"		"	"	A ₂	"	"	"
42						"	"	"		"	"	"		"	"	A ₁	"	"	"
43						"	"	"		"	"	"		"	"	A ₀	"	"	"
44						5.5 V	"	"		"	"	"		"	"	CE	"	"	"
45						0.1 V	5.5 V	"		"	"	"		"	"	A ₁₀	"	"	"
46						"	0.1 V	5.5 V		"	"	"		"	"	OE	"	"	"
47						"	"	0.1 V		5.5 V	"	"		"	"	A ₁₁	"	"	"
48						"	"	"		0.1 V	5.5 V	"		"	"	A ₉	"	"	"
49						"	"	"		"	0.1 V	5.5 V		"	"	A ₈	"	"	"
50						"	"	"		"	"	0.1 V		5.5 V	"	WE	"	"	"

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TABLE III. Group A inspections - for device types 01 through 11 - Continued.

Subgroup	Symbol	MIL-STD-883 Method	Case X1 Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
				1/C	2/B	A12	A7	A6	A5	A4	A3	A2	A1	A0	1/C	1/00	1/01	1/02	GND	N/C
A1, 2, 3	I _{RLZ}	3020	51		3/	3/	3/	3/	3/	3/	3/	3/	3/	3/		GND			GND	
			52																	
			53																	
			54																	
			55																	
			56																	
			57																	
			58																	
	I _{RIH2}	3021	59													5.5 V				
			60														5.5 V			
			61															5.5 V		
			62																	
			63																	
			64																	
			65																	
			66																	
A4, A4	I _{CI}	3012	57		4/	4/	4/	4/	4/	4/	4/	4/	4/	4/		4/	4/	4/	4/	
			58																	
A1, 2, 3	I _{DE}	01-06	69																	
			70																	
			71																	
A9, 10, 11	V _{OE}	01-06	72		5/	5/	5/	5/	5/	5/	5/	5/	5/	5/		6/	6/	6/	GND	
			73													5/	5/	5/	GND	
A7, 8	V _{TH}		74																	
			75																	
A9, 10, 11	t _{AVAV}	01	76			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	
			77			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	
	t _{ELQV}	01	78			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	
			79			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	
	t _{ELQV}	01	80			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	
			81			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	
	t _{ELQV}	01	82			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	
			83			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	
	t _{ELQV}	01	84			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	
			85			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	
	t _{ELQV}	01	86			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	
			87			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	

See footnotes at end of table.

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TABLE III. Group A inspections - for device types 01 through 11 - Continued.

Case Y	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	Measured terminal	Test limits		Unit
Case X	15	16	17	18	19	20	21	22		23	24	25	26	27	28		Min	Max	
Test no.	1/03	1/04	1/05	1/06	1/07	CE	A ₁₂	OE	V/C	A ₁₁	A ₉	A ₈	V/C	LF	V _{CC}				
51						3/	3/	3/		3/	3/	3/		3/	5.5 V	1/00	-10	+10	μA
52						"	"	"		"	"	"		"	"	1/01	"	"	"
53						"	"	"		"	"	"		"	"	1/02	"	"	"
54						"	"	"		"	"	"		"	"	1/03	"	"	"
55						"	"	"		"	"	"		"	"	1/04	"	"	"
56						"	"	"		"	"	"		"	"	1/05	"	"	"
57						"	"	"		"	"	"		"	"	1/06	"	"	"
58						"	"	"		"	"	"		"	"	1/07	"	"	"
59						"	"	"		"	"	"		"	"	1/00	"	"	"
60						"	"	"		"	"	"		"	"	1/01	"	"	"
61						"	"	"		"	"	"		"	"	1/02	"	"	"
62	5.5 V					"	"	"		"	"	"		"	"	1/03	"	"	"
63		5.5 V				"	"	"		"	"	"		"	"	1/04	"	"	"
64			5.5 V			"	"	"		"	"	"		"	"	1/05	"	"	"
65				5.5 V		"	"	"		"	"	"		"	"	1/06	"	"	"
66					5.5 V	"	"	"		"	"	"		"	"	1/07	"	"	"
67	4/	4/	4/	4/	4/	"	"	"		"	"	"		"	4/	A11 inputs		6	pF
68	8/	8/	8/	8/	8/	"	"	"		"	"	"		"	8/	A11 1/0s		10	pF
69						10.1 V		22 V						12.0 V	5.5 V	OE		10	μA
70						5.5 V		16 V						16 V	"	WE		"	"
71						5.5 V		16 V							"	OE		"	"
72	6/	6/	6/	6/	6/	5/	5/	22 V		5/	5/	5/		5/	5/	5/	18	22	V
73	6/	6/	6/	6/	6/	16 V	5/	5/		5/	16 V	5/		5/	5/	5/	14	16	V
74																8/	2.0	V _{CC} +1	"
75																8/	-0.3	0.8	"
76	6/	6/	6/	6/	6/	7/	7/	7/		7/	7/	7/		7/	7/	7/	450		ns
																	350		"
																	300		"
																	250		"
77	6/	6/	6/	6/	6/	7/	7/	7/		7/	7/	7/		7/	7/	7/		450	ns
																		350	"
																		300	"
																		250	"
78	6/	6/	6/	6/	6/	7/	7/	7/		7/	7/	7/		7/	7/	7/		450	ns
																		350	"
																		300	"
																		250	"
79	6/	6/	6/	6/	6/	7/	7/	7/		7/	7/	7/		7/	7/	7/		150	ns
																		100	ns
80	6/	6/	6/	6/	6/	7/	7/	7/		7/	7/	7/		7/	7/	7/	10		ns
81	6/	6/	6/	6/	6/	7/	7/	7/		7/	7/	7/		7/	7/	7/		100	ns
																		80	ns
																		60	ns

TABLE III. Group A inspections - for device types 01 through 11 - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
			Case X																	
			Test no.	N/C	R/B	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	N/C	I/00	I/01	I/02	GND	N/C
A9, 10, 11	t _{OLQX}		82			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	GND	
	t _{OHQZ} 01 02,03, 05,07, 04,06, 08-11		83			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	"	
	t _{AXQX} 01-06 07-11		84			7/	7/	7/	7/	7/	7/	7/	7/	7/		6/	6/	6/	"	
	t _{WLAV} 01-08, 10,11 9		85			9/	9/	9/	9/	9/	9/	9/	9/	9/		6/	6/	6/	"	
	t _{ELAV} 01-08, 10,11 9		86			9/	9/	9/	9/	9/	9/	9/	9/	9/		6/	6/	6/	"	
	t _{AVWL} t _{AVEL} t _{WLAX} 01-06 07-11		87 88 89			9/	9/	9/	9/	9/	9/	9/	9/	9/		6/	6/	6/	"	
	t _{ELAX} 01-06 07-11		90			"	"	"	"	"	"	"	"	"		"	"	"	"	
	t _{ELWL} t _{WL EL} t _{WL EH} t _{EHWH} t _{EL FH} t _{WLWH} t _{OHWL} t _{OH EL} t _{WHOL} t _{EHOL} t _{WHWL} t _{EH EL} t _{WLDY} 01-06 07-11		91 92 93 94 95 96 97 98 99 100 101 102 103			"	"	"	"	"	"	"	"	"		"	"	"	"	
	t _{DVWH} 01-06		104			"	"	"	"	"	"	"	"	"		"	"	"	"	
	t _{DVEH} 07-11		105			"	"	"	"	"	"	"	"	"		"	"	"	"	

See footnotes at end of table.

TABLE III. Group A inspections - for device types 01 through 11 - Continued.

Case Y	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	Measured terminal	Test limits		Unit
Case X	15	16	17	18	19	20	21	22		23	24	25	26	27	28		Min	Max	
Test no.	1/03	1/04	1/05	1/06	1/07	CE	A ₁₀	OE	N/C	A ₁₁	A ₉	A ₈	N/C	WE	V _{CC}				
82	6/	6/	6/	6/	6/	7/	7/	7/		7/	7/	7/		7/	7/	7/	10		ns
83	6/	6/	6/	6/	6/	7/	7/	7/		7/	7/	7/		7/	7/	7/		100 80 60	" " "
84	6/	6/	6/	6/	6/	7/	7/	7/		7/	7/	7/		7/	7/	7/	10 0		" "
85	6/	6/	6/	6/	6/	9/	9/	9/		9/	9/	9/		9/	9/	9/		10 2	ms "
86	5/	6/	6/	5/	5/	9/	9/	9/		9/	9/	9/		9/	9/	9/		10 2	" "
87	6/	6/	6/	6/	6/	9/	9/	9/		9/	9/	9/		9/	9/	9/	10 10		ns "
88	"	"	"	"	"	"	"	"		"	"	"		"	"	"			"
89	"	"	"	"	"	"	"	"		"	"	"		"	"	"	200 50		" "
90	"	"	"	"	"	"	"	"		"	"	"		"	"	"	200 50		" "
91	"	"	"	"	"	"	"	"		"	"	"		"	"	"	0		"
92	"	"	"	"	"	"	"	"		"	"	"		"	"	"	0		"
93	"	"	"	"	"	"	"	"		"	"	"		"	"	"	0		"
94	"	"	"	"	"	"	"	"		"	"	"		"	"	"	0		"
95	"	"	"	"	"	"	"	"		"	"	"		"	"	"	150		"
96	"	"	"	"	"	"	"	"		"	"	"		"	"	"	150		"
97	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		"
98	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		"
99	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		"
100	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		"
101	"	"	"	"	"	"	"	"		"	"	"		"	"	"	50		"
102	"	"	"	"	"	"	"	"		"	"	"		"	"	"	50		"
103	"	"	"	"	"	"	"	"		"	"	"		"	"	"	300 1		" μs
104	"	"	"	"	"	"	"	"		"	"	"		"	"	"	100		ns
105	"	"	"	"	"	"	"	"		"	"	"		"	"	"	50		ns

TABLE III. Group A inspections - for device types 01 through 11 - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
			Case X		1	2	3	4	5	6	7	8	9	10		11	12	13	14	
			Test no.	N/C	R/B	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	N/C	I/00	I/01	I/02	GND	N/C
49, A10, A11	tWHDX		106			9/	9/	9/	9/	9/	9/	9/	9/	9/		6/	6/	6/	GND	
	tCHDX		107			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tWHM 1 01-06		108			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tWLWL 1 01-06		109			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tWHWL 2 01-06		110			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tWHRL/ tEURL 07-11		111			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tRHAY 07-11		112			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tQVWL 01-06		113			10/	10/	10/	10/	10/	10/	10/	10/	10/		"	"	"	"	
	tWHOL 01-06		114			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tLOV 01-06		115			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tELOV 01-06		116			"	"	"	"	"	"	"	"	"		"	"	"	"	
	02, 05 03 04, 06																			
	tWHM 1 01-06		117			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tWHM 2 01-06		118			"	"	"	"	"	"	"	"	"		"	"	"	"	
	VDF 01-06		119			5/	5/	5/	5/	5/	5/	5/	5/	5/		6/	6/	6/	"	
	tELM 01-06		120			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tQVWL 01-06		121			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tWHDX 01-06		122			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tWLWL 01-06		123			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tWHEH 01-06		124			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tVOEHM 01-06		125			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tWHVDEL 01-06		126			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tWLWL 01-06		127			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tELWL 07-11		128			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tQVHWHH 07-11		129			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tWHWL 3 07-11		130			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tWLOVHL 07-11		131			"	"	"	"	"	"	"	"	"		"	"	"	"	
	tQUEH 07-11		132			"	"	"	"	"	"	"	"	"		"	"	"	"	
	VH 07-11		133			"	"	"	"	"	"	"	"	"		"	"	"	"	

See footnotes on next page.

TABLE III. Group A inspections - for device types 01 through 11 - Continued.

Case Y	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	Measured terminal	Test limits		Unit
Case X	15	16	17	18	19	20	21	22		23	24	25	26	27	28		Min	Max	
Test no.	1/03	1/04	1/05	1/06	1/07	CE	A ₁₀	OE	N/C	A ₁₁	A ₉	A ₈	N/C	WE	V _{CC}				
106	6/	6/	6/	6/	6/	9/	9/	9/		9/	9/	9/		9/	9/	9/	20		ns
107	"	"	"	"	"	"	"	"		"	"	"		"	"	"	20		ns
108	"	"	"	"	"	"	"	"		"	"	"		"	"	"	50		ns
109	"	"	"	"	"	"	"	"		"	"	"		"	"	"	3	20	μs
110	"	"	"	"	"	"	"	"		"	"	"		"	"	"		10	ns
111	"	"	"	"	"	"	"	"		"	"	"		"	"	"		200	ns
112	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		μs
113	"	"	"	"	"	10/	10/	10/		10/	10/	10/		10/	10/	10/	500		μs
114	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		ns
115	"	"	"	"	"	"	"	"		"	"	"		"	"	"		150	ns
116	"	"	"	"	"	"	"	"		"	"	"		"	"	"		450	ns
																		350	ns
																		300	ns
117	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		ns
118	"	"	"	"	"	"	"	"		"	"	"		"	"	"		10	ms
119	6/	6/	6/	6/	6/	5/	5/	5/		5/	5/	5/		5/	5/	5/	18	22	V
120	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		ns
121	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		"
122	"	"	"	"	"	"	"	"		"	"	"		"	"	"	50		"
123	"	"	"	"	"	"	"	"		"	"	"		"	"	"	150		"
124	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		"
125	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		"
126	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		"
127	"	"	"	"	"	"	"	"		"	"	"		"	"	"		10	ms
128	"	"	"	"	"	"	"	"		"	"	"		"	"	"	1		μs
129	"	"	"	"	"	"	"	"		"	"	"		"	"	"	1		μs
130	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		ms
131	"	"	"	"	"	"	"	"		"	"	"		"	"	"	1		μs
132	"	"	"	"	"	"	"	"		"	"	"		"	"	"	10		μs
133	"	"	"	"	"	"	"	"		"	"	"		"	"	"	14	16	V

- 1/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels are $V_{IL} = 0.8 \text{ V}$ and $V_{IH} = 2.0 \text{ V}$.
- 2/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels are $V_{IL} = 0.8 \text{ V}$ and $V_{IH} = 2.0 \text{ V}$.
- 3/ Terminal conditions for the output leakage current test shall be as follows:
 - a. $V_{IH} = 2.0 \text{ V}$; $V_{IL} = 0.8 \text{ V}$.
 - b. For I_{OL7} : Select an appropriate address to acquire a logic "1" on the designated output. Apply V_{IH} to $\overline{CE}$. Measure the leakage current while applying the specified voltage.
 - c. For I_{OH7} : Select an appropriate address to acquire a logic "0" on the designated output. Apply V_{IH} to $\overline{CE}$. Measure the leakage current while applying the specified voltage.
- 4/ Input-output capacitance shall be measured between the designated terminal and the GND pin under the following conditions: $V_I = 0 \text{ V}$, $f = 1 \text{ MHz}$, oscillator voltage = 50 mV rms maximum. Unused pins are open.
- 5/ These tests in subgroups 9, 10, and 11 are the chip erase cycle limits. These parameters shall be verified during functional testing, subgroups 7 and 8, by application of the timing limits and signal level in table I. Input-output conditions appear in table IV. Timing diagrams appear on figure 7. Subgroups 7, 8, 9, 10, and 11 shall be performed with $V_{CC} = 4.5 \text{ V}$ and $V_{CC} = 5.5 \text{ V}$.
- 6/ The output are loaded in accordance with figure 10 (or equivalent).
- 7/ For these test in subgroups 9, 10, and 11, the addressing pattern test shown on figure 9 (pattern 1) shall be used for device types 01-06. For device types 07-11 the following addressing pattern-parameter combinations shall be used: t_{AVQV} (pattern 3), t_{ELQV} (pattern 4), t_{OLQV} , t_{EHQZ} , t_{OHQZ} (pattern 2) (see figure 9 as applicable). Input-output conditions appear in table IV. Timing diagrams appear on figure 5. Subgroups 9, 10, and 11 shall be performed with $V_{CC} = 4.5 \text{ V}$ and $V_{CC} = 5.5 \text{ V}$.
- 8/ A functional test shall verify the dc input and output levels and applicable patterns as appropriate. All address locations shall be tested. Terminal conditions are as follows:
 - a. Inputs: $H = 2.0 \text{ V}$; $L = 0.8 \text{ V}$.
 - b. Outputs: $H = 2.4 \text{ V}$ minimum and $L = 0.4 \text{ V}$ maximum. When using single level comparators, 1.5 V reference may be used for functional tests.
 - c. The functional tests shall be performed with $V_{CC} = 4.5 \text{ V}$ and $V_{CC} = 5.5 \text{ V}$.
- 9/ These tests in subgroups 9, 10, and 11 are the byte write cycle limits. These parameters shall be verified during functional testing, subgroups 7 and 8, by application of the timing limits in table I. Input-output conditions appear in table IV. Timing diagrams appear on figure 6. Subgroups 7, 8, 9, 10, and 11 shall be performed with $V_{CC} = 4.5 \text{ V}$ and $V_{CC} = 5.5 \text{ V}$. $\overline{WE}$ and $\overline{CE}$ both must be active to initiate a write cycle; therefore, the sequence of $\overline{WE}$ or $\overline{CE}$ (e.g., for $\overline{WE}$ or $\overline{CE}$ controlled write) is verified interchangeable without duplicate testing.
- 10/ These tests in subgroups 9, 10, and 11 are the page mode write cycle limits. These parameters shall be verified during the functional testing, subgroups 7 and 8 by applications of the timing limits in table I. Input-output conditions appear in table IV. Timing diagrams appear on figure 6. Subgroups 7, 8, 9, 10, and 11 shall performed with $V_{CC} = 4.5 \text{ V}$ and $V_{CC} = 5.5 \text{ V}$.

TABLE IV. Input-output pulse levels for table III, subgroups 7, 8, 9, 10, and 11. 1/ 2/ 3/

Symbol	Terminals	A	B	Device type	Unit
V _{CC}	V _{CC}	4.5	5.5	A11	V
V _{IH}	Logic inputs, address and control pins	2.4	2.4	A11	V
V _{IL}	Logic inputs, address and control pins	0.4	0.4	A11	V
V _{OH}	Logic output, compare level 4/	2.0	2.0	A11	V
V _{OL}	Logic output, compare level 4/	0.8	0.8	A11	V
t _{AVQV}	Address	450.0 350.0 300.0 250.0 250.0	450.0 350.0 300.0 250.0 250.0	01 02,05,07 03 04,06,08,09 10,11	ns ns ns ns ns
t _{ELQV}	Chip enable	450.0 350.0 300.0 250.0 250.0	450.0 350.0 300.0 250.0 250.0	01 02,05,07 03 04,06,08,09 10,11	ns ns ns ns ns
t _{OLQV}	Output enable	150.0 100.0	150.0 100.0	01-06 07-11	ns ns
t _{AXQX}	I/00-I/07	10.0 0.0	10.0 0.0	01-06 07-11	ns ns

1/ Timing waveforms for subgroups 9, 10, and 11 are shown on figure 5.

2/ Timing waveforms for subgroups 7 and 8 (high and low) are shown on figure 6.

3/ The data pattern on figure 8 (its complement or equivalent) shall be used.

4/ When using a single level comparator, 1.5 V reference may be used for functional tests.

TABLE V. High voltage chip erasure conditions.

Test	Symbol	Conditions $V_{CC} = +5 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V dc}$ $-55^{\circ}\text{C} < T_C < +125^{\circ}\text{C}$ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Output enable voltage	V_{OE}	See figure 7	01-06	18	22	V
CE to WE setup time	t_{ELWL}		01-06	10		ns
Data to WE setup time	t_{DVWL}		01-06	10		ns
Data hold after WE high	t_{WHDX}		01-06	50		ns
Write pulse width	t_{WLWH}		01-06	150		ns
CE to WE hold time	t_{WHEH}		01-06	50		ns
V_{OE} to WE setup time	t_{VOEHWL}		01-06	10		ns
V_{OE} hold time	t_{WHVOEL}		01-06	10		ns
Write cycle time	t_{WLWL}		01-06		10	ms
CE setup time	t_{ELWH}	See figure 7	07-11	1		μs
Output setup time	t_{OVHWH}		07-11	1		μs
WE pulse width	t_{WHWL3}		07-11	10		ms
OE hold time	t_{WHOVHL}		07-11	1		μs
Erase recovery	t_{OHEH}		07-11	10		μs
OE and WE high voltage	V_h		07-11	14	16	V

4.5.4.3 Chip erase. The device is erased by setting the $\overline{OE}$ pin and $\overline{WE}$ pin to V_h (see figure 7), while all the I/O pins are in high impedance. After chip erasure, all bits are in the "H" state (applies to device types 07-11).

4.5.5 Read mode operation. The device is in the read mode whenever the $\overline{CE}$ and $\overline{OE}$ pins are at V_{IL} and the $\overline{WE}$ pin is at V_{IH} . The waveforms and timing relationships shown on figure 5 and the test conditions and limits specified in table I shall be applied (applies to all devices types).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. The devices covered by this specification require electrostatic protection.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.3 Ordering data. The contract or purchase order should specify the following.

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.
- h. Requirements for "JAN" marking.

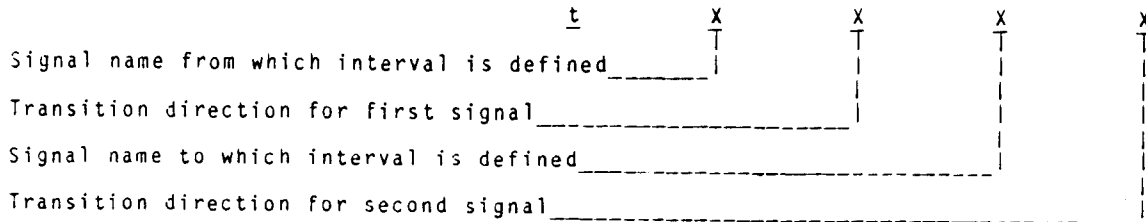
6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331 (including terms and symbols for device terminals) and as follows.

V_{SS}	Common or reference voltage mode.
V_{CC}	Supply voltage.
V_{OE}	Output enable voltage during chip erase (device types 01-06).
V_h	Output enable and write enable voltage during chip erase (device types 07-11).
A_0-A_{12}	Address inputs used to address 1 of 2048/8 bit locations in static storage array.

$\overline{CE}$	Chip enable used with the output enable ($\overline{OE}$) signal to control the state of the 8 data I/O signals.
$\overline{OE}$	Output enable used to control the I/O terminals.
DQ0-DQ7	Data I/O, 8-bit wide data bus.
$\overline{WE}$	Write enable input used to select a write mode.
I_{CC}	Supply current (standby and active).
I_{OE}	Output enable high voltage current.
I_{IH}, I_{IL}	Input leakage currents.
I_{OHZ}, I_{OLZ}	High impedance output leakage current.
V_{IL}	Logical low input voltage.
V_{IH}	Logical high input voltage.
V_{OL}	Logical low output voltage.
V_{OH}	Logical high output voltage.
C_I	Input capacitance.
C_O	Output capacitance.
t_{AVAV}	Cycle time from one read to next read.
t_{ELQV}	Chip enable access time.
t_{AVQV}	Address access time.
t_{OLQV}	Output enable access time.
t_{ELQX}	Chip enable to output in low Z.
t_{EHQZ}	Chip enable to output in high Z.
t_{OLQX}	Output enable to output in low Z.
t_{OHQZ}	Output enable to output in high Z.
t_{AXQX}	Output hold from address change.
t_{WLAV}	Cycle time during $\overline{WE}$ write operation.
t_{ELAV}	Cycle time during $\overline{CE}$ write operation.
t_{AVWL}	Address to $\overline{WE}$ setup time.
t_{AVEL}	Address to $\overline{CE}$ setup time.
t_{WLAX}	Address hold time after $\overline{WE}$ low.
t_{ELAX}	Address hold time after $\overline{CE}$ low.
t_{ELWL}	Chip enable to $\overline{WE}$ setup time.
t_{WLEL}	Write enable to $\overline{CE}$ setup time.
t_{WHEH}	Chip enable hold time after $\overline{WE}$ high.
t_{EHHH}	Write enable hold time after $\overline{CE}$ high.

t _{ELEH}	Chip enable pulse width during write.
t _{OHHL}	Output enable to $\overline{WE}$ setup time.
t _{OHCL}	Output enable to $\overline{CE}$ setup time.
t _{WHOL}	Output enable hold time after $\overline{WE}$ high.
t _{EHOL}	Output enable hold time after $\overline{CE}$ high.
t _{WLWH}	Write enable pulse width during write.
t _{WHWL}	Minimum write enable high time.
t _{EHCL}	Minimum chip enable high time after write.
t _{OVWH}	Data in setup time before $\overline{WE}$ high.
t _{OVEH}	Data in setup time before $\overline{CE}$ high.
t _{WHDX}	Data hold time after $\overline{WE}$ high.
t _{EHDX}	Data hold time after $\overline{CE}$ high.
t _{ALDV}	Maximum time to valid data after $\overline{WE}$ low.
t _{ELDV}	Maximum time to valid data after $\overline{CE}$ low.
t _{VOEHWL}	V _{OE} setup time to $\overline{WE}$ low (chip erase).
t _{WHVDEL}	V _{OE} hold time after $\overline{WE}$ high (chip erase).
t _{WLWL}	Cycle time during chip erase operation.
t _{WHWL1}	Minimum write enable high time during page write.
t _{WHWL2}	Write cycle time during page mode.
t _{OHWL1}	Output enable hold time during page mode.
t _{WHRL}	Time to device busy.
t _{RHAV}	Delay from ready to next write.
t _{QVWL}	Data valid to next write.
t _{OVWL}	Data to $\overline{WE}$ setup time (chip erase).
t _{ELWH}	$\overline{CE}$ setup time (chip erase).
t _{OVnHWH}	Output setup time (chip erase).
t _{WHWL3}	$\overline{WE}$ pulse width (chip erase).
t _{WLDVnL}	$\overline{OE}$ pulse time (chip erase). Erase recovery (chip erase).

6.4.1 Timing parameter abbreviations. All timing abbreviations use lower case character with upper case character subscripts. The initial character is always t and is followed by four descriptors. These characters specify two signal points arranged in "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. (Note there are exceptions for undefined signals.)



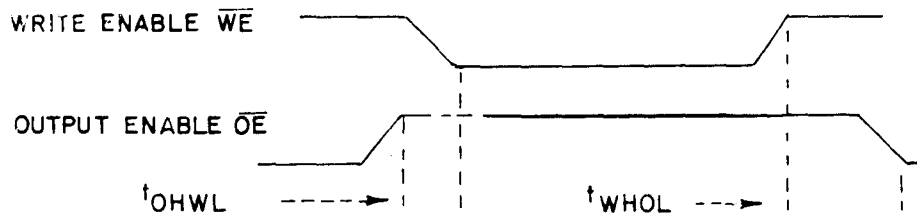
a. Signal definitions:

A = Address	D = Data in	Q = Data out
W = Write enable	E = Chip enable	O = Output enable
P = VCC	R = Ready/busy	

b. Transition definitions.

H = Transition to high	L = Transition to low
V = Transition to valid	X = Transition to invalid
Z = Transition to high impedance	

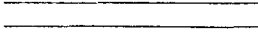
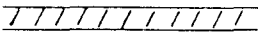
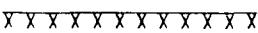
Example:



The example shows OE to WE setup time defined as t_{OHWL} and OE hold time after WE high defined as t_{WHOL} .

c. Timing limits: The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, response from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

d. Waveforms:

Waveforms symbol	Input	Output
	Must be valid	Will be valid
	Change from low to high	Will change from low to high
	Change from high to low	Will change from high to low
	Do not care any change permitted	Changing state unknown
	Not applicable	Change to high impedance

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer length and lead forming shall not affect the part number.

6.6 Handling. MOS devices shall be handled with certain precautions to avoid damage due to accumulation of static charge. Input protective devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended.

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment, tools, and operator.
- c. Handling of devices by the leads should be avoided.
- d. Devices should be stored in conductive foam or carriers.
- e. The use of plastic, rubber or silk in MOS area should be avoided.
- f. Relative humidity should be maintained above 50 percent, if practical.

6.7 Testing. Testing by interference is the validation of the performance of a parameter by measurement of the correct performance of a dependent parameter or function.

6.8 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>	<u>Symbol/ CAGE number</u>
01	X2864A-45/XICOR Inc.	CEUD/60395
02	X2864A-35/XICOR Inc.	---
03	X2864A-30/XICOR Inc.	---
04	X2864A-25/XICOR Inc.	---
05	X2864A-35/XICOR Inc.	---
06	X2864A-25/XICOR Inc.	---
07	2864-350/SEEQ Tech.	CEUC/61394
08	2864-250/SEEQ Tech.	---
09	2864H-250/SEEQ Tech.	---
10	5564-250/SEEQ Tech.	---
11	5564-250/SEEQ Tech.	---

Custodians:

Air Force - 17
 Army - ER
 Navy - EC

Review activities:

Army - AR, MI
 Navy - OS, SH, TD
 Air Force - 11, 19, 85, 99
 DLA - ES

User activities:

Army - SM
 Navy - AS, CG, MC

Preparing activity:

Air Force - 17

Agent:

DLA - ES

(Project 5962-0999)