

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, NMOS, 16,384 BIT,
ELECTRICALLY ERASABLE, PROGRAMMABLE READ-ONLY MEMORY (EEPROM),
MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, N-channel MOS, 2,048 words/8 bit, 5.0 volt electrically erasable programmable read-only memory microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device types. The device types shall be as follows:

<u>Device type</u>	<u>Circuit organization</u>	<u>Access time</u>
01	2048 Words/8 bit	450 ns
02	2048 Words/8 bit	350 ns
03	2048 Words/8 bit	300 ns
04	2048 Words/8 bit	250 ns

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

<u>Outline letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
J	D-3 (24-lead, 1/2" x 1 1/4"), dual-in-line package
X	C-2 (32-terminal, .455" x .550"), rectangular chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	- - - - -	-1.0 to +7.0 V
All inputs/outputs voltage range	- - - - -	-1.0 to +7.0 V
Chip erase voltage range (V_{GE})	- - - - -	-0.3 to +22.0 V
Operating case temperature range	- - - - -	-55°C to +125°C
Storage temperature range	- - - - -	-65°C to +150°C
Continuous power dissipation	- - - - -	1 Watt
Lead temperature (soldering, 10 seconds)	- - - - -	+300°C
Maximum junction temperature (T_J) 2/	- - - - -	+175°C
Thermal resistance, junction to case (θ_{JC}):		
Case J-	- - - - -	18.0°C/W
Case X-	- - - - -	5.5°C/W

1/ Under absolute maximum ratings, the voltage values are with respect to the ground terminal (V_{SS}).

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening condition in accordance with method 5004 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RADC (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

	Device types	Min	Max	Units
Supply voltages:				
V _{CC} - - - - -	All	4.5	5.5	V dc
V _{SS} - - - - -	All	0.0	0.0	V dc
High level input voltages:				
(V _{IH})- - - - -	All	2.0	V _{CC} +1	V dc
Low level input voltage:				
(V _{IL})- - - - -	All	-0.5	0.8	V dc
Operating case temperature (T _C)- - - - -	All	-55	+125	°C
High level chip erase voltage:				
(V _{OE} on OE)- - - - -	All	20	22	V dc

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. In the event of conflict between MIL-M-38510 and this detail specification, the text of this detail specification shall take precedence.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3. Upon implementing design changes, the manufacturer must submit a new block diagram to the qualifying activity for inclusion in this specification. The block diagram shall clearly define the row address inputs and the column address inputs.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be as specified in table II for the applicable device class. The subgroups of table III constitutes the minimum electrical test requirements for screening, qualification, and quality conformance by device class.

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 47 (see MIL-M-38510, appendix E).

3.8 Processing EEPROM's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.8.1 Erase of EEPROM's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.4.

3.8.2 Programming of EEPROM's. When specified, devices shall be programmed in accordance with the procedures and characteristics specified in 4.5.3.

3.8.3 Verification of erasure or programmability of EEPROM's. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that is not in the proper state shall constitute a device failure and that device shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, as applicable, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in (method 1015 of MIL-STD-883).
 1. Test condition D or E using circuit shown on figure 4 (or equivalent).
 2. $T_A = +125^{\circ}\text{C}$, minimum.
 3. Prior to burn-in, the devices shall be programmed with the data pattern shown in figure 9. After verification (see 3.8.3), burn-in shall be performed. Following burn-in, the pattern in each device shall again be verified. Devices verified to have bits not in the proper state shall constitute a device failure and shall be included in the PDA calculation.
- b. Interim and final electrical parameters are as specified in table II. Interim electrical test parameters prior to burn-in must be performed by the manufacturer. The following patterns (min) must be programmed, read and verified: checkerboard, checkerboard complement, all one's, all zero's.

Text continued on page 7.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $V_{CC} = +5 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$ $-55^{\circ}\text{C} < T_C < +125^{\circ}\text{C}$ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Vpp supply current	$I_{CC1}(A)$	$\overline{WE} = V_{IH}$, $\overline{CE} = \overline{OE} = V_{IL}$	A11		140	mA
	$I_{CC2}(SB)$	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$	A11		60	mA
Low level output voltage	V_{OL}	$V_{CC} = 5.5 \text{ V dc}$, $I_{OL} = 2.1 \text{ mA}$	A11		0.4	V
High level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V dc}$, $I_{OH} = -400 \mu\text{A}$	A11	2.4		V
Input leakage current	I_{IL}	$V_I = 0.0 \text{ V dc}$	A11	-10	10	μA
	I_{IH}	$V_I = 5.5 \text{ V dc}$	A11	-10	10	μA
High impedance output leakage current	I_{OLZ}	$V_I = 0.0 \text{ V dc}$, $\overline{OE} = V_{IH}$	A11	-10	10	μA
	I_{OHZ}	$V_I = 5.5 \text{ V dc}$, $\overline{OE} = V_{IH}$	A11	-10	10	μA
Input capacitance 2/	C_I	$V_I = 0 \text{ V}$, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, $f = 1 \text{ MHz}$ (see 4.4.1c)	A11		6	pF
Output capacitance 2/	C_O	$V_O = 0 \text{ V}$, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, $f = 1 \text{ MHz}$ (see 4.4.1c)	A11		10	pF
Output-enable high voltage input current	I_{OE}	$\overline{WE} = V_{IH}$, $\overline{CE} = V_{IL}$, $V_{OE} = 22 \text{ V dc}$	A11		10	μA
$\overline{OE}$ high voltage (chip erase)	V_{OE}		A11	20	22	V
Input logic high voltage	V_{IH}		A11	2.0	$V_{CC} + 1$	V
Input logic low voltage	V_{IL}		A11	-0.5	0.8	V
Read cycle time	t_{AVAV}	(See figures 5-8)	01	450		ns
			02	350		ns
			03	300		ns
			04	250		ns
Chip-enable access time	t_{ELQV}		01		450	ns
			02		350	ns
			03		300	ns
			04		250	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions $V_{CC} = +5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$ $-55^{\circ}\text{C} < T_C < +125^{\circ}\text{C}$ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Address access time	tAVQV	(See figures 5-8)	01		450	ns
			02		350	ns
			03		300	ns
			04		250	ns
Output-enable access time	tOLQV		01		150	ns
			02		150	ns
			03		150	ns
			04		150	ns
Chip-enable to output in low Z	tELQX		A11	10		ns
Chip-enable to output in high Z	tEHQZ		01	10	150	ns
			02	10	150	ns
			03	10	100	ns
			04	10	80	ns
Output enable to output in low Z	tOLQX		A11	10		ns
Output enable to output in high Z	tOHQZ		01	10	150	ns
			02	10	150	ns
			03	10	100	ns
			04	10	80	ns
Output hold from address change	tAXQX		A11	10		ns
Write cycle time $\overline{WE}$ write	tWLAV		A11		10	ms
Write cycle time $\overline{CE}$ write	tELAV		A11		10	ms
Address to $\overline{WE}$ setup time	tAVWL		A11	10		ns
Address to $\overline{CE}$ setup time	tAVEL		A11	10		ns
Address hold time after $\overline{WE}$ low	tWLAX		A11	200		ns
Address hold time after $\overline{CE}$ low	tELAX		A11	200		ns
Chip-enable to $\overline{WE}$ setup time	tELWL		A11	0		ns
Write-enable to $\overline{CE}$ setup time	tWLEL		A11	0		ns
Chip-enable hold time after $\overline{WE}$ high	tWHEH		A11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions $V_{CC} = +5V \pm 10\%$, $V_{SS} = 0V$ $-55^{\circ}C < T_C < +125^{\circ}C$ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Write-enable hold time after CE high	t _{EHWH}	(See figures 5-8)	All	0		ns
Chip-enable to end of write input	t _{ELEH}		All	150		ns
Write pulse width	t _{WLWH}		All	150		ns
Output enable setup time	t _{OHWL} , t _{OHSL}		All	10		ns
Output enable hold time	t _{WHOL} , t _{EHOL}		All	10		ns
Write control recovery time	t _{WHWL} , t _{EHSL}		All	50		ns
Data valid time	t _{WLDV} and t _{ELDV}		All		1	μs
Data setup	t _{DVWH} and t _{DVSL}		All	150		ns
Data hold time	t _{WHDX} and t _{EHDX}		All	20		ns

1/ DC and read and write modes.

2/ This parameter is only sampled and not 100% tested.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1, 2, 7, 8, 9, 10	1, 2, 7, 8, 9, 10
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group B test requirements (method 5005) subgroup 5	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical parameters (method 5005)	N/A	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Additional electrical subgroups for group C endurance life test	N/A	1, 2, 3, 7, 8, 9, 10, 11

1/ *The PDA applies to subgroups 1 and 7 (see 4.2c).

2/ For all electrical tests, the device shall be programmed to the pattern specified.

3/ Any or all subgroups may be combined when using high-speed testers.

- c. Percent defective allowable (PDA) - The PDA for class B devices shall be as specified in MIL-M-38510. The PDA is specified as 5 percent for class B devices based on failures from group A, subgroups 1, and 7 after cooldown as final electrical tests in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. When interim electrical parameter tests are performed, failures resulting from this screening may be excluded from the PDA. All screening failures of group A, subgroups 1 and 7, after burn-in divided by the total number of devices submitted to burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.
- d. An endurance test (using the minimum number of write/erase cycles specified by the device manufacturer) shall be performed at +25°C on each device at any point prior to data retention test of 4.2e (this test can be performed at wafer sort).
- e. A data retention test shall be performed at any time after packaging but prior to burn-in and shall consist of the following:
 1. Place a charge on all memory cells in each device such that the cell will read opposite the state that the cell would read in its equilibrium state (worst pattern).
 2. Verify pattern (see 3.8.3) at +25°C.
 3. Remove all device terminal connections (including supply voltages).
 4. Perform a high temperature storage for 72 hours at 140°C, or 24 hours at 170°C.
 5. Restore device terminal connections.
 6. Verify patterns (see 3.8.3) at +25°C.
- f. After completion of all screening, the devices shall be erased and verified prior to delivery (except devices submitted for groups A, B, C, and D testing and endurance and data retention qualification).

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type on this specification, the slower device type may be part I qualified by conducting only group A electrical tests and any electricals specified as additional group C subgroups and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall consist of the subgroups and LTPD values shown in table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

- c. C_I and C_O , subgroup 4, shall be measured only for initial qualification and after process or design changes which may affect input/output capacitance. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz (see table III).
- d. Subgroup 12 shall be added to group A inspection requirements for class B devices using an LTPD of 10 and class S devices using an LTPD of 5 and consist of procedures, test conditions and limits specified in table III.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

- a. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. The option to categorize devices as ESD sensitive without performing the test is not allowed. Device types categorized as ESD sensitive shall be further tested using 3015 modified as follows:
 - 1. Table I pin combination number (4) shall be "input (B) to $V+(A)$ ". An additional pin combination, number (6), shall be Input (A) connected to $V+$ to V_{SS} connected to common (B) .
 - 2. The test sequence specified in 3b of method 3015 of MIL-STD-883 shall be repeated an additional 1-1/2 times rather than the two specified (six combinations $\times$ 2.5 = 15, one combination only per device).
 - 3. Only those device types that pass ESDS testing at 1,000 volts or greater shall be considered as conforming to the requirements of this specification.
- b. All classes and devices selected for testing shall be programmed (see 3.8.2) with the pattern shown on figure 9. After completion of all testing, the devices shall be erased and verified (except devices submitted for group C and D testing).
- c. Operating life test for class S devices shall be in accordance with table IIa (subgroup 5) of method 5005 of MIL-STD-883, using the circuit shown in figure 4 or equivalent.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End point electrical tests shall be as specified in table II herein.
- b. Endurance life test and extended data retention test: A special endurance life test shall be performed using an LTPD = 5. The samples shall be selected from the devices submitted for group C testing and shall be subjected to the following tests and examinations:
 - 1. Two groups of devices shall be formed, called test cell 1 and test cell 2. An LTPD = 5 applies to each group.
 - 2. Test cell 1 shall be subjected to 10,000 write/erase cycles at -55°C .
 - 3. Test cell 2 shall be subjected to 10,000 write/erase cycles at $+125^{\circ}\text{C}$.
 - 4. After completion of write/erase cycling for test cell 1 and test cell 2, perform group A, subgroups 1, 7, and 9 tests at $+25^{\circ}\text{C}$.
 - 5. Two new groups of devices shall be formed, called test cell 3 and test cell 4.
 - a. Test cell 3 shall be formed by combining 1/2 of the devices from test cell 1 with 1/2 of the devices from test cell 2.
 - b. Test cell 4 shall be formed by combining the remaining 1/2 of the devices from test cell 1 with the remaining 1/2 of the devices from test cell 2.

Text continued on page 27.

Device type 01, 02, 03 and 04.

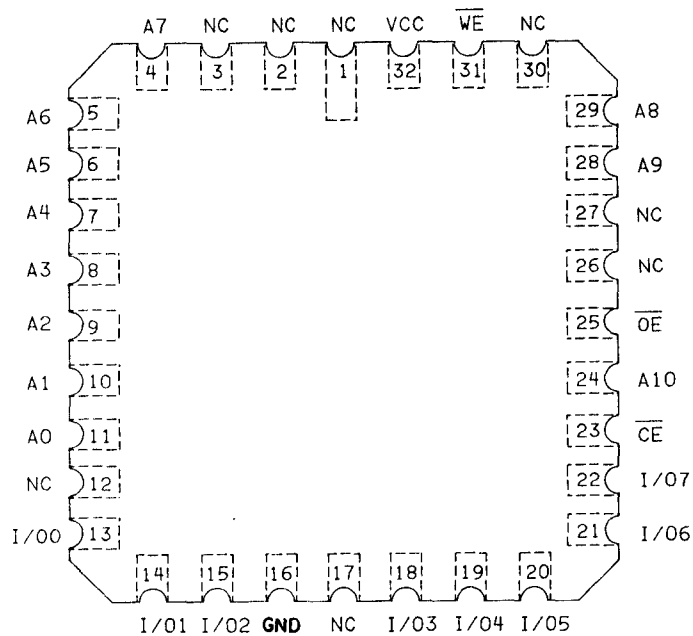
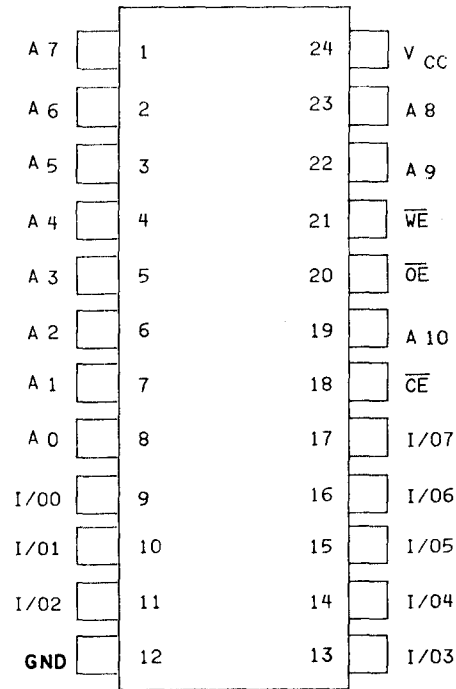


FIGURE 1. Terminal connections.

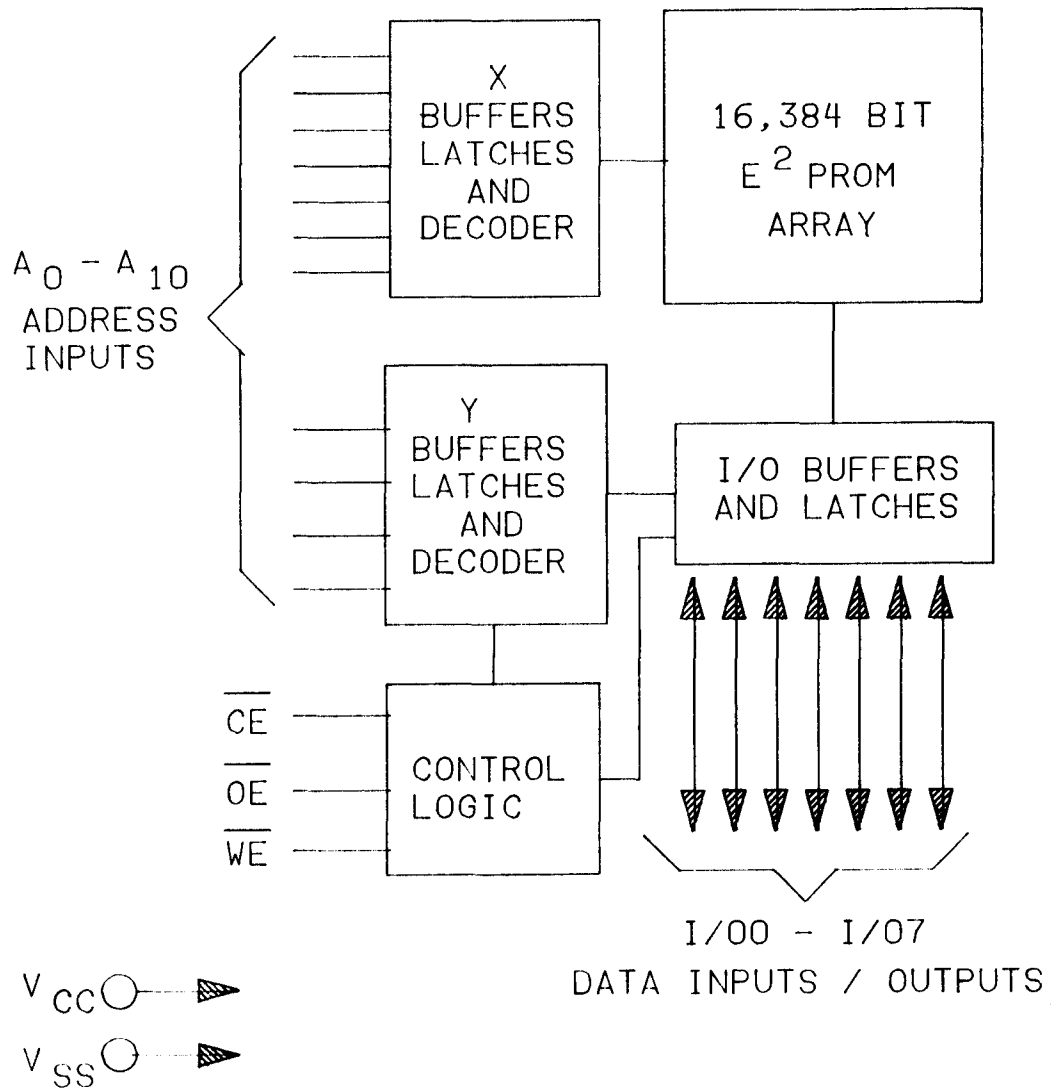
MODE SELECTION

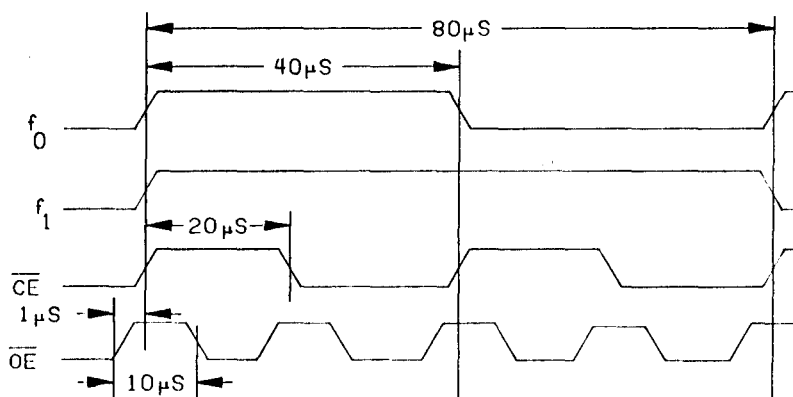
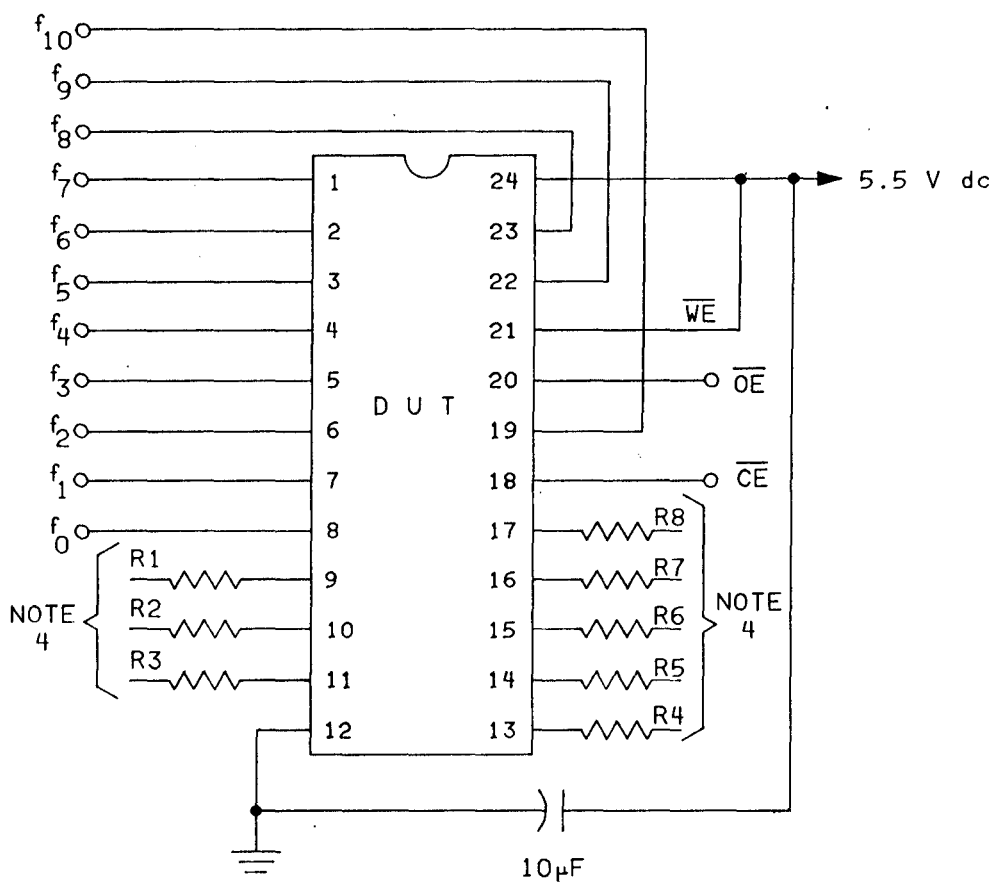
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O0 to I/O7	Power
L	L	H	Read	D _{Out}	Active
L	H	L	Write	D _{In}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	-	-
X	X	H	Write Inhibit	-	-
L	20-22V	L	Chip Erase	D _{In} =H	Active

Note: X = Input may be high, low, or open.

FIGURE 2: Truth table

Device Types 01, 02, 03 and 04

FIGURE 3: Functional block diagram.



Notes:

1. $V_{IH} = 2.0V$ to V_{CC} , $V_{IL} = -0.1$ to $0.8V$
2. $f_0 = 12.5$ kHz square wave
3. $f_1 = f_0 \div 2$, $f_2 = f_1 \div 2$, ..., $f_{10} = f_9 \div 2$
4. $R1$ thru $R8 = 1/0$

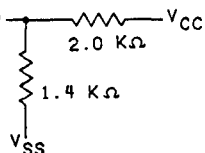
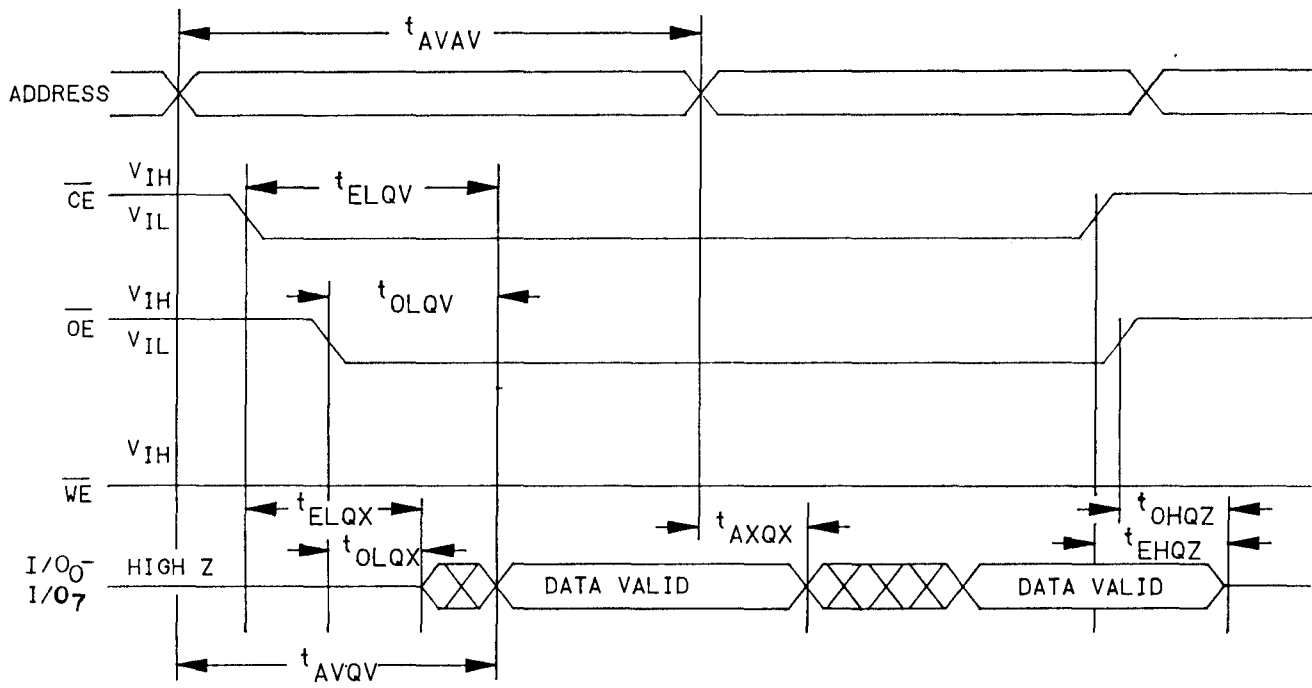
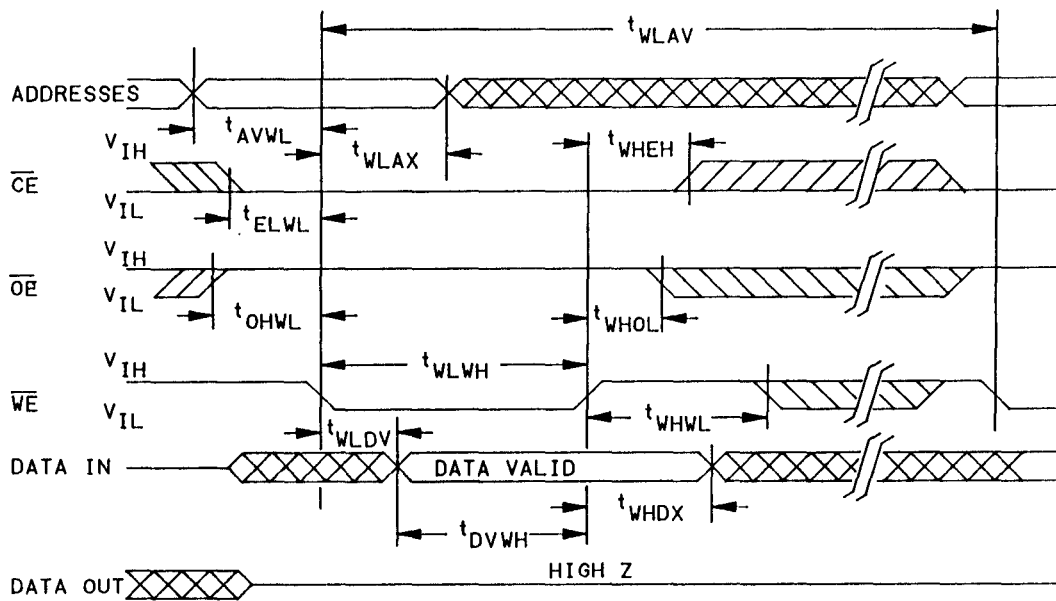
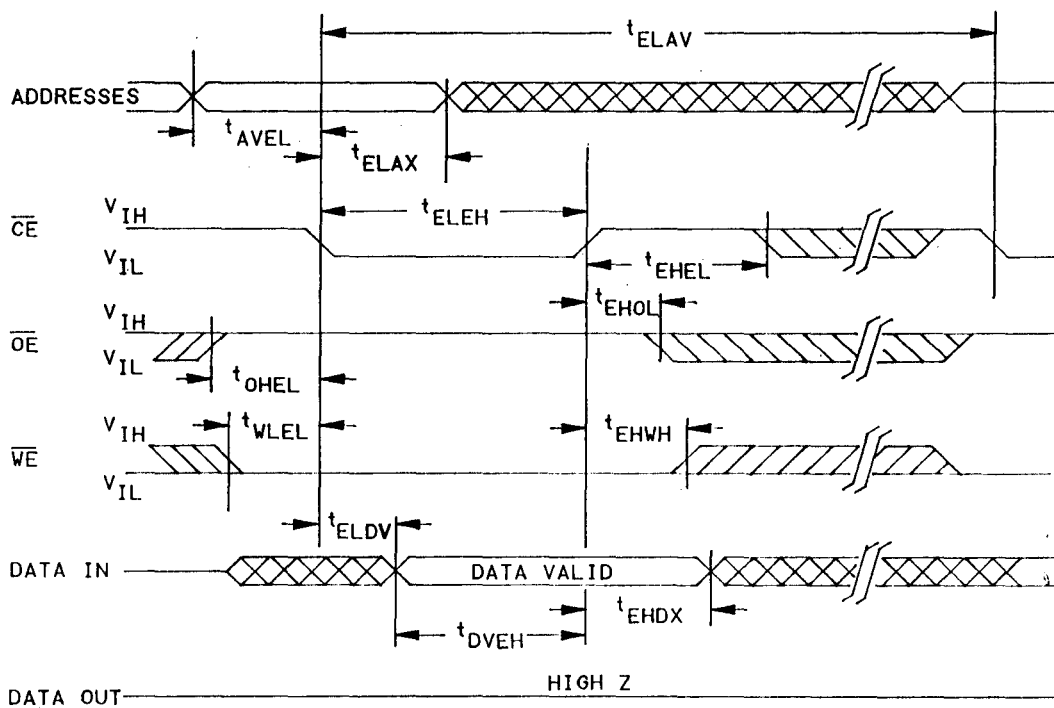


FIGURE 4: Burn-in and operating life test circuit.

FIGURE 5. Read mode waveforms.

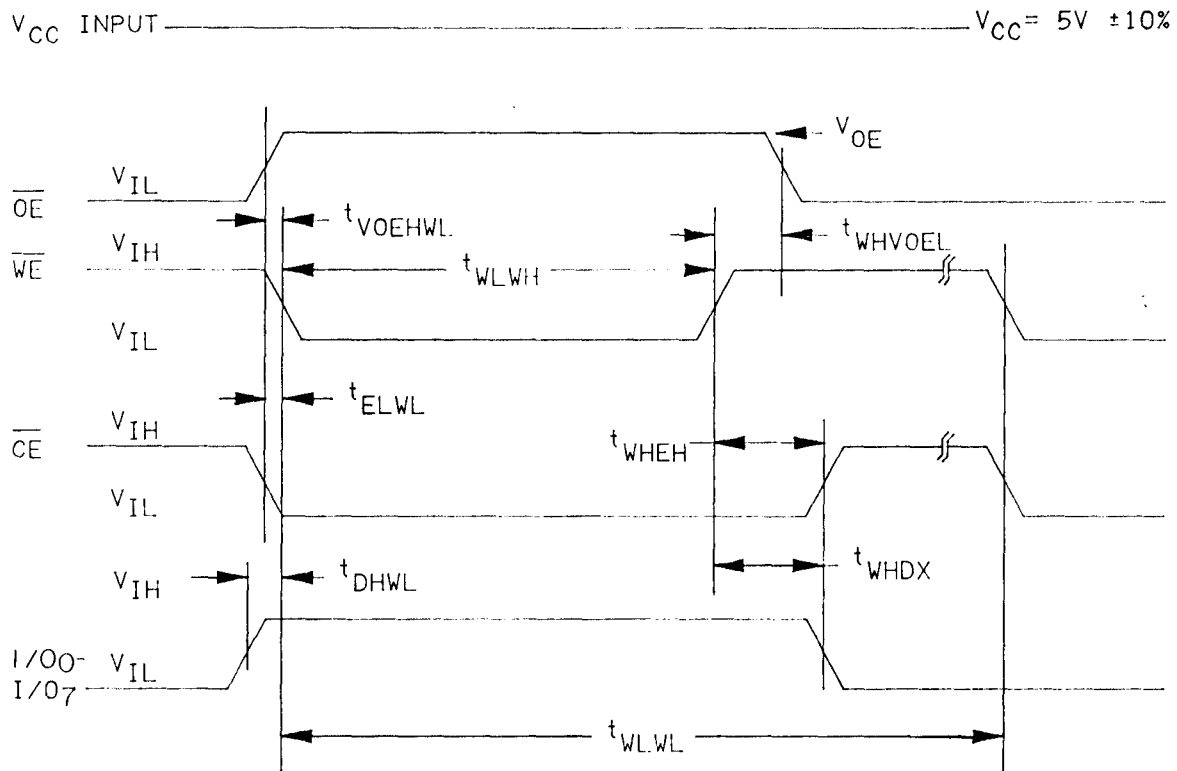


$\overline{WE}$ controlled write mode waveforms.



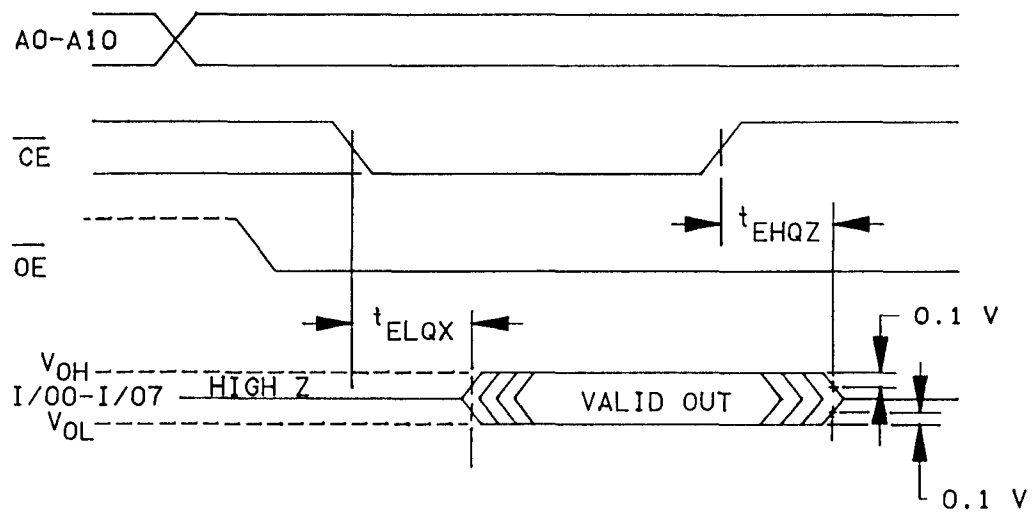
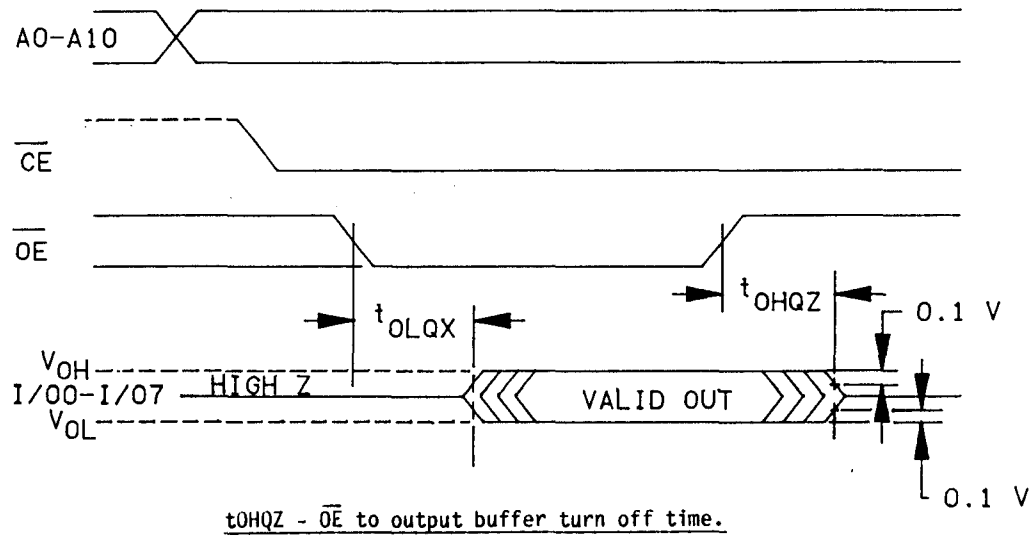
$\overline{CE}$ controlled write mode waveforms.

FIGURE 6. $\overline{WE}$ and $\overline{CE}$ write mode waveforms.



Note: All timing is referenced to $\overline{WE}$ edges.

FIGURE 7: Chip erase mode waveforms.



t_{EHQZ} - $\overline{CE}$ to output buffer turn off time.

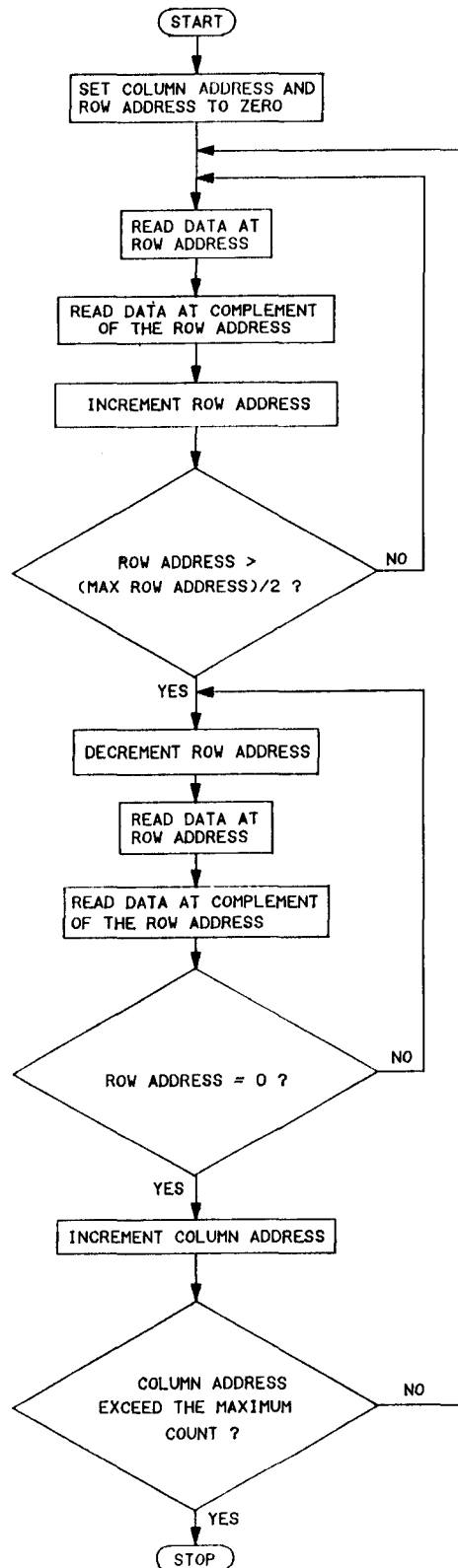
FIGURE 8. Output buffer turn off times.

		Column Address <u>1/</u> <u>2/</u>															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R O W	0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
	1	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
	2	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
	3	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
	.																
	.																
	.																
	112	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
	A 113	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
	D 114	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
	D 115	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
	R .																
	E .																
	S .																
	S 124	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
	125	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
	<u>1/</u> 126	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
	<u>2/</u> 127	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55

Data Output 3/

- 1/ All address numbers shown in decimal.
 2/ Each column/row address location corresponds to 1 Byte.
 3/ All data numbers shown in Hexidecimal.
 AA = 10101010 55 = 01010101

FIGURE 9: Data pattern.

FIGURE 10: Row complement test.

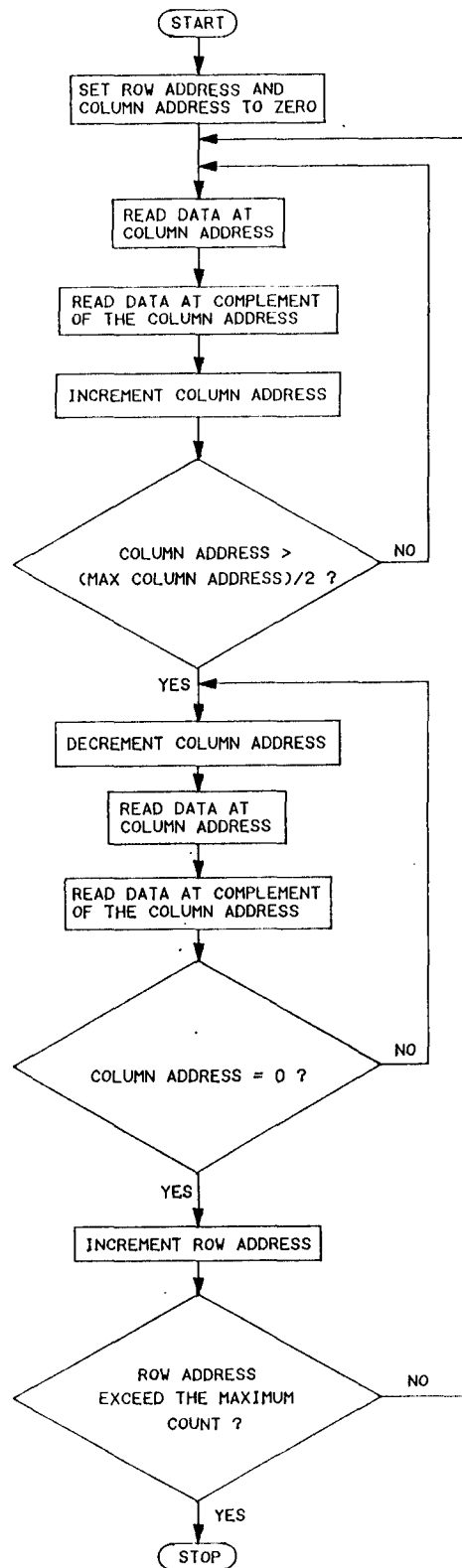
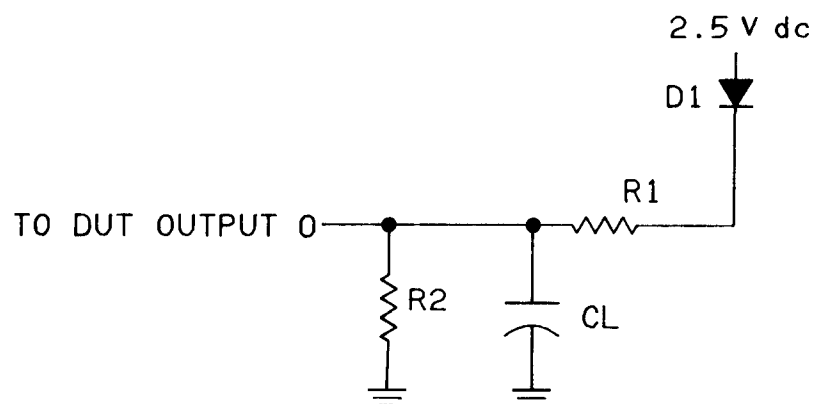


FIGURE 11: Column complement test.



NOTES:

1. CL = 50 pF (minimum) includes jig and probe capacitance.
2. D1 = 1N914
3. R1 is adjusted for IOL.
4. R2 = 6K ohm + or - 5%.

FIGURE 12: Switching time load circuit.

TABLE III. Group A inspection. 1/

Subgroup	Symbol	MIL-STD-883-method	Case J	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Test limits		Unit	
			Case X	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20	21	22	23	24	25	31	28	29	32	Measured terminal	Min		Max
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	1/00	1/01	1/02	GND	1/03	1/04	1/05	1/06	1/07	CE	A10	DE	WE	A9	A8	VCC				
T _C = +25°C	V _{OH}	3006	1	2/	2/	2/	2/	2/	2/	2/	2/	0.4 mA	0.4 mA		GND						0.8 V	2/	0.8 V	2/	2/	2/	4.5 V	1/00	2.4	V	
			2	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1/01	"	"
			3	"	"	"	"	"	"	"	"	"	"	0.4 mA	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1/02	"	"
			4	"	"	"	"	"	"	"	"	"	"		0.4 mA	"	"	"	"	"	"	"	"	"	"	"	"	"	1/03	"	"
			5	"	"	"	"	"	"	"	"	"	"			0.4 mA	"	"	"	"	"	"	"	"	"	"	"	"	1/04	"	"
			6	"	"	"	"	"	"	"	"	"	"				0.4 mA	"	"	"	"	"	"	"	"	"	"	"	1/05	"	"
			7	"	"	"	"	"	"	"	"	"	"					0.4 mA	"	"	"	"	"	"	"	"	"	"	1/06	"	"
			8	"	"	"	"	"	"	"	"	"	"						0.4 mA	"	"	"	"	"	"	"	"	1/07	"	"	
	V _{OL}	3007	9	3/	3/	3/	3/	3/	3/	3/	3/	3/	2.1 mA	2.1 mA		"					"	3/	"	3/	3/	3/	"	1/00		0.4	
			10	"	"	"	"	"	"	"	"	"	"		2.1 mA	"	"	"	"	"	"	"	"	"	"	"	"	"	1/01	"	"
			11	"	"	"	"	"	"	"	"	"	"			2.1 mA	"	"	"	"	"	"	"	"	"	"	"	"	1/02	"	"
			12	"	"	"	"	"	"	"	"	"	"				2.1 mA	"	"	"	"	"	"	"	"	"	"	"	1/03	"	"
			13	"	"	"	"	"	"	"	"	"	"					2.1 mA	"	"	"	"	"	"	"	"	"	"	1/04	"	"
			14	"	"	"	"	"	"	"	"	"	"						2.1 mA	"	"	"	"	"	"	"	"	"	1/05	"	"
			15	"	"	"	"	"	"	"	"	"	"							2.1 mA	"	"	"	"	"	"	"	"	1/06	"	"
			16	"	"	"	"	"	"	"	"	"	"								2.1 mA	"	"	"	"	"	"	1/07	"	"	
	IOHZ		17	4/	4/	4/	4/	4/	4/	4/	4/	4/	5.5 V	5.5 V		"					4/	4/	4/	4/	4/	4/	5.5 V	1/00	-10	+10	μA
			18	"	"	"	"	"	"	"	"	"	"		5.5 V	"	"				"	"	"	"	"	"	"	"	1/01	"	"
			19	"	"	"	"	"	"	"	"	"	"			5.5 V	"	"			"	"	"	"	"	"	"	"	1/02	"	"
			20	"	"	"	"	"	"	"	"	"	"				5.5 V	"	"		"	"	"	"	"	"	"	"	1/03	"	"
			21	"	"	"	"	"	"	"	"	"	"					5.5 V	"	"		"	"	"	"	"	"	"	1/04	"	"
			22	"	"	"	"	"	"	"	"	"	"						5.5 V	"	"		"	"	"	"	"	"	1/05	"	"
			23	"	"	"	"	"	"	"	"	"	"							5.5 V	"	"	"	"	"	"	"	"	1/06	"	"
			24	"	"	"	"	"	"	"	"	"	"								5.5 V	"	"	"	"	"	"	"	1/07	"	"
	IOL2		25	"	"	"	"	"	"	"	"	"	GND	GND		"					"	"	"	"	"	"	"	"	1/00	"	"
			26	"	"	"	"	"	"	"	"	"		GND	"	"				"	"	"	"	"	"	"	"	"	1/01	"	"
			27	"	"	"	"	"	"	"	"	"			GND	"	"			"	"	"	"	"	"	"	"	"	1/02	"	"
			28	"	"	"	"	"	"	"	"	"				GND	"	"			"	"	"	"	"	"	"	"	1/03	"	"
			29	"	"	"	"	"	"	"	"	"					GND	"	"		"	"	"	"	"	"	"	"	1/04	"	"
			30	"	"	"	"	"	"	"	"	"						GND	"	"		"	"	"	"	"	"	"	1/05	"	"
			31	"	"	"	"	"	"	"	"	"							GND	"	"	"	"	"	"	"	"	"	1/06	"	"
			32	"	"	"	"	"	"	"	"	"								GND	"	"	"	"	"	"	"	"	1/07	"	"
	IIH	3010	33	5.5 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V				"					0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	"	A7	"	"	
			34	0.0 V	5.5 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V				"						"	"	"	"	"	"	"	A6	"	"	
			35	"	0.0 V	5.5 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V				"						"	"	"	"	"	"	"	"	A5	"	"
			36	"	"	0.0 V	5.5 V	0.0 V	0.0 V	0.0 V	0.0 V				"						"	"	"	"	"	"	"	"	A4	"	"
			37	"	"	"	0.0 V	5.5 V	0.0 V	0.0 V	0.0 V				"						"	"	"	"	"	"	"	"	A3	"	"
			38	"	"	"	"	0.0 V	5.5 V	0.0 V	0.0 V				"						"	"	"	"	"	"	"	"	A2	"	"
			39	"	"	"	"	"	0.0 V	5.5 V	0.0 V				"						"	"	"	"	"	"	"	"	A1	"	"
			40	"	"	"	"	"	"	0.0 V	5.5 V				"						"	"	"	"	"	"	"	"	A0	"	"
			41	"	"	"	"	"	"	"	0.0 V				"						"	"	"	"	"	"	"	"	CE	"	"
			42	"	"	"	"	"	"	"	"				"						5.5 V	5.5 V					A10	"	"	"	
			43	"	"	"	"	"	"	"	"				"						0.0 V	0.0 V					DE	"	"	"	
			44	"	"	"	"	"	"	"	"				"						"	5.5 V	5.5 V				WE	"	"	"	
			45	"	"	"	"	"	"	"	"				"						"	0.0 V	0.0 V				A9	"	"	"	
			46	"	"	"	"	"	"	"	"				"						"	0.0 V	0.0 V				A8	"	"	"	

See footnotes at end of table.

TABLE III. Group A Inspection - Continued. 1/

Subgroup	Symbol	MIL-STD-883-method	Case J	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Test limits					
			Case X	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20	21	22	23	24	31	28	29	32	Measured terminal	Min	Max	Unit			
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	I/O0	I/O1	I/O2	GND	I/O3	I/O4	I/O5	I/O6	I/O7	CE	A10	DE	WE	A9	A8	VCC						
1 T _C = +25°C	IIL	3009	47	0.0 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V				GND						5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A7	-10	+10	μA		
			48	5.5 V	10.0 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A6			"	
			49		5.5 V	10.0 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V											5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A5			"	
			50			5.5 V	10.0 V	5.5 V	5.5 V	5.5 V	5.5 V											5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A4			"	
			51				10.0 V	5.5 V	5.5 V	5.5 V	5.5 V											5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A3			"	
			52					10.0 V	5.5 V	5.5 V	5.5 V											5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A2			"	
			53						10.0 V	5.5 V	5.5 V											5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A1			"	
			54							10.0 V	5.5 V											5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A0			"	
			55								5.5 V											5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	CE			"	
			56																			5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A10			"	
57																			5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	DE			"				
58																				5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	WE			"			
59																					5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A9			"			
60																						5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	A8			"			
	ICC2	3005	61	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC									2.0 V	VCC	0.6 V	VCC	VCC	VCC	VCC	"	VCC		60	nA		
	ICC1	3005	62	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC									0.8 V	VCC	0.8 V	VCC	VCC	VCC	VCC	"	VCC		140	nA		
2	Same tests, terminal conditions, and limits as subgroup 1, except T _C = +125°C.																																
3	Same tests, terminal conditions, and limits as subgroup 1, except T _C = -55°C.																																
4	C _I	3012	63	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	All inputs		6	pF		
	C _O	3012	64	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	All I/Os		10	pF		
7	Functional tests	3014	65	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	I/O0 thru I/O7		5/				
8	Same tests, terminal conditions and limits as subgroup 7, except T _C = +125°C and -55°C.																																
9 T _C = +25°C	tAVQV	01 02 03 04	66	7/	7/	7/	7/	7/	7/	7/	7/	8/	8/	8/	GND	8/	8/	8/	8/	8/	7/	7/	7/	7/	7/	7/	7/	1/00		450 350 300 250	ns		
			67	"	"	"	"	"	"	"	"	"	8/	8/	8/	"	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	thru		450 350 300 250	"	
			68	"	"	"	"	"	"	"	"	"	8/	8/	8/	"	8/	8/	8/	8/	8/	"	"	"	"	"	"	"			150	"	
			69	"	"	"	"	"	"	"	"	"	8/	8/	8/	"	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	1/07	10		"	
	tWLV	01 02 03 04	70	9/	9/	9/	9/	9/	9/	9/	9/	8/	8/	8/	"	8/	8/	8/	8/	8/	9/	9/	9/	9/	9/	9/	9/	1/00		10 200 0	ms		
			71	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	thru			"		
			72	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"		
			73	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"		
	tWLV	01 02	74	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1/07			"		
			75	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"		

See footnotes at end of table.

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See footnotes at end of table.

- 1/ Terminal conditions:
 - a. Outputs not designated are open or resistively coupled to GND or voltage less than or equal to V_{CC} .
 - b. Inputs not designated are high ≥ 2.0 V or low ≤ 0.8 V.
- 2/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels are $V_{IL} = 0.8$ V and $V_{IH} = 2.0$ V.
- 3/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels are $V_{IL} = 0.8$ V and $V_{IH} = 2.0$ V.
- 4/ Terminal conditions for the output leakage current test shall be as follows:
 - a. $V_{IH} = 2.0$ V; $V_{IL} = 0.8$ V.
 - b. For I_{OLZ} : Select an appropriate address to acquire a logic "1" on the designated output. Apply V_{IH} to CE and V_{IL} to OE. Measure the leakage current while applying the specified voltage.
 - c. For I_{OHZ} : Select an appropriate address to acquire a logic "0" on the designated output. Applying V_{IL} to CE and V_{IH} to OE. Measure the leakage current while applying the specified voltage.
- 5/ Input/output capacitance shall be measured between the designated terminal and the GND pin under the following conditions: $V_I = 0$ V, $f = 1$ MHz, oscillator voltage = 50 mV rms maximum. Unused pins are open.
- 6/ The functional tests shall verify the applicable pattern. All bits shall be tested. Terminal conditions are as follows:
 - a. Inputs: H = 2.0 V to V_{CC} ; L = 0.0 V to 0.8 V.
 - b. Outputs: Output voltage shall be either:
 1. H = 2.4 V minimum and L = 0.4 V maximum when using a high-speed checker double comparator.
 2. H > 1.5 V and L < 1.5 V when using a high-speed checker single comparator.
 - c. The functional tests shall be performed with $V_{CC} = 4.5$ V and $V_{CC} = 5.5$ V.
- 7/ For these tests in subgroups 9, 10, and 11, the row and column complement test shown on figures 10 and 11 shall be used. Input/output conditions appear in table IV. Timing diagrams appear on figure 5. Subgroups 9, 10, and 11 shall be performed with $V_{CC} = 4.5$ V and 5.5 V.
- 8/ The outputs are loaded per figure 12.

- 9/ These tests in subgroups 9, 10, and 11 are the byte write cycle limits. These parameters shall be verified during functional testing. Input/output conditions appear in table IV. Timing diagrams appear on figure 6. Subgroups 9, 10, and 11 shall be performed with $V_{CC} = 4.5\text{ V}$ and 5.5 V .
- 10/ These tests in subgroups 9, 10, and 11 are the mass erase/program cycle limits. These parameters shall be verified during the following test sequence:
- Mass erase and verify (initialize to all 1's).
 - Mass program all 0's and verify.
 - Mass erase and verify
- Input/output conditions appear in table IV. Timing diagrams appear on figure 7. Subgroups 9, 10, and 11 shall be performed with $V_{CC} = 4.5\text{ V}$ and 5.5 V .
- 11/ For subgroup 12, input conditions appear in table IV. Timing waveforms appear on figure 8. The outputs are loaded per figure 12. Additional terminal conditions are as follows:
- $V_{CC} = 4.5\text{ V}$ and $V_{CC} = 5.5\text{ V}$.
 - Output disable times (t_{OHQZ} and t_{EHQZ}): A tristate condition is detected when the output voltage is between ($V_{OH}-100\text{ mV}$) and ($V_{OL}+100\text{ mV}$).
 - Output enable times (t_{OLQX} and t_{ELQX}): An active condition is detected when the output voltage is less than 0.4 V or greater than 2.4 V .

TABLE IV. Input/output for table III, subgroups 7, 9, 10, and 11. 1/ 2/ 3/

Symbol	Terminals	A	B	Device type	Units
V _{CC}	V _{CC}	4.5	5.5	A11	V
V _{IH}	Logic inputs	2.0	2.0	A11	V
V _{IL}	Logic inputs	0.8	0.8	A11	V
V _{OH}	Logic output compare level	2.4	2.4	A11	V
V _{OL}	Logic output compare level	0.4	0.4	A11	V
$\overline{WE}$	Write enable	2.0	2.0	A11	V
$\overline{CE}$	Chip enable	0.4	0.4	A11	V
$\overline{OE}$	Output enable	0.4	0.4	A11	V
t _{AVQV}	Address	450.0	450.0	01	ns
		350.0	350.0	02	ns
		300.0	300.0	03	ns
		250.0	250.0	04	ns
t _{ELQV}	Chip enable	450.0	450.0	01	ns
		350.0	350.0	02	ns
		300.0	300.0	03	ns
		250.0	250.0	04	ns
t _{OLQV}	Output enable	450.0	450.0	01	ns
		350.0	350.0	02	ns
		300.0	300.0	03	ns
		250.0	250.0	04	ns
t _{AXQX}	I/00 - I/07	10.0	10.0	A11	ns

1/ For subgroups 9, 10, and 11, the address complement test on figures 10 and 11 shall be used.

2/ Timings waveforms for subgroups 9, 10, and 11 are shown on figure 5.

3/ The data pattern on figure 9 (or its complement) shall be used.

6. Extended data retention test -- test cell 3

- a. Program all bits in each device with the data pattern representing the worst case data retention pattern (see 4.2e.1).
- b. Bake all devices, unbiased, for 1,000 hours (minimum) at +140°C.
- c. Read and verify pattern at +25°C. (see 3.8.3).
- d. Perform endpoint electrical tests per table II.

7. Operation life test -- test cell 4

- a. Program all devices with the data pattern shown in figure 9 (see 3.8.2).
- b. Perform steady state life test (method 1005 of MIL-STD-883).
 1. Test condition D or E as specified in 4.5.2 and figure 4 (or equivalent).
 2. Ambient temperature +125°C (minimum).
 3. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
 4. Perform endpoint electrical tests per table II.
8. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing). A device failing the erase/verify shall be considered a failure.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

- a. End point electrical parameters shall be as specified in table II herein.
- b. All devices selected for testing shall be programmed (see 3.8.2) with the pattern in figure 9. After completion of all testing, the devices shall be erased and verified. Where the use of electrical rejects are permitted, no programming or erasure or verification is required.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate table and as follows:

Note - In order to prevent spurious device erasure or write, a logic high state must be applied to $\overline{WE}$ or to $\overline{CE}$ simultaneously before the application of V_{CC} , and removed simultaneously after the removal of V_{CC} .

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Life test, burn-in, cooldown and electrical test procedure. When devices are measured at 25°C following application of the steady state life or burn-in test condition, all devices shall be cooled to 35°C or within 10°C of power stable condition prior to removal of bias voltages/signals. Any electrical tests required shall first be performed at -55°C or 25°C prior to any 125°C tests that are required.

4.5.3 Programming procedure. The following procedure shall be followed when programming (write) is performed. The waveforms and timing relationships shown on figure 5 and the conditions specified in table V shall be adhered to. Initially, and after each chip erasure (see 4.5.4), all bits are in the "H" state (output high). Information is introduced by selectively programming a "L" and/or "H" into the desired bit locations. A programmed "L" can be changed to an "H" by programming an "H". No erasure is necessary (see 4.5.4).

TABLE V. High voltage chip erasure conditions. 1/

Test	Symbol	Conditions $V_{CC} = 4.5-5.5$ V dc, $V_{SS} = 0$ V dc $-55^{\circ}\text{C} < T_C < 125^{\circ}\text{C}$ unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Output enable voltage	V_{OE}	See figure 7	A11	20	22	V
$\overline{CE}$ to $\overline{WE}$ setup time	t_{ELWL}		A11	10		ns
Data to $\overline{WE}$ setup time	t_{DHWL}		A11	10		ns
Data hold after $\overline{WE}$ high	t_{WHDX}		A11	50		ns
Write pulse width	t_{WLWH}		A11	175		ns
$\overline{WE}$ to $\overline{CE}$ hold time	t_{WHEH}		A11	50		ns
V_{OE} setup time to $\overline{WE}$	t_{VOEHWL}		A11	10		ns
V_{OE} hold time after $\overline{WE}$ high	t_{WHVOEL}		A11	10		ns
Write cycle time	t_{WLWL}		A11		10	ms

1/ $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V.

4.5.4 Erasing procedure.

- a. Chip erase. The device is erased by setting the output enable pin to 20.0 volts (see figure 7), while all other inputs are set in the normal byte erase mode (see 4.5.4b). After chip erasure, all bits are in the "H" state.
- b. Byte erase. A byte is erased by simultaneously programming a "H" state into each bit at the selected address (see 4.5.3).

4.5.5 Read mode operation. The device is in the read mode whenever $\overline{OE}$ and $\overline{WE}$ are at logic "L" (low level) and the V_{IH} . The waveforms and timing relationships shown on figure 5 and the test conditions and limits specified in table III shall be applied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. The devices covered by this specification require electrostatic protection.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logistic purposes.

6.2 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- h. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols and definitions used herein are defined in MIL-M-38510, MIL-STD-1331 (including terms and symbols for device terminals) and as follows:

V_{SS} - - - - -	Common or reference voltage mode.
V_{CC} - - - - -	Supply voltage.
V_{OE} - - - - -	Output-enable voltage during chip erase.
A0-A10 - - - - -	Address inputs used to address 1 of 2048/8 bit locations in static storage array.
$\overline{CE}$ - - - - -	Chip-enable used along with the output enable ($\overline{OE}$) signal to control the state of the 8 data I/O signals.

$\overline{OE}$ - - - - -	Output-enable used to control the data-out terminals.
I/OO-I/O7- - - - -	Data input-output, 8 bit wide data bus through which data is stored or accessed.
WE - - - - -	Write enable input used to select the read, write, or erase modes.
I _{CC} - - - - -	Supply current (standby and active).
I _{OE} - - - - -	Output-enable ($\overline{OE}$) high voltage current.
I _{IH} , I _{IL} - - - - -	Input leakage currents.
I _{OHZ} , I _{OLZ} - - - - -	High impedance output leakage currents.
V _{IL} - - - - -	Logical low input voltage.
V _{IH} - - - - -	Logical high input voltage.
V _{OL} - - - - -	Logical low output voltage.
V _{OH} - - - - -	Logical high output voltage.
C _I - - - - -	Input capacitance.
C _O - - - - -	Output capacitance.
t _{AVAV} - - - - -	Cycle time during read.
t _{ELQV} - - - - -	Chip-enable access time.
t _{AVQV} - - - - -	Address access time.
t _{OLQV} - - - - -	Output enable access time.
t _{ELQX} - - - - -	Chip-enable to output in low Z.
t _{EHQZ} - - - - -	Chip-enable to output in high Z.
t _{OLQX} - - - - -	Output-enable to output in low Z.
t _{OHQZ} - - - - -	Output-enable to output in high Z.
t _{AXQX} - - - - -	Output hold from address change.
t _{WLAV} - - - - -	Cycle time during $\overline{WE}$ write operation.
t _{ELAV} - - - - -	Cycle time during $\overline{CE}$ write operation.
t _{AVWL} - - - - -	Address to $\overline{WE}$ setup time.
t _{AVEL} - - - - -	Address to $\overline{CE}$ setup time.
t _{WLAX} - - - - -	Address hold time after $\overline{WE}$ low.
t _{ELAX} - - - - -	Address hold time after $\overline{CE}$ low.
t _{ELWL} - - - - -	Chip-enable to $\overline{WE}$ setup time.
t _{WLLEL} - - - - -	Write-enable to $\overline{CE}$ setup time.
t _{WHEH} - - - - -	Chip-enable hold time after $\overline{WE}$ high.
t _{EHWH} - - - - -	Write-enable hold time after $\overline{CE}$ high.

tELEH- - - - -	Chip-enable pulse width during write.
tOHWL- - - - -	Output-enable to $\overline{WE}$ setup time.
tOHEL- - - - -	Output-enable to $\overline{CE}$ setup time.
tWHOL- - - - -	Output-enable hold time after $\overline{WE}$ high.
tEHOL- - - - -	Output-enable hold time after $\overline{CE}$ high.
tWLWH- - - - -	Write-enable pulse width during write.
tWHWL- - - - -	Minimum write-enable high time.
tEHEL- - - - -	Minimum chip-enable high time after write.
tDVWH- - - - -	Data in setup time before $\overline{WE}$ high.
tDVEH- - - - -	Data in setup time before $\overline{CE}$ high.
tWHDX- - - - -	Data hold time after $\overline{WE}$ high.
tEHDX- - - - -	Data hold time after $\overline{CE}$ high.
tWLDV- - - - -	Maximum time to valid data after $\overline{WE}$ low.
tELDV- - - - -	Maximum time to valid data after $\overline{CE}$ low.
tVOEHWL- - - - -	V_{OE} setup time to $\overline{WE}$ low (chip erase).
tWHVOEL- - - - -	V_{OE} hold time after $\overline{WE}$ high (chip erase).
tWLWL- - - - -	Cycle time during chip erase operation.

6.3.1 Timing parameter abbreviations. All timing abbreviations use a lower case "t" followed by four upper case descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and transition. Thus, the format is:

Signal name from which interval is defined	t	X	X	X	X
Transition direction for first signal		T	T	T	T
Signal name to which interval is defined					
Transition direction for second signal					

a. Signal definitions:

A = Address

I = Data in

O = Data out

CE = Chip enable

OE = Output enable

WE = Write enable

b. Transition definitions:

H = Transition to high

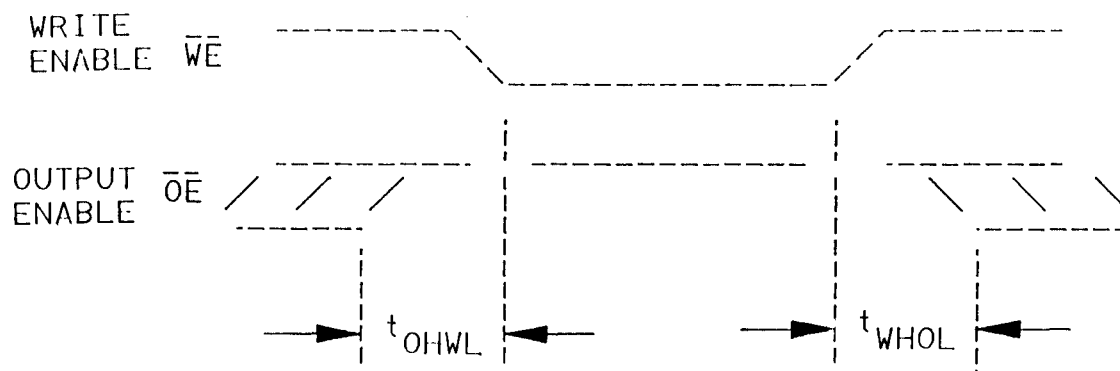
L = Transition to low

V = Transition to valid

X = Transition to invalid or don't care

Z = Transition to off (high impedance)

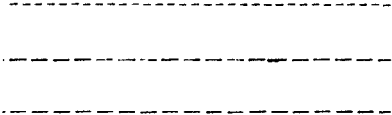
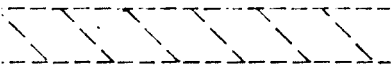
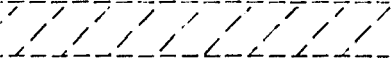
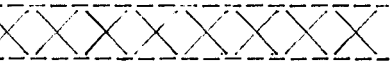
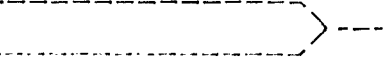
EXAMPLE:



The example shows output enable to $\overline{WE}$ setup time defined as t_{OHWL} and output enable hold time after $\overline{WE}$ high defined as t_{WHOL} .

- c. Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

d. Waveforms:

Waveform Symbol	Input	Output
	Must be valid	Will be valid
	Change from H to L	Will change from H to L
	Change from L to H	Will change from L to H
	Don't care any change permitted	Changing state unknown
		High impedance

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation to static charge. Input protective devices have been designed to the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment and tools.
- c. Handling of devices by the leads should be avoided.
- d. Devices should be stored in conductive foam or carriers.
- e. The uses of plastic, rubber, or silk in MOS areas should be avoided.
- f. Relative humidity should be maintained above 50 percent, if practical.
- g. Operator should be grounded when handling devices.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>	<u>CAGE number</u>
01	X2816A-45/XICOR Inc.	60395
02	X2816A-35/XICOR Inc.	--
03	X2816A-30/XICOR Inc.	--
04	X2816A-25/XICOR Inc.	--

Custodians:

Air Force - 17
Army - ER
Navy - EC

Review activities:

Air Force - 11, 19, 85, 99
Army - AR, MI
Navy - OS, SH, TD
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC

Preparing activity:

Air Force - 17

Agent:

DLA - ES

(Project 5962-0908)