

MILITARY SPECIFICATION

MICROCIRCUIT, DIGITAL, 262,144 BIT, MOS, ULTRAVIOLET ERASABLE
PROGRAMMABLE READ-ONLY MEMORY (EPROM)
MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon N-channel MOS erasable programmable read-only memory microcircuits which employ the ultraviolet light erasing technique. Two product assurance classes and a choice of case outline and lead finishes are provided for each type and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device types. The device types shall be as follows:

<u>Device type</u>	<u>Circuit</u>
01	32,768 8 bit EPROM (250 ns)
02	32,768 8 bit EPROM (200 ns)
03	32,768 8 bit EPROM (170 ns)

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

<u>Outline letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
Y	D-10 (28-lead, 1/2" x 1-3/8"), dual-in-line package Transparent lid to permit UV light erasure
Z	C-12 (32-terminal RECT. CC. 450" x .550") Transparent lid to permit UV light erasure

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC}) 1/	- - - - -	-0.6 V dc to 6.25 V dc
All input or output voltages-	- - - - -	-0.6 V dc to 6.25 V dc
Program input (V_{pp}) - - - - -	- - - - -	-0.6 V dc to 13.0 V dc
Operating case temperature range (T_C) - - -	- - -	-55°C to +125°C
Storage temperature range - - - - -	- - - - -	-65°C to +150°C
Lead temperature (soldering, 10 seconds)-	-	+260°C
Thermal resistance, junction-to-case (θ_{JC})-	-	30°C/W
Maximum power dissipation (P_D)- - - - -	- - - - -	1.0 watt
Junction temperature (T_J) 2/- - - - -	- - - - -	+175°C

1/ All voltages referenced to V_{SS} .

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions per method 5004 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	- - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	- -	2.0 V dc
Maximum low-level input voltage (V_{IL})	- -	0.8 V dc
High-level program input voltage (V_{PP})	- -	12.5 V
Case operating temperature range (T_C)	- - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this specification.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3. Upon implementing design changes, the manufacturer must submit a new block diagram to the qualifying activity for inclusion in this specification. The block diagram shall clearly define the row address inputs and the column address inputs.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

TABLE I. Electrical performance characteristics (device types 01, 02, 03).

Test	Symbol	Conditions $\frac{1}{-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}}$	Device type	Limits		Unit
				Min	Max	
High-level input voltage	V_{IH}		A11	2.0	$V_{CC} + 1$	V
Low-level input voltage	V_{IL}		A11	-0.1	0.8	V
High-level output voltage	V_{OH}	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -400\text{ }\mu\text{A}$	A11	2.4		V
Low-level output voltage	V_{OL}	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 2.1\text{ mA}$	A11		0.45	V
Output leakage current	I_{OHZ}	$V_O = 2.4\text{ V}$	A11	-10	+10	μA
	I_{OLZ}	$V_O = 0.4\text{ V}$				
High-level input current	I_{IH}	Address, $\overline{CE}$, $\overline{OE}$ $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ $V_{IN} = V_{CC}$	A11	-10	+10	μA
Low-level input current	I_{IL}	Address, $\overline{CE}$, $\overline{OE}$ $V_{CC} = 5.5\text{ V}$ $V_{IN} = 0.0\text{ V}$	A11	-10	+10	μA
Supply current (standby)	I_{CC1}	$\overline{CE} = V_{IH}$ $\overline{OE} = V_{IL}$ $V_{CC} = 5.5\text{ V}$ Output open	A11		50	mA
Supply current (active)	I_{CC2}	$\overline{CE} = V_{IL}$ $V_{CC} = 5.5\text{ V}$ Output open	01,02		125	mA
			03		140	mA
V_{pp} current read/standby	I_{PP1}	$V_{pp} = 5.5\text{ V}$	A11		5	mA
Input capacitance	C_i	$V_I = 0\text{ V}$, $f = 1\text{ MHz}$	A11		6	pF
Output capacitance	C_o	$V_O = 0\text{ V}$, $f = 1\text{ MHz}$	A11		12	pF
Margin voltage	V_m	HMOS IIE	A11	5.9		V
Address inputs to outputs (access time)	t_{AVQV}	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ (see figure 4)	01		250	ns
			02		200	ns
			03		170	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics (device types 01, 02, 03) - Continued.

Test	Symbol	Conditions ^{1/} $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$	Device type	Limits		Unit
				Min	Max	
Chip enable to outputs (access time)	t_{ELQV}	$\overline{OE} = V_{IL}$ $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ (see figure 4)	01		250	ns
			02		200	ns
			03		170	ns
Output enable to outputs (access time)	t_{OLQV}	$\overline{CE} = V_{IL}$ $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ (see figure 4)	01		130	ns
			02,03		75	ns
Address to outputs hold	t_{AXQX}	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ (see figure 4)	A11	0		ns
Output enable high to output float	t_{OHQZ}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ (see figure 4)	A11	0	55	ns
Chip enable high to output float	t_{EHQZ}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ (see figure 4)	A11	0	100	ns

^{1/} Complete terminal conditions shall be specified in table III.

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	1/ 2/ 3/ 4/ 5/	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	2,8,10	2,8,10
Final electrical test parameters (method 5004)	1*,2,3,7* 9,10,11	1*,2,3,7* 8,9,10,11
Group A test requirements (method 5005)	1,2,3,4, 7,8,9,10, 11	1,2,3,4, 7,8,9,10, 11
Group B test requirements (method 5005)	1,2,3,4, 7,9,10, 11	N/A
Group C end-point electrical parameters (method 5005)	N/A	2,8,10
Group D end-point electrical parameters (method 5005)	2,8,10	2,8,10

1/ (*)PDA applies to subgroup 1 and 7 (see 4.2c).

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroup 7 shall consist of verifying the specified pattern.

4/ For all electrical tests, the device shall be programmed to the pattern specified.

5/ Test number 8 in subgroup S and B are to be run hot only.

3.7 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.7.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedure and characteristics specified in 4.8.

3.7.2 Programmability of EPROMS. When specified, device shall be programmed to the specified pattern using the procedures and characteristics specified in 4.7 and table IV.

3.7.3 Verification of erasure or programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 47 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in (method 1015 of MIL-STD-883).
 - (1) Test condition D or E using the circuit shown on figure 5, or equivalent.
 - (2) $T_A = +125^{\circ}\text{C}$ minimum.
- b. Interim and final electrical tests shall be as specified in table II, except interim electrical parameters tests prior to burn-in are optional at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) for class S devices shall be as specified in MIL-M-38510. The PDA for class B devices shall be 5 percent based on failures from group A, subgroups 1 and 7, test after cooldown as final electrical parameter tests are performed prior to burn-in, failures resulting from pre-burn-in screening may be excluded from the PDA. The verified failures of group A, subgroups 1 and 7, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.
- d. EPROM data retention test flow.
 - (1) Program (i.e., charge the floating gate) a minimum of 95 percent of the bit locations, including the slowest programming cell (manufacturer to provide information on which are the slowest programming cells for a particular design). The remaining cells shall provide a worst case speed pattern.
 - (2) Bake, unbiased, for 72 hours at $+140^{\circ}\text{C}$ to screen for data retention lifetime.
 - (3) Perform "raw class" testing ($+25^{\circ}\text{C}$), which includes a margin test. For the margin test, use $V_m = +5.9\text{ V}$ and loose timing ($t_{ACC} \geq 1\text{ }\mu\text{s}$).
 - (4) Perform a dynamic burn-in per MIL-STD-883.
 - (5) Perform post-burn in electrical checks at $+25^{\circ}\text{C}$ and $+125^{\circ}\text{C}$, to include margin testing ($V_m = +5.9\text{ V}$, $t_{ACC} \geq 1\text{ }\mu\text{s}$).
 - (6) Erase device; then program the remaining bits which were not programmed in step 1 above.
 - (7) Perform electrical testing at -55°C , to include a margin test ($V_m = +5.9\text{ V}$, $t_{ACC} \geq 1\text{ }\mu\text{s}$).
 - (8) Erase device; perform erase check.
 - (9) Mark and package.
 - (10) Perform final quality assurance procedures.
- e. After completion of all testing, the devices shall be erased and verified prior to delivery (except devices submitted for groups A, B, C, and D testing).

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Qualification data for subgroups 7, 9, 10, and 11 shall be attributes only.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies one device type which is manufactured identically to other device type on this specification, then the other device types may be part I qualified by conducting only group A electrical tests and submitting data in accordance with MIL-M-38510, appendix D (i.e. groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. Subgroups 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. Half the devices selected for testing shall be programmed with the pattern shown on figure 7. The remaining devices shall be programmed with the complement of the pattern shown on figure 7. After completion of all testing, the devices shall be erased and verified (except submitted for group B, C, and D testing).
- d. Subgroup 4 (C_i and C_o measurements) shall be measured only for initial qualification and after process or design change which may affect capacitance.
- e. Subgroup 12 shall be added to group A inspection requirements for class B devices using an LTPD of 10 and consist of procedures, test conditions and limits specified in table III.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

- a. A special subgroup shall be added using an LTPD of 15 for classes S and B. This subgroup shall consist of a high voltage test of the input protection circuits, and shall be tested per MIL-STD-883C, method 3015.
- b. Steady-state life test for class S devices shall be in accordance with table IIa (subgroup 5) of method 5005 of MIL-STD-883, using the circuit on figure 5.
- c. Half the devices selected for class S electrical testing shall be programmed with the pattern shown on figure 7. The remaining devices shall be programmed with the complement of the pattern shown on figure 7. After completion of all testing, the devices shall be erased and verified (except devices submitted for group C and D testing).

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical tests shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E using the circuit shown on figure 5, or equivalent.
 - (2) $T_A = +125^\circ\text{C}$ minimum.
 - (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.
 - (4) The devices selected for testing shall be programmed with a random pattern (i.e., data programmed should exhibit no pattern dependency). After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

- c. A reprogrammability test shall be added to group C inspection prior to performing the steady-state life test (see 4.4.3b) using an LTPD of 10. The devices to be submitted to the steady-state life testing shall be subjected to the following tests and examinations:

- (1) Each device in the sample shall be subjected to a minimum of 50 program and erase cycles. Each cycle shall consist of the following steps:
 - a. Program half the devices with the pattern shown on figure 7 program the remaining devices with the complement of the pattern shown on figure 7.
 - b. Verify patterns (see 3.7.3).
 - c. Erase (see 3.7.1).
 - d. Verify pattern erasure (see 3.7.3).

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. The devices selected for testing shall be programmed with a random pattern (i.e., data programmed should exhibit no pattern dependency). After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

4.4.5 Constant acceleration. The constant acceleration tests of groups C and D shall be performed using test condition D.

4.5 Methods of inspection. Methods of inspection shall be specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Inspection of packaging. The sampling and inspection of the preservation, packing and container marking shall be in accordance with the requirements of MIL-M-38510.

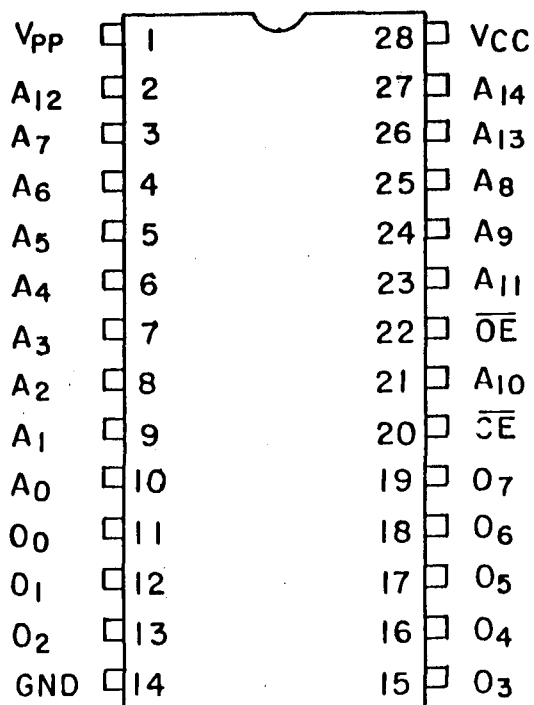
4.7 Programming procedure. The following procedure shall be followed when programming and verification testing is performed. The waveforms and timing relationships shown in figure 6 and test conditions and limits specified in table IV shall be adhered to:

- a. Initially, and after each erasure, all bits are in the "H" state (output high). Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure.
- b. The programming algorithm (see figure 11) utilizes two different pulse types: Initial and overprogram. The duration of the initial CE pulse(s) is one millisecond which will then be followed by a longer overprogram pulse of length 3X millisecond. Where X is an iteration counter and is equal to the number of the initial one-millisecond pulses applied to a particular addressed location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for, before the overprogram pulse is applied.
- c. A verify should be performed on the programmed bits to determine that they were correctly programmed. The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6.0 \text{ V}$ and $V_{pp} = 12.5 \text{ V}$. When the programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{pp} = 5.0 \text{ V}$.

4.8 Erasing procedure. The device is erased by exposure to high intensity short wave ultraviolet light at a wavelength to 253.7 nm. The recommended integrated dose (i.e., UV intensity X exposure time) is a minimum of 15 W-s/cm². The EPROM should be placed about 1 inch away from the light source for a period of 20 minutes. After erasure all bits are in the high state.

5. PACKAGING

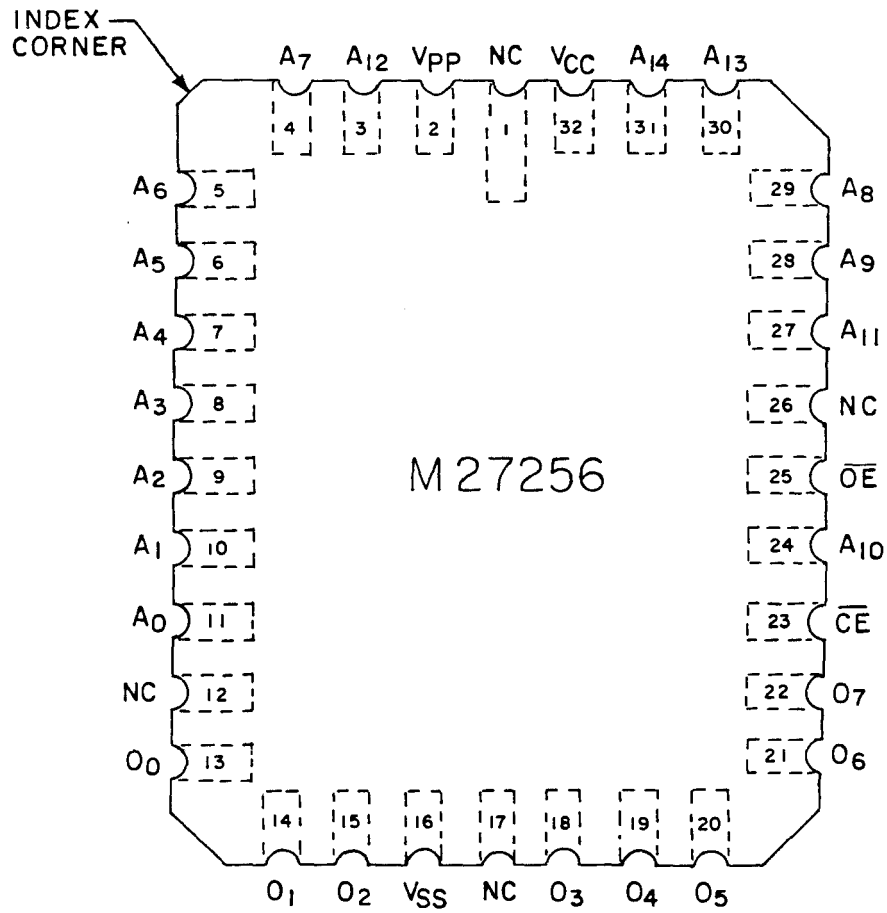
5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. The devices covered by this specification require electrostatic protection.

Device types 01, 02, and 03

Case Y

FIGURE 1. Terminal connections.

Device types 01, 02, and 03



Case Z

FIGURE 1. Terminal connections - Continued.

Unprogrammed

Word in	Inputs				Outputs
	$\overline{CE}$	$\overline{OE}$	V_{PP}	A14-A0	00-07
X	V_{IL}	V_{IL}	V_{CC}	X	V_{OH}
X	V_{IH}	X	V_{CC}	X	HI-Z
X	X	V_{IH}	V_{CC}	X	HI-Z

X = Irrelevant
 HI-Z = High-impedance state

Mode selection

Mode	Inputs				Outputs
	$\overline{CE}$	$\overline{OE}$	A9	V_{PP}	00-07
Read	V_{IL}	V_{IL}	X	V_{CC}	D_{out}
Output disable	V_{IL}	V_{IH}	X	V_{CC}	HI-Z
Standby	V_{IH}	X	X	V_{CC}	HI-Z
Program	V_{IL}	V_{IH}	X	V_{PP}	D_{in}
Verify	V_{IH}	V_{IL}	X	V_{PP}	D_{out}
Optional verify	V_{IL}	V_{IL}	X	V_{PP}	D_{out}
Program inhibit	V_{IH}	V_{IH}	X	V_{PP}	HI-Z
Identifier	V_{IL}	V_{IL}	V_H	V_{CC}	Code

X = Irrelevant
 HI-Z = High-impedance state
 V_H = 12.0 V +/- 0.5 V

FIGURE 2. Truth tables.

Device types 01, 02, and 03

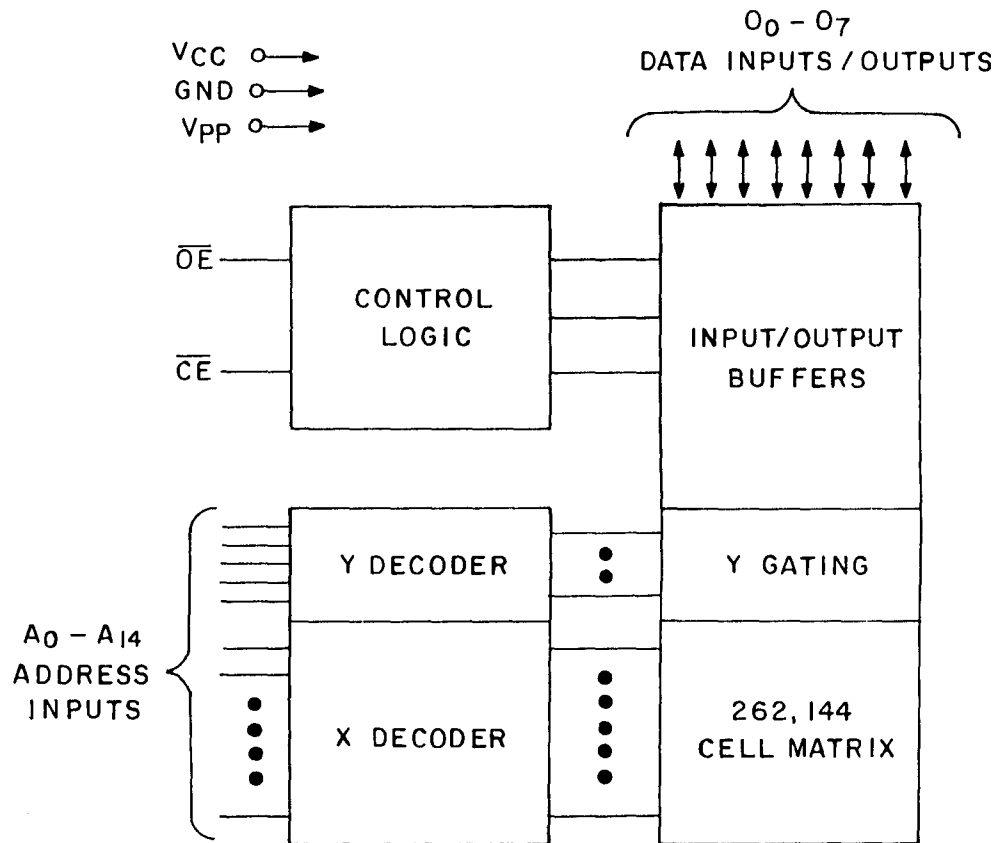
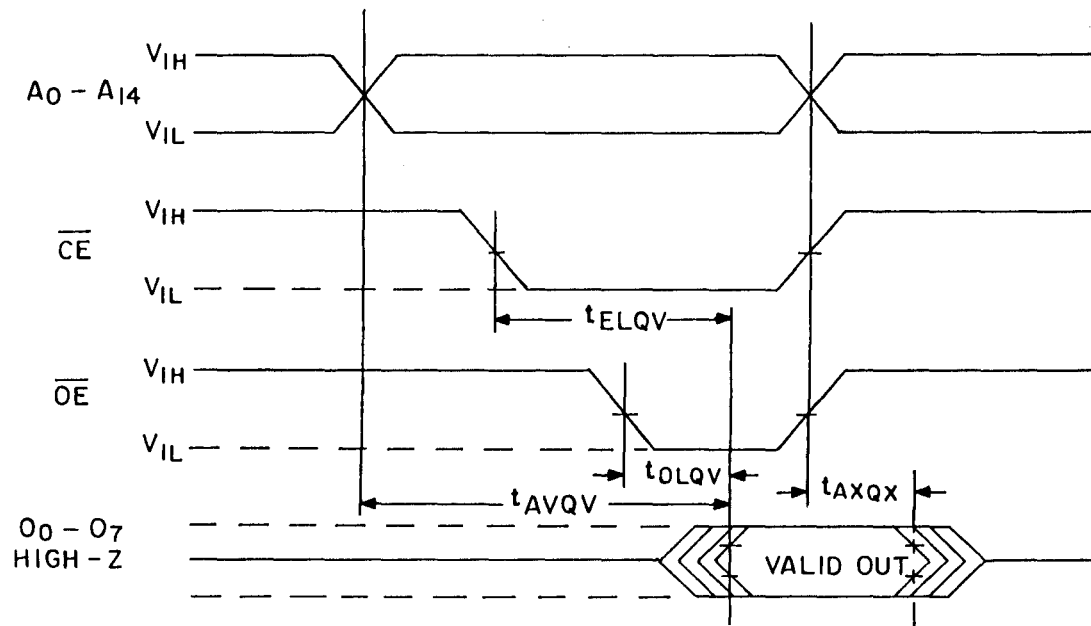
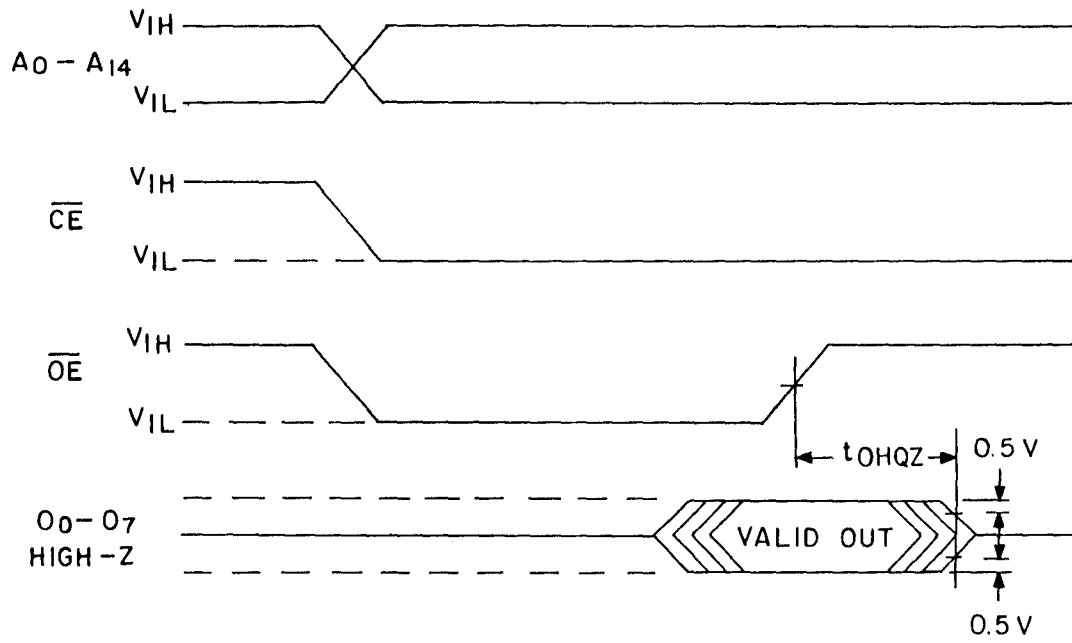


FIGURE 3. Functional block diagram.



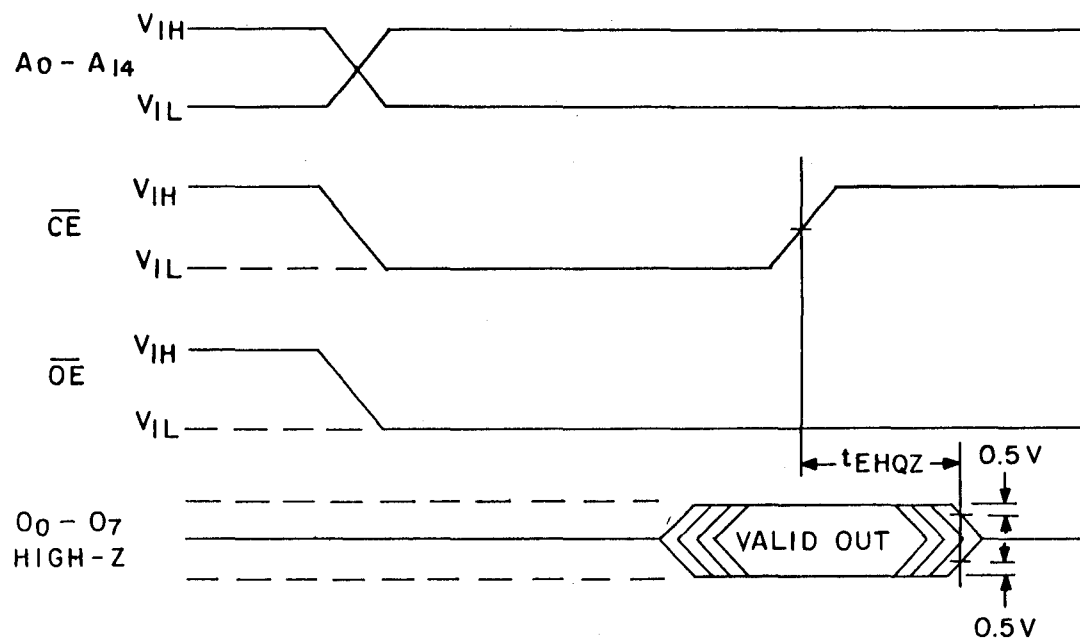
Read timing

FIGURE 4. A.C. Waveforms.



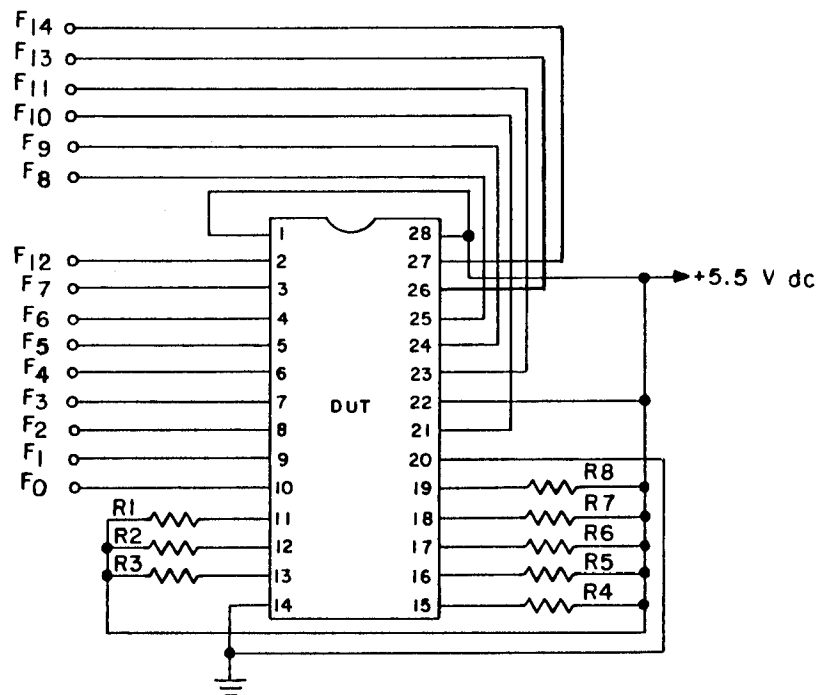
Output disable timing

FIGURE 4. A.C. Waveforms -Continued.



Output disable timing

FIGURE 4. A.C. Waveforms -Continued.

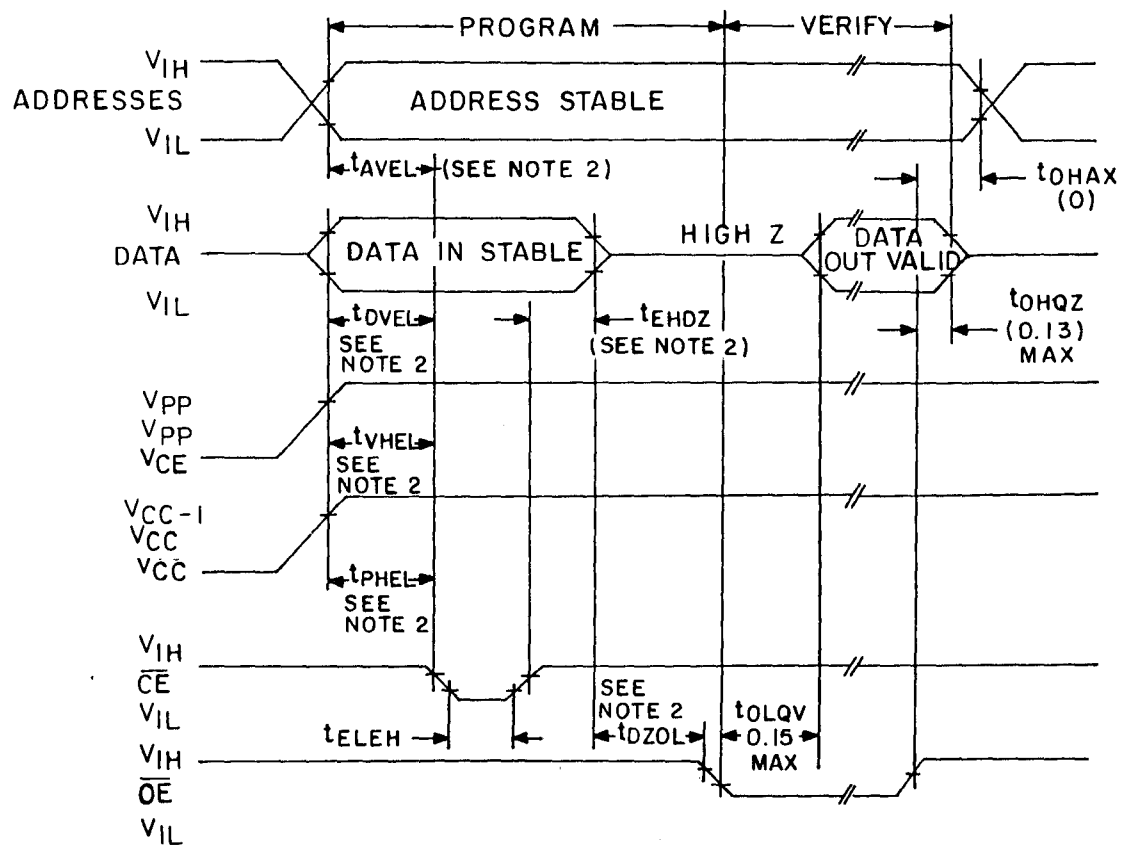


NOTES:

1. R_1 thru $R_8 = 1.0 \text{ k } \Omega \pm 5.0\%$.
2. All pulse generators have the following characteristics:
 $V_{IL} = 0.0 \text{ V}$ minimum to 0.65 V maximum
 $V_{IH} = 2.2 \text{ V}$ minimum to 5.50 V maximum
 $50\% \pm 15\%$ duty cycle and frequencies as specified in note 3.
3. Input frequencies are as follows:
frequency ($\pm 20\%$)

$$\begin{aligned}
 F_0 &= 16 \text{ kHz} < F_0 < 100 \text{ kHz} \\
 F_1 &= 1/2 F_0 \\
 F_2 &= 1/2 F_1 \\
 F_3 &= 1/2 F_2 \\
 F_4 &= 1/2 F_3 \\
 F_5 &= 1/2 F_4 \\
 F_6 &= 1/2 F_5 \\
 F_7 &= 1/2 F_6 \\
 F_8 &= 1/2 F_7 \\
 F_9 &= 1/2 F_8 \\
 F_{10} &= 1/2 F_9 \\
 F_{11} &= 1/2 F_{10} \\
 F_{12} &= 1/2 F_{11} \\
 F_{13} &= 1/2 F_{12} \\
 F_{14} &= 1/2 F_{13}
 \end{aligned}$$

FIGURE 5. Burn-in and steady state life test circuit.



NOTES:

1. All time shown in () are minimum and in μsec unless otherwise specified.
2. The input timing reference level is 0.8 V for a V_{IL} and 2 V for a V_{IH} .
3. t_{OLQV} and t_{HQZ} are characteristics of the device but must be accommodated by the programmer.
4. When programming the device a 0.1 μF capacitor is required across V_{pp} and GND to suppress spurious voltage transients which can damage the device.

FIGURE 6. Programming waveforms.

TABLE III. Group A Inspection. 1/ 2/

Subgroup	Symbol	MIL-STD-883-method	Case	Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																					
			Case	Z	2	3	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20	21	22	27	28	29	30	31	32	Min	Max																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																										
			Test no.	V _{pp}	A12	A7	A6	A5	A4	A3	A2	A1	A0	00	01	02	GND	03	04	05	06	07	-CE	A10	-DE	A11	A9	A8	A13			A14		V _{CC}																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																							
T _C = +25°C	V _{DH}	3006	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	00	01	02	03	04	05	06	07	2.4		V																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																												
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	00	01	02	03	04	05	06	07																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	00	01	02	03	04	05	06	07																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	00	01	02	03	04	05	06	07																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	00	01	02	03	04	05	06	07																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	00	01	02	03	04	05	06	07																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
	V _{OL}	3037	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	00	01	02	03	04	05	06	07	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.

See footnotes at end of table.

TABLE III. Group A inspection - Continued.

Subgroup	Symbol	MIL-STD-883-method	Case Y	Case Z														Test no.														Measured terminal	Test limits		Unit		
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		Min	Max			
				2	3	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20	21	22	23	24	25	27	28	29	30	31	32						
			Test no.	V _{pp}	A12	A7	A6	A5	A4	A3	A2	A1	A0	00	01	02	GND																				
1 T _C = +25°C	ICC1	3025	67	5.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GND																V _{CC}		50	mA	
	ICC2 01 02 03		68	"	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			"																V _{CC}		125 125 140	mA " "	
	IPP1		69	"	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			"																V _{pp}		5	"	
2, 3		Same tests, terminal conditions and limits as subgroup 1, except T _C = +125°C and -55°C.																																			
4	IC _i	3012	70	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	A11 inputs	6	pF		
	IC _o		71	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	A11 outputs	12	pF		
7	Functional tests	3014	72	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	00 thru 07	5/			
9		Same tests, terminal conditions and limits as subgroup 4, except T _C = +125°C.																																			
9	TAQV 01		73	V _{CC}	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	8/	8/	8/	GND	8/	8/	8/	8/	8/	7/	7/	7/	7/	7/	7/	7/	7/	7/	00 thru 07	250 200 170	ns " "		
	TELQV 01		74	"													"																	250 200 170	ns " "		
	TOLQV 01		75	"													"																	130 75 75	ns " "		
	TAQV 02 03		76	"													"																	0			
10, 11		Same tests, terminal conditions and limits as subgroup 6, except T _C = +125°C and -55°C.																																			
12	T040Z		77	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	GND	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	00 thru 07	55	ps "		

- 1/ Terminal conditions:
 - a. Outputs not designated are open or resistively coupled to GND or voltage.
 - b. Inputs not designated are high > 2.0 V or low < 0.8 V.
- 2/ V_{CC} must be applied simultaneously or before V_{pp} and removed simultaneously or after V_{pp} .
- 3/ Before performing electrical tests, half the devices submitted for acceptance shall be programmed with the pattern shown on figure 7. The remaining devices shall be programmed with the complement of the pattern shown on figure 7. $V_{IH} = 2.0$ V and $V_{IL} = 0.8$ V shall be applied to the applicable address pins to set the measured terminal in the proper state for measurement.
- 4/ Terminal conditions for the output leakage current test shall be as follows:
 - a. $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V.
 - b. For I_{OLZ} , select an appropriate address to acquire a logic one on the designated output. Apply V_{IH} to $\overline{CE}$ and V_{IL} to $\overline{OE}$. Measure the leakage current while applying the specified voltage.
 - c. For I_{OHZ} , select an appropriate address to acquire a logic zero on the designated output. Apply V_{IL} to $\overline{CE}$ and V_{IH} to $\overline{OE}$. Measure the leakage current while applying the specified voltage.
- 5/ Input/output capacitance shall be measured between the designated terminal and the GND pin under the following conditions: $V_{CC} = V_I = V_O = 0$ V, $f = 1$ MHz.
- 6/ Terminal conditions are as follows:
 - a. Inputs, see table V for V_{IL} and V_{IH} values.
 - b. Outputs, see table V for V_{OL} and V_{OH} values.
 - c. The functional tests shall be performed with $V_{CC} = 4.5$ V to $V_{CC} = 5.5$ V.
- 7/ For subgroups 9, 10 and 11, the address complement test shown on figures 8 and 9 shall be used. Input/output conditions appear in table V. Timing diagrams appear on figure 4. Subgroups 9, 10 and 11 shall be performed with $V_{CC} = 4.5$ V and 5.5 V.
- 8/ The outputs are loaded in accordance with figure 10.
- 9/ For subgroup 12, input/output conditions appear in table V. Timing waveforms appear on figure 4. The outputs are loaded in accordance with figure 10. Additional terminal conditions are as follows:
 - a. For subgroup 12, $V_{CC} = 4.5$ V and $V_{CC} = 5.5$ V.
 - b. Output disable time from $\overline{CE}$ (see figure 4).
 1. Output in logic low state - select an appropriate address to acquire a logic zero to the designated output $\overline{OE} = V_{IL}$.
 2. Output in logic high state - select an appropriate address to acquire a logic one to the designated output $\overline{OE} = V_{IL}$.
 - c. Output disable time from $\overline{OE}$ (see figure 4).
 1. Output in logic low state - select an appropriate address to acquire a logic zero to the designated output $\overline{CE} = V_{IL}$.
 2. Output in logic high state - select an appropriate address to acquire a logic one to the designated output $\overline{CE} = V_{IL}$.

TABLE IV. Programming characteristic.Recommended timing requirements for programming, $T_C = +25^\circ\text{C}$

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
t_{ELEH}	Pulse width, program pulse $\overline{\text{CE}}$	Initial <u>1/</u>	.95	1.0	1.05	ms
		Overprogram <u>2/</u>	2.85		78.75	
t_{PHEL}	V_{CC} setup time		2			ms
t_{VHEL}	V_{pp} setup time		2			ms
t_{AVEL}	Address setup time		2			μs
t_{DVEL}	Data setup time		2			μs
t_{DZOL}	$\overline{\text{OE}}$ setup time		2			μs
t_{OHAX}	Address hold time		0			μs
t_{EHDZ}	Data hold time		2			μs
V_{pp}	Programming supply voltage		12.2	12.5	12.8	V
V_{CC}	Programming supply voltage		5.75	6.0	6.25	V
I_{pp2}	V_{CC} supply current (program) $\overline{\text{CE}} = V_{\text{IL}}$				50	mA
V_{IH}	High level input voltage		2.0		$V_{\text{CC}}-1$	V
V_{IL}	Low level input voltage		-0.1		0.8	V

1/ Initial program pulse width tolerance is 1 ms +/-5%.2/ The length of the overprogram pulse width may vary from 2.8 ms to 78.75 ms as a function of iteration counter value X.

TABLE V. Input/output conditions.
 For table III subgroups 9, 10, 11, 12.

Symbol	Terminatons	A	B	Unit
V_{CC}	V_{CC}	4.5	5.5	V
V_{IH}	Logic inputs	2.4	2.4	V
V_{IL}	Logic inputs	0.45	0.45	V
V_{OH} <u>1/</u>	Logic outputs	2.0	2.0	V
V_{OL} <u>1/</u>	Logic outputs	0.8	0.8	V

1/ Output compare levels for subgroups 9, 10 and 11.

ADD: 0 1 2 3 4 5 6 7 8 9 A B C D E F	ADD: 0 1 2 3 4 5 6 7 8 9 A B C D E F
0	55000000000000000000000000000000
90	00000000000000008100000000000000
B0	000000000000000000000000000000081
D0	00000000008100000000000000000000
F0	0000000000000000000000000000810000
180	000000000000000000000000000000081
1A0	00000000000000810000000000000000
1C0	0000000000000000000000000000810000
1E0	00000000008100000000000000000000
290	00000000000000000000000000000008100
2B0	00000000000081000000000000000000
2D0	000000000000000000000000000081000000
2F0	00000000810000000000000000000000
380	00000000000081000000000000000000
3A0	00000000000000000000000000008100
3C0	00000000810000000000000000000000
3E0	000000000000000000000000000081000000
410	00000000000000810000000000000000
430	000000000000000000000000000000081
450	00000000008100000000000000000000
470	0000000000000000000000000000810000
500	000000000000000000000000000000081
520	00000000000000810000000000000000
540	0000000000000000000000000000810000
560	00000000008100000000000000000000
610	000000000000000000000000000008100
630	00000000000081000000000000000000
650	000000000000000000000000000081000000
670	00000000810000000000000000000000
700	00000000000000810000000000000000
720	00000000000000000000000000008100
740	00000000810000000000000000000000
760	000000000000000000000000000081000000
890	00000081000000000000000000000000
8B0	00000000000000000000000000008100000000
8D0	0081000000000000000000000000000000
8F0	0000000000000000000081000000000000
980	000000000000000000000000008100000000
9A0	0000008100000000000000000000000000
9C0	0000000000000000000081000000000000
9E0	0081000000000000000000000000000000
A80	0000000000000000000000810000000000
AB0	0000810000000000000000000000000000
AD0	0000000000000000008100000000000000
AF0	8100000000000000000000000000000000
B80	0000810000000000000000000000000000
BA0	0000000000000000000000810000000000
BC0	8100000000000000000000000000000000
BE0	0000000000000000008100000000000000
C10	0000008100000000000000000000000000
C30	0000000000000000000000008100000000
C50	0081000000000000000000000000000000
C70	0000000000000000000081000000000000
D00	0000000000000000000000008100000000
D20	0000008100000000000000000000000000
D40	0000000000000000000081000000000000
D60	0081000000000000000000000000000000
E10	00000000000000000000810000000000
E30	0000810000000000000000000000000000
E50	00000000000000008100000000000000
E70	8100000000000000000000000000000000
F00	0000810000000000000000000000000000
F20	000000000000000000000000810000000000
F40	8100000000000000000000000000000000
F60	0000000000000000810000000000000000
1090	00000000000000420000000000000000
10B0	000000000000000000000000000000042
10D0	00000000004200000000000000000000
10F0	00000000000000000000000000000420000
1180	000000000000000000000000000000042
11A0	00000000000004200000000000000000
11C0	0000000000000000000000000000042000
11E0	0000000000420000000000000000000000
1290	000000000000000000000000000004200
12B0	0000000000004200000000000000000000
12D0	0000000000000000000000000420000000
12F0	0000000042000000000000000000000000
1380	0000000000004200000000000000000000
13A0	000000000000000000000000000004200
13C0	0000000042000000000000000000000000
13E0	00000000000000000000000000042000000
1410	0000000000000420000000000000000000
1430	0000000000000000000000000000042
1450	0000000000420000000000000000000000
1470	00000000000000000000000000000420000
1500	000000000000000000000000000000042
1520	0000000000000420000000000000000000
1540	00000000000000000000000000000420000
1560	0000000000420000000000000000000000
1610	000000000000000000000000000004200
1630	0000000000004200000000000000000000
1650	0000000000000000000000000420000000
1670	0000000042000000000000000000000000
1700	0000000000004200000000000000000000
1720	000000000000000000000000000004200
1740	0000000042000000000000000000000000
1760	00000000000000000000000000042000000
1890	0000004200000000000000000000000000
18B0	0000000000000000000000004200000000
18D0	0042000000000000000000000000000000
18F0	0000000000000000000042000000000000
1980	0000000000000000000000004200000000
19A0	0000004200000000000000000000000000
19C0	0000000000000000000042000000000000
19E0	0042000000000000000000000000000000
1A90	0000000000000000000000420000000000
1AB0	0000420000000000000000000000000000
1AD0	0000000000000000420000000000000000
1AF0	4200000000000000000000000000000000
1B80	0000420000000000000000000000000000
1BA0	0000000000000000000000420000000000
1BC0	4200000000000000000000000000000000
1BE0	0000000000000000420000000000000000
1C10	0000004200000000000000000000000000
1C30	0000000000000000000000004200000000
1C50	0042000000000000000000000000000000
1C70	00000000000000000042000000000000
1D00	0000000000000000000000004200000000

FIGURE 7. Data pattern.

ADD: 0 1 2 3 4 5 6 7 8 9 A B C D E F	ADD: 0 1 2 3 4 5 6 7 8 9 A B C D E F
1D20 00000042000000000000000000000000	2C10 00000024000000000000000000000000
1D40 0000000000000000000042000000000000	2C30 0000000000000000000000000240000000
1D60 00420000000000000000000000000000	2C50 0024000000000000000000000000000000
1E10 0000000000000000000000420000000000	2C70 0000000000000000000002400000000000
1E30 00004200000000000000000000000000	2D00 0000000000000000000000024000000000
1E50 0000000000000000420000000000000000	2D20 00000024000000000000000000000000
1E70 42000000000000000000000000000000	2D40 0000000000000000000002400000000000
1F00 00004200000000000000000000000000	2D60 00240000000000000000000000000000
1F20 00000000000000000000004200000000	2E10 00000000000000000000024000000000
1F40 42000000000000000000000000000000	2E30 00002400000000000000000000000000
1F60 00000000000000000042000000000000	2E50 00000000000000000240000000000000
2090 00000000000000024000000000000000	2E70 24000000000000000000000000000000
20B0 0000000000000000000000000000024	2F00 00002400000000000000000000000000
20D0 00000000024000000000000000000000	2F20 00000000000000000000024000000000
20F0 00000000000000000000000000240000	2F40 24000000000000000000000000000000
2180 0000000000000000000000000000024	2F60 00000000000000000240000000000000
21A0 00000000000002400000000000000000	3090 00000000000001800000000000000000
21C0 00000000000000000000000000240000	30B0 000000000000000000000000000000018
21E0 00000000024000000000000000000000	30D0 00000000001800000000000000000000
2290 0000000000000000000000000002400	30F0 00000000000000000000000000180000
22B0 00000000000240000000000000000000	3180 0000000000000000000000000000018
22D0 00000000000000000000000024000000	31A0 00000000000001800000000000000000
22F0 00000002400000000000000000000000	31C0 000000000000000000000000000180000
2380 00000000000240000000000000000000	31E0 00000000001800000000000000000000
23A0 0000000000000000000000000002400	3290 00000000000000000000000000001800
23C0 00000002400000000000000000000000	32B0 00000000000018000000000000000000
23E0 00000000024000000000000000000000	32D0 0000000000000000000000000018000000
2410 00000000000002400000000000000000	32F0 00000000180000000000000000000000
2430 0000000000000000000000000000024	3380 00000000000018000000000000000000
2450 00000000024000000000000000000000	33A0 00000000000000000000000000001800
2470 00000000000000000000000000240000	33C0 00000000180000000000000000000000
2500 0000000000000000000000000000024	33E0 0000000000000000000000000018000000
2520 00000000000002400000000000000000	3410 00000000000000180000000000000000
2540 00000000000000000000000000240000	3430 000000000000000000000000000000018
2560 00000000024000000000000000000000	3450 00000000000180000000000000000000
2610 000000000000000000000000000002400	3470 0000000000000000000000000000180000
2630 00000000000240000000000000000000	3500 000000000000000000000000000000018
2650 00000000000000000000000002400000	3520 00000000000000180000000000000000
2670 00000002400000000000000000000000	3540 0000000000000000000000000000180000
2700 00000000000240000000000000000000	3560 00000000000180000000000000000000
2720 000000000000000000000000000002400	3610 00000000000000000000000000001800
2740 00000002400000000000000000000000	3630 00000000000018000000000000000000
2760 00000000000000000000000002400000	3650 000000000000000000000000000018000000
2890 00000024000000000000000000000000	3670 00000000180000000000000000000000
28B0 00000000000000000000000240000000	3700 00000000000018000000000000000000
28D0 00240000000000000000000000000000	3720 000000000000000000000000000001800
28F0 00000000000000000240000000000000	3740 00000000180000000000000000000000
2980 00000000000000000000000240000000	3760 0000000000000000000000000018000000
29A0 00000024000000000000000000000000	3890 00000018000000000000000000000000
29C0 00000000000000000240000000000000	38B0 0000000000000000000000001800000000
29E0 00240000000000000000000000000000	38D0 00180000000000000000000000000000
2A90 00000000000000000000240000000000	38F0 00000000000000000000180000000000
2AB0 00002400000000000000000000000000	3980 0000000000000000000000001800000000
2AD0 00000000000000024000000000000000	39A0 00000018000000000000000000000000
2AF0 24000000000000000000000000000000	39C0 00000000000000000000180000000000
2B80 00002400000000000000000000000000	39E0 00180000000000000000000000000000
2BA0 00000000000000000002400000000000	3A90 0000000000000000000000180000000000
2BC0 24000000000000000000000000000000	3AB0 00001800000000000000000000000000
2BE0 00000000000000024000000000000000	3AD0 00000000000000001800000000000000

FIGURE 7. Data pattern - Continued.

[illegible]

FIGURE 7. Data pattern - Continued.

ADD: 0 1 2 3 4 5 6 7 8 9 A B C D E F	ADD: 0 1 2 3 4 5 6 7 8 9 A B C D E F
5820 00000000240000000000000000000000	6790 0000000000000000000420000000000000
5840 00000000000000000000000000000002400	67B0 004200000000000000000000000000000000
5860 0000000000002400000000000000000000	67D0 000000000000000000000000042000000000
5880 0000000024000000000000000000000000	67F0 0000000420000000000000000000000000
5900 000000000000000000000000000240000000	6800 000000000000000000000000000420000000
5920 0000000000002400000000000000000000	6820 000000000420000000000000000000000000
5940 00000000000000000000000000000002400	6840 0000000000000000000000000000000004200
5960 00000000000000000000000000000002400	6860 000000000000042000000000000000000000
5A00 0000000000240000000000000000000000	6880 0000000004200000000000000000000000
5A20 0000000000000000000000000002400000	68A0 000000000000000000000000000420000000
5A40 0000000000000240000000000000000000	68C0 0000000000000000000000000000000000
5A60 0000000000000000000000000000000024	68E0 0000000000000000000000000000000004200
5A80 0000000000000000000000000002400000	68F0 0000000000000000000000000000000000
5B00 0000000002400000000000000000000000	6900 0000000000042000000000000000000000
5B20 0000000002400000000000000000000000	6920 000000000000000000000000000420000000
5B40 000000000000000000000000000000024	6940 000000000000000000000000000420000000
5B60 0000000000000000000000000000000000	6960 0000000000000420000000000000000000
5B80 0000000000024000000000000000000000	6980 0000000000000000000000000000000000
5BA0 00000000000000000000000000000002400	69A0 000000000000000000000000000420000000
5BC0 00000000000000000000000000000000024	69C0 000000000000000000000000000420000000
5BE0 0000000000000000000000000000000000	69E0 00000000000000000000000000000000042
5C00 00000000000000000000000000024000000	69F0 0000000000000000000000000000000000
5C20 0000000002400000000000000000000000	6A00 0000000000042000000000000000000000
5C40 0000000002400000000000000000000000	6A20 000000000000000000000000000004200000
5C60 0000000000000000000000000000000000	6A40 000000000000000420000000000000000000
5C80 0000000000000000000000000240000000	6A60 00000000000000000000000000000000042
5CA0 0000000024000000000000000000000000	6A80 000000000000000000000000000000000420000
5CC0 00000000000000000000000000000002400	6AA0 000000000000000000000000000000000000
5CE0 0000000000002400000000000000000000	6AC0 00000000000000000000000000000000042
5D00 0000000024000000000000000000000000	6AE0 000000000000000000000000000000000000
5D20 0000000000000000000000000240000000	6B00 0000000000000000000000000000042000000
5D40 0000000000000000000000000240000000	6B20 0000000000042000000000000000000000
5D60 0000000000000000000000000000000000	6B40 00000000000000000000000000000000042
5D80 0000000000000000000000000240000000	6B60 000000000000000004200000000000000000
5DA0 0000000000000000000000000240000000	6B80 0000000000000000000000000420000000
5DC0 0000000000024000000000000000000000	6BA0 0000000004200000000000000000000000
5DE0 000000000000000000000000000002400	6BC0 0000000000000000000000000000000004200
5E00 0000000000240000000000000000000000	6BE0 0000000000000420000000000000000000
5E20 0000000000000000000000000002400000	6BF0 0000000004200000000000000000000000
5E40 0000000000000000000000000000000000	6C00 000000000000000000000000000420000000
5E60 000000000000000000000000000000024	6C20 000000000000000000000000000420000000
5E80 0000000000000000000000000002400000	6C40 00000000000000000000000000000000042
5EA0 0000000000000000000000000000000000	6C60 0000000000000000000000000000000000
5EC0 0000000000000240000000000000000000	6C80 0000000000000000000000000420000000
5EE0 000000000000000000000000000000024	6CA0 0000000004200000000000000000000000
5F00 0000000000000000000000000002400000	6CC0 0000000000000000000000000000000004200
5F20 0000000002400000000000000000000000	6CE0 0000000000000420000000000000000000
5F40 0000000002400000000000000000000000	6D00 0000000004200000000000000000000000
5F60 0000000000000000000000000000000000	6D20 0000000000000000000000000000042000000
5F80 000000000000000000000000000000024	6D40 0000000000000000000000000000000000
5FA0 0000000000000000000000000000000000	6D60 0000000000000420000000000000000000
5FC0 0000000000000000000000000000000000	6D80 0000000000000000000000000000000004200
5FE0 0000000000000240000000000000000000	6DA0 0000000000000000000000000000000000
6000 0000000000000000042000000000000000	6DC0 0000000000000000000000000000000000
6020 4200000000000000000000000000000000	6DE0 00000000000000000000000000000000042
6040 000000000000000000000000042000000000	6DF0 0000000000000000000000000000000000
6060 0000420000000000000000000000000000	6E00 0000000000042000000000000000000000
6080 0000000000000000000000000000000000	6E20 00000000000000000000000000000000042
60A0 4200000000000000000000000000000000	6E40 0000000000000000000000000000000000
60C0 0000000000000000042000000000000000	6E60 0000000000000000000000000000000000
60E0 0000000000000000000000000000000000	6E80 0000000000000000000000000000000000
6100 0000000000000000042000000000000000	6EA0 000000000000000000000000000004200000
6120 0000000000000000000420000000000000	6EC0 0000000000000004200000000000000000
6140 0000000000000000000000000000000000	6EE0 00000000000000000000000000000000042
6160 0000420000000000000000000000000000	6EF0 000000000000000000000000000004200000
6180 0000000000000000000000000000000000	6F00 0000000000000000000000000000000000
61A0 000000000000000000000000042000000000	6F20 8100000000000000000000000000000000
61C0 0042000000000000000000000000000000	6F40 00000000000000000000000008100000000000
61E0 0000000000000000000000000000000000	6F60 0000810000000000000000000000000000
6200 0042000000000000000000000000000000	6F80 8100000000000000000000000000000000
6220 0000000000000000000420000000000000	6FA0 0000000000000000000000000000000000
6240 0000000420000000000000000000000000	6FC0 0000000000000000000810000000000000
6260 000000000000000000000000042000000000	6FE0 0000810000000000000000000000000000
6280 0000000000000000000042000000000000	6F00 0000000000000000000008100000000000
62A0 0042000000000000000000000000000000	6F20 0081000000000000000000000000000000
62C0 000000000000000000000000042000000000	6F40 0000000000000000000081000000000000
62E0 0000000000000000000000000000000000	6F60 0000008100000000000000000000000000
6300 0000000000000000000042000000000000	6F80 0000000000000000000000810000000000
6320 0042000000000000000000000000000000	6FA0 000000000000000000000000810000000000
6340 000000000000000000000000042000000000	6FC0 000000000000000000000000081000000000
6360 0000000000000000000000000000000000	6FE0 0000000000000000000000000000000000
6380 000000000000000000000000042000000000	6F00 0000000000000000000000000000000000
63A0 4200000000000000000000000000000000	6F20 0081000000000000000000000000000000
63C0 000000000000000000000000042000000000	6F40 000000000000000000000000081000000000
63E0 0000420000000000000000000000000000	6F60 0000000000000000000000000000000000
6400 0000000000000000000000000000000000	6F80 0000000000000000000000000000000000
6420 0000420000000000000000000000000000	6FA0 000000000000000000000000081000000000
6440 0000000000000000000000000000000000	6FC0 0000000000000000000000000000000000
6460 0000000000000000000000000000000000	6FE0 0000000000000000000000000000000000
6480 000000000000000000000000042000000000	6F00 0000000000000000000000000000000000
64A0 4200000000000000000000000000000000	6F20 0000000000000000000000000000000000
64C0 000000000000000000000000042000000000	6F40 0000008100000000000000000000000000
64E0 0000420000000000000000000000000000	6F60 0000000000000000000000000000000000
6500 0000000000000000000000000000000000	6F80 0000000000000000000000000000000000
6520 0000000000000000000000000000000000	6FA0 000000000000000000000000081000000000
6540 0000000000000000000000000000000000	6FC0 0000000000000000000000000000000000
6560 000000000000000000000000042000000000	6FE0 0000000000000000000000000000000000
6580 0000420000000000000000000000000000	6F00 00FF00FF00FF00FF00FF00FF00FF00FF00FF
65A0 0000000000000000000000000000000000	6F20 00FF00FF00FF00FF00FF00FF00FF00FF00FF
65C0 000000000000000000000000042000000000	6F40 00000000000000000000000008100000000000
65E0 0042000000000000000000000000000000	6F60 8100000000000000000000000000000000
6600 0000000000000000000000000000000000	6F80 000000000000000000000000081000000000
6620 000000000000000000000000042000000000	6FA0 0000000000000000000000000000000000
6640 0000000000000000000000000000000000	6FC0 0000000000000000000000000000000000
6660 0000000000000000000000000000000000	6FE0 0000000000000000000000000000000000
6680 0000000000000000000000000000000000	6F00 0000000000000000000000000000000000
66A0 000000000000000000000000042000000000	6F20 0000000000000000000000000000000000
66C0 0000000420000000000000000000000000	6F40 0000810000000000000000000000000000
66E0 000000000000000000000000042000000000	6F60 8100000000000000000000000000000000

FIGURE 7. Data pattern - Continued.

ADD: 0 1 2 3 4 5 6 7 8 9 A B C D E F	ADD: 0 1 2 3 4 5 6 7 8 9 A B C D E F
75B0 00000000000000000000000000000000	7A40 00000000000000000000000000000000
75D0 00000000000000000000000000000000	7A60 00000000000000000000000000000000
75F0 00000000000000000000000000000000	7B10 00000000000000000000000000000000
7680 00000000000000000000000000000000	7B30 00000000000000000000000000000000
76A0 00000000000000000000000000000000	7B50 00000000000000000000000000000000
76C0 00000000000000000000000000000000	7B70 00000000000000000000000000000000
76E0 00000000000000000000000000000000	7C80 00000000000000000000000000000000
7790 00000000000000000000000000000000	7CA0 00000000000000000000000000000000
77B0 00000000000000000000000000000000	7CC0 00000000000000000000000000000000
77D0 00000000000000000000000000000000	7CE0 00000000000000000000000000000000
77E0 FF00FF00FF00FF00FF00FF00FF00FF00FF	7D90 00000000000000000000000000000000
77F0 00FF00FF00FF00FF00FF00FF00FF00FF00	7DB0 00000000000000000000000000000000
7800 00000000000000000000000000000000	7DD0 00000000000000000000000000000000
7820 00000000000000000000000000000000	7DF0 00000000000000000000000000000000
7840 00000000000000000000000000000000	7E80 00000000000000000000000000000000
7860 00000000000000000000000000000000	7EAO 00000000000000000000000000000000
7910 00000000000000000000000000000000	7EC0 00000000000000000000000000000000
7930 00000000000000000000000000000000	7EE0 00000000000000000000000000000000
7950 00000000000000000000000000000000	7F90 00000000000000000000000000000000
7970 00000000000000000000000000000000	7FB0 00000000000000000000000000000000
7A00 00000000000000000000000000000000	7FD0 00000000000000000000000000000000
7A20 00000000000000000000000000000000	7FF0 00000000000000000000000000000000

NOTES:

1. The device shall be programmed with all zeros except for the address locations identified in the pattern list.

FIGURE 7. Data pattern - Continued.

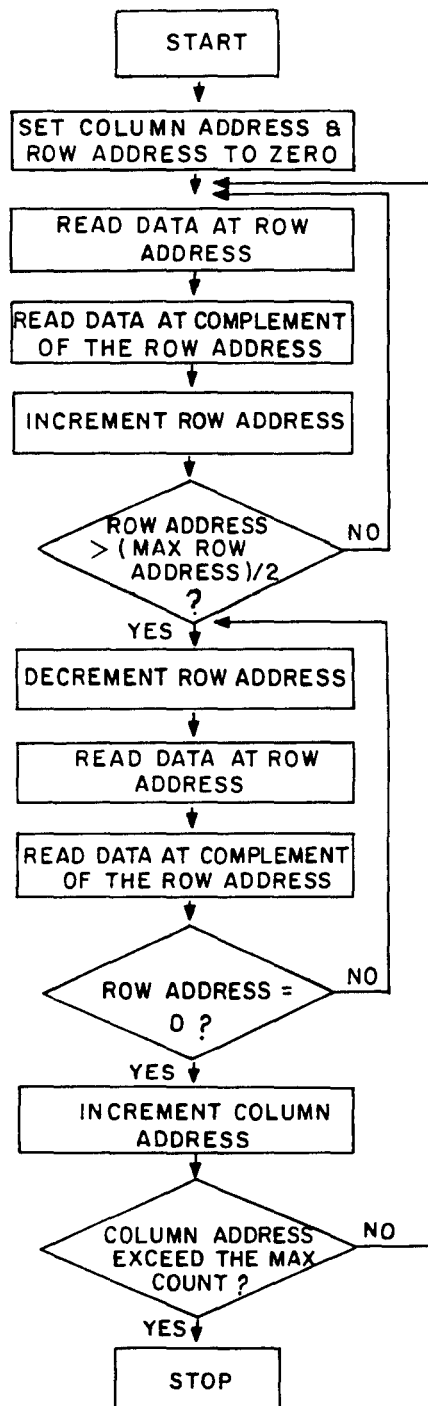


FIGURE 8. Row complement test.

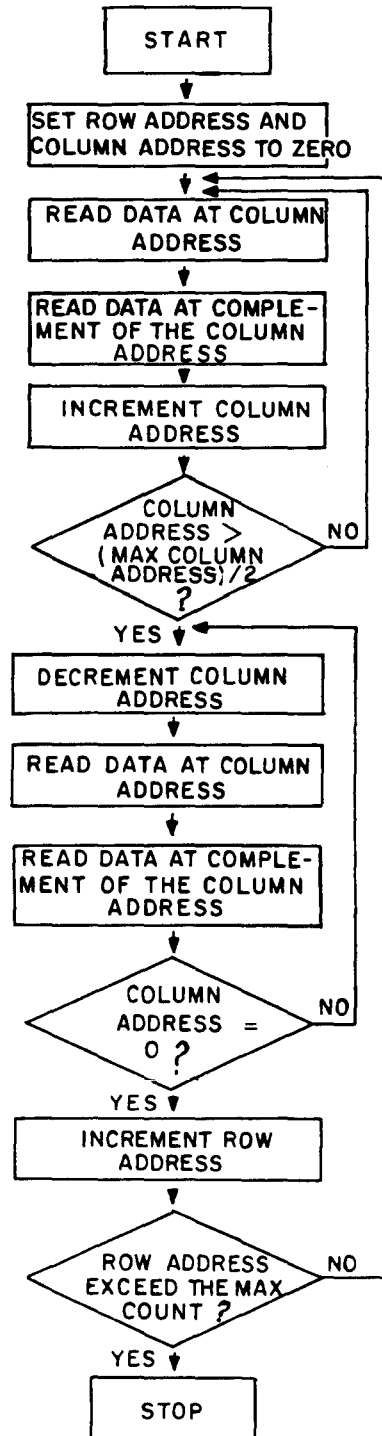


FIGURE 9. Column complement test.

A.C. TESTING LOAD CIRCUIT

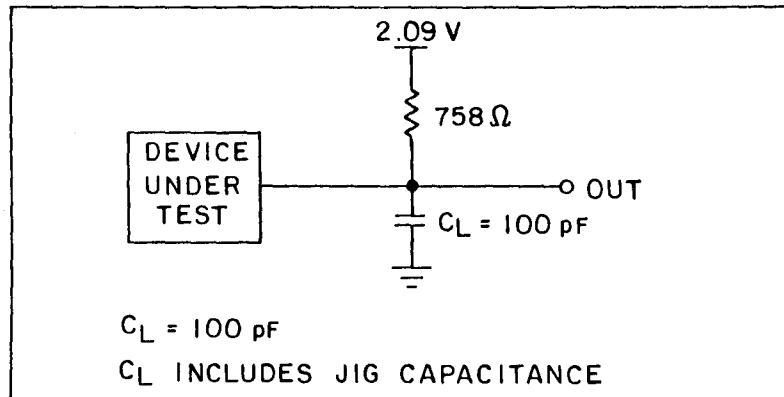


FIGURE 10. Load circuit.

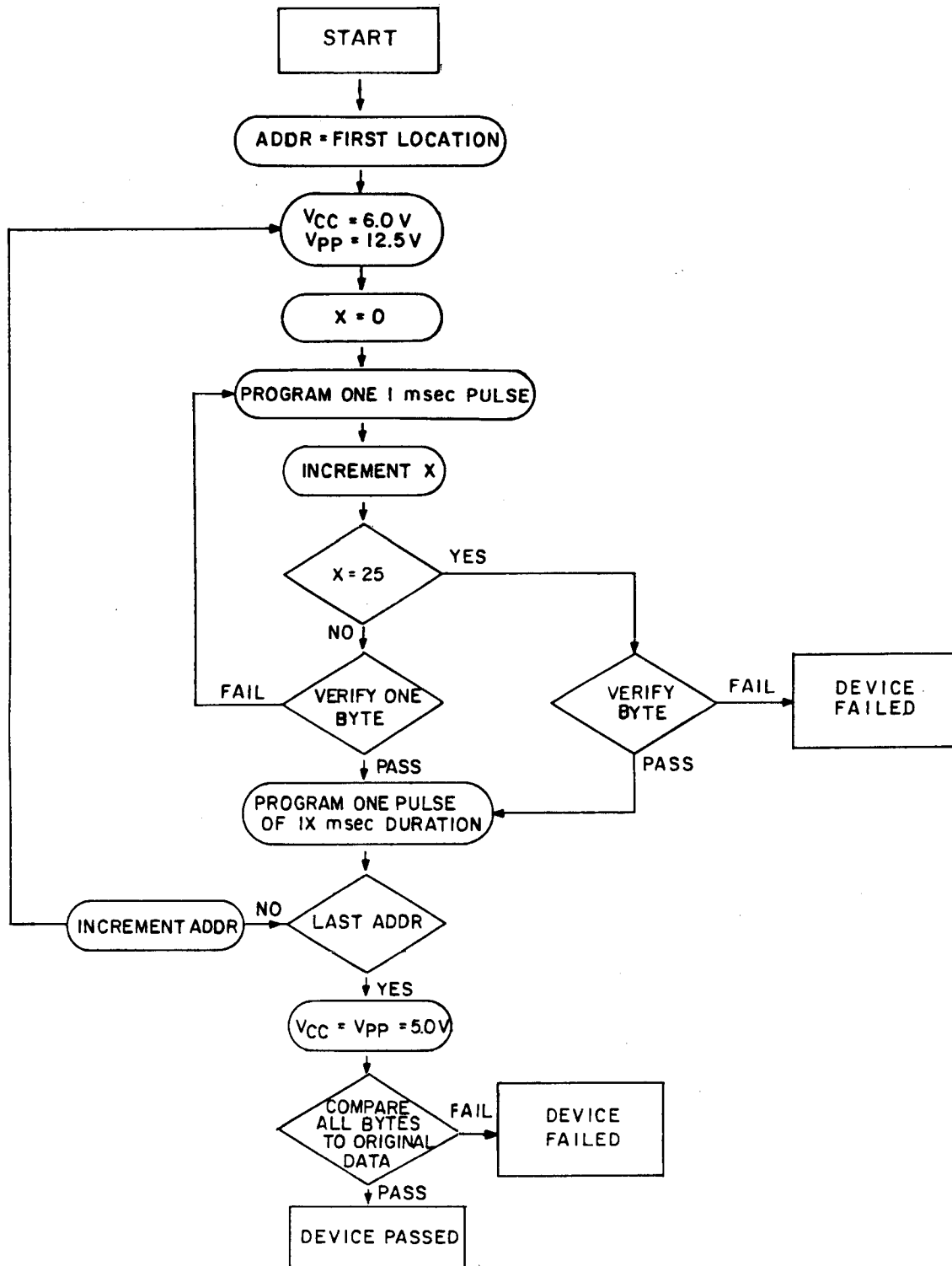


FIGURE 11. Programming flowchart.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special lead lengths, or lead forming, if applicable. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.
- h. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

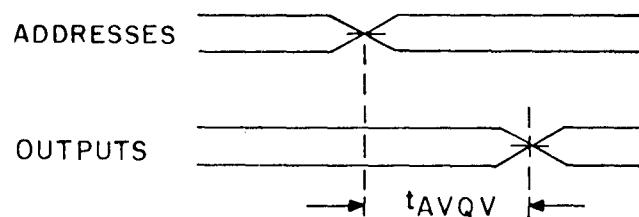
V_{CC} - - - - -	Supply voltage. Voltage values are with respect to ground, unless otherwise specified, throughout this detail specification.
V_{PP} - - - - -	Program supply voltage.
$A_0 - A_{14}$ - - - - -	Address inputs, used to address 1 of 32,768/8 bit locations in static storage array.
$\overline{CE}$ - - - - -	Chip-enable, used along with the output enable (OE) signal to control the state of the data-out terminals.
$\overline{OE}$ - - - - -	Output-enable, used to control the data-out terminals.
$00 - 07$ - - - - -	Data input-output, 8 bit wide data bus through which data is stored or accessed.
I_{CC} - - - - -	Supply current.
I_{PP} - - - - -	V_{PP} current.
I_{IH}, I_{IL} - - - - -	Input leakage currents.
I_{OHZ} - - - - -	High impedance output leakage currents.
V_{IL} - - - - -	Logical low input voltage.
V_{IH} - - - - -	Logical high input voltage.
V_{OL} - - - - -	Logical low output voltage.
V_{OH} - - - - -	Logical high output voltage.
C_i - - - - -	Input capacitance.
C_o - - - - -	Output capacitance.
t_{AVQV} - - - - -	Address access time.
t_{ELQV} - - - - -	Chip-enable access time.
t_{OLQV} - - - - -	Output-enable access time.
t_{AXQX} - - - - -	Address to data invalid.
t_{AVEL} - - - - -	Address setup time.
t_{OHAX} - - - - -	Address hold time.
t_{OHQZ} - - - - -	Output-enable high to output float.
t_{DVEL} - - - - -	Data to CE setup time.
t_{EHDZ} - - - - -	Data hold time.
t_{ELEH} - - - - -	Program pulse width.
t_{VHEL} - - - - -	V_{PP} setup time.
t_{EHQZ} - - - - -	Chip enable high to output float.
t_{PHEL} - - - - -	V_{CC} setup time.
t_{DZOL} - - - - -	Output enable setup time.

6.3.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always t and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transition. Thus the format is:

		t	X	X	X	X
Signal name from which interval is defined	_____					
Transition direction for first signal	_____					
Signal name to which interval is defined	_____					
Transition direction for second signal	_____					

- a. A = Address
 D = Data in
 Q = Data out
 E = Chip-enable
 O = Output-enable
 P = V_{CC}
 V = V_{pp}
- b. H = Transition to high
 L = Transition to low
 V = Transition to valid
 X = Transition to invalid or don't care
 Z = Transition to off (high impedance)

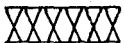
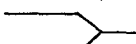
Example:



The example shows access time defined at t_{AVQV} time from address valid to output valid.

- c. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

d.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DONT CARE: ANY CHANGE PERMITTED	CHANGING/ STATE UNKNOWN
	—	HIGH IMPEDANCE

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Handling. MOS devices shall be handled with certain precautions to avoid damage due to accumulation of static charge. Input protective devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment and tools.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS area.
- f. Maintain relative humidity above 50 percent, if practical.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	27256-250
02	27256-200
03	27256-170

Custodians:

Army - ER
Navy - EC
Air Force - 17

Review activities:

Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC
DLA - ES

Preparing activity:

Air Force - 17

Agent:

DLA - ES

(Project 5962-0883)