

MICROCIRCUITS, DIGITAL, 4096 BIT, CMOS,
ULTRAVIOLET ERASABLE, PROGRAMMABLE READ-ONLY
MEMORY (EPROM), MONOLITHIC SILICON

1. SCOPE

1.2 Part number. The part number shall be in accordance with MIL-M-38510. The "JAN" or "J" certification mark shall not be used.

1.2.1 Device type. The device type shall be as follows:

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

1.3 Absolute maximum ratings:

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ For absolute maximum ratings, voltage values are with respect to ground, unless otherwise specified. Throughout the remainder of this detail specification, voltage values are with respect to ground.

FSC 5962

1.4 Recommended operating conditions.

Supply voltage, V_{CC} - - - - - +4.5 to +5.5 V
 Minimum high-level input voltage, V_{IH} - - - - - 2.5 V
 Maximum low-level input voltage, V_{IL} - - - - - 0.8 V
 High-level program input voltage, $V_{IH}(PRG)$ - - - 38 to 42 V
 Case operating temperature range - - - - - -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications, standards, and handbooks, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards (DoDISS) specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification For

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Function table.

3.2.2.1 Programmed devices. The requirements for supplying programmed devices are not part of this specification. The function table for programmed devices is shown on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with MIL-M-38510 and 1.2.3 herein.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/ $T_C = -55^\circ$ to $+125^\circ C$	Limits		Unit
			Min	Max	
High-level input voltage	V_{IH}	$V_{DD} = 4.5$ to 5.5 V $\bar{E}_1, S$	2.5		V
		$V_{DD} = 4.5$ to 5.5 V All addresses	2.7		V
Low-level input voltage	V_{IL}	$V_{DD} = 4.5$ to 5.5 V All inputs $\bar{E}_1, S$ all addresses		0.8	V
Input leakage current (any input)	I_{IH}	$V_{IN} = 5.5$ V, $V_{DD} = 5.5$ V		+1.0	μA
	I_{IL}	$V_{DD} = 5.5$ V, $V_{IN} = 0$ V	-1.0		μA
High-level output voltage	V_{OH1}	$I_{OH} = -0.2$ mA, $V_{CC} = 4.5$ V	2.4		V
	V_{OH2}	$I_{OUT} = 0$, $V_{CC} = 4.5$ V	4.49		V
Low-level output voltage	V_{OL1}	$I_{OL} = 2.0$ mA, $V_{CC} = 5.5$ V		0.45	V
	V_{OL2}	$I_{OUT} = 0$, $V_{CC} = 5.5$ V		GND + 0.01	V
Output leakage 3/	I_{OZH}	$V_{OUT} = 5.5$ V, $\bar{E}_1 = V_{IH}$ $V_{CC} = 5.5$ V		+1.0	μA
	I_{OZL}	$\bar{E}_1 = V_{IH}$, $V_{OUT} = 0$ V $V_{CC} = 5.5$ V	-1.0		μA
Supply current (standby)	I_{DDSB}	$V_{IN} = 5.5$ V, $V_{DD} = 5.5$ V		100	μA
	I_{CCSB}	$V_{IN} = 5.5$ V, $V_{CC} = 5.5$ V		40	μA
Supply current (operating)	I_{DDOP}	$f = 1$ MHz, $(I_{DD} + I_{CC})$ $V_{DD} = 5.5$ V		6	mA
Input capacitance	C_i	$V_R = 0$ V		7.0	pF
Output capacitance	C_o	$V_R = 0$ V		10.0	pF
Access time from $\bar{E}_1$	TE1LQV	See figure 4		600	ns
Output enable time from $\bar{S}$	TSLQV	See figure 4		150	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions ^{2/} $T_C = -55^\circ$ to $+125^\circ\text{C}$	Limits		Unit
			Min	Max	
Output disable time from $\bar{E}_1$	TE1HQZ	See figure 4		150	ns
$\bar{E}_1$ pulse width (positive)	TE1HE1L	See figure 4	150		ns
$\bar{E}_1$ pulse width (negative)	TE1LE1H	See figure 4	600		ns
Address setup time	TAVE1L	See figure 4	0		ns
Address hold time from $\bar{E}_1$	TE1LAX	See figure 4		100	ns
Chip enable setup time	TE2VE1L	See figure 4	0		ns
Chip enable hold time	TE1LE2X	See figure 4		100	ns

1/ DC and read mode. $V_{CC} = V_{DD}$.

2/ See table III for exact pin test conditions.

3/ Connect all address inputs and the $\bar{S}_1$ input to V_{IH} and measure I_{OZH} and I_{OZL} with the output under test connected through a current meter to the voltage specified.

4/ V_{pp} may be directly connected to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{pp} .

3.5 Electrical test requirements. Electrical test requirements shall be as specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container. The "JAN" or "J" certification mark shall not be used.

3.7 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.7.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.7.

3.7.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6 and table IV.

3.7.3 Verification of erasure or programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)
	Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7*,9
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Group C end-point electrical parameters (method 5005)	1,2,3,7,8
Additional electrical subgroups for group C periodic inspection	None
Group D end-point electrical parameters (method 5005)	1,2,3,7,8

Notes:

1. (*) PDA applies to subgroup 1 and 7 (see 4.2c).
2. Any or all subgroups may be combined when using high-speed testers.
3. Subgroup 7 and 8 shall consist of verifying the binary count pattern.
4. For all electrical tests, the device shall be programmed to the pattern specified.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

3.9 Manufacturer eligibility. To be eligible to supply microcircuits to this specification a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line, not necessarily the line producing the device type described herein.

3.10 Certification. Certification in accordance with MIL-M-38510 is not required for this device.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following conditional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883). Test condition D or E, using the circuits shown on figure 5, or equivalent.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

- c. The percent defective allowable (PDA) for class B devices shall be 10 percent based on failures from group A, subgroups 1 and 7, test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroups 1 and 7, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.
- d. A programmability test shall be performed when programming the devices using a LTPD of 10.
- e. A bit retention test shall be performed prior to burn-in and shall consist of the following:
 - (1) Program all devices with the complement of the binary count pattern (see 3.7.2 and 4.2d).
 - (2) Verify pattern (see 3.7.3).
 - (3) Remove all device terminal connections (including supply voltages).
 - (4) Perform a high temperature storage for 48 hours at 150°C.
 - (5) Restore device terminal connections.
 - (6) Verify pattern (see 3.7.3).
 - (7) Erase the pattern and program, devices with a binary count pattern (see 3.7.2).
 - (8) Verify pattern (see 3.7.3).
 - (9) Burn-in (see 4.2a).
 - (10) Verify pattern (see 3.7.3) at 25°C, and at 125°C.
- f. After completion of all testing, the devices shall be erased and verified prior to delivery (except devices submitted for groups A, B, C, and D testing).

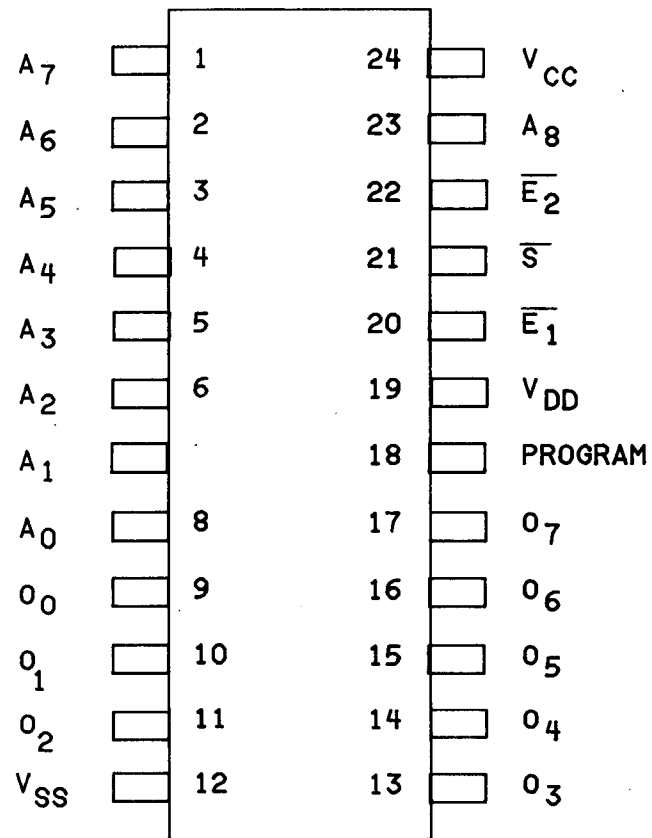
4.3 Qualification inspection. Qualification inspection is not required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Generic test data may be used to satisfy the requirements for group C and D inspections (see 6.7).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups B, C, and D testing).

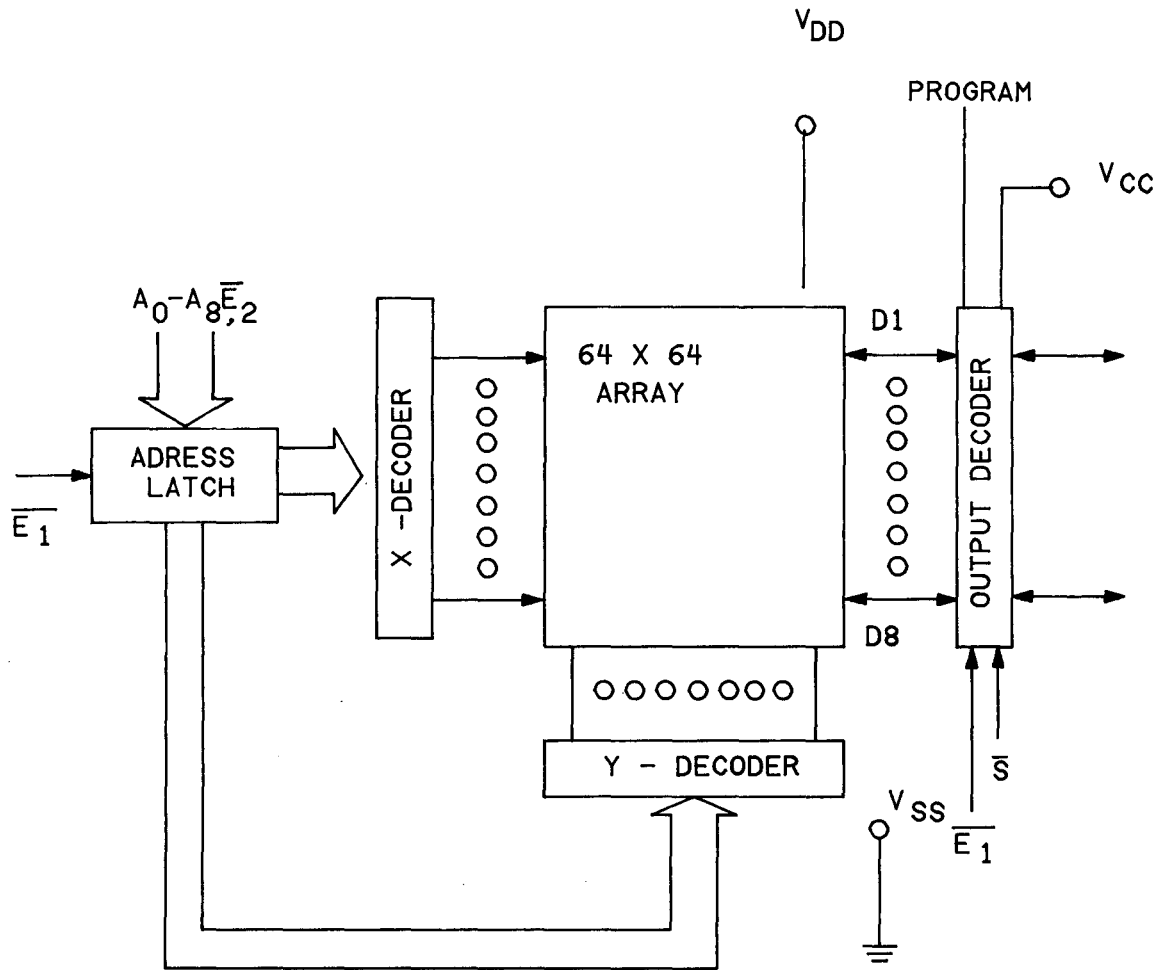
CASE J

FIGURE 1. Terminal connections.

TIME REF	$\overline{E1}$	$\overline{E2}^*$	S	A	OUTPUTS Q	NOTES
-1	H	X	X	X	Z	DEVICE INACTIVE
0		L	X	V	Z	CYCLE BEGINS; ADDRESSES, $\overline{E2}$ LATCHED*
1	L	X	X	X	Z	INTERNAL OPERATIONS ONLY
2	L	X	L	X	A	OUTPUTS ACTIVE UNDER CONTROL OF $\overline{E1}$, $\overline{S}$
3	L	X	L	X	V	OUTPUTS VALID AFTER ACCESS TIME
4		X	L	X	V	READ COMPLETE
5	H	X	X	X	Z	CYCLE ENDS (SAME AS -1)

NOTE, SEE FIGURE 4 FOR TIME REF.

FIGURE 2. Function table.

FIGURE 3. Function block diagram.

READ CYCLE TIMING

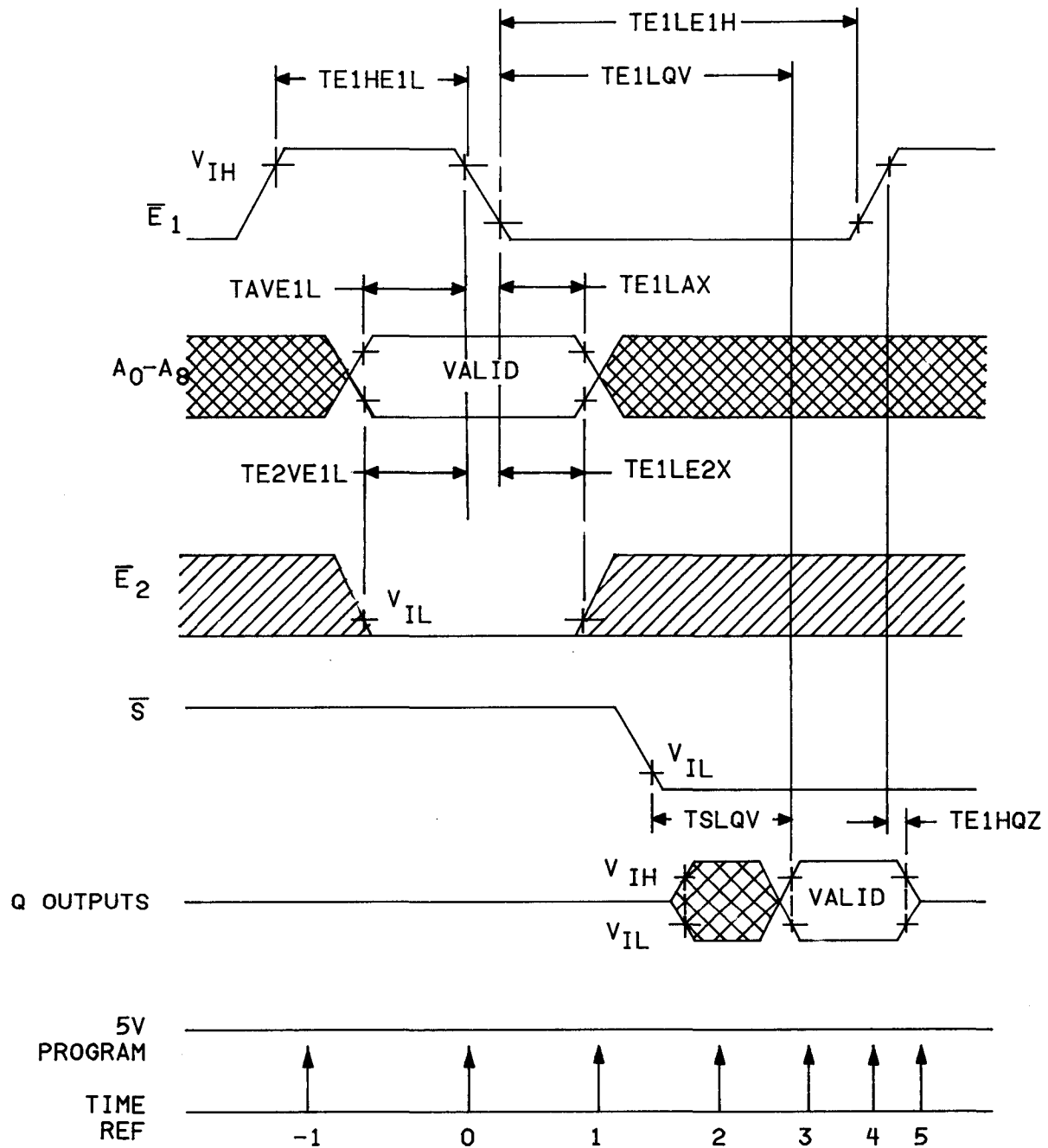
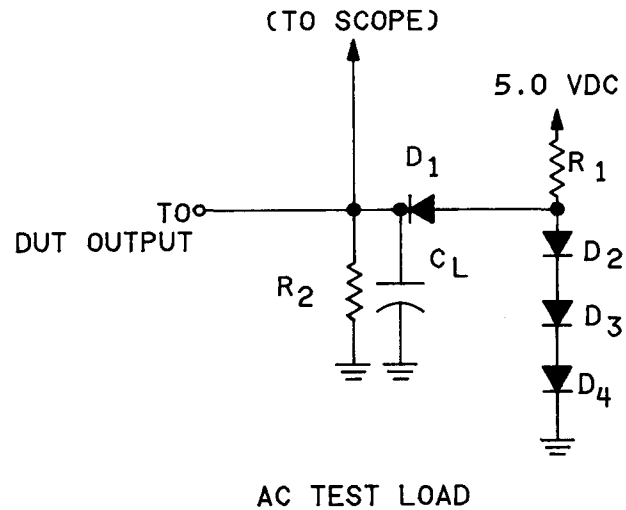


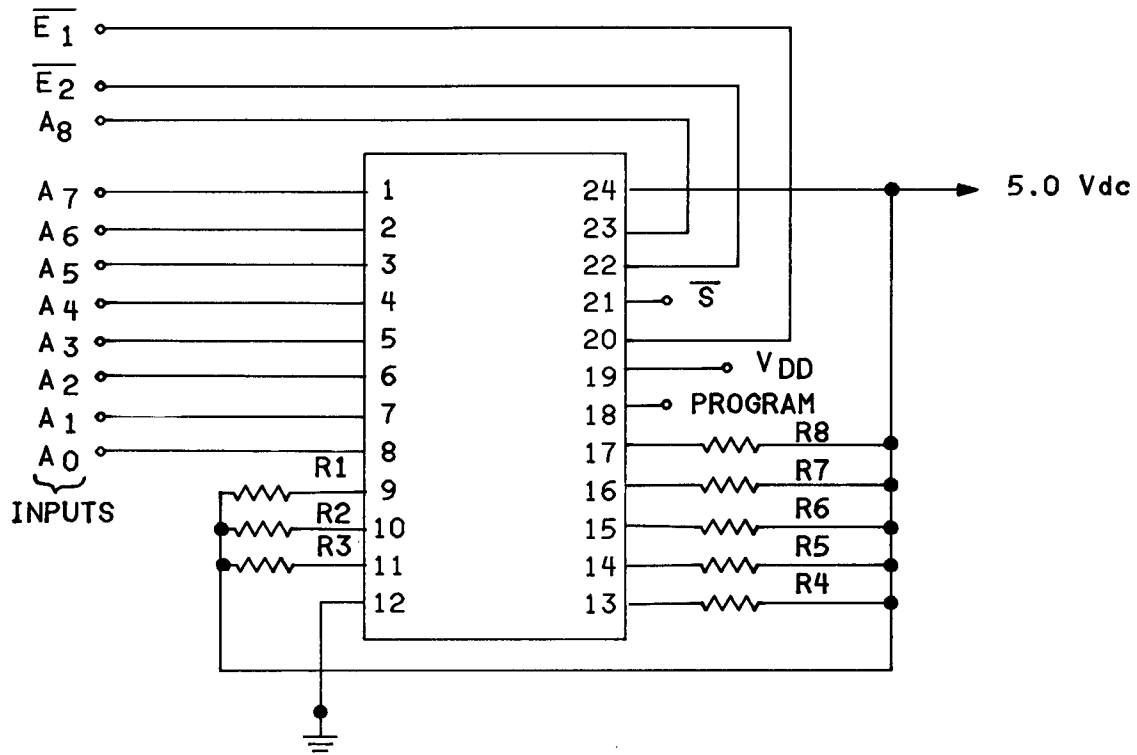
FIGURE 4. Propagation delay time test circuit and waveforms.



NOTES:

1. $C_L = 50$ pF includes jig and probe capacitance.
2. Input rise and fall times ≤ 20 ns.
3. Input pulse levels 0.8 V to 2.5 V.
4. Timing measurement reference levels: Inputs V_{IH} and V_{IL} , Outputs 8.0 V and 2.0 V.
5. $R_1 = 2.0$ k Ω $\pm 5\%$; $R_2 = 12$ k Ω $\pm 5\%$.
 $D_1 =$ MMD6150 or equivalent.
 $D_2, D_3, D_4 =$ MMD7000 or equivalent.

FIGURE 4. Propagation delay time test circuit and waveforms - Continued.



NOTES:

1. R1 thru R8 = $3.6\text{ k}\Omega \pm 5\%$ when $\overline{S}$ input is pulsed
 $= 1.0\text{ k}\Omega \pm 5\%$ when S is at $V_{IH} \geq 2.5\text{ V}$.
2. Input signal characteristics: Amplitude: $V_{IH} \geq 2.5\text{ V}$, $V_{IL} \leq 0.8\text{ V}$;
Duty Cycle = 75%; $t_{THL} \leq 100\text{ Ms}$ and the following PRR ($\pm 20\%$).

Input	PRR	Input	PRR
	$16\text{ kHz} \leq F_1 \leq 100\text{ kHz}$	A ₅	$F_0 \div 32$
	($F_0 = \text{FF output}$)	A ₆	$F_0 \div 64$
A ₀	$F_0 = F_1 \div 2$	A ₇	$F_0 \div 128$
A ₁	$F_0 \div 2$	A ₈	$F_0 \div 256$
A ₂	$F_0 \div 4$	$\overline{E}_2$	GND
A ₃	$F_0 \div 8$	$\overline{E}_1$	F_1
A ₄	$F_0 \div 16$	PROGRAM	GND
		$\overline{S}$	GND

FIGURE 5. Burn-in and steady state life test circuit.

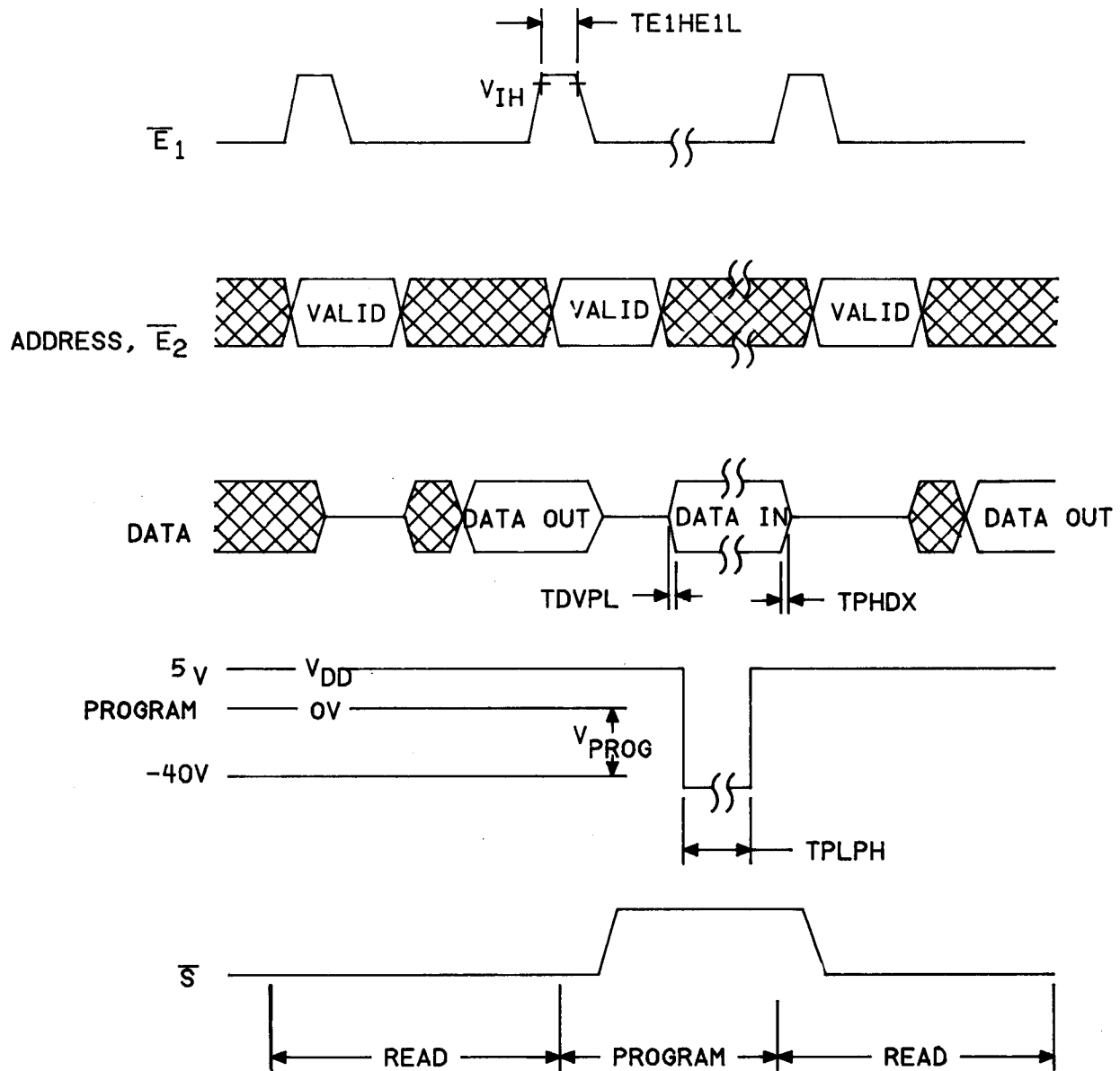


FIGURE 6. Programming waveforms.

TABLE III. Group A

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13		
				A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	O ₀	O ₁	O ₂	V _{SS}	O ₃		
1 T _C = 25°C	V _{OH1}	3006	1	1/	1/	1/	1/	1/	1/	1/	1/	-0.2 mA				GND		
			2										-0.2 mA					
			3											-0.2 mA				
			4														-0.2 mA	
			5															
			6															
			7															
			8															
	V _{OH2}		9										0.0 mA					
			10											0.0 mA				
			11												0.0 mA			
			12															0.0 mA
			13															
			14															
			15															
			16	↓	↓	↓	↓	↓	↓	↓	↓	↓						
	V _{OL1}	3007	17	2/	2/	2/	2/	2/	2/	2/	2/	2.0 mA						
			18										2.0 mA					
			19											2.0 mA				
			20														2.0 mA	
			21															
			22															
			23															
			24															
	V _{OL2}		25										0.0 mA					
			26											0.0 mA				
			27												0.0 mA			
			28														0.0 mA	
			29															
			30															
			31															
			32	↓	↓	↓	↓	↓	↓	↓	↓	↓					↓	

See footnotes at end of table III.

inspection.

Test no.	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		
	0 ₄	0 ₅	0 ₆	0 ₇	PGM	V _{DD}	$\bar{E}_1$	$\bar{S}$	$\bar{E}_2$	A ₈	V _{CC}		Min	Max	Unit
1					2.7 V	4.5 V	0.8 V	0.8 V	0.8 V	$\frac{1}{2}$	4.5 V	0 ₀	2.4		V
2												0 ₁			
3												0 ₂			
4												0 ₃			
5	-0.2 mA											0 ₄			
6		-0.2 mA										0 ₅			
7			-0.2 mA									0 ₆			
8				-0.2 mA								0 ₇			
9												0 ₀	4.49		
10												0 ₁			
11												0 ₂			
12												0 ₃			
13	0.0 mA											0 ₄			
14		0.0 mA										0 ₅			
15			0.0 mA									0 ₆			
16				0.0 mA								0 ₇			
17						5.5 V				$\frac{2}{2}$	5.5 V	0 ₀		0.45	
18												0 ₁			
19												0 ₂			
20												0 ₃			
21	2.0 mA											0 ₄			
22		2.0 mA										0 ₅			
23			2.0 mA									0 ₆			
24				2.0 mA								0 ₇			
25												0 ₀		0.01	
26												0 ₁			
27												0 ₂			
28												0 ₃			
29	0.0 mA											0 ₄			
30		0.0 mA										0 ₅			
31			0.0 mA									0 ₆			
32				0.0 mA								0 ₇			

TABLE III. Group A

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13
				A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	O ₀	O ₁	O ₂	V _{SS}	O ₃
$T_C = 25^\circ\text{C}$ ↓	I_{IH} ↓	3010	33	5.5 V											GND	
			34		5.5 V											
			35			5.5 V										
			36				5.5 V									
			37					5.5 V								
			38						5.5 V							
			39							5.5 V						
			40								5.5 V					
			41													
			42													
			43													
			44													
			45													
	I_{IL} ↓		46	0.0 V												
			47		0.0 V											
			48			0.0 V										
			49				0.0 V									
			50					0.0 V								
			51						0.0 V							
			52							0.0 V						
			53								0.0 V					
			54													
			55													
			56													
			57													
			58													
	I_{OZH} ↓		59									5.5 V				
			60										5.5 V			
			61											5.5 V		
			62													5.5 V
			63													
			64													
			65													
			66													

See footnotes at end of table III.

inspection - Continued.

Test no.	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		
	0 ₄	0 ₅	0 ₆	0 ₇	PGM	V _{DD}	E ₁	S	E ₂	A ₈	V _{CC}		Min	Max	Unit
33						5.5 V					5.5 V	A ₇		1.0	μA
34												A ₆			
35												A ₅			
36												A ₄			
37												A ₃			
38												A ₂			
39												A ₁			
40												A ₀			
41										5.5 V		A ₈			
42									5.5 V			E ₂			
43								5.5 V				S			
44							5.5 V					E ₁			
45					5.5 V							PGM			
46												A ₇	-1.0		
47												A ₆			
48												A ₅			
49												A ₄			
50												A ₃			
51												A ₂			
52												A ₁			
53												A ₀			
54										0.0 V		A ₈			
55									0.0 V			E ₂			
56								0.0 V				S			
57							0.0 V					E ₁			
58					0.0 V							PGM			
59							2.7 V					0 ₀		1.0	
60												0 ₁			
61												0 ₂			
62												0 ₃			
63	5.5 V											0 ₄			
64		5.5 V										0 ₅			
65			5.5 V									0 ₆			
66				5.5 V								0 ₇			

TABLE III. Group A

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13
				A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	O ₀	O ₁	O ₂	V _{SS}	O ₃
1 T _C = 25°C	I _{OZL}		67									0.0 V			GND	
			68										0.0 V			
			69											0.0 V		
			70													0.0 V
			71													
			72													
			73													
			74													
	I _{CCSB}	3005	75	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V					
			76								0.0 V					
			77							0.0 V						
			78						0.0 V							
			79					0.0 V								
			80				0.0 V									
			81			0.0 V										
			82		0.0 V											
	C _i 3/	3012	83	0.0 V												
			84													
			85													
			86													
			87													
			88								0.0 V					
			89									0.0 V				
			90										0.0 V			
	C _o 3/		91													0.0 V
			92													
			93													
			94													
			95													
			96	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V				GND	
			97	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V				GND	
	I _{DDSB}		96	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V				GND	
	I _{DDOP}		97	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V				GND	

See footnotes at end of table III.

inspection - Continued.

Test no.	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		
	0 ₄	0 ₅	0 ₆	0 ₇	PGM	V _{DD}	E ₁	S	E ₂	A ₈	V _{CC}		Min	Max	Unit
67						5.5 V	2.7 V				5.5 V	0 ₀	-1.0	1.0	μA
68						↓	↓				↓	0 ₁	↓	↓	↓
69						↓	↓				↓	0 ₂	↓	↓	↓
70						↓	↓				↓	0 ₃	↓	↓	↓
71	0.0 V					↓	↓				↓	0 ₄	↓	↓	↓
72		0.0 V				↓	↓				↓	0 ₅	↓	↓	↓
73			0.0 V			↓	↓				↓	0 ₆	↓	↓	↓
74				0.0 V		↓	↓				↓	0 ₇	↓	↓	↓
75						↓	0.0 V				↓	V _{CC}		40	↓
76												A ₀		7.0	pF
77												A ₁		↓	↓
78												A ₂		↓	↓
79												A ₃		↓	↓
80												A ₄		↓	↓
81												A ₅		↓	↓
82												A ₆		↓	↓
83												A ₇		↓	↓
84										0.0 V		A ₈		↓	↓
85									0.0 V			E ₂		↓	↓
86								0.0 V				S		↓	↓
87							0.0 V					E ₁		↓	↓
88												0 ₀		10.0	↓
89												0 ₁		↓	↓
90												0 ₂		↓	↓
91												0 ₃		↓	↓
92	0.0 V											0 ₄		↓	↓
93		0.0 V										0 ₅		↓	↓
94			0.0 V									0 ₆		↓	↓
95				0.0 V								0 ₇		↓	↓
96						5.5 V	2.7 V		GND	5.5 V	5.5 V	V _{DD}		100	μA
97						5.5 V	0.0 V	0.0 V	GND	5.5 V	5.5 V	V _{DD}		6	mA

TABLE III. Group A

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13
				A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	O ₀	O ₁	O ₂	V _{SS}	O ₃
2	Same tests, terminal conditions, and limits as in subgroup 1 except T _C = 125°C and test numbers 76 through 95.															
3	Same tests, terminal conditions, and limits as in subgroup 1 except T _C = -55°C and test numbers 76 through 95.															
7	Functional tests	98		4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/
8	Same tests, terminal conditions, and limits as in subgroup 7 except T _C = 125°C and T _C = -55°C.															
9 T _C = 25°C	TE1LQV	Fig. 4	99	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	GND	5/
	TSLQV		100													
	TE1HQZ		101													
	TE1HE1L		102													
	TE1LE1H		103													
	TAVE1L		104													
	TE1LAX		105													
	TE2VE1L		106													
	TE1LE2X		107	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
10	Same tests, terminal conditions, and limits as in subgroup 9 except T _C = +125°C.															
11	Same tests, terminal conditions, and limits as in subgroup 9 except T _C = -55°C.															

1/ Before performing electrical tests, a binary count pattern shall be programmed into the devices submitted for acceptance. V_{IH} = 2.7 V minimum shall be applied to the applicable address pins to set the measured terminal in the proper state for measurement.

2/ V_{IL} = 0.8 V maximum.

3/ Capacitance shall be measured with a suitable instrument that allows approximately 0 V bias and the ac measurement signal shall be small enough to not forward bias the diode and cause erroneous readings.

4/ Tests shall verify binary count pattern. All bits shall be tested with the following conditions:

- V_{CC} = 5.5 V and repeat with V_{CC} = 4.5 V.
- Inputs: V_{IH} = 2.5 V = E₁ = S₁ and Address inputs = 2.7 V.
- Outputs: Output voltage shall be either
 - H = 2.4 V minimum and L = 0.45 V maximum when using a high speed checker double comparator
 - H ≥ 1.0 V and L ≤ 1.0 V when using a high speed checker single comparator

5/ Each output shall be connected to the load circuit shown on figure 4 and propagation delay times shall be measured as follows:

- Condition address inputs A₀ thru A₇ to set outputs under test to the "L" and other test to "H".
- Address inputs to outputs.

6/ See table I herein for supply voltages and test limits.

inspection - Continued.

Test no.	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		
	0 ₄	0 ₅	0 ₆	0 ₇	PGM	V _{DD}	$\overline{E}_1$	$\overline{S}$	$\overline{E}_2$	A ₈	V _{CC}		Min	Max	Unit
98	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	All outputs	4/	4/	
99	5/	5/	5/	5/	5/	5/	6/	6/	GND	5/	6/	All outputs		600	ns
100														150	
101														150	
102													150		
103													600		
104													0		
105														100	
106													0		
107	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓		100	↓

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

- a. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).
- b. A special subgroup shall be added using a LTPD of 15 for class B. This subgroup shall consist of a high voltage test of the input protection circuits, VZAP (see 4.9).

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical test parameters shall be as specified in table II herein.
- b. Steady state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, using the circuit shown on figure 5, or equivalent.
 - (2) $T_C = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1000 hours, except as permitted by appendix B of MIL-M-38510, and method 1005 of MIL-STD-883.
 - (4) All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).
- c. A reprogrammability test shall be added to group C inspection prior to performing the steady state life test (see 4.4.3b). The devices to be submitted to the steady state life testing shall be subjected to the following tests and examinations:
 - (1) Each device in the sample shall be subjected to a minimum of 50 program and erase cycles. Each cycle shall consist of the following steps.
 - (a) Program all devices with a binary count pattern.
 - (b) Verify pattern (see 3.7.3).
 - (c) Erase (see 3.7.1).
 - (d) Verify pattern (see 3.7.3).

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Programming procedure. The following procedures shall be followed when programming and verification testing is performed. The waveforms and timing relationships shown on figure 6 and the test conditions and limits specified in table IV shall be adhered to.

- a. Initially, and after erasure, all bits are in the "H" state (output high). Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet erasure.
- b. In the program mode, V_{CC} and V_{DD} are tied together to the normal operating supply. High logic levels at all of the appropriate chip inputs and outputs must be set at $V_{DD} - 2$ V minimum. Low logic levels must be set at $V_{SS} + 0.8$ V maximum. Addressing of the desired location in PROGRAM mode is done as in READ mode. Address and data lines are set at the desired logic levels, and PROGRAM and chip select ($\bar{S}$) pins are set high. The address is latched by the downward edge on the strobe line ($\bar{E}_1$). During valid DATA IN time, the PROGRAM pin is pulsed from V_{DD} to -40 V. This pulse initiates the programming of the device to the levels set on the data outputs. Duty cycle limitations are specified from chip heat dissipation considerations. Pulse rise and fall times shall not be faster than $5 \mu s$.
- c. During programming, the power supply should be capable of limiting peak instantaneous current to 100 mA.
- d. The programming pin is driven from V_{DD} to -40 V (± 2 V) by pulses of 20 milliseconds duration. Program the same location a maximum of five times. Pulse rise and fall times of 10 microseconds are recommended. Note that any individual location may be programmed at any time.
- e. Addresses and data should be presented to the device within the recommended setup/hold time and high/low logic level margins.
- f. A verify should be performed on the programmed bit to determine that the bit was correctly programmed. Repeat steps a through d for all other bit locations to be programmed.
- g. Reverify all bit locations.
- h. Any bit that does not verify as in proper state shall be a reject.

4.7 Erasing procedure. The device may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of $2537\text{\AA}$. The recommended integrated dose i.e., (UV intensity x exposure time) is 10 W s/cm^2 . The lamps should be used without short-wave filters, and the device to be erased should be placed about one inch away from the lamp tubes. For best results it is recommended that the device remain inactive for 5 minutes after erasure, before programming.

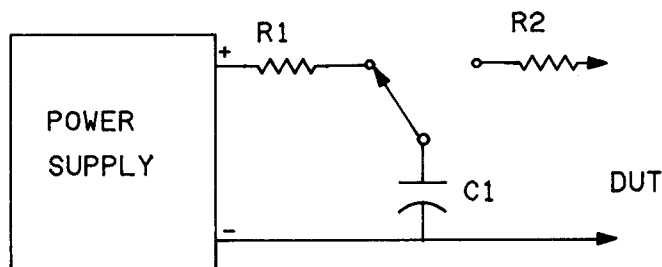
4.8 Read mode operation. In a typical READ operation, the address lines are latched by a downward edge on the strobe line, E_1 . The chip must then be selected by driving pin 21 (S) low. If the chip has been selected the data outputs become valid an access time (TE_{1LQV}) after the downward strobe edge. The data outputs remain valid until the strobe line is returned to a high level. Both S and E_2 may be tied low during the READ cycle. Note that E_2 is latched by the downward strobe edge, but S is not. The PROGRAM pin must be tied high to V_{DD} .

TABLE IV. Programming characteristics.

Parameter	Symbol	Test conditions $V_{CC} = V_{DD} = 5.0 \text{ V} \pm 5\%$ $T_A = 25^\circ\text{C}$	Limits		Unit
			Min	Max	
Program pin load current	I_{PROG}			100	mA
Programming pulse amplitude	V_{PROG}		38	42	V
V_{CC} current	I_{CC}			5	mA
V_{DD} current	I_{DD}			100	mA
Address input high voltage	V_{IHA}		2.75		V
Address input low voltage	V_{ILA}			0.8	V
Data input high voltage	V_{IH}		2.75		V
Data input low voltage	V_{IL}			0.8	V
Program pulse width	T_{PLPH}	$t_{\text{rise}} = t_{\text{fall}} = 5 \mu\text{s}$	18	22	ms
Program pulse duty cycle				75%	
Data setup time	T_{DVPL}		9		μs
Data hold time	T_{PHDX}		9		μs
Strobe pulse width	T_{E1HE1L}		150		ns
Address setup time	T_{AVE1L}		0		ns
Address hold time	T_{E1LE1X}		100		ns
Access time	T_{E1LQV}			1000	ns

4.9 High voltage (V_{ZAP}) test of input protection circuits. One input terminal of the device under test (DUT) shall be subjected to a voltage pulse of 150 volts from a 100-picofarad source in the following test sequence:

- Measure I_{IH} and I_{IL} at one input terminal of the DUT at 25°C. These measurements shall be made in accordance with table III herein. The test limits for a single terminal measurement of I_{IH} and I_{IL} shall be ± 10 μA , maximum.
- In the circuit below, charge the capacitor to -150 V. Then, using the same terminal of the device as selected above for leakage measurements, switch the capacitor to discharge into the device terminal. Then repeat the procedure with +150 V (see figure 7.)
- Within 24 hours, repeat the I_{IH} and I_{IL} measurements on the same terminal as performed above. At this time DUT exhibiting leakage currents in excess of the specified limits is defective.



R1 = Appropriate current-limiting resistance.

R2 = 1.5 k Ω $\pm 5\%$

C1 = 100 pF $\pm 20\%$

Power supply voltage = V_{ZAP} = +150 Vdc and -150 Vdc

FIGURE 7. High voltage (V_{ZAP}) test.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. The devices covered by this specification require electrostatic protection.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use for logistic support of existing equipment.

6.3 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

TE1LQV - - -	Access time from $\bar{E}_1$, or program access time
TSLQV- - -	Output enable time
TE1HQZ - - -	Output disable time
TE1HE1L- - -	$\bar{E}_1$ pulse width (positive), or program strobe pulse width
TE1LE1H- - -	$\bar{E}_1$ pulse width (negative)
TAVE1L - - -	Address setup time
TE1LAX - - -	Address hold time
TE2VE1L- - -	Chip enable setup time
TE1LE2X- - -	Chip enable hold time
TPLPH- - -	Program pulse width
TDVPL- - -	Data setup time for programming
TPHDX- - -	Data hold time for programming

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.6 Handling. CMOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. These CMOS devices are fabricated with a silicon gate technology, including input protection, which reduces the susceptibility to damage. However, the following handling practices are recommended:

- a. Devices should be handled on benches with conductive and grounded surfaces.
- b. Ground test equipment and tools.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS area.
- f. Maintain relative humidity above 50 percent, if practical.

6.7 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process from the same plant as the die represented. Group D (see 4.4.4) generic data shall be on date codes no more than one year old and on the same package type (see terms, definitions, and symbols of MIL-M-38510) and from the same plant as the package represented. The vendor is required to retain generic data for a period of not less than 36 months from the date of shipment.

6.8 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

6.9 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic-industry type</u>
01	6654

6.10 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodian:
Air Force - 17

Preparing activity:
Air Force - 17

Review activities:
Air Force - 11, 19, 85, 99
DLA - ES

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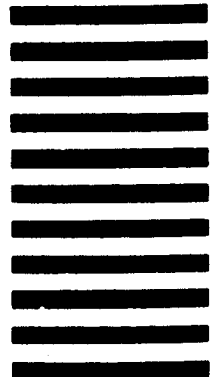
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