

MILITARY SPECIFICATION

MICROCIRCUITS, LINEAR, SAMPLE AND HOLD CIRCUITS, MONOLITHIC SILICON

Reactivated for new design as of 15 October 2003. May be used for either new or existing design acquisition.
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This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF-38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, sample and hold circuits. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4)

1.2 Part or identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

<u>Device type</u>	<u>Circuit</u>
01	Sample and hold circuits, 10 kΩ load
02	Sample and hold circuits, 2 kΩ load

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outline. The case outline is as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
G	MACY1-X8	8	Can
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, 3990 East Broad St., Columbus, OH 43218-3990, or emailed to linear@dsccl.dla.mil . Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil .
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1.3 Absolute maximum ratings.

Supply voltage range	±18 V
Input voltage range	±18 V <u>1/</u>
Logic to logic reference differential voltage	+7 V, -30 V
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited <u>2/</u>
Lead temperature (soldering, 60 seconds)	+300°C
Junction temperature (T _J)	+175°C <u>3/</u>
Hold capacitor short circuit duration	10 seconds

1.4 Recommended operating conditions.

Supply voltage range	±5 V to ±15 V
Ambient operating temperature range (T _A)	-55°C to +125°C
Hold capacitor type	Teflon <u>4/</u>

1.5 Power and thermal characteristics.

Case outlines	Maximum allowable power dissipation	Maximum θ_{JC}	Maximum θ_{JA}
G	330 mW at T _A = +125°C	40°C/W	150°C/W
P	400 mW at T _A = +125°C	35°C/W	120°C/W

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ The absolute maximum input voltage shall not exceed the power supply voltages.

2/ Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

3/ For short term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), T_J = 275°C.

4/ Sample and hold performance is highly dependent on having a quality "hold" capacitor with low dielectric absorption over -55°C ≤ T_A ≤ 125°C.

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein the text of this document shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections and logic diagram. The terminal connections and logic diagram shall be as specified on figure 1.

3.3.2 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.

3.3.3 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and unless otherwise specified, apply over the full recommended ambient operating temperature range for supply voltages from ± 5 V to ± 18 V. Unless otherwise specified, the device is in the "sample" mode with $C_H = 0.01 \mu\text{F}$. With ± 15 V supplies, the input voltage range is from -11.5 V to $+11.5$ V. The logic reference voltage is 0 V and the logic voltage for "sample" mode is 2.5 V. Specific test conditions and limits are shown in table III.

3.5.1 Offset null circuits. The nulling inputs shall be capable of being nulled 1 mV beyond the specified offset voltage limits for $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ using the circuit of figure 2.

3.5.2 Instability oscillations. The devices shall be free of oscillations when operated in the test circuits of this specification.

3.6 Electrical test requirements. Electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 60 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C ±V _{CC} = ±15 V, see figure 3 and 3.5 unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Input offset voltage <u>1/</u>	V _{IO}	±V _{CC} = ±5 V to ±15 V, T _A = +25°C	01,02	-3	3	mV
		±V _{CC} = ±5 V to ±15 V, -55°C ≤ T _A ≤ +125°C		-5	5	
Input offset voltage temperature sensitivity	ΔV _{IO} /	T _A = -55°C to +25°C	01,02	-20	20	μV/°C
	ΔT	T _A = +25°C to +125°C		-20	20	
Input bias current <u>1/</u>	I _{IB}	±V _{CC} = ±5 V to ±15 V, T _A = +25°C	01,02	-1	25	nA
		±V _{CC} = ±5 V to ±15 V, -55°C ≤ T _A ≤ +125°C		-25	75	
Input impedance <u>2/</u>	Z _I	T _A = +25°C	01,02	2		GΩ
		-55°C ≤ T _A ≤ +125°C		1		
Gain error	A _E	V _{IN} = -11.5 V to +11.5 V, R _L = 10 kΩ, T _A = +25°C	01,02	-0.005	+0.005	%
		V _{IN} = -11.5 V to +11.5 V, R _L = 10 kΩ, -55°C ≤ T _A ≤ +125°C		-0.02	+0.02	
		V _{IN} = -10 V to +10 V, R _L = 2 kΩ, T _A = +25°C	02	-0.005	+0.005	
		V _{IN} = -10 V to +10 V, R _L = 2 kΩ, -55°C ≤ T _A ≤ +125°C		-0.02	+0.02	
		V _{CC} = ±5 V, R _L = 10 kΩ, V _{IN} = -2 V to +2 V, T _A = +25°C	01,02	-0.02	+0.02	
		V _{CC} = ±5 V, V _{IN} = -2 V to +2 V, R _L = 10 kΩ, -55°C ≤ T _A ≤ +125°C		-0.04	+0.04	
Input offset voltage adjustment	V _{IO} (ADJ+)	V _{IN} = 0 V, V _{OFFSET ADJ} at +V _{CC}	01,02	+6		mV
	V _{IO} (ADJ-)	V _{IN} = 0 V, V _{OFFSET ADJ} at 1 kΩ from +V _{CC} , 20 kΩ from 0 V			-6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C ±V _{CC} = ±15 V, see figure 3 and 3.5 unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Power supply rejection ratio	+PSRR	+V _{CC} = +12 V to +18 V, -V _{CC} = -18 V, V _{IN} = 0 V	01,02	80		dB
	-PSRR	+V _{CC} = +18 V, V _{IN} = 0 V -V _{CC} = -12 V to -18 V		80		
Feedthrough rejection <u>3/</u> ratio	FRR	V _{IN} = ±11.5 V, hold mode, see figure 4, T _A = +25°C	01,02	86		dB
		V _{IN} = ±11.5 V, hold mode, see figure 4, -55°C ≤ T _A ≤ +125°C		80		
	FRR _{ac}	V _{IN} = 20 V _{PP} at 1 kHz, T _A = +25°C hold mode, see figure 5		86		
Series charge resistance <u>4/</u>	R _{SC}	V _{IN} = 0 V to 0.4 V; measure current change to ground at HOLD CAPACITOR terminal pin	01,02	75	400	Ω
Output impedance	Z _O	V _{HOLD CAP.} = V _{HC} = 0 V, hold mode, see figure 6, I _O = ±1 mA	01,02		2	Ω
“Hold” step voltage <u>5/</u>	V _{HS}	V _{LOGIC} = 4 V, tr ≤ 50 ns, see figure 7, V _{OUT} = ±11.5 V, T _A = +25°C	01,02	-2	2	mV
		V _{LOGIC} = 4 V, tr ≤ 50 ns, see figure 7, V _{OUT} = ±11.5 V, -55°C ≤ T _A ≤ +125°C		-5	5	
Supply current	I _{CC}	T _A = -55°C	01	1	6.5	mA
			02	1	7.0	
		+25°C ≤ T _A ≤ +125°C	01	1	5.5	
			02	1	6.0	
Logic input current (high)	I _{IH}	V _{LOGIC} = 5.5 V, +V _{CC} = 8.5 V, -V _{CC} = -21.5 V	01,02	0	10	μA
Logic input current (low)	I _{IL}	V _{LOGIC} = 0 V, +V _{CC} = 21.5 V, -V _{CC} = -8.5 V	01,02	-1	1	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ $\pm V_{CC} = \pm 15\text{ V}$, see figure 3 and 3.5 unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Output short circuit current (positive output)	$I_{OS}(+)$	$V_{IN} = 10\text{ V}$, $t \leq 25\text{ ms}$, short circuit to 0 V	01	-25		mA
			02	-30		
Output short circuit current (negative output)	$I_{OS}(-)$	$V_{IN} = -10\text{ V}$, $t \leq 25\text{ ms}$, short circuit to 0 V	01		25	mA
			02		30	
Hold mode leakage current (positive output)	$I_{HL}(+) \underline{6/}$	$V_{IN} = 0\text{ V}$, $+V_{CC} = 3.5\text{ V}$, $T_A = +25^{\circ}\text{C}$, $-V_{CC} = -26.5\text{ V}$, see figure 8	01,02	-100	100	pA
		$V_{IN} = 0\text{ V}$, $+V_{CC} = 3.5\text{ V}$, $T_A = +125^{\circ}\text{C}$, $-V_{CC} = -26.5\text{ V}$, see figure 8		-50	50	nA
Hold mode leakage current (negative output)	$I_{HL}(-) \underline{6/}$	$V_{IN} = 0\text{ V}$, $+V_{CC} = 26.5\text{ V}$, $T_A = +25^{\circ}\text{C}$, $-V_{CC} = -3.5\text{ V}$, see figure 8	01,02	-100	100	pA
		$V_{IN} = 0\text{ V}$, $+V_{CC} = 26.5\text{ V}$, $T_A = +125^{\circ}\text{C}$, $-V_{CC} = -3.5\text{ V}$, see figure 8		-50	50	nA
Hold capacitor charge current (positive output)	$I_{CH}(+)$	$V_{IN} = 11.5\text{ V}$, $V_{HC} = 9.5\text{ V}$, $T_A = +25^{\circ}\text{C}$	01,02		-3	mA
		$V_{IN} = 11.5\text{ V}$, $V_{HC} = 9.5\text{ V}$, $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$			-2	
Hold capacitor charge current (negative output)	$I_{CH}(-)$	$V_{IN} = -11.5\text{ V}$, $V_{HC} = -9.5\text{ V}$, $T_A = +25^{\circ}\text{C}$	01,02	3		mA
		$V_{IN} = 11.5\text{ V}$, $V_{HC} = 9.5\text{ V}$, $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		2		
Differential logic threshold	$V_{TH}(H)$	$V_{IN} = -2\text{ V}$, $V_{LOGIC} = 2\text{ V}$ (check for $I_{HOLD\ CAP} \geq 1\text{ mA}$)	01,02		2	V
	$V_{TH}(L)$	$V_{IN} = -2\text{ V}$, $V_{LOGIC} = 0.8\text{ V}$ (check for $I_{HOLD\ CAP} \leq 10\text{ }\mu\text{A}$)		0.8		
Acquisition time (0.1 % error)	$t_{aq} \underline{7/}$	$V_{IN} = 0\text{ V}$ to 10 V , 10 V to 0 V , 0 V to -10 V , -10 V to 0 V , $C_L = 100\text{ pF}$, $T_A = +25^{\circ}\text{C}$, see figures 9 to 11	01,02		25	μs
Aperture time	$t_{ap} \underline{8/}$	$V_{IN} = 0\text{ V}$ to $+10\text{ V}$, 10 V to 0 V , 0 V to -10 V , -10 V to 0 V , $V_O \leq 1\text{ mV}$, $T_A = +25^{\circ}\text{C}$, see figures 12 to 15	01,02		300	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C ±V _{CC} = ±15 V, see figure 7 and 3.5 unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Transient response <u>9/</u> (settling time)	TR _(ts)	V _{IN} = 100 mV step, T _A = +25°C, C _H = 1000 pF, R _L = 10 kΩ, C _L = 100 pF, see figure 16, to 10% of final value,	01,02		2.5	μs
Transient response <u>9/</u> (overshoot)	TR _(os)	V _{IN} = 100 mV step, T _A = +25°C, C _H = 1000 pF, R _L = 10 kΩ, C _L = 100 pF, see figure 16	01,02		40	%
Noise	en(H) en(S)	Hold mode, sample mode 10 Hz to 10 kHz, see figure 17, T _A = +25°C	01,02		10	μVrms
Settling time	t _s	V _{IN} = 0 V, V _O ≤ 1 mV, hold mode, see figure 18, T _A = +25°C	01,02		1.5	μs

- 1/ This parameter is specified at V_{CM} = 0 V, -11.5 V, and +11.5 V with ±V_{CC} = ±15 V, and at V_{CM} = -2 V and +2 V with ±V_{CC} = ±5 V.
- 2/ Input impedance is calculated from the V_{IO} and I_{IB} common mode voltage end-point range data.
- 3/ Feedthrough rejection ratio is very sensitive to stray capacitance between the signal INPUT (pin 3) and HOLD CAPACITOR (pin 6). For instance 0.5 pF of external coupling with a .01 μF hold capacitor would equal the specification limit of the device.
(For example: FRR = 20 log ((0.01 μF) / 0.5 pF) = 20 log (2 × 10⁴) = 86 dB).
- 4/ Series charge resistance along with input signal slew rate and an external hold capacitor determine the dynamic sampling error of the device in its application (for example; DSE = K × R_{SC} × SR where K is a proportionality constant).
- 5/ The external hold capacitor should be either Teflon or polystyrene so that dielectric absorption is minimized. This will insure that excessive “sag back” after capacitor “sample” mode charging does not occur. “Hold” step is sensitive to stray capacitance coupling between input logic signals and the “hold” capacitor.
- 6/ Hold mode leakage current is actually JFET junction leakage current which doubles (approximately) for each 10°C increase in junction temperature. Measurement at -55°C is not necessary since expected values are too small for typical test systems.
- 7/ Acquisition time at 125°C typically increases from 20 % to 100 % above the 25°C value.
- 8/ Aperture time at 125°C typically increases 110 % above the 25°C value.
- 9/ Transient response shall be measured at the common mode voltage limits (for example, V_{CM} = -11.5 V and +11.5 V). Any high frequency ringing shall be over within 1 microsecond. After its peak the major loop response shall be without further oscillations.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3	1*, 2, 3
Group A test requirements	1, 2, 3, 7, 8	1, 2, 3, 7, 8
Group B electrical test parameters when using the method 5005 QCI option	1, 2, 3 and table IV delta limits	N/A
Group C end-point electrical parameters	1, 2, 3 and table IV delta limits	1 and table IV delta limits
Group D end-point electrical parameters	1, 2, 3	1

*PDA applies to subgroup 1.

4. VERIFICATION.

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Additional screening for space level product shall be as specified in MIL-PRF-38535. Reverse bias burn-in shall apply to class S devices only.

NOTE: If accelerated high-temperature test conditions are used (condition F), the device manufacturer shall ensure that at least 85 percent of the applied voltage is dropped across the device at temperature. The device is not considered functional under accelerated test conditions.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, 6, 9, 10, and 11 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

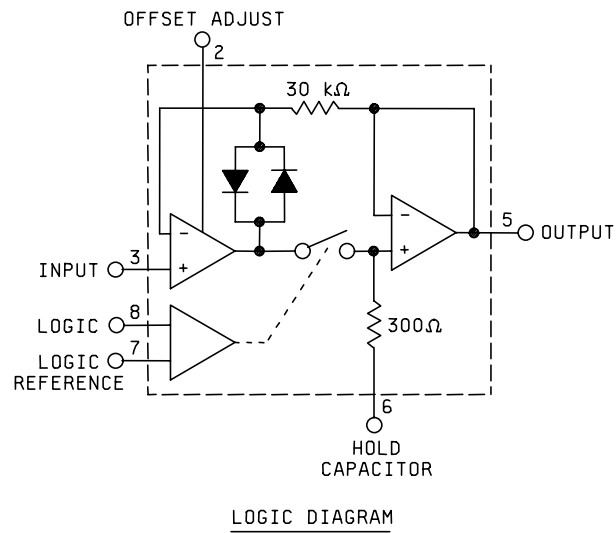
4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

- a. End point electrical parameters shall be as specified in table II herein.
- b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional and positive when flowing into the referenced terminal.



DEVICE TYPES 01 AND 02
CASE G

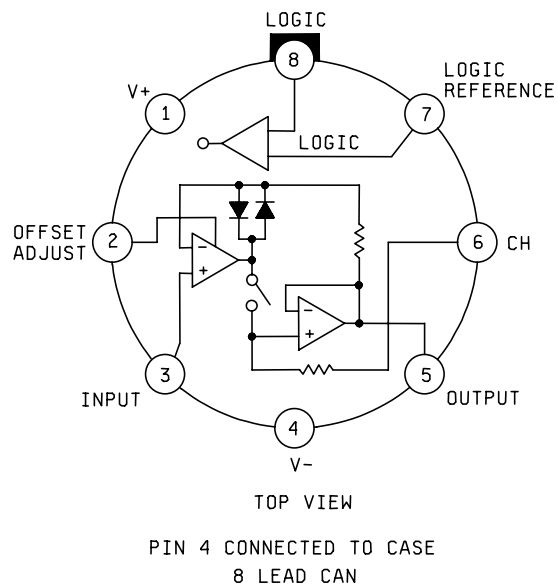


Figure 1. Terminal connections and logic diagram.

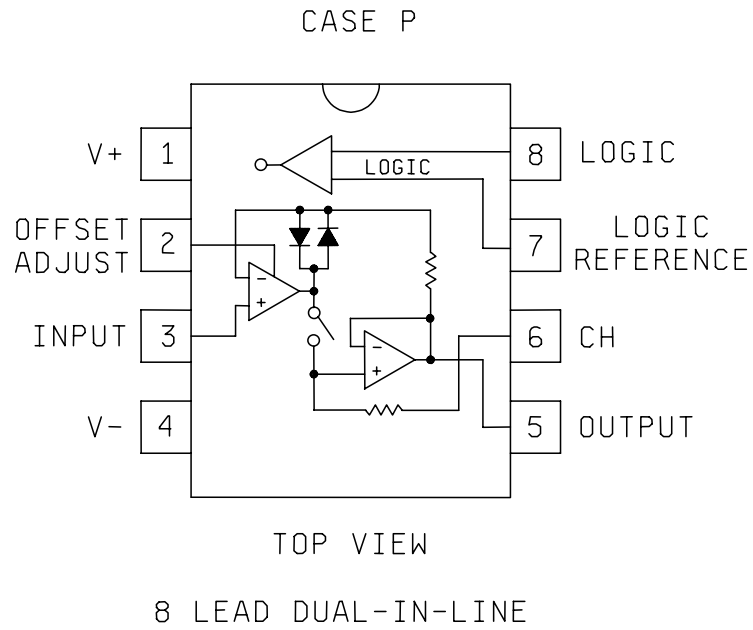


Figure 1. Terminal connections and logic diagram – Continued.

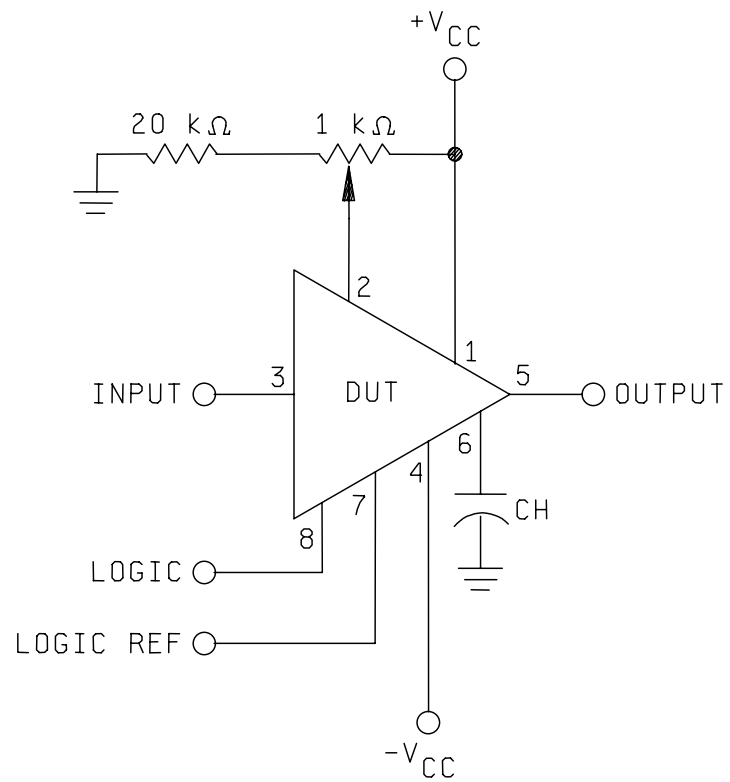
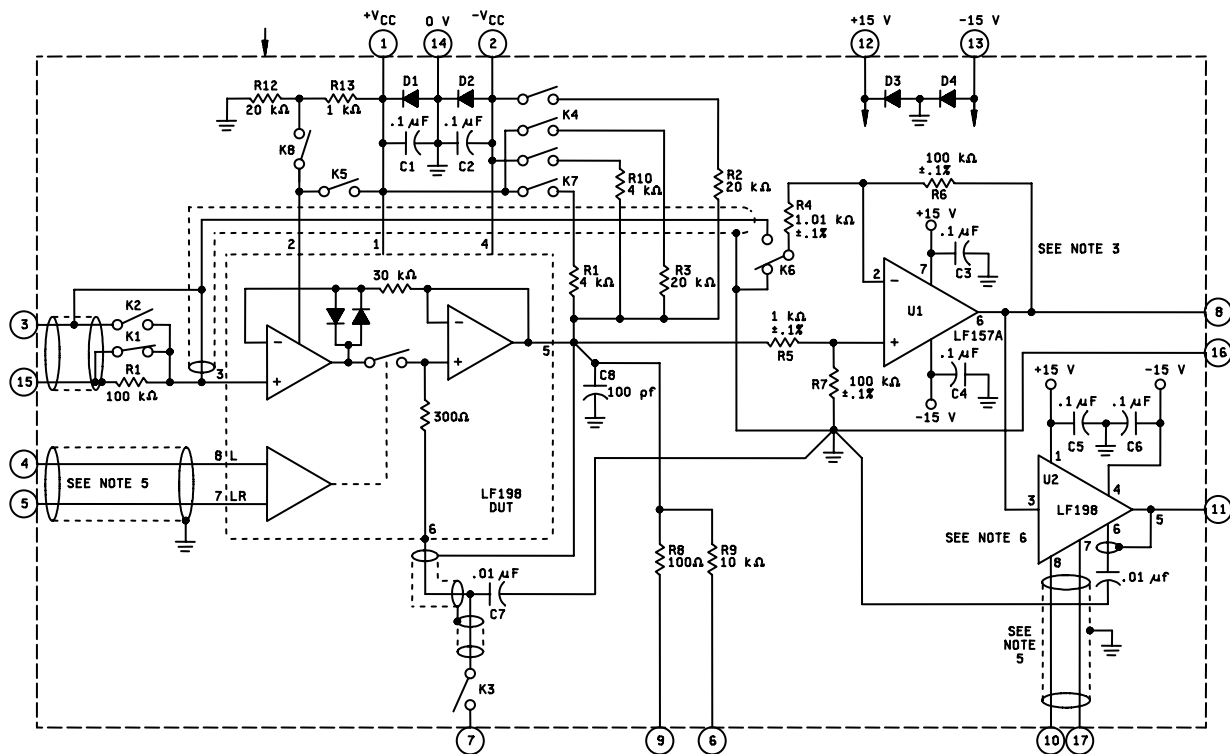


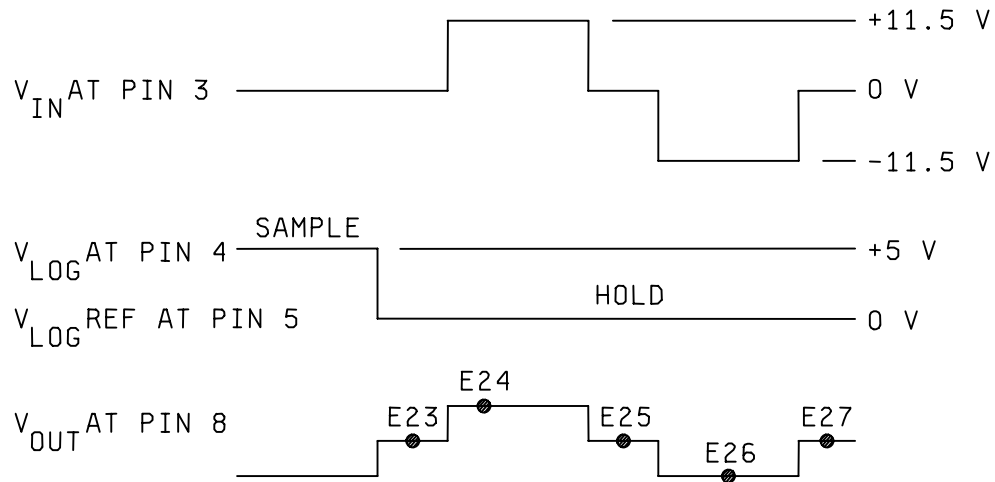
FIGURE 2. Offset null circuit.



NOTES:

1. Last component designations are R13, C9, U2, D4, and K8
2. All resistors are $\pm 1\%$ film unless otherwise stated.
3. U1 offset error shall be measured with pin 9 grounded and the device under test (D.U.T.) removed. This error shall be removed in the software calculations.
4. Relay control inputs are not shown.
5. A speed-up circuit is required in series with the logic input for rise times greater than $0.5\ \mu\text{s}$.
6. The adapter S/H U2 is required for $T_A = 125^\circ\text{C}$ testing of some parameters.

FIGURE 3. Test circuit for static and dynamic tests.



$$\begin{aligned}
 FRR &= 20 \log 1150/E24 - E23 \\
 FRR &= 20 \log 1150/E25 - E24 \\
 FRR &= 20 \log 1150/E26 - E25 \\
 FRR &= 20 \log 1150/E27 - E26
 \end{aligned}$$

FIGURE 4. Feedthrough rejection test timing waveforms.

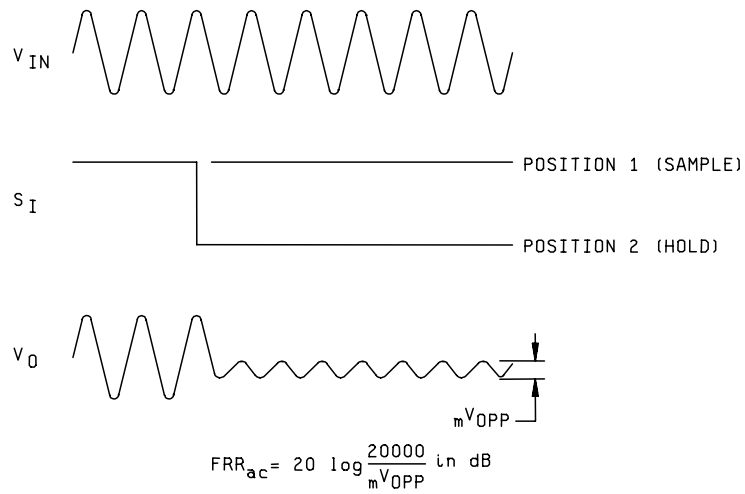
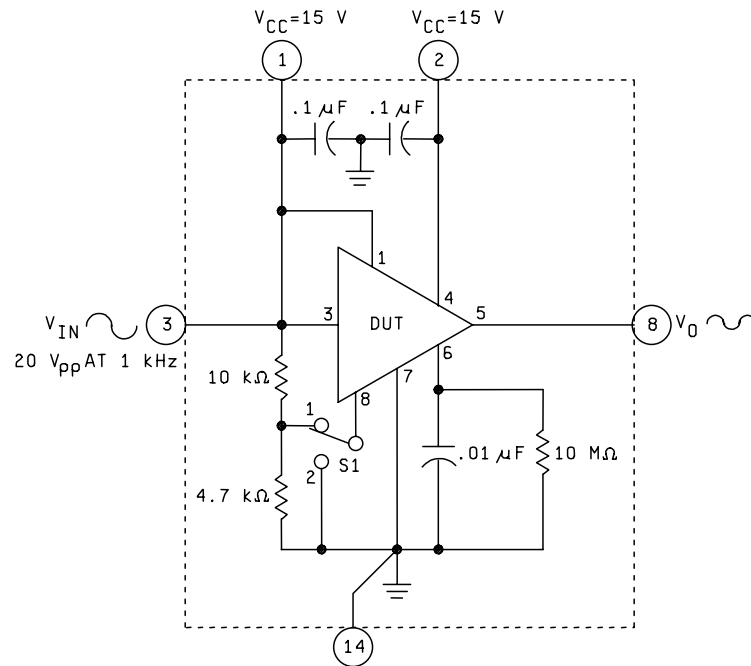


FIGURE 5. Test circuit for ac feedthrough rejection.

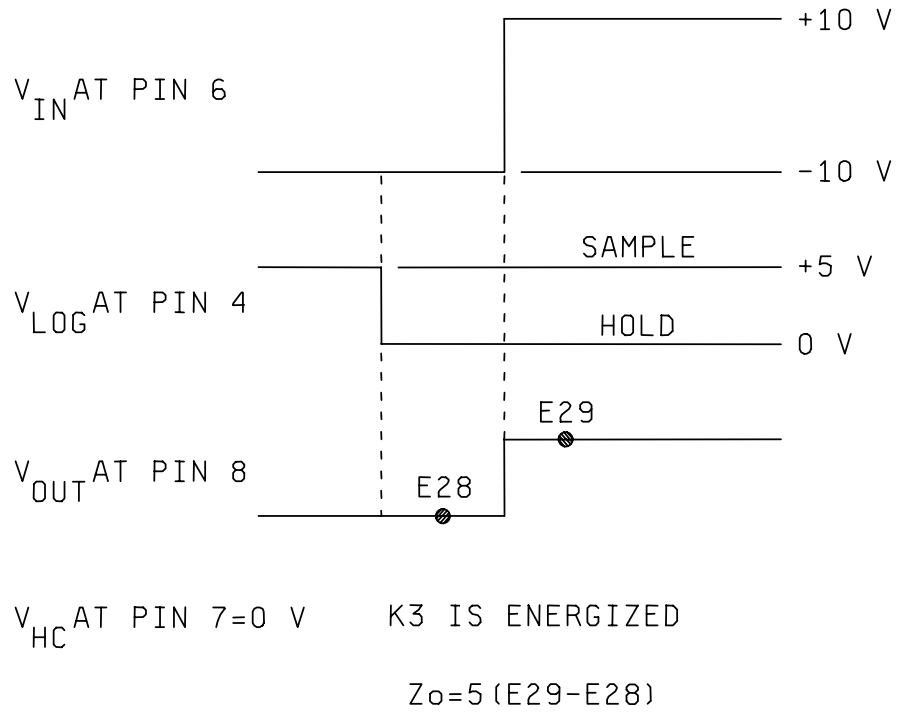
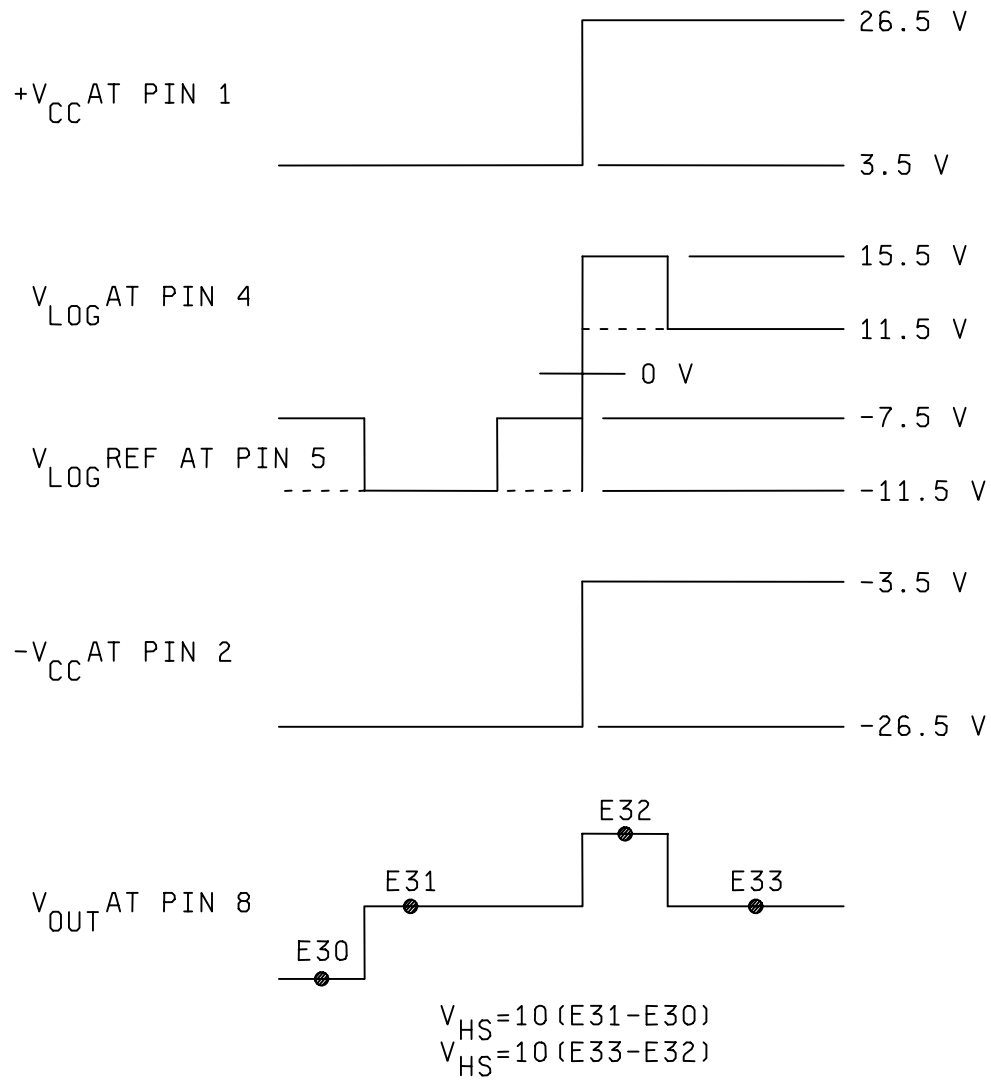
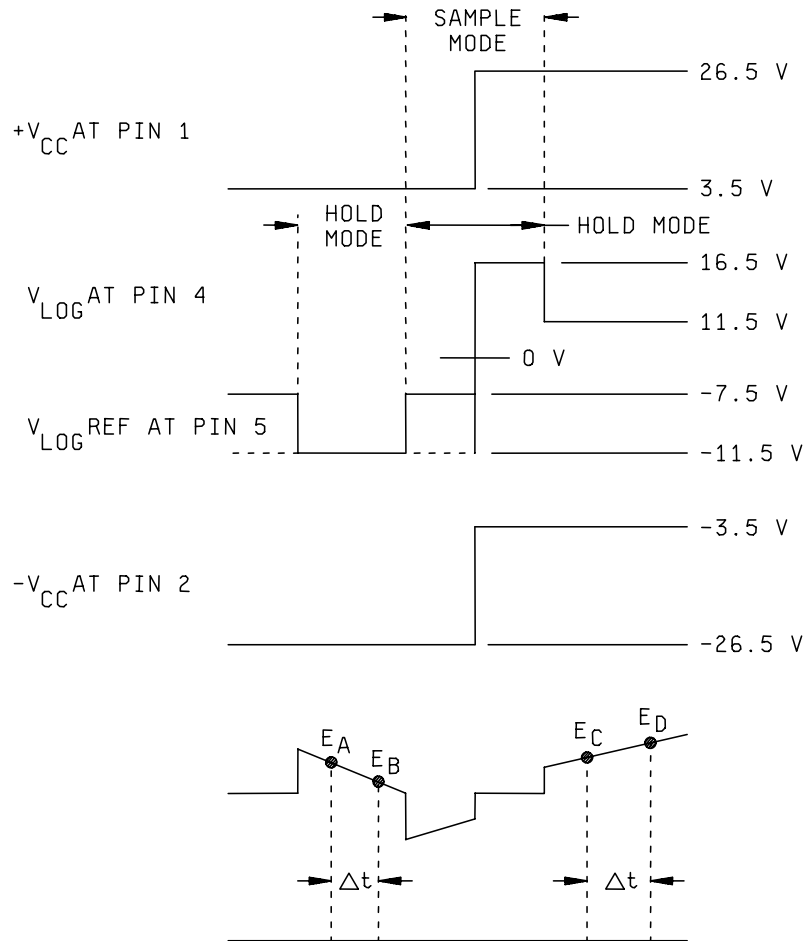


FIGURE 6. Output Impedance test timing.

FIGURE 7. Hold step timing waveforms.



$$I_{HL}(+) = K (E_A - E_B)$$

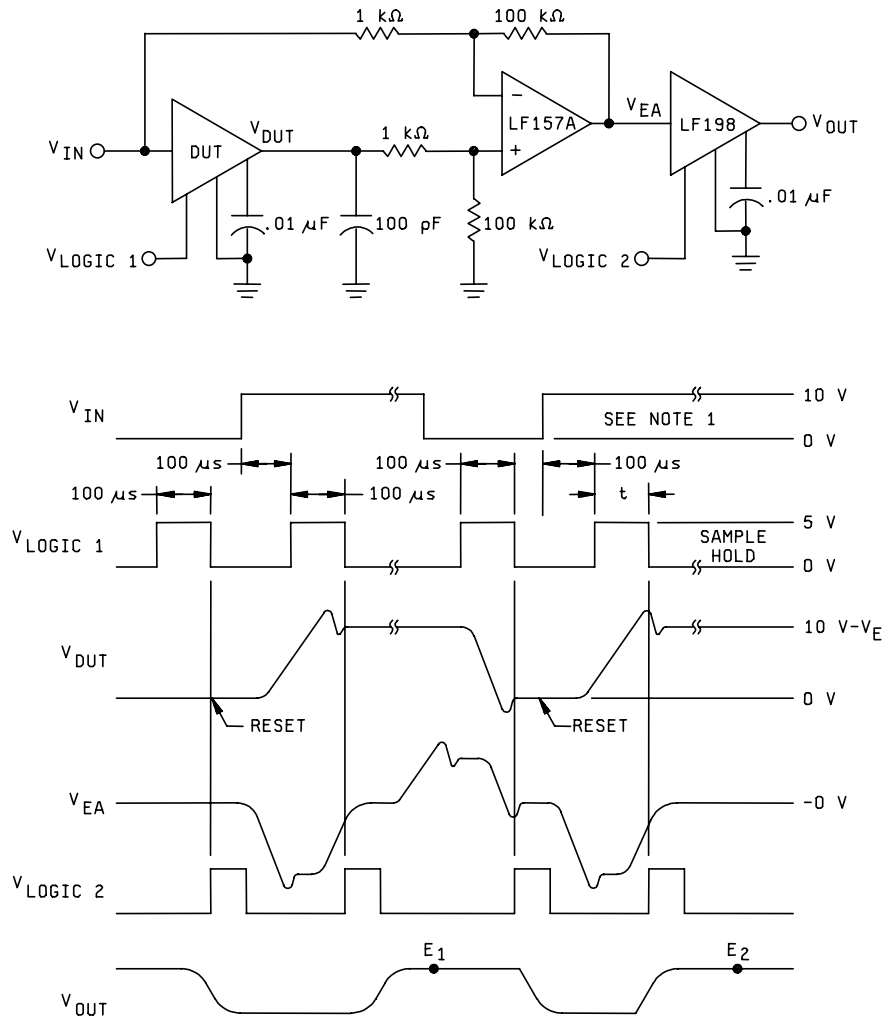
$$I_{HL}(-) = K (E_C - E_D)$$

$$I_{HL}(+) = C \Delta V / \Delta t = (C / \Delta t) (\Delta V_O / 100) = K \Delta V_O \text{ where } C = 0.01 \mu\text{F}$$

$$\Delta V_O = (E_A - E_B) \text{ or } (E_C - E_D)$$

Temperature	Δt	K	ΔV_O Units	I_L Units
25°C	100 ms	1	mV	pA
125°C	10 ms	0.1	mV	nA

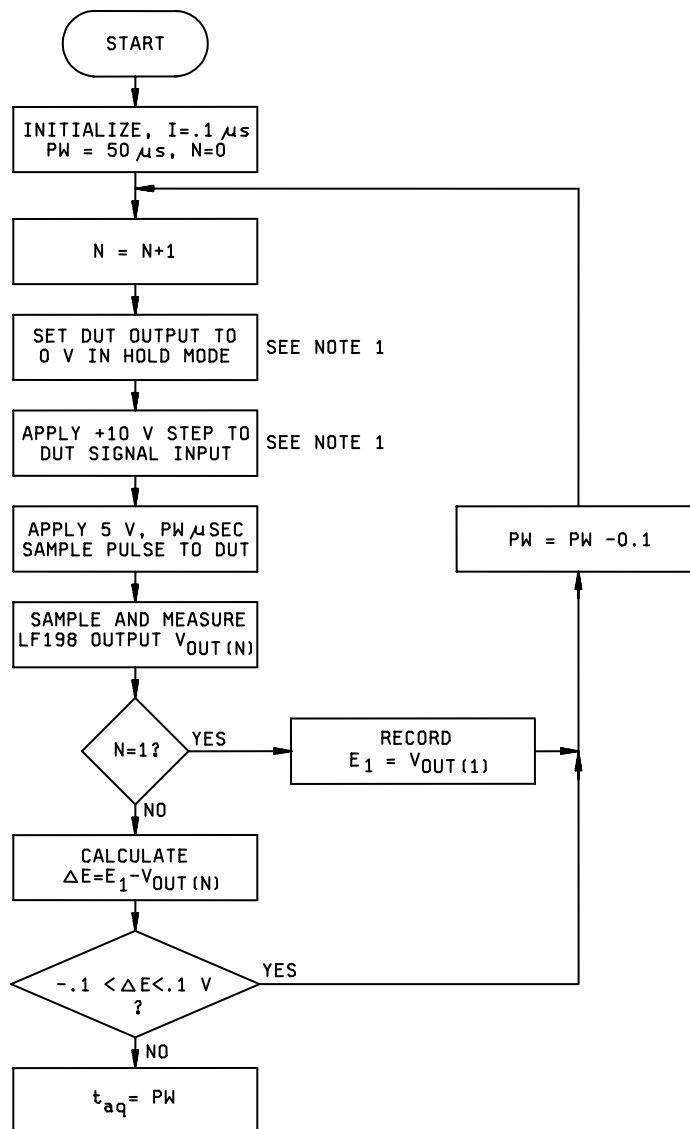
FIGURE 8. Hold leakage current timing waveforms.



NOTES:

1. Acquisition time is equal to the logic sample pulse width which yields an output error from steady state of 10 mV at the device under test (D.U.T.) output or 1 V at the differential amp output (for example; pulse width $t = t_{aq}$ when $E1 - E2 = 0.1$ V).
2. Only the 0 V to +10 V step is shown. The other transitions as per figure 10 shall also be tested.

FIGURE 9. Acquisition time test circuit and wavforms.



Notes:

1. Repeat above procedure for three other cases as follows: -10 V step from 0, -10 V step from +10 V and +10 V step from -10 V.

FIGURE 10. Acquisition time flow chart.

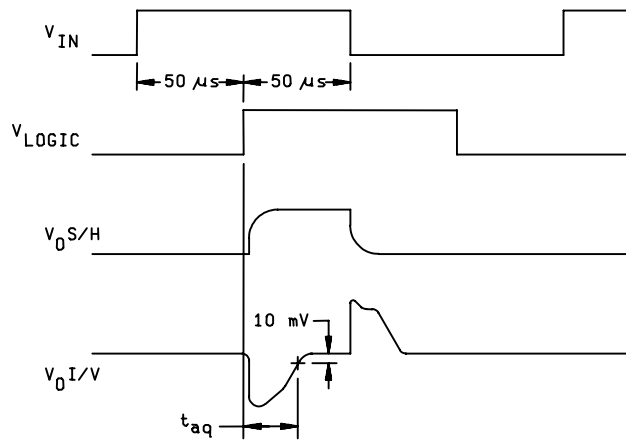
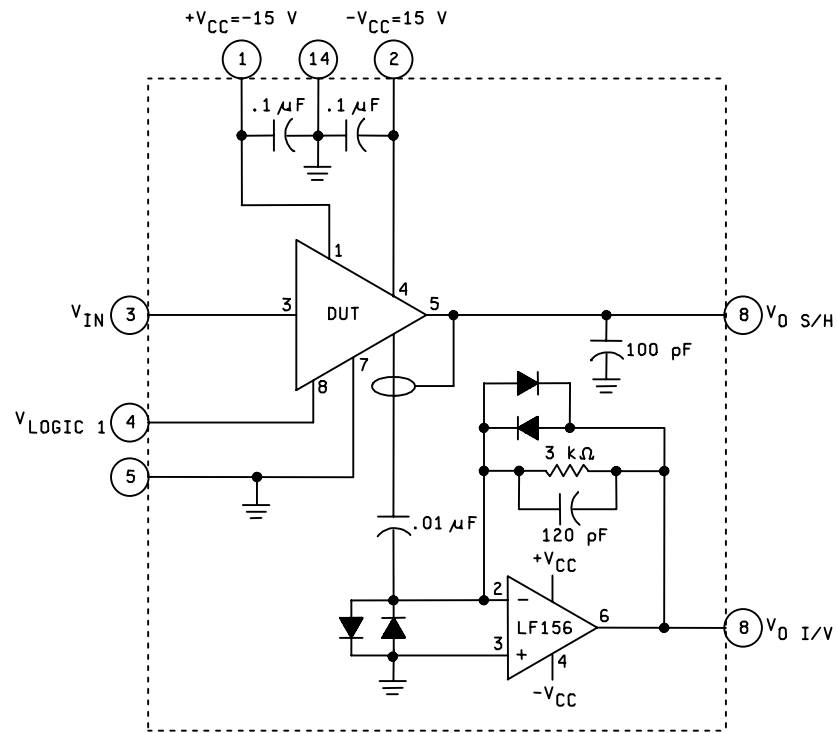
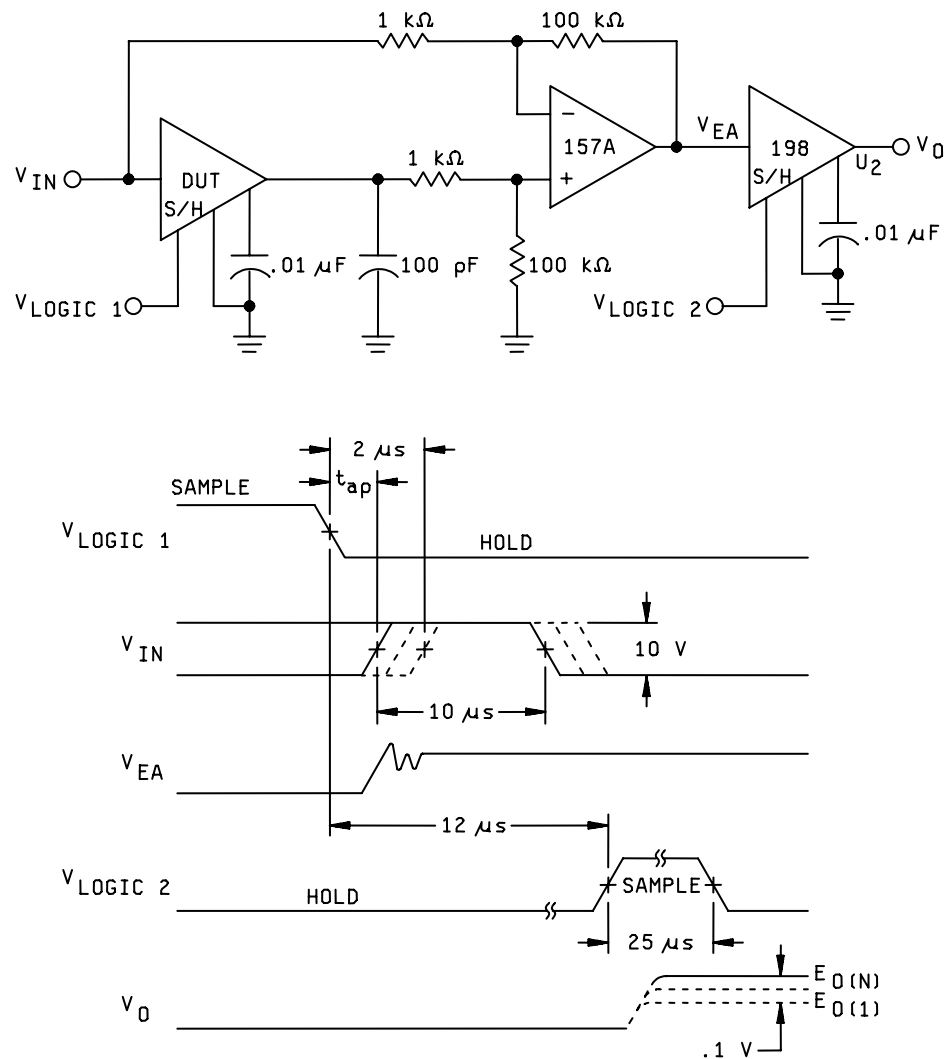


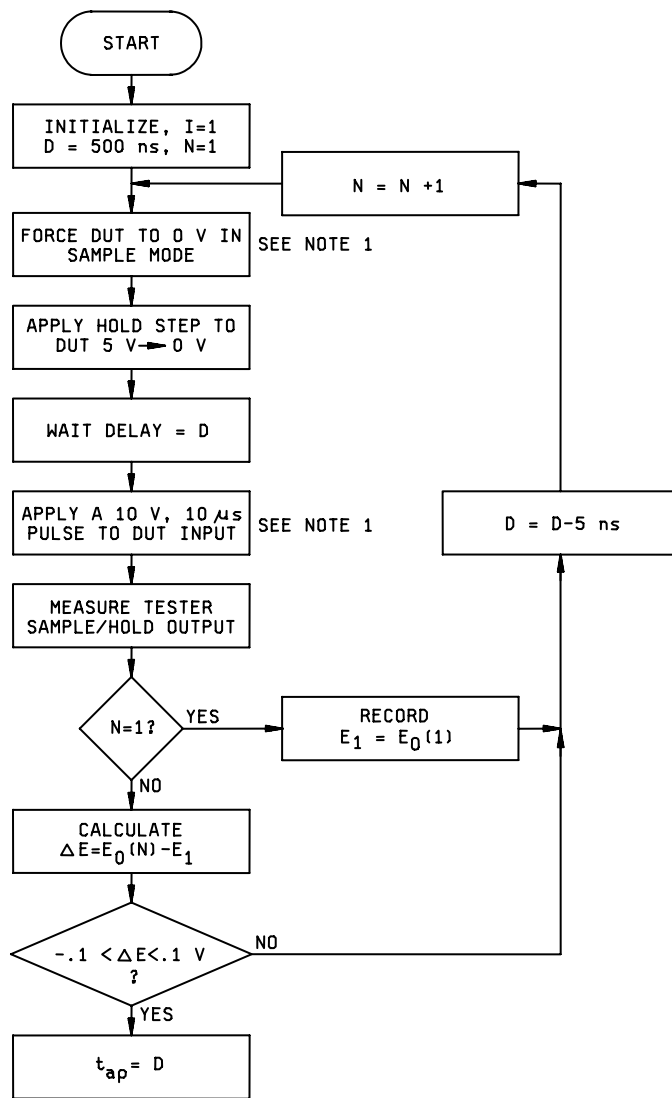
FIGURE 11. Alternate acquisition time test circuit.



NOTES:

1. Aperture time is equal to the time delay from the $V_{LOGIC 1}$ device under test (D.U.T.) 'hold' command step to the 10 V input transition which yields a 0.1 volt output error from its 2 μs delayed value $E_0(1)$.
2. A flow chart for the automatic determination of aperture time is shown in figure 13. All four combinations of 10 V input and 5 V logic signals shall be checked.
3. The adapter S/H U2 holds the 'data' voltage for the measurement system.

FIGURE 12. Aperture time test circuit.



NOTE:

1. Repeat above procedure for three other cases as follows:
 - a) Start at 0 V and apply a -10 V pulse.
 - b) Start at 10 V and apply a -10 V pulse.
 - c) Start at -10 V and apply a +10 V pulse.

FIGURE 13. Aperture time flow chart.

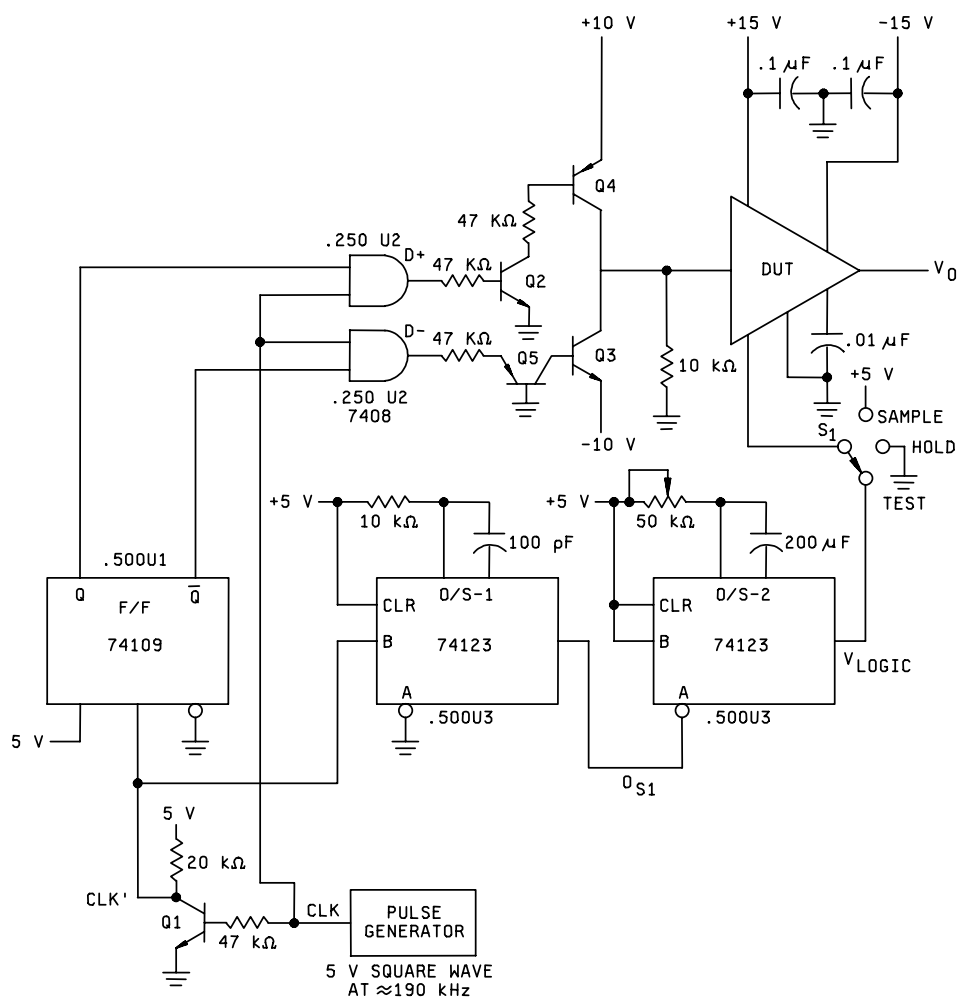
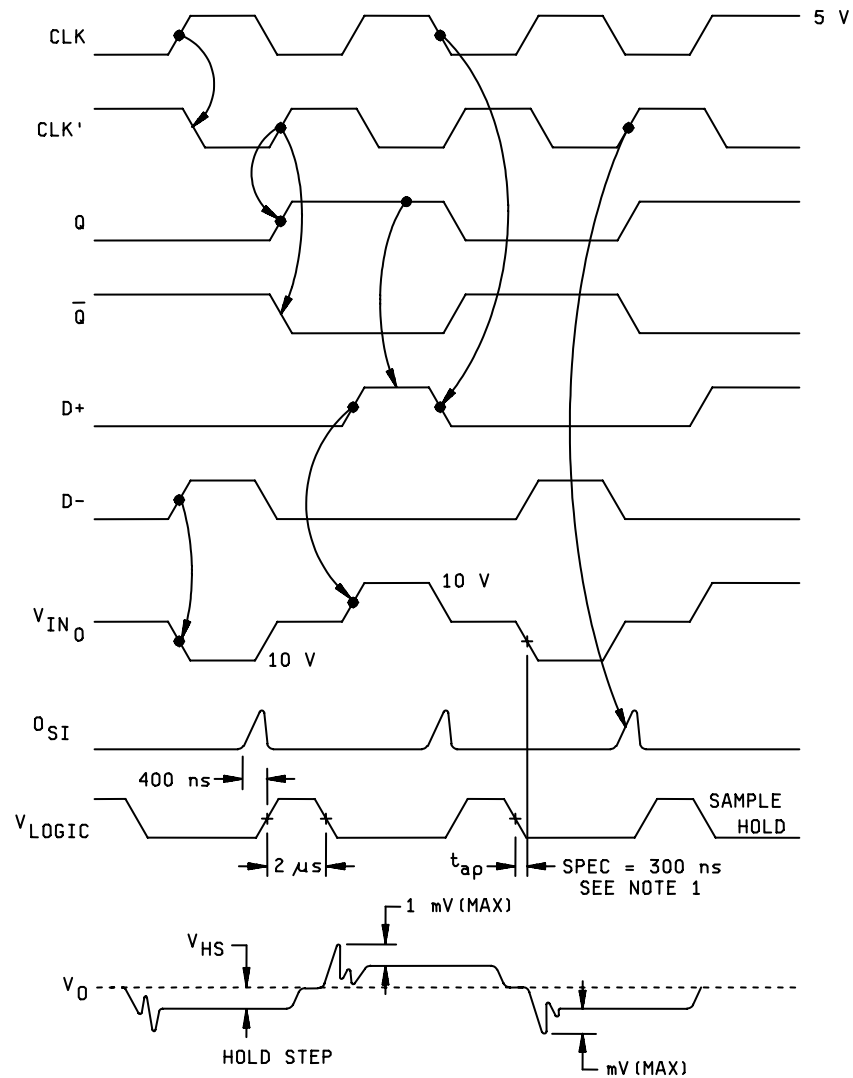


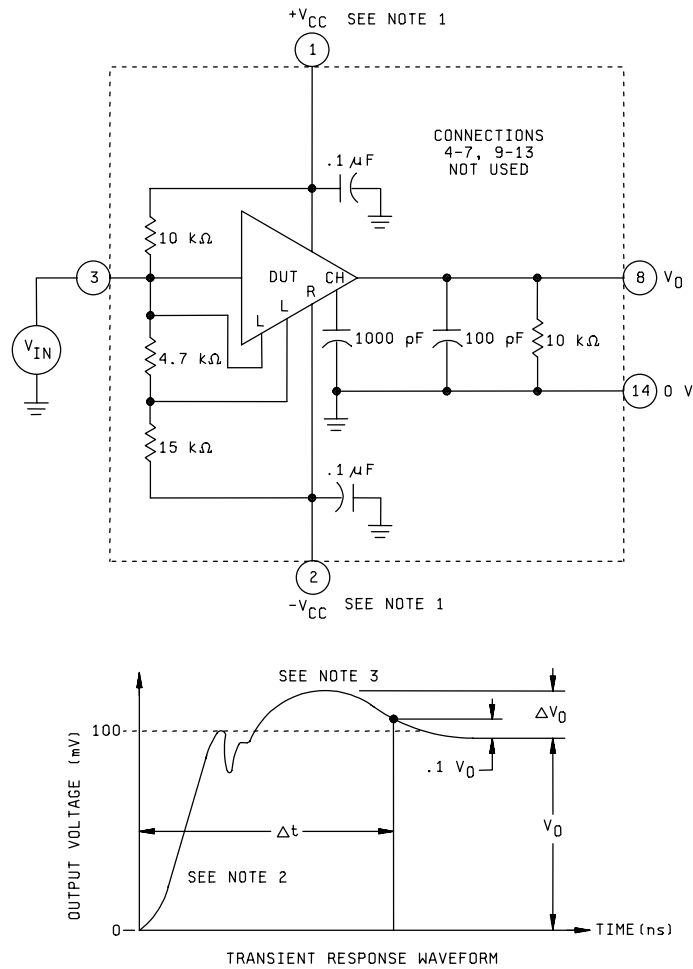
FIGURE 14. Alternate aperture time test circuit.



NOTE:

1. The clock frequency and logic pulse width are adjusted so that there is a 300 nanosecond delay from the logic hold transition to a $\pm 10 \text{ V}$ input transition. For these conditions the effect on the output shall be less than 1 mV. Laboratory instruments may be used to apply similar input conditions.

FIGURE 15. Alternate aperture time test waveforms.

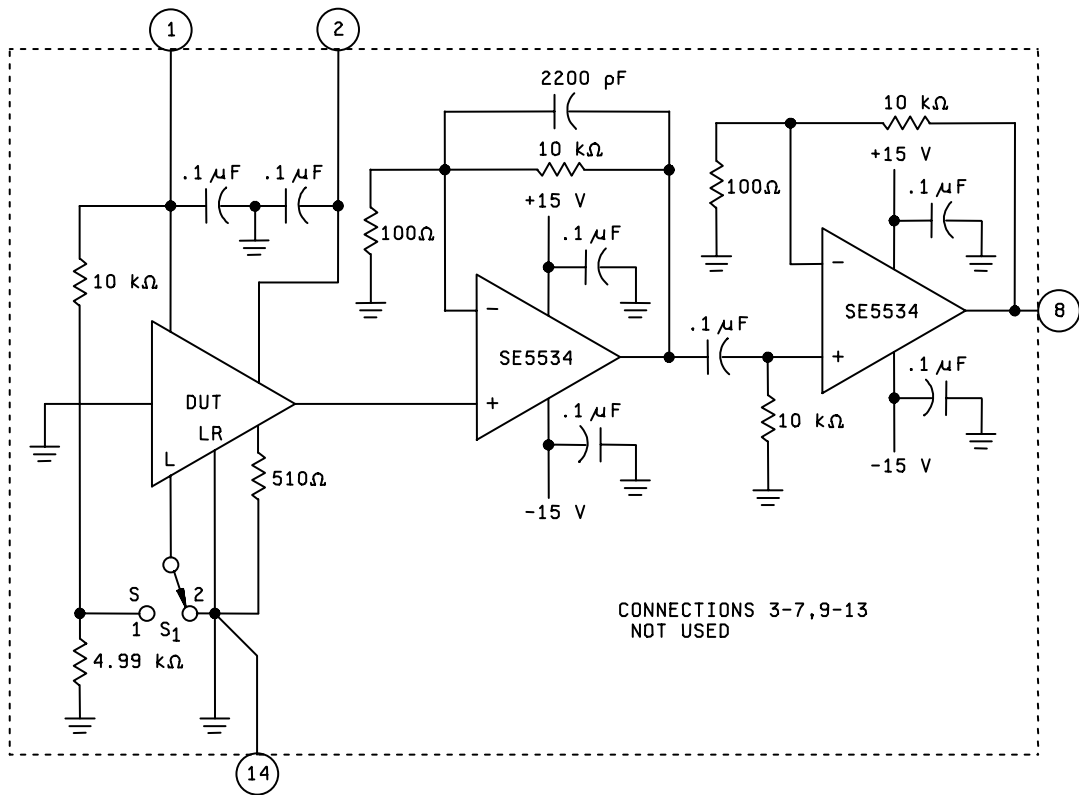


Parameter symbol	Input pulse signal at $t_r \leq 50\text{ ns}$	Output pulse signal (see notes)	Equation
$TR_{(ts)}$	100 mV	Above waveform	$TR_{(ts)} = \Delta t$
$TR_{(os)}$	100 mV	Above waveform	$TR_{(os)} = \Delta V_O / V_O$

NOTES:

1. $+V_{CC}$ and $-V_{CC}$ shall be at the common mode limits.
(For example: first +3.5 V, -26.5 V and then +26.5 V, -3.5 V.)
2. Any high frequency ringing shall be over within $2\text{ }\mu\text{s}$.
3. After its peak the major loop response shall be without further oscillations.

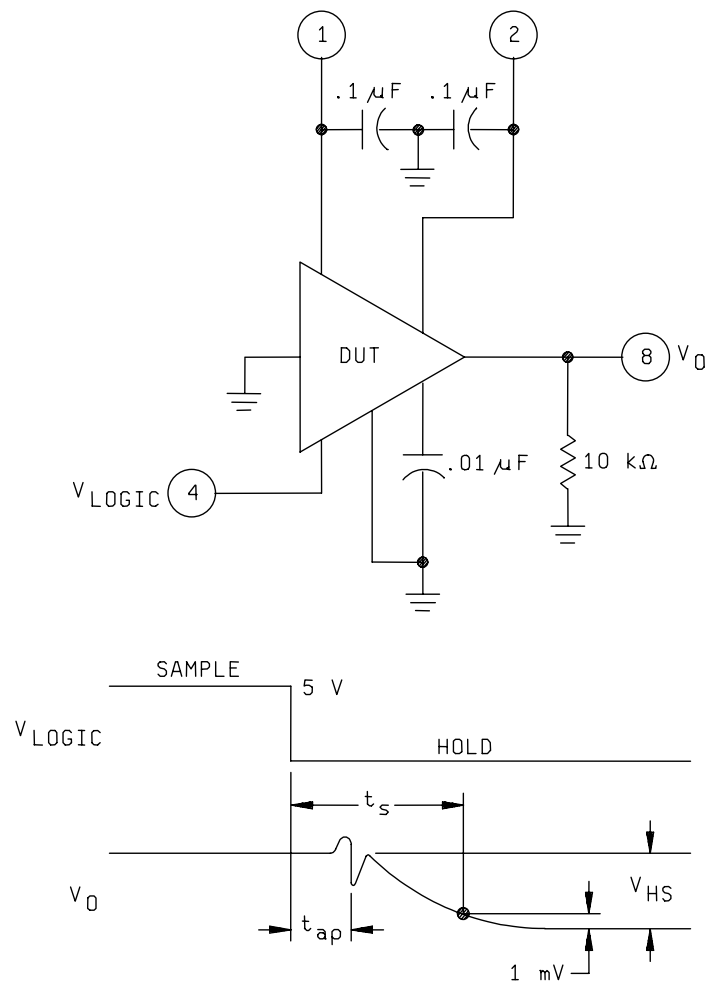
FIGURE 16. Transient response test circuit and waveform.

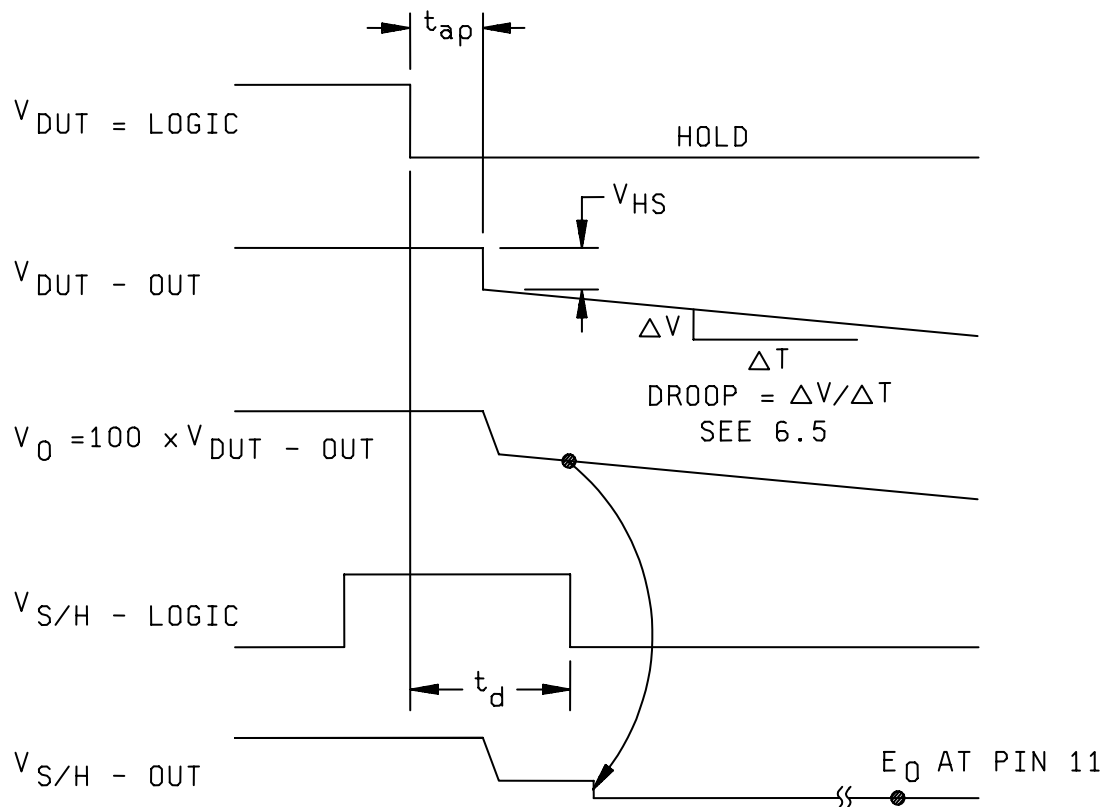


Symbol	S1	Measure		Input Noise Equation	Units
		Value	Units		
$e_n(S)$	1	E_o	mVrms	$e_n(S) = 0.1 E_o$	μVrms
$e_n(H)$	2	E_o	mVrms	$e_n(H) = 0.1 E_o$	μVrms

- NOTES:
- 1. The circuit components are designed to provide an effective “brickwall” bandwidth from 10 Hz to 10 kHz.
 - 2. Measurement should be made with a true rms voltmeter with at least 20 kHz bandwidth.
 - 3. The filter pole frequencies are related to the effective noise pass band frequencies as follows:
 $f_{LE} = 2/\pi \times f_{LP}$; $f_{HE} = \pi/2 \times f_{HP}$.

FIGURE 17. Noise test circuit.

FIGURE 18. Hold mode settling time test circuit.



NOTES:

1. At 125°C hold mode leakage current causes excessive droop rate of the hold capacitor voltage.
(For example: maximum droop rate = $\Delta V / \Delta t = I / C = 100 \text{ nA} / 0.01 \mu\text{F} = 10 \text{ mV} / \text{ms}$)
2. In order to minimize the droop error, the test fixture S/H at 25°C is used to acquire and hold the voltage until the measurement system can do its function.
3. See figure 3 test circuit.

FIGURE 19. 125°C D.U.T. hold mode measurements.

TABLE III. Group A inspection for all device types.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Notes	Adapter pin numbers							Energized relays	Measured pin			Equation <u>1/</u>	Limits		Unit		
					1	2	3	4	5	6	7		No.	Value	Units			Max			
Calibration			1	2/	Apply 0 V to pin 9 with D.U.T removed.							None	8	E ₁	V	V _{CAL} = 10 E ₁	-2	2	mV		
1 T _A = +25°C	V _{IO}	4001	2	3/	3.5 V	-26.5 V	Open	-9 V	-11.5 V	Open	Open	"	"	E ₂	V	V _{IO} = 10 (E ₂ – E ₁)	-3	3	mV		
		"	3	"	26.5 V	-3.5 V	"	14 V	11.5 V	"	"	"	"	E ₃	"	V _{IO} = 10 (E ₃ – E ₁)	"	"	"		
		"	4	"	15 V	-15 V	"	2.5 V	0 V	"	"	"	"	E ₄	"	V _{IO} = 10 (E ₄ – E ₁)	"	"	"		
		"	5	"	7 V	-3 V	"	4.5 V	2 V	"	"	"	"	E ₅	"	V _{IO} = 10 (E ₅ – E ₁)	"	"	"		
		"	6	"	3 V	-7 V	"	0.5 V	-2 V	"	"	"	"	E ₆	"	V _{IO} = 10 (E ₆ – E ₁)	"	"	"		
		"	6	"	3 V	-7 V	"	0.5 V	-2 V	"	"	"	"	E ₆	"	V _{IO} = 10 (E ₆ – E ₁)	"	"	"		
	I _{IB}	4001	7	"	3.5 V	-26.5 V	"	-9 V	-11.5 V	"	"	K1	"	E ₇	"	I _{IB} = 100 (E ₂ – E ₇)	-1	25	nA		
		"	8	"	26.5 V	-3.5 V	"	14 V	11.5 V	"	"	"	"	E ₈	"	I _{IB} = 100 (E ₃ – E ₈)	"	"	"		
		"	9	"	15 V	-15 V	"	2.5 V	0 V	"	"	"	"	E ₉	"	I _{IB} = 100 (E ₄ – E ₉)	"	"	"		
		"	10	"	7 V	-3 V	"	4.5 V	2 V	"	"	"	"	E ₁₀	"	I _{IB} = 100 (E ₅ – E ₁₀)	"	"	"		
		"	11	"	3 V	-7 V	"	0.5 V	-2 V	"	"	"	"	E ₁₁	"	I _{IB} = 100 (E ₆ – E ₁₁)	"	"	"		
	Z _I		12		Calculate value using data from tests 2, 3, 7, and 8											Z _I = 0.23 / E ₂ +E ₈ –E ₃ –E ₇			2		GΩ
	A _E		13		3.5 V	-26.5 V	Open	-9 V	-11.5 V	Open	Open	K4	8	E ₁₂	V	A _E = (E ₁₂ – E ₁₃) / 23	-0.005	.005	%		
					26.5 V	-3.5 V	"	14 V	11.5 V	"	"	K4	"	E ₁₃	"		"	"	"		
			14	-02 only	5 V	-25 V	"	-7.5 V	-10 V	"	"	K7	"	E ₁₄	"	A _E = (E ₁₄ – E ₁₅) / 20	-0.005	.005	"		
				25 V	-5 V	"	12.5 V	10 V	"	"	K7	"	E ₁₅	"		"	"	"			
		15		3 V	-7 V	"	0.5 V	-2 V	"	"	K4	"	E ₁₆	"	A _E = (E ₁₆ – E ₁₇) / 4	-0.02	.02	"			
				7 V	-3 V	"	4.5 V	2 V	"	"	K4	"	E ₁₇	"		"	"	"			
V _{IO} ADJ(+)		16		15 V	-15 V	"	2.5 V	0 V	"	"	K5	"	E ₁₈	"	V _{IO} ADJ(+) = 10 (E ₄ – E ₁₈)	6		mV			
V _{IO} ADJ(-)		17		15 V	-15 V	"	2.5 V	0 V	"	"	K8	"	E ₁₉	"	V _{IO} ADJ(-) = 10 (E ₄ – E ₁₉)		-6	mV			
+PSRR	4003	18		18 V	-18 V	"	2.5 V	0 V	"	"	None	"	E ₂₀	"	+PSRR = 20 log 600/(E ₂₀ – E ₂₁)	80		dB			
				12 V	-18 V	"	-0.5 V	-3 V	"	"	None	"	E ₂₁	"		"	"	"			
-PSRR	4003	19		18 V	-12 V	"	5.5 V	3 V	"	"	None	"	E ₂₂	"	-PSRR = 20 log 600/(E ₂₀ – E ₂₂)	80		dB			
FRR		20	4/ 5/	15 V	-15 V	See fig. 4 timing		0 V	"	"	K1, K2	"	E ₂₃	"	FRR = 20 log 1150/(E ₂₄ – E ₂₃)	86		dB			
		21	"	"	"			"	"	"	"	"	E ₂₄	"	FRR = 20 log 1150/(E ₂₅ – E ₂₄)	"	"	"			
		22	"	"	"			"	"	"	"	"	E ₂₅	"	FRR = 20 log 1150/(E ₂₆ – E ₂₅)	"	"	"			
		23	"	"	"			"	"	"	"	"	E ₂₆	"	FRR = 20 log 1150/(E ₂₇ – E ₂₆)	"	"	"			
					"	"	See fig. 6 timing		"	"	"	"	"	E ₂₇	"		"	"	"		
	24	6/	15 V	-15 V	0 V	-10 V			0 V	K3	"	E ₂₈	"	ZO = 5 (E ₂₉ – E ₂₈)		"	Ω				
			"	"	10 V	0 V			0 V	"	"	E ₂₉	"		"	"	"				
			"	"	"	"			"	"	"	E ₃₀	"		"	"	"				
ZO	V _{HS}		25	5/ 7/	3.5 V	-26.5 V	See fig. 7 timing		-11.5 V	Open	Open	K6	"	E ₃₁	"	V _{HS} = 10 (E ₃₁ – E ₃₀)	-2	"	mV		
				"	3.5 V	-26.5 V			-11.5 V	"	"	"	"	E ₃₂	"		"	"	"		
			26	"	26.5 V	-3.5 V			11.5 V	"	"	"	"	E ₃₃	"	V _{HS} = 10 (E ₃₃ – E ₃₂)	"	"	"		
				26.5 V	-3.5 V	11.5 V			"	"	"	"	E ₃₃	"		"	"	"			
I _{CC}		27		15 V	-15 V	Open	2.5 V	0 V	"	"	None	2	I ₁	mA	I _{CC} = I ₁	1	5.5	mA			
														Type 02	1	6.0	mA				
R _{SC}		28		15 V	-15 V	0 V	2.5 V	0 V	"	0 V	K1,K2,K3	7	I ₂	mA	RSC = 400 / (I ₃ – I ₂)	75	400	Ω			
				15 V	-15 V	0.4 V	2.5 V	0 V	"	0 V	K1,K2,K3	7	I ₃	mA							

See footnotes at end of table.

TABLE III. Group A inspection for all device types – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Notes	Adapter pin numbers							Energized relays	Measured pin			Equation $\frac{1}{2}$	Limits		Unit
					1	2	3	4	5	6	7		No.	Value	Units		Min	Max	
1 $T_A = +25^\circ\text{C}$	I_{IH}		29	<u>8/</u>	8.5 V	-21.5 V	Open	5.5 V	0 V	Open	Open	None	4	I_4	μA	$I_{IH} = I_4$	0	10	μA
			30	"	8.5 V	-21.5 V	"	0 V	5.5 V	"	"	"	5	I_5	"	$I_{IH} = I_5$	0	10	"
	I_{IL}		31	"	21.5 V	-8.5 V	"	0 V	5.5 V	"	"	"	4	I_6	"	$I_{IL} = I_6$	-1.0	1.0	"
			32	"	21.5 V	-8.5 V	"	5.5 V	0 V	"	"	"	5	I_7	"	$I_{IL} = I_7$	-1.0	1.0	"
	$I_{OS(+)}$	3011	33	<u>9/</u>	15 V	-15 V	10 V	2.5 V	0 V	"	"	K1,K2	9	I_8	mA	$I_{OS(+)} = I_8$ Type 01 Type 02	-25		mA
	$I_{OS(-)}$	3011	34	<u>9/</u>	15 V	-15 V	-10 V	2.5 V	0 V	"	"	K1,K2	9	I_9	"	$I_{OS(-)} = I_9$ Type 01 Type 02	-30		mA
	$I_{HL(+)}$		35	<u>10/</u>	3.5 V	-26.5 V	See fig. 8 timing $\Delta t = 100 \text{ ms}$	-11.5 V	"	"	"	None	8	E_{34}	mV	$I_{HL(+)} = (E_{35} - E_{34})$	-100	100	pA
													"	E_{35}	mV		"	"	"
	$I_{HL(-)}$		36	<u>10/</u>	26.5 V	-3.5 V		11.5 V	"	"	"	"	"	E_{36}	mV	$I_{HL(-)} = (E_{37} - E_{36})$	"	"	"
													"	E_{37}	mV		"	"	"
	$I_{CH(+)}$		37	<u>11/</u>	15 V	-15 V	11.5 V	2.5 V	0 V	"	9.5 V	K1,K2,K3	7	I_{10}	mA	$I_{CH(+)} = I_{10}$		-3	mA
	$I_{CH(-)}$		38	<u>11/</u>	"	"	-11.5 V	2.5 V	"	"	-9.5 V	"	"	I_{11}	mA	$I_{CH(-)} = I_{11}$	3		mA
	$V_{TH(H)}$		39	<u>12/</u>	"	"	-2 V	2.0 V	"	"	0 V	"	"	I_{12}	mA	$V_{TH(H)} \leq 2 \text{ V if } I_{12} \geq 1 \text{ mA}$	1		mA
	$V_{TH(L)}$		40	<u>12/</u>	"	"	-2 V	0.8 V	"	"	0 V	"	"	I_{13}	μA	$V_{TH(L)} \leq 0.5 \text{ V if } -10 < I_{13} < 10 \mu\text{A}$	-10	10	μA
2 $T_A = +125^\circ\text{C}$	V_{IO}	4001	41	<u>2/ 3/</u>	3.5 V	-26.5 V	Open	-9 V	-11.5 V	Open	Open	None	8	E_{38}	V	$V_{IO} = 10 (E_{38} - E_1)$ $V_{IO} = 10 (E_{39} - E_1)$ $V_{IO} = 10 (E_{40} - E_1)$ $V_{IO} = 10 (E_{41} - E_1)$ $V_{IO} = 10 (E_{42} - E_1)$	-5	5	mV
		"	42	"	26.5 V	-3.5 V	"	14 V	11.5 V	"	"	"	"	E_{39}	"		"	"	"
		"	43	"	15 V	-15 V	"	2.5 V	0 V	"	"	"	"	E_{40}	"		"	"	"
		"	44	"	7 V	-3 V	"	4.5 V	2 V	"	"	"	"	E_{41}	"		"	"	"
		"	45	"	3 V	-7 V	"	0.5 V	-2 V	"	"	"	"	E_{42}	"		"	"	"
	I_{IB}	4001	46	<u>3/</u>	3.5 V	-26.5 V	"	9 V	-11.5 V	"	"	K1	"	E_{43}	"	$I_{IB} = 100 (E_{38} - E_{43})$ $I_{IB} = 100 (E_{39} - E_{44})$ $I_{IB} = 100 (E_{40} - E_{45})$ $I_{IB} = 100 (E_{41} - E_{46})$ $I_{IB} = 100 (E_{42} - E_{47})$	-25	75	nA
		"	47	"	26.5 V	-3.5 V	"	14 V	11.5 V	"	"	"	"	E_{44}	"		"	"	"
		"	48	"	15 V	-15 V	"	2.5 V	0 V	"	"	"	"	E_{45}	"		"	"	"
		"	49	"	7 V	-3 V	"	4.5 V	2 V	"	"	"	"	E_{46}	"		"	"	"
		"	50	"	3 V	-7 V	"	0.5 V	-2 V	"	"	"	"	E_{47}	"		"	"	"
	Z_I		51	Calculate value using data from tests 41, 42, 46, and 47.												$Z_I = 0.23 / E_{38} + E_{44} - E_{39} - E_{43} $	1		$\text{G}\Omega$
	A_E		52		3.5 V	-26.5 V	Open	-9 V	-11.5 V	Open	Open	K4	8	E_{48}	V	$A_E = (E_{48} - E_{49}) / 23$	-0.02	0.02	%
					26.5 V	-3.5 V	"	14 V	11.5 V	"	"	K4	"	E_{49}	"				"
			53	-02 only	5 V	-25 V	"	-7.5 V	-10 V	"	"	K7	"	E_{50}	"		-0.02	0.02	"
	$V_{IO \text{ ADJ}(+)}$				25 V	-5 V	"	12.5 V	10 V	"	"	K7	"	E_{51}	"	$A_E = (E_{50} - E_{51}) / 20$			"
			54		3 V	-7 V	"	0.5 V	-2 V	"	"	K4	"	E_{52}	"		-0.04	0.04	"
					7 V	-3 V	"	4.5 V	2 V	"	"	K4	"	E_{53}	"				"
	$V_{IO \text{ ADJ}(-)}$		55		15 V	-15 V	"	2.5 V	0 V	"	"	K5	"	E_{54}	"	$V_{IO \text{ ADJ}(+)} = 10 (E_{40} - E_{54})$	6		mV
			56		15 V	-15 V	"	2.5 V	0 V	"	"	K8	"	E_{55}	"	$V_{IO \text{ ADJ}(-)} = 10 (E_{40} - E_{55})$		-6	mV

See footnotes at end of time.

TABLE III. Group A inspection for all device types – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Notes	Adapter pin numbers							Energized relays	Measured pin			Equation $\frac{1}{2}$	Limits		Unit
					1	2	3	4	5	6	7		No.	Value	Units			Max	
2 $T_A = +125^{\circ}\text{C}$	+PSRR	4003	57		18 V 12 V	-18 V -18 V	Open "	2.5 V -0.5 V	0 V -3 V	Open "	Open "	None None	8 "	E ₅₆ E ₅₇	V "	+PSRR = 20 log 600/(E ₅₆ – E ₅₇)	80 "		dB
	-PSRR	4003	58		18 V	-12 V	"	5.5 V	3 V	"	"	None	"	E ₅₈	"	-PSRR = 20 log 600/(E ₅₆ – E ₅₈)	80 "		dB
	FRR		59	4/ 5/ 13/	15 V	-15 V	See fig. 4 timing wave- forms and fig. 19	0 V	"	"	"	K1, K2	11	E ₅₉	"	FRR = 20 log 1150/(E ₆₀ – E ₅₉) FRR = 20 log 1150/(E ₆₁ – E ₆₀) FRR = 20 log 1150/(E ₆₂ – E ₆₁) FRR = 20 log 1150/(E ₆₃ – E ₆₂)	80 "		dB
			60	"	"	"		"	"	"	"	E ₆₀	"	"	"				
			61	"	"	"		"	"	"	"	E ₆₁	"	"	"				
			62	"	"	"		"	"	"	"	E ₆₂ E ₆₃	"	"	"				
	Z _O		63	6/ 13/ "	15 V 15 V	-15 V -15 V	See fig. 6 and fig. 19	0 V 0 V	-10 V 10 V	0 V 0 V	K3 K3	" "	E ₆₄ E ₆₅	" "	Z _O = 5 (E ₆₅ – E ₆₄)			Ω	
	V _{HS}		64	5/ 7/ 13/	3.5 V	-26.5 V		See fig. 7 and fig. 19	-11.5 V	Open	Open	K6 "	" "	E ₆₆ E ₆₇	" "	V _{HS} = 10 (E ₆₇ – E ₆₆)	-2 "	5	mV
			65	"	26.5 V	-3.5 V	11.5 V		"	"	"	"	E ₆₈ E ₆₉	" "	V _{HS} = 10 (E ₆₉ – E ₆₈)	-5 "	5	"	
	I _{CC}		66		15 V	-15 V	Open	2.5 V	0 V	"	"	None	2	I ₁₄	mA	I _{CC} = I ₁₄ Type 01 Type 02	1	5.5	mA
																	1	6.0	mA
	R _{SC}		67		15 V 15 V	-15 V -15 V	0 V 0.4 V	2.5 V 2.5 V	0 V 0 V	" "	0 V 0 V	K1,K2,K3	7	I ₁₅ I ₁₆	mA mA	R _{SC} = 400 / (I ₁₆ – I ₁₅)	75	400	Ω
	I _{IH}		68 69		8.5 V	-21.5 V	Open	5.5 V	0 V	Open	Open	None	4 5	I ₁₇ I ₁₈	μA	I _{IH} = I ₁₇ I _{IH} = I ₁₈	0 0	10 10	μA
	I _{IL}		70 71		21.5 V	-8.5 V	"	0 V	5.5 V	"	"	"	4 5	I ₁₉ I ₂₀	"	I _{IL} = I ₁₉ I _{IL} = I ₂₀	-1.0 -1.0	1.0 1.0	"
	I _{OS} (+)	3011	72	9/	15 V	-15 V	10 V	2.5 V	0 V	"	"	K1,K2	9	I ₂₁	mA	I _{OS} (+) = I ₈ Type 01 Type 02	-25 -30		mA
I _{OS} (-)	3011	73	9/	15 V	-15 V	-10 V	2.5 V	0 V	"	"	K1,K2	9	I ₂₂	"	I _{OS} (-) = I ₉ Type 01 Type 02		30	"	
I _{IHL} (+)		74	10/ 13/	3.5 V	-26.5 V	See fig. 8 and fig. 19 Δt = 10 ms	-11.5 V	"	"	None	11	E ₇₀	mV	I _{IHL} (+) = 0.1 (E ₇₁ – E ₇₀)	-25 -30	50	nA		
															"	E ₇₁	mV	"	"
I _{IHL} (-)		75	10/ 13/	26.5 V	-3.5 V		11.5 V	"	"	"	"	E ₇₂	mV	I _{IHL} (-) = 0.1 (E ₇₃ – E ₇₂)	"	"	"		
															"	E ₇₃	mV	"	"
I _{CH} (+)		76	11/	15 V	-15 V	11.5 V	2.5 V	0 V	"	9.5 V	K1,K2,K3	7	I ₂₃	mA	I _{CH} (+) = I ₂₃		-2	mA	
I _{CH} (-)		77	11/	"	"	-11.5 V	2.5 V	"	"	-9.5 V	"	"	I ₂₄	mA	I _{CH} (-) = I ₂₄	2		mA	
V _{TH} (H)		78	12/	"	"	-2 V	2.0 V	"	"	0 V	"	"	I ₂₅	mA	V _{TH} (H) ≤ 2 V if I ₂₅ ≥ 1 mA	1		mA	
V _{TH} (L)		79	12/	"	"	-2 V	0.8 V	"	"	0 V	"	"	I ₂₆	μA	V _{TH} (L) ≥ 0.8 V if -10 < I ₂₆ < 10 μA	-10	10	μA	

See footnotes at end of table.

TABLE III. Group A inspection for all device types – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Notes	Adapter pin numbers							Energized relays	Measured pin			Equation <u>1/</u>	Limits		Unit
					1	2	3	4	5	6	7		No.	Value	Units			Max	
3 T _A = -55°C	V _{IO}	4001	80	<u>3/</u>	3.5 V	-26.5 V	Open	-9 V	-11.5 V	Open	Open	None	8	E74	V	V _{IO} = 10 (E74 – E1)	-5	5	mV
		"	81	"	26.5 V	-3.5 V	"	14 V	11.5 V	"	"	"	"	E75	"	V _{IO} = 10 (E75 – E1)	"	"	"
		"	82	"	15 V	-15 V	"	2.5 V	0 V	"	"	"	"	E76	"	V _{IO} = 10 (E76 – E1)	"	"	"
		"	83	"	7 V	-3 V	"	4.5 V	2 V	"	"	"	"	E77	"	V _{IO} = 10 (E77 – E1)	"	"	"
		"	84	"	3 V	-7 V	"	0.5 V	-2 V	"	"	"	"	E78	"	V _{IO} = 10 (E78 – E1)	"	"	"
	I _{IB}	4001	85	<u>3/</u>	3.5 V	-26.5 V	"	-9 V	-11.5 V	"	"	K1	"	E79	"	I _{IB} = 100 (E74 – E79)	-25	75	nA
		"	86	"	26.5 V	-3.5 V	"	14 V	11.5 V	"	"	"	"	E80	"	I _{IB} = 100 (E75 – E80)	"	"	"
		"	87	"	15 V	-15 V	"	2.5 V	0 V	"	"	"	"	E81	"	I _{IB} = 100 (E76 – E81)	"	"	"
		"	88	"	7 V	-3 V	"	4.5 V	2 V	"	"	"	"	E82	"	I _{IB} = 100 (E77 – E82)	"	"	"
		"	89	"	3 V	-7 V	"	0.5 V	-2 V	"	"	"	"	E83	"	I _{IB} = 100 (E78 – E83)	"	"	"
	Z _I		90		Calculate value using data from tests 80, 81, 85, and 86											Z _I = 0.23 / E74 + E80 – E75 – E79	1		GΩ
	A _E		91		3.5 V	-26.5 V	Open	-9 V	-11.5 V	Open	Open	K4	8	E84	V	A _E = (E84 – E85) / 23	-0.2	.02	%
					26.5 V	-3.5 V	"	14 V	11.5 V	"	"	K4	"	E85	"				"
			92	-02 only	5 V	-25 V	"	-7.5 V	-10 V	"	"	K7	"	E86	"	A _E = (E86 – E87) / 20	-0.2	.02	"
					25 V	-5 V	"	12.5 V	10 V	"	"	K7	"	E87	"				"
			93		3 V	-7 V	"	0.5 V	-2 V	"	"	K4	"	E88	"	A _E = (E88 – E89) / 4	-0.4	.04	"
					7 V	-3 V	"	4.5 V	2 V	"	"	K4	"	E89	"				"
	V _{IO} ADJ(+)		94		15 V	-15 V	"	2.5 V	0 V	"	"	K5	"	E90	"	V _{IO} ADJ(+) = 10 (E76 – E90)	6		mV
	V _{IO} ADJ(-)		95		15 V	-15 V	"	2.5 V	0 V	"	"	K8	"	E91	"	V _{IO} ADJ(-) = 10 (E76 – E91)		-6	mV
	+PSRR	4003	96		18 V	-18 V	Open	2.5 V	0 V	Open	Open	None	"	E92	"	+PSRR = 20 log 600/(E92 – E93)	80		dB
					12 V	-18 V	"	-0.5 V	-3 V	"	"	None	"	E93	"		"		
	-PSRR	4003	97		18 V	-12 V	"	5.5 V	3 V	"	"	None	"	E94	"	-PSRR = 20 log 600/(E92 – E94)	80		dB
			98	<u>4/ 5/</u>	15 V	-15 V	See fig. 4 timing		0 V	"	"	K1, K2	"	E95	"	FRR = 20 log 1150/(E96 – E95)	80		dB
			99	"	"	"			"	"	"	"	"	E96	"	FRR = 20 log 1150/(E97 – E96)	"		"
			100	"	"	"			"	"	"	"	"	E97	"	FRR = 20 log 1150/(E98 – E97)	"		"
			101	"	"	"			"	"	"	"	"	E98	"	FRR = 20 log 1150/(E99 – E98)	"		"
				"	"	"			"	"	"	"	"	E99	"		"		"
	Z _O		102	<u>6/</u>	15 V	-15 V	See fig. 6.		0 V	-10 V	0 V	K3	"	E100	"	Z _O = 5 (E101 – E100)			Ω
					15 V	-15 V			0 V	10 V	0 V	K3	"	E101	"				
	V _{HS}		103	<u>5/ Z/</u>	3.5 V	-26.5 V	See fig. 7		-11.5 V	Open	Open	K6	"	E102	"	V _{HS} = 10 (E103 – E102)	-5	5	mV
				"	3.5 V	-26.5 V			-11.5 V	"	"	"	"	E103	"		"		"
			104	"	26.5 V	-3.5 V			11.5 V	"	"	"	"	E104	"	V _{HS} = 10 (E105 – E104)	-5	5	"
				"	26.5 V	-3.5 V			11.5 V	"	"	"	"	E105	"		"		"
	I _{CC}		105		15 V	-15 V	Open	2.5 V	0 V	"	"	None	2	I27	mA	I _{CC} = I27	1	6.5	mA
																Type 01			
																Type 02	1	7.0	mA
	R _{SC}		106		15 V	-15 V	0 V	2.5 V	0 V	"	0 V	K1,K2,K3	7	I28	mA	R _{SC} = 400 / (I29 – I28)	75	400	Ω
					15 V	-15 V	0.4 V	2.5 V	0 V	"	0 V	"	"	I29	mA				

See footnotes at end of table.

TABLE III. Group A inspection for all device types – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test no.	Notes	Adapter pin numbers							Energized relays	Measured pin			Equation <u>1/</u>	Limits		Unit	
					1	2	3	4	5	6	7		No.	Value	Units		Min	Max		
3 T _A = -55°C	I _{IH}		107	<u>1/</u>	8.5 V	-21.5 V	Open	5.5 V	0 V	Open	Open	None	4	I ₃₀	μA	I _{IH} = I ₃₀	0	10	μA	
			108	"	"	"	"	0 V	5.5 V	"	"	"	5	I ₃₁	"	I _{IH} = I ₃₁	0	10	"	
		110	"	"	"	"	5.5 V	0 V	"	"	"	5	I ₃₃	"	I _{IL} = I ₃₃	-1.0	1.0	"		
		30	"																	
	V _{TH} (L)		116	<u>12/</u>	"	"	-2 V	0.8 V	"	"	0 V	"	"	I ₃₉	mA	V _{TH} (L) ≥ 0.8 V if -10 ≤ I ₃₉ ≤ 10 μA	-10	10	μA	
	7 T _A = +25°C	t _{aq}		117	<u>14/ 15/</u>	15 V	-15 V	See fig. 9, 10, and 11		0 V	Open	Open	K1,K2,K6	11	t ₁	μs	t _{aq} = t ₁ t _{aq} = t ₂ t _{aq} = t ₃ t _{aq} = t ₄		25	μs
				118	"	"			"	"	Open	"	"	t ₂	"	"				
				119	"	"			"	"	"	"	"	t ₃	"	"				
				120	"	"			"	"	"	"	"	t ₄	"	"				
		122	"	"			"	"	"	"	"	t ₆	"	"						
		123	"	"			"	"	"	"	"	t ₇	"	"						
		124	"	"			"	"	"	"	"	t ₈	"	"						
		128	"	26.5 V	-3.5 V			"	"	"	"	"	t ₁₁	μs	TR _(ts) = Δt = t ₁₁		2.5	μs		
		130	"	26. V	-3.5 V			"	"	"	"	"	V ₀₂ , ΔV ₀₂	mV	TR _(OS) = 100 ΔV ₀₂ / V ₀₂		40	%		
en _(H)			132	<u>20/</u>	15 V	-15 V	See fig. 17		"	"	"	"	"	E ₁₀₈	mVrms	en _(H) = 0.1 E ₁₀₈		10	μVrms	
8 T _A = +125°C		ΔV _{IO} / ΔT			ΔV _{IO} / ΔT = [V _{IO} (test 43) – V _{IO} (test 4)] / 100°C												-20	20	μV/°C	
8 T _A = -55°C		ΔV _{IO} / ΔT	133		ΔV _{IO} / ΔT = [V _{IO} (test 82) – V _{IO} (test 4)] / 80°C												-20	20	μV/°C	

See footnotes at end of table.

TABLE III. Group A inspection – Continued.

- 1/ The equations take into account the test amplifier gain of 100 and other circuit constants so that the calculated value is in table I units.
- 2/ In order to remove test amplifier offset from the data values measure the offset of U1 on pin 8 with pin 9 grounded and the device under test removed. Software subtraction techniques shall be used to correct the data.
- 3/ Common mode input range conditions are exercised by grounding the signal input and swinging the power supplies to their nominal levels minus the common mode voltage.
For example for $V_{CM} = +11.5 \text{ V}$, $+V_{CC} = 15 \text{ V}$, $-11.5 = 3.5 \text{ V}$ and $-V_{CC} = -15 \text{ V} - 11.5 \text{ V} = -26.5 \text{ V}$.
- 4/ With a 0 V signal input the device under test logic input is switched from 5 V to 0 V. This resets the system in the hold mode. The test amplifier output is measured immediately after each 11.5 V change at the signal output.
- 5/ Logic input step changes should have a rise time of 0.5 μs or less.
- 6/ E28 and E29 are measured with the device under test in the hold mode and with the hold capacitor terminal grounded.
- 7/ For the hold mode step test, the first and second measurements are made with the device under test in the sample and hold modes, respectively. The hold measurements should be made within 50 μs of the device under test hold command, especially at $+125^\circ\text{C}$.
- 8/ High and low state logic input currents shall be measured over the common mode voltage range as shown.
- 9/ The output shall be shorted to ground for 25 ms or less.
- 10/ Hold leakage current at 25°C is determined by measuring the droop referred to the test amplifier output over a 100 ms interval.
- 11/ The charge current measurements on pin 7 are referenced to forced voltage of 9.5 V and -9.5 V , respectively.
- 12/ With worst case logic threshold voltages applied, the hold capacitor terminal output current is measured to determine if the device is in the correct operating mode. The logic threshold levels for $V_{TH(H)}$ and $V_{TH(L)}$ are guaranteed by measuring the hold capacitor current.
For $V_{TH(H)}$ hold capacitor current $\geq 1 \text{ mA}$. For $V_{TH(L)}$ hold capacitor current $\leq 10 \mu\text{A}$.
- 13/ Hold mode droop at 125°C due to high JFET leakage current will tend to mask the data for V_{HS} , Z_O , and FRR. To preclude this effect from happening, the test adapter sample/hold circuit, which is not at an elevated temperature, should be used to acquire and hold the data for the measurement system.
- 14/ Step the signal input from 0 V to +10 V. After a delay of $\approx 100 \mu\text{s}$, generate a 100 μs sample mode pulse. The difference between the input and device under test output is monitored with a 100 V/V differential amplifier followed by tester sample/hold circuit. Reduce the device under test sample mode pulse width until there is a 100 mV (.01%) change at the tester sample/hold output from the 100 μs pulse value. The sample mode pulse width for this condition is the acquisition time. Repeat the above procedure for input signal transitions of 10 V to 0 V, 0 V to -10 V , and -10 V to 0 V. Figure 10 shows an automatic flow chart method and figure 11 shows a simplified manual method for determining acquisition time.
- 15/ Even with a Teflon hold capacitor servicing the device under test sample hold circuit, dielectric absorption errors can occur when dynamic signals are applied to the device under test input. To minimize these errors, the error amplifier output should be measured immediately after the test event. The tester sample and hold circuit is used to hold the analog data for the slower responding automatic measurement system.

TABLE III. Group A inspection – Continued.

- 16/ Step the logic input from 5 V to 0 V with the input at 0 V. After a 2 μ s time delay, step the signal input up to 10 V. For this condition the device under test output should be $\approx$ 0 V. Gradually decrease the delay until a 100 mV (.01 %) shift occurs at the tester sample/hold output. Repeat the above procedure for input signal transitions of 10 V to 0 V, 0 V to -10 V, and -10 V to 0 V. The delay corresponding to the 100 mV shift is equal to the aperture time. See figures 12 through 15.
- 17/ Settling time is determined as shown on figure 18 as the time for the S/H to settle within 1 mV of final value after the hold command is given.
- 18/ Dynamic feedthrough rejection is determined in the hold mode with a signal input of 20 V_{PP} at a frequency of 1 kHz.
- 19/ Overshoot TR_(OS) and settling time TR_(ts) are indicative of the stability of the device
- 20/ Broadband noise en_(S) and en_(H) is measured with a 10,000 V/V low noise bandpass amplifier as shown on figure 17.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service, or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

TABLE IV. Group C end point electrical parameters.(T_A = 25°C, ±V_{CC} = ±15 V for all device types)

Table III test no.	Test	Limits		Delta limits		Units
		Min	Max	Min	Max	
4	V _{IO}	-3	+3	-0.5	+0.5	mV
9	I _{IB}	-1	25	-2.5	2.5	nA

6.0 NOTES

This section contains information of a general or explanatory nature that may be helpful, but it is not mandatory.

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of the specification.
- b. PIN and compliance identifier, if applicable (see 1.2).
- c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirements for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- i. Requirements for "JAN" marking.
- j. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43218-3990.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

A_E	Gain error. The ratio of "sample" mode output voltage swing to input common mode voltage swing expressed in percent. To the user this can be interpreted as the percentage deviation from unity gain.
$DR(+), DR(-)$	Droop rate. The rate of change of hold capacitor voltage with time due to "hold" mode leakage current. Note that $I_{HL} = C_H \times \Delta V_{HC} / \Delta t = C_H \times DR$.
DSE	Dynamic sampling error. The error introduced into the held output due to a changing analog input when the "hold" command is given. This error is proportional to the product of input signal slew rate, hold capacitance, and the series charge resistor.
$en(S), en(H)$	Noise. The total rms noise of the device that exists within a 10 Hz to 10 kHz "brickwall" bandwidth. Both "sample" mode, $en(S)$, and "hold" mode, $en(H)$, specifications exist.
FRR	Feedthrough rejection ratio. The ratio in dB of an input voltage change to a "hold" mode output voltage change.
$I_{CH}(+), I_{CH}(-)$	Hold capacitor charge current. The current that the input amplifier can supply to charge up the hold capacitor.
$I_{HL}(+), I_{HL}(-)$	Hold mode leakage current. The input bias current of the output buffer amplifier. This leakage current causes a droop rate error of the external hold capacitor.
I_{IB}	Input bias current. The current flowing into the signal input for any rated common mode voltage condition.
I_{IH}, I_{IL}	Logic input current. The current into a mode control input for a forward bias (high state), I_{IH} , condition or a below threshold (low state), I_{IL} , condition.
$I_{OS}(+), I_{OS}(-)$	Output short circuit current. The "sample" mode output short circuit current to ground with +10 V and -10 V applied at the input for $I_{OS}(+)$ and $I_{OS}(-)$, respectively.
+PSRR, -PSRR	Power supply rejection ratio. The ratio in dB of the change in $+V_{CC}$ or $-V_{CC}$ voltage to the change in offset voltage measured at the output with the opposite $-V_{CC}$ or $+V_{CC}$ voltage held constant.

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t_{ap}	Aperture time. The delay required between the "hold" command and a 10 volt input signal transition such that the resulting output change is less than 1 mV.
t_{aq}	Acquisition time. The time, in terms of minimum sample pulse width, that is required for the device to acquire a 10 volt full scale change to within a specified error band of final value for a specified hold capacitor size.
$TR_{(OS)}$	Transient response (overshoot). The percentage ratio of signal overshoot to the 100 mV final value. This parameter is related to circuit phase margin and stability.
$TR_{(ts)}$	Transient response (settling time). The small signal time interval from the application of a 100 mV pulse to the time when the output enters and remains within 10 percent of its final value.
t_s	Hold settling time. The time required for the output to settle within 1 mV of final value after the "hold" command is given.
V_{CM}	Common mode voltage. The voltage of the input terminal with respect to a voltage midway between $+V_{CC}$ and $-V_{CC}$.
V_{HC}	Hold capacitor voltage. The voltage "held" by the external hold capacitor.
V_{HS}	"Hold" step voltage. The output voltage change with a fixed input voltage when the device is switched from "sample" to "hold" mode with a 4 V logic signal.
V_{IO}	Input offset voltage. The "sample" mode output to input dc voltage for any rated common mode voltage condition.

6.6 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

<u>Military device type</u>	<u>Generic-industry type</u>
01	198
02	5537

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:	Preparing activity:
Army – CR	DLA - CC
Navy - EC	
Air Force - 11	Project 5962-2005-026
NASA - NA	
DLA – CC	
Review activities:	
Army - MI, SM	
Navy - AS, CG, MC, SH, TD	
Air Force – 03, 19, 99	

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://assist.daps.dla.mil>.