

MILITARY SPECIFICATION

MICROCIRCUITS, LINEAR, LOW POWER, LOW NOISE, BI-FET OPERATIONAL AMPLIFIERS, MONOLITHIC SILICON

Reactivated after 21 December 2004 and may be used for either new or existing design acquisition.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF-38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, BI-FET operational amplifiers. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.3)

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The BI-FET operational amplifiers shall be internally compensated and are distinguished by the following circuit characteristics:

Device type	Circuit
01	Single operational amplifier, BI-FET, low power
02	Dual operational amplifier, BI-FET, low power
03	Quad operational amplifier, BI-FET, low power
04	Single operational amplifier, BI-FET
05	Dual operational amplifier, BI-FET
06 1/	Quad operational amplifier, BI-FET

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outline. The case outline are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDIP1-F14 or CDFP2-F14	14	Flat pack
G	MACY1-X8	8	Can
H	GDIP1-F10 or CDFP2-F10	10	Flat pack
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line

1/ Devices may be monolithic or they may consist of two separate independent die.

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, 3990 East Broad St., Columbus, OH 43218-3990, or email linear@dsccl.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil>.

1.3 Absolute maximum ratings.

Supply voltage range	±18 V
Input voltage range	± 15 V <u>1/</u>
Differential input voltage range	± 30 V
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited <u>2/</u>
Lead temperature (soldering, 60 seconds)	+300°C
Junction temperature (T _J)	+175°C <u>3/</u>

1.4 Recommended operating conditions.

Supply voltage range	±5 V to ±15 V dc
Ambient temperature range (T _A)	-55°C to +125°C

1.5 Power and thermal characteristics.

Package	Case outline	Maximum allowable Power dissipation	Maximum θ _{JC}	Maximum θ _{JA}
14-lead dual-in-line	C	400 mW at T _A = +125°C	35°C/W	120°C/W
14-lead flat pack	D	350 mW at T _A = +125°C	60°C/W	140°C/W
8-lead can	G	330 mW at T _A = +125°C	40°C/W	150°C/W
10-lead flat pack	H	290 mW at T _A = +125°C	70°C/W	170°C/W
8-lead dual-in-line	P	400 mW at T _A = +125°C	35°C/W	120°C/W

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

- 1/ The absolute maximum negative input voltage is equal to the negative power supply voltage.
- 2/ Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
- 3/ For short term test (in the specific burn-in and steady-state life test configuration when required and up to 168 hours maximum), T_J = +275°C.

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. This slash sheet has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the Qualifying Activity.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity (DSCC-VA) upon request.

3.3.3 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. For dual and quad packages, the idle devices shall be connected as grounded followers or in the case of devices maintained in servo test loops, the idle devices shall have their outputs forced to ground via the output control voltage.

3.5.1 Offset null circuits. The nulling inputs shall be capable of being nulled 1 mV beyond the specified offset voltage limits for $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ using the circuit of figure 2.

3.5.2 Instability oscillations. The device shall be free of oscillations when operated in the test circuits of this specification.

3.6 Electrical test requirements. Electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.8 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8.1 Certification/compliance mark. The certification mark for device classes Q and V shall be "QML" or "Q" as required in MIL-PRF-38535. For class Q product built in accordance with A.3.2.2 of MIL-PRF-38535 or the alternative approved by the Qualifying Activity, the "QD" certification mark shall be used in place of the "QML" or "Q" certification mark.

3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 85 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Characteristics	Symbol	Conditions <u>1/</u> ±V _{CC} = ±15 V (see 3.4 and figure 3 unless otherwise specified)		Device type	Limits		Units
					Min	Max	
Input offset voltage	V _{IO}	±V _{CC} = ±5V at V _{CM} = 0 V, and ±V _{CC} = ±15 V at V _{CM} = ±11 V, 0 V	T _A = +25°C -55°C ≤ T _A ≤ +125°C	All	-5 -7	5 7	mV
Input offset voltage temperature sensitivity	ΔV _{IO} / ΔT	V _{CM} = 0 V		All	-30	30	μV/°C
Input offset current	I _{IO} <u>2/</u>	V _{CM} = 0 V, t ≤ 25 ms, T _J = +25°C		All	-100	100	pA
		V _{CM} = 0 V, t ≤ 25 ms, T _J = +125°C			-20	20	nA
Input bias current <u>3/ 4/</u>	+I _{IB} , -I _{IB}	V _{CC} = ±15 V, V _{CM} = +11 V, t ≤ 25 ms, T _J = +25°C		All	-200	1,200	pA
		V _{CC} = ±15 V, V _{CM} = +11 V, t ≤ 25 ms, T _J = +125°C			-10	70	nA
		±V _{CC} = ±15 V, V _{CM} = 0 V, t ≤ 25 ms, T _J = +25°C		All	-200	200	pA
		±V _{CC} = ±15 V, V _{CM} = 0 V, t ≤ 25 ms T _J = +125°C			-10	50	nA
		±V _{CC} = ±15 V, V _{CM} = -11 V, t ≤ 25 ms, T _J = +25°C		All	-400	200	pA
		±V _{CC} = ±15 V, V _{CM} = -11 V, t ≤ 25 ms, T _J = +125°C			-10	50	nA
Power supply rejection ration	+PSRR	+V _{CC} = 20 V, 10 V; -V _{CC} = -15 V		All	80		dB
	-PSRR	+V _{CC} = 15 V; -V _{CC} = -20 V, -10 V			80		
Input voltage <u>5/</u> common mode rejection	CMR	-11 V ≤ V _{CM} ≤ 11 V		All	80		dB
Adjustment for <u>6/</u> input offset voltage	V _{IO} (ADJ+)	V _{CM} = 0 V		01, 02 04, 05	+8		mV
	V _{IO} (ADJ-)	V _{CM} = 0 V				-8	
Output short <u>7/</u> circuit current (for positive output)	I _{OS} (+)	t ≤ 25 ms (short circuit to ground)		01, 02, 03	-40		mA
				04, 05, 06	-80		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Characteristics	Symbol	Conditions <u>1/</u> $\pm V_{CC} = \pm 15\text{ V}$ (see 3.4 and figure 3 unless otherwise specified)	Device type	Limits		Units
				Min	Max	
Output short circuit <u>7/</u> current (for negative output)	$I_{OS(-)}$	$t \leq 25\text{ ms}$ (short circuit to ground)	01, 02, 03		40	mA
			04, 05, 06		80	
Supply current (per amplifier)	I_{CC}	$T_A = -55^\circ\text{C}$	01, 02, 03		0.3	mA
			04, 05, 06		4	
		$+25^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	01, 02, 03		0.3	
			04, 05, 06		3.5	
Output voltage swing (maximum)	$+V_{OP},$ $-V_{OP}$	$R_L = 10\text{ k}\Omega$	All	± 12		V
		$R_L = 2\text{ k}\Omega$	04, 05, 06	± 10		
Open loop voltage <u>8/</u> gain (single ended)	$A_{VS(+)}$	$V_{OUT} = 0\text{ V to } 10\text{ V}, R_L = 10\text{ k}\Omega,$ $T_A = +25^\circ\text{C}$	01, 02, 03	5		V/mV
		$V_{OUT} = 0\text{ V to } 10\text{ V}, R_L = 10\text{ k}\Omega,$ $T_A = -55^\circ\text{C}, +125^\circ\text{C}$		4		
		$V_{OUT} = 0\text{ V to } 10\text{ V}, R_L = 2\text{ k}\Omega,$ $T_A = +25^\circ\text{C}$	04, 05, 06	50		
		$V_{OUT} = 0\text{ V to } 10\text{ V}, R_L = 2\text{ k}\Omega,$ $T_A = -55^\circ\text{C}, +125^\circ\text{C}$		25		
	$A_{VS(-)}$	$V_{OUT} = -10\text{ V to } 0\text{ V}, R_L = 10\text{ k}\Omega,$ $T_A = +25^\circ\text{C}$	01, 02, 03	5		
		$V_{OUT} = -10\text{ V to } 0\text{ V}, R_L = 10\text{ k}\Omega,$ $T_A = -55^\circ\text{C}, +125^\circ\text{C}$		4		
		$V_{OUT} = -10\text{ V to } 0\text{ V}, R_L = 2\text{ k}\Omega,$ $T_A = +25^\circ\text{C}$	04, 05, 06	50		
		$V_{OUT} = -10\text{ V to } 0\text{ V}, R_L = 2\text{ k}\Omega,$ $T_A = -55^\circ\text{C}, +125^\circ\text{C}$		25		
Open loop voltage <u>8/</u> gain (single ended)	A_{VS}	$\pm V_{CC} = \pm 5\text{ V}; R_L = 10\text{ k}\Omega$ $V_{OUT} = \pm 2\text{ V}$	01, 02, 03	3		V/mV
			04, 05, 06	20		
Transient response rise time	$TR_{(tr)}$	$R_L = 10\text{ k}\Omega, A_V = 1, V_{IN} = 50\text{ mV};$ $C_L = 100\text{ pF},$ (see figure 4)	01, 02, 03		400	ns
		$R_L = 2\text{ k}\Omega, A_V = 1, V_{IN} = 50\text{ mV};$ $C_L = 100\text{ pF},$ (see figure 4)	04, 05, 06		200	

See footnotes at end of table.

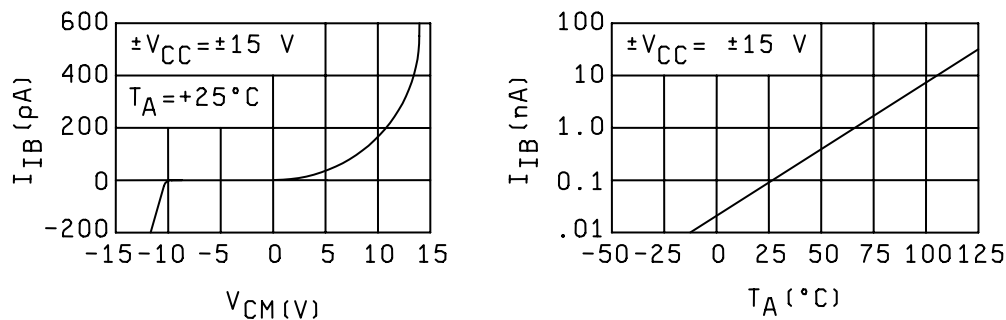
TABLE I. Electrical performance characteristics – Continued.

Characteristics	Symbol	Conditions <u>1/</u> $\pm V_{CC} = \pm 15\text{ V}$ (see 3.4 and figure 3 unless otherwise specified)	Device type	Limits		Units
				Min	Max	
Transient response overshoot	$TR_{(os)}$	$R_L = 10\text{ k}\Omega$, $A_V = 1$, $V_{IN} = 50\text{ mV}$; $C_L = 100\text{ pF}$, (see figure 4)	01, 02, 03		20	%
		$R_L = 2\text{ k}\Omega$, $A_V = 1$, $V_{IN} = 50\text{ mV}$; $C_L = 100\text{ pF}$, (see figure 4)	04, 05, 06		40	
Slew rate	$SR(+)$ and $SR(-)$	$V_{IN} = \pm 5\text{ V}$; $A_V = 1$, (see figure 4), $T_A = +25^\circ\text{C}$	01, 02, 03	0.8		$\text{V}/\mu\text{s}$
			04, 05, 06	7		
		$V_{IN} = \pm 5\text{ V}$; $A_V = 1$, (see figure 4), $T_A = -55^\circ\text{C}, +125^\circ\text{C}$	01, 02, 03	0.7		
			04, 05, 06	5		
Settling time	$ts+$ and $ts(-)$	(0.1 percent error), $A_V = 1$, (see figure 5), $T_A = 25^\circ\text{C}$	01, 02, 03		6,000	ns
			04, 05, 06		1,500	
Noise (referred to input) broadband	$NI_{(BB)}$	Bandwidth = 10 kHz, (see figure 6), $T_A = 25^\circ\text{C}$	All		15	$\mu\text{V rms}$
Noise (referred to input) popcorn	$NI_{(PC)}$	Bandwidth = 10 kHz, (see figure 6), $T_A = 25^\circ\text{C}$	All		80	$\mu\text{V pk}$
Channel separation <u>9/</u>	CS	See figure 7, $T_A = 25^\circ\text{C}$	02, 03, 05, 06	80		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

- 1/ For devices marked with the “Q” certification mark, the parameters listed herein may be guaranteed if not tested to the limits specified in accordance with the manufacturer’s QM plan.
- 2/ I_{IO} is calculated as the difference between $+I_{IB}$ and $-I_{IB}$.
- 3/ Bias current is actually junction leakage current which double (approximately) for each 10°C increase in junction temperature (T_J). To minimize thermal transient due to warm-up, measurements for bias current must be made within 25 ms after power is first applied to the device for test.
- 4/ Bias current is sensitive to power supply voltage, common mode voltage, and temperature as shown by the following typical curves:



- 5/ CMR is calculated from V_{IO} measurements at $V_{CM} = +11$ V and -11 V.
- 6/ Offset adjustment pins do not exist for 8-pin dual and 14-pin quad packages.
- 7/ Continuous limits shall be considerable lower. Protection for shorts to either supply exists providing that $T_J(\text{max}) \leq 175^{\circ}\text{C}$.
- 8/ Because of thermal feedback effects from output to input, open loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional acquisition documents.
- 9/ Channel separation is applicable only for the dual and quad devices.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 4	1*, 2, 3, 4
Group A test requirements	1, 2, 3, 4, 5, 6, 7, 8, 12	1, 2, 3, 4, 5, 6, 7, 8, 12
Group B electrical test parameters when using the method 5005 QCI option	1,2,3, and table IV delta limits	N/A
Group C end-point electrical parameters	1,2,3, and table IV delta limits	1 and table IV delta limits
Additional electrical subgroups for group C periodic inspections	N/A	---
Group D end-point electrical parameters	1, 2, 3	1

*PDA applies to subgroup 1.

4. VERIFICATION.

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

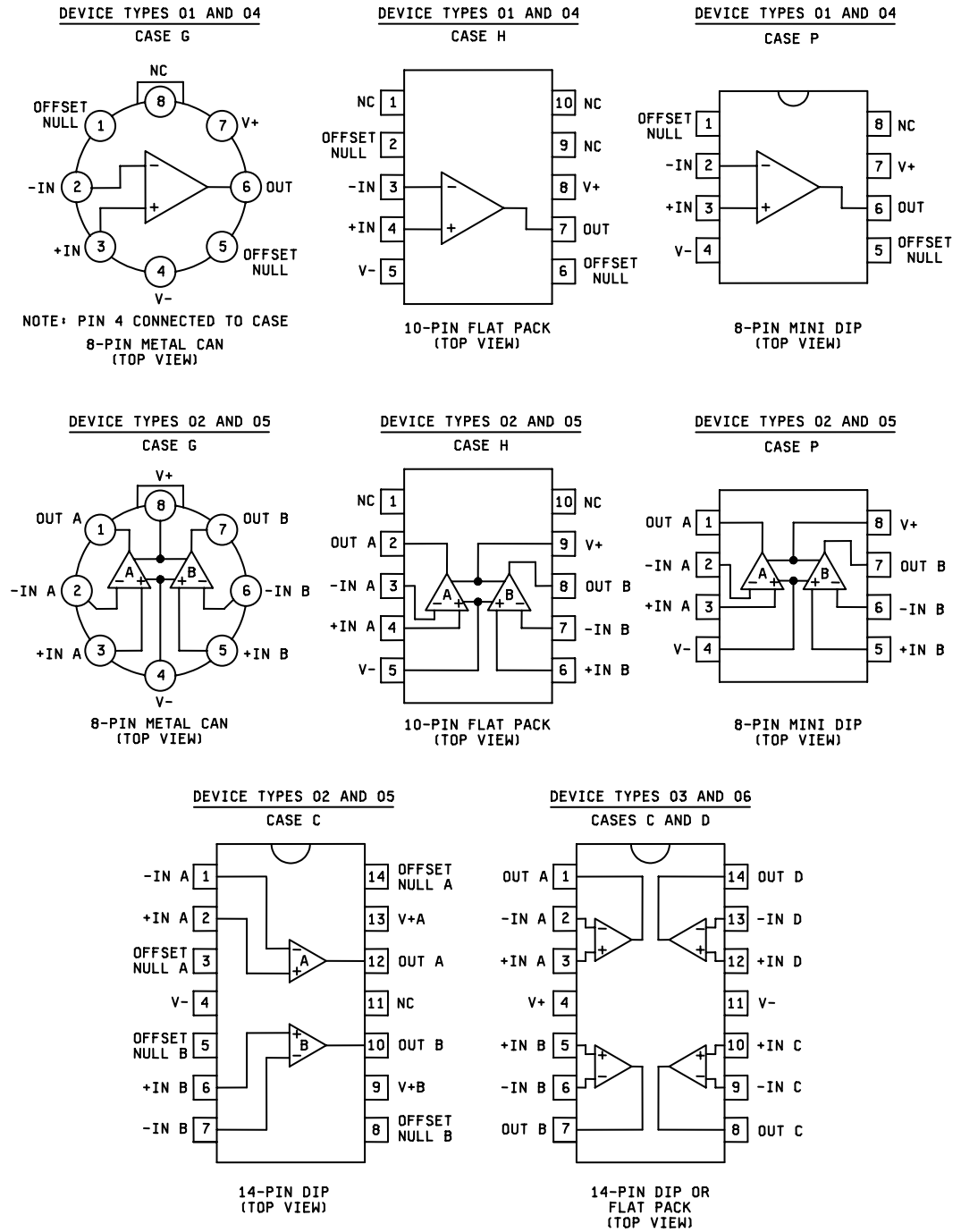
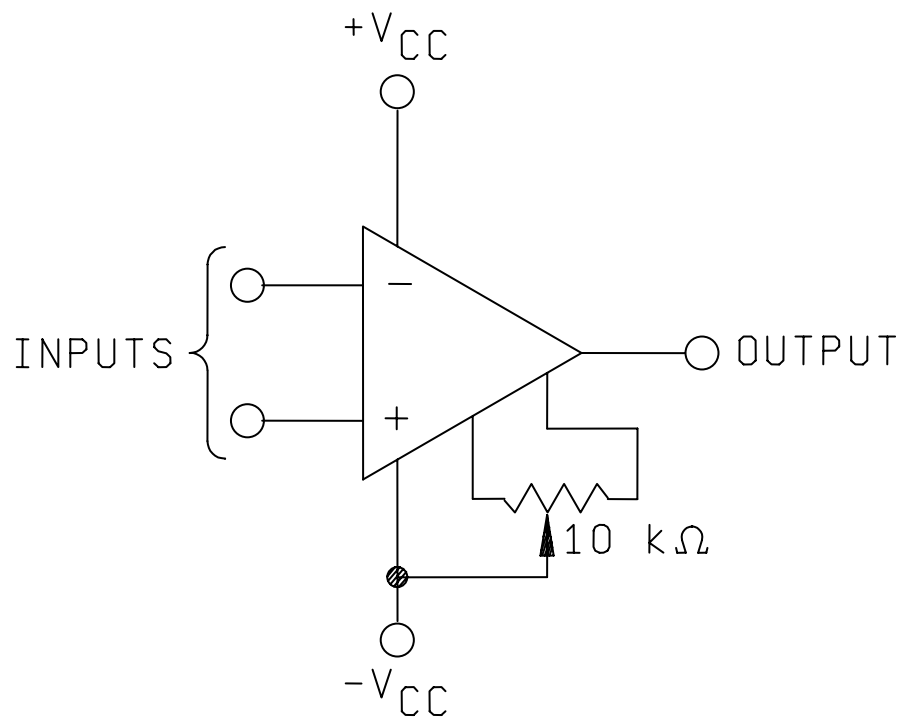
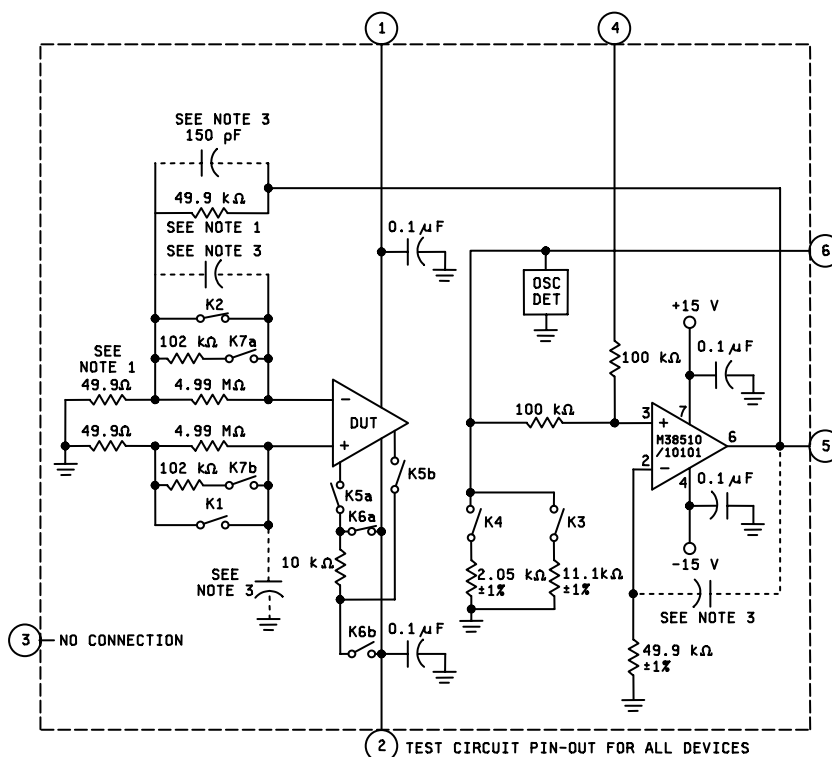


Figure 1. Terminal connections.

**NOTES:**

Available on device types 01 and 04. Available on device types 02 and 05 in case outline C package only.

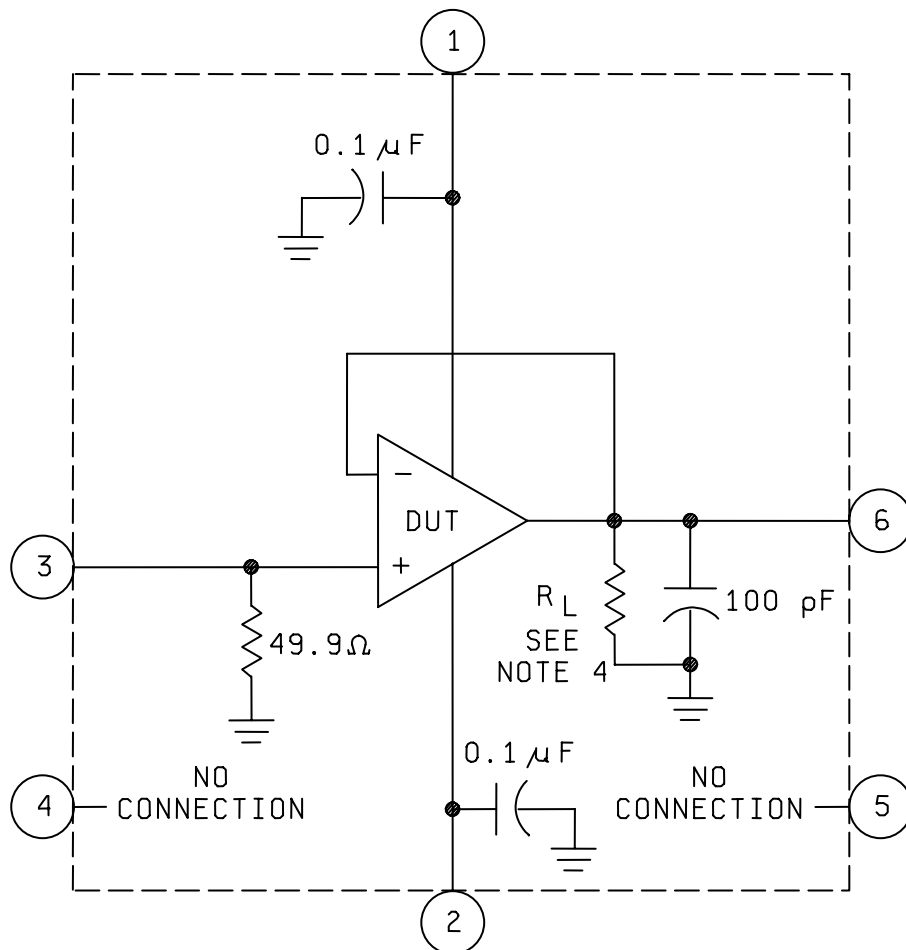
FIGURE 2. Offset null circuit.



NOTES:

1. All resistors are ± 0.1 percent tolerance and all capacitors are ± 10 percent tolerance unless otherwise specified.
2. Precautions shall be taken to prevent damage to the device under test (DUT) during insertion into socket and change of state of relays (for example, disable voltage supplies, current limit $\pm V_{CC}$, etc.).
3. Compensation capacitors should be added as required for test circuit stability. Two general methods for stability compensation exist. One method is with a capacitor for nulling amplifier feedback. The other method is with a capacitor in parallel with the 49.9 kΩ closed loop feedback resistor. Both methods should not be used simultaneously. Proper wiring procedures shall be followed to prevent unwanted coupling and oscillations, etc. Loop response and settling time shall be consistent with the test rate such that any value has settled for at least 5 loop time constants before the value is measured.
4. Adequate settling time should be allowed such that each parameter has settled to within 5 percent of its final value.
5. All relays are shown in the normal deenergized state.
6. The nulling amplifier shall be a M38510/10101XXX. Saturation of the nulling amplifier is not allowed on tests where the E (pin 5) value is measured.
7. The load resistors 2050 Ω and 11.1 kΩ yield effective load resistances of 2 kΩ and 10 kΩ respectively.
8. Any oscillation greater than 300 mV in amplitude (peak-to-peak) shall be the cause for device failure.
9. Selection relays for the dual and quad devices are not shown.

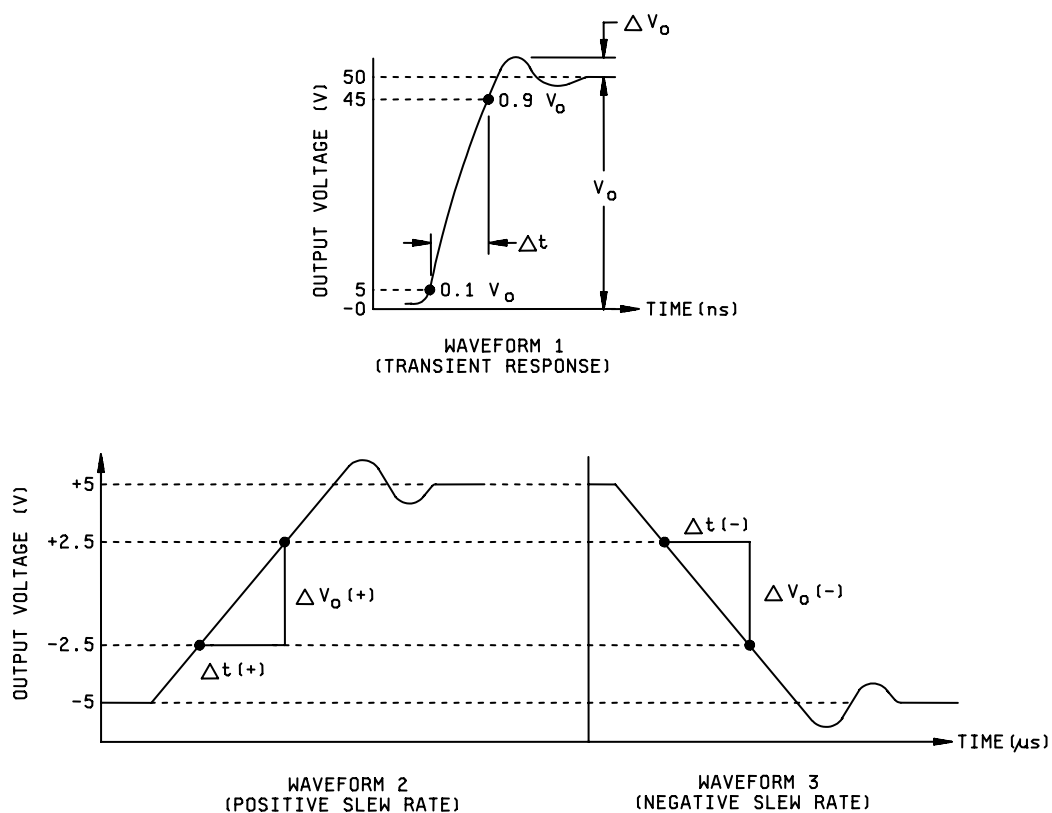
FIGURE 3. Test circuit for static tests.



NOTES:

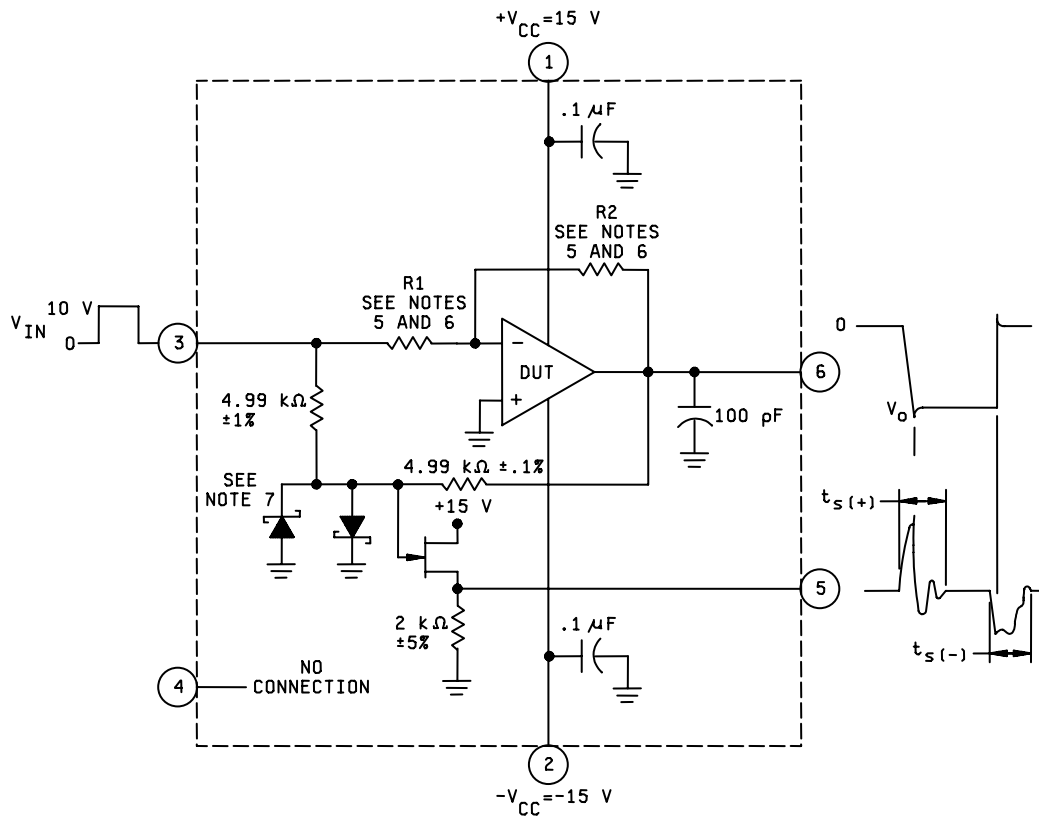
1. Resistors are ± 1.0 percent tolerance and all capacitors are ± 10 percent tolerance.
2. Precautions shall be taken to prevent damage to the device under test (DUT) during insertion into socket and in applying power.
3. Pulse input and output characteristics are shown on the next page.
4. For device types 01-03, $R_L = 10 \text{ k}\Omega$, for device types 04-06, $R_L = 2 \text{ k}\Omega$.
5. Selection circuitry for dual and quad devices is not shown.

FIGURE 4. Test circuit for transient response and slew rate.



Parameter symbol	Input pulse signal at $t_r \leq 50$ ns	Output pulse signal	Equation
$TR_{(tr)}$	+50 mV	Waveform 1	$TR_{(tr)} = \Delta t$
$TR_{(os)}$	+50 mV	Waveform 1	$TR_{(os)} = 100 (\Delta V_O / V_O)\%$
$SR(+)$	-5 V to +5 V step	Waveform 2	$SR(+) = \Delta V_O(+)/\Delta t(+)$
$SR(-)$	+5 V to -5 V step	Waveform 3	$SR(-) = \Delta V_O(-)/\Delta t(-)$

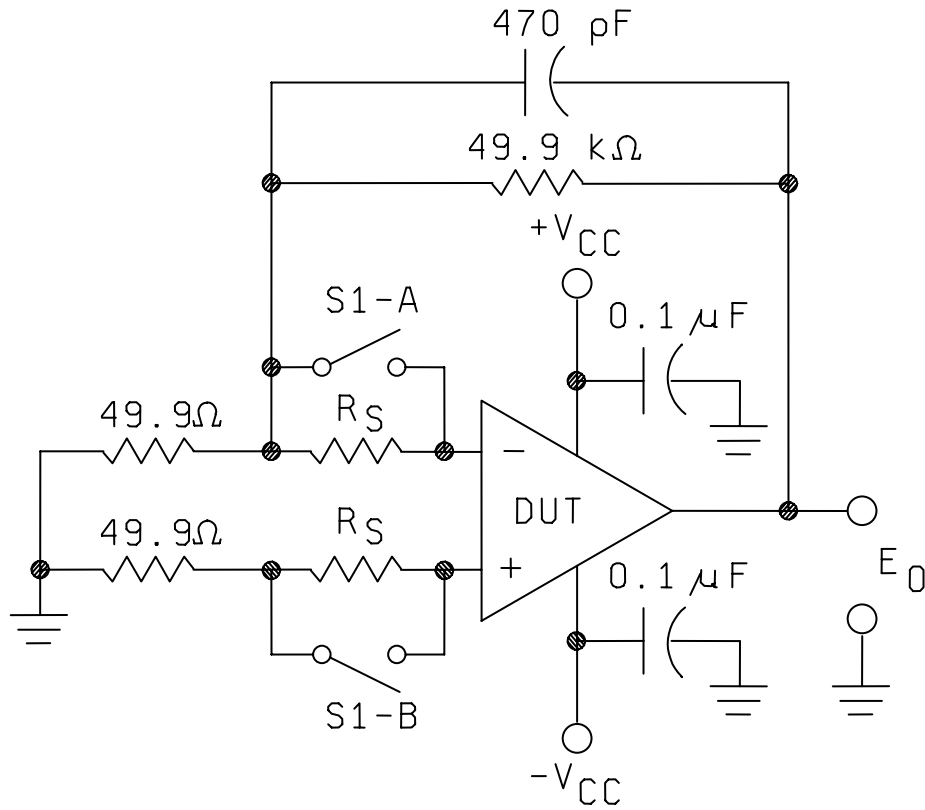
FIGURE 4. Test circuit for transient response and slew rate – Continued.



NOTES:

1. Resistors are ± 0.1 percent tolerance and all capacitors are ± 10 percent unless otherwise specified.
2. Precautions shall be taken to prevent damage to the device under test (DUT) during insertion into socket and in applying power.
3. Selection circuitry for dual and quad devices is not shown.
4. Settling time t_s , measured on pin 5, is the interval during which the summing mode is not nulled to within ± 5 mV.
5. For device types 01, 02, and 03, $R_1 = R_2 = 10$ k Ω .
6. For device types 04, 05, and 06, $R_1 = R_2 = 2$ k Ω .
7. 1N5711 Schottky diodes. Add as needed to limit oscilloscope overdrive caused by the instantaneous transition of V_{IN} .

FIGURE 5. Test circuit for settling time.

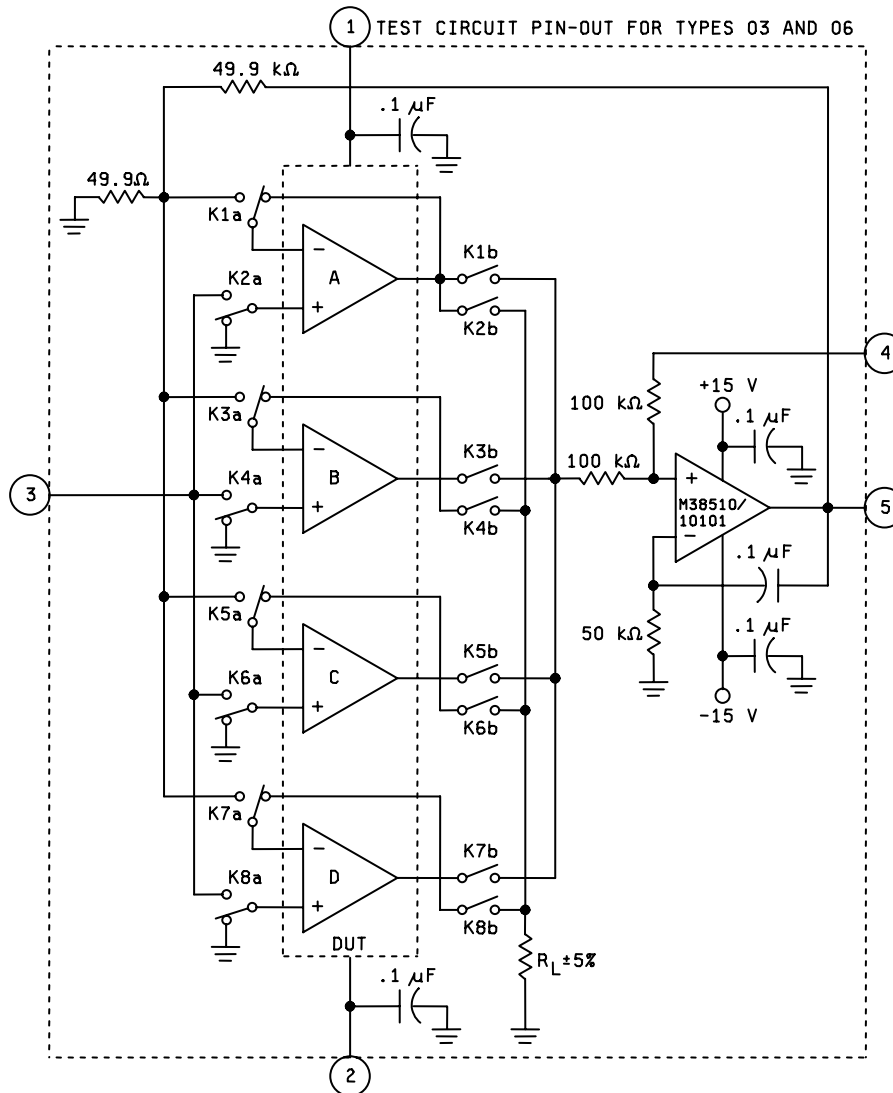


Noise (Referred to input)	Symbol	S1	Measure		Measured equation	Parameter units
			Value	Units		
Broadband	$N_{1(BB)}$	Closed	E_0	mV rms	$E_0 / 1000$	$\mu\text{V rms}$
Popcorn	$N_{1(PC)}$	Open	E_0	mV pk	$E_0 / 1000$	$\mu\text{V pk}$

NOTES:

1. $R_S = 100 \text{ k}\Omega$.
2. E_0 shall be measured with a true rms voltmeter with a bandwidth of 10 Hz to 15 kHz (minimum).
3. The 470 pF capacitor and 49.9 k Ω resistor yield a circuit noise bandwidth of 10 kHz.

FIGURE 6. Noise test circuit.



Notes:

1. Resistors are ± 0.1 percent and capacitors are ± 10 percent tolerance, unless otherwise specified.
2. All relay contacts are shown in the normal deenergized state.
3. $R_L = 10 \text{ k}\Omega$ for device types 01, 02, and 03, $R_L = 2 \text{ k}\Omega$ for device types 04, 05, and 06.

FIGURE 7. Test circuit for channel separation.

TABLE III. Group A inspection for all device types.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Notes	Adapter pin numbers				Energized relays	Measured pin			Equation ^{1/}	Device types	Limits		Unit	
					1	2	3	4		No.	Value	Unit			Min	Max		
1 T _A = 25°C	V _{IO}	4001	1	<u>2/</u>	26 V	-4 V	OPEN	-11 V	NONE	5	E1	V	V _{IO} = E1	ALL	-5	5	mV	
			2	<u>2/</u>	4 V	-26 V	OPEN	11 V	NONE	5	E2	V	V _{IO} = E2	ALL	-5	5	"	
			3	<u>2/</u>	15 V	-15 V	OPEN	0 V	NONE	5	E3	V	V _{IO} = E3	ALL	-5	5	"	
			4	<u>2/</u>	5 V	-5 V	OPEN	0 V	NONE	5	E4	V	V _{IO} = E4	ALL	-5	5	"	
	+I _{IB}	4001	5	<u>2/</u>	26 V	-4 V	OPEN	-11 V	K1	5	E5	V	+I _{IB} = 200 (E1-E5)	ALL	-400	200	pA	
			6	<u>2/</u>	15 V	-15 V	OPEN	0 V	K1	5	E6	V	+I _{IB} = 200 (E3-E6)	ALL	-200	200	"	
			7	<u>2/</u>	4 V	-26 V	OPEN	11 V	K1	5	E7	V	+I _{IB} = 200 (E2-E7)	ALL	-200	1,200	"	
	-I _{IB}	4001	8	<u>2/</u>	26 V	-4 V	OPEN	-11 V	K2	5	E8	V	-I _{IB} = 200 (E8-E1)	ALL	-400	200	pA	
			9	<u>2/</u>	15 V	-15 V	OPEN	0 V	K2	5	E9	V	-I _{IB} = 200 (E9-E3)	ALL	-200	200	"	
			10	<u>2/</u>	4 V	-26 V	OPEN	11 V	K2	5	E10	V	-I _{IB} = 200 (E10-E2)	ALL	-200	1,200	"	
	I _{IO}	4001	11	<u>2/</u>	CALCULATE VALUE USING DATA FROM TESTS 3, 6, and 9. <u>3/</u>							I _{IO} = 200 (2E3-E6-E9)	ALL	-100	100	pA		
	+PSRR	4003	12	----	20 V	-15 V	OPEN	0 V	NONE	5	E11	V	+PSRR = 20 log $\left \frac{10^4}{(E_{11} - E_{12})} \right $	ALL	80	----	dB	
	10 V				-15 V	OPEN	0 V	NONE	5	E12	V							
	-PSRR		13	----	15 V	-20 V	OPEN	0 V	NONE	5	E13	V	-PSRR = 20 log $\left \frac{10^4}{(E_{13} - E_{14})} \right $	ALL	80	----	dB	
	15 V				-10 V	OPEN	0 V	NONE	5	E14	V							
			14	<u>4/</u>	CALCULATE VALUE USING DATA FROM TESTS 1 and 2.							CMR = 20 log $\left \frac{22000}{(E1 - E2)} \right $	ALL	80	----	dB		
	CMR	V _{IO} ADJ(+)	----	15	<u>5/</u>	15 V	-15 V	OPEN	0 V	K5	5	E15	V	V _{IO} ADJ(+) = (E3 - E15)	01, 02 04, 05	8	----	mV
		V _{IO} ADJ(-)	-----	16	<u>5/</u>	15 V	-15 V	OPEN	0 V	K5, K6	5	E16	V	V _{IO} ADJ(-) = (E3 - E16)	01, 02 04, 05	----	-8	mV
		I _{OS} (+)	3011	17	<u>6/</u>	15 V	-15 V	OPEN	-10 V	NONE	6	I1	mA	I _{OS} (+) = I1	01, 02, 03 04, 05, 06	-40 -80	---- ----	mA
		I _{OS} (-)		18	<u>6/</u>	15 V	-15 V	OPEN	10 V	NONE	6	I2	mA	I _{OS} (-) = I2	01, 02, 03 04, 05, 06	---- 80	40 80	mA
		I _{CC}	3005	19	----	15 V	-15 V	OPEN	0 V	NONE	2	I3	mA	I _{CC} = I3 <u>7/</u>	01, 02, 03 04, 05, 06	---- 3.5	0.3 3.5	mA
2 T _A = +125°C	V _{IO}	4001	20	<u>2/</u>	26 V	-4 V	OPEN	-11 V	NONE	5	E15	V	V _{IO} = E15	ALL	-7	7	mV	
			21	<u>2/</u>	4 V	-26 V	OPEN	11 V	NONE	5	E16	V	V _{IO} = E16	ALL	-7	7	"	
			22	<u>2/</u>	15 V	-15 V	OPEN	0 V	NONE	5	E17	V	V _{IO} = E17	ALL	-7	7	"	
			23	<u>2/</u>	5 V	-5 V	OPEN	0 V	NONE	5	E18	V	V _{IO} = E18	ALL	-7	7	"	
	$\frac{\Delta V_{IO}}{\Delta T}$	4001	24	<u>8/</u>	$\frac{\Delta V_{IO}}{\Delta T} = \frac{[V_{IO}(\text{test 22}) - V_{IO}(\text{test 3})]}{100^\circ\text{C}}$								ALL	-30	30	μV/°C		

See footnotes at end of table.

TABLE III. Group A inspection for all device types – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Notes	Adapter pin numbers				Energized relays	Measured pin			Equation <u>1/</u>	Device types	Limits		Unit	
					1	2	3	4		No.	Value	Unit			Min	Max		
2 T _A = 125°C	+I _{IB}	4001	25	<u>2/</u>	26 V	-4 V	OPEN	-11 V	K1, K7	5	E19	V	+I _{IB} = 10 (E15-E19)	ALL	-10	50	nA	
			26	<u>2/</u>	15 V	-15 V	OPEN	0 V	K1, K7	5	E20	V	+I _{IB} = 10 (E17-E20)	ALL	-10	50	"	
			27	<u>2/</u>	4 V	-26 V	OPEN	11 V	K1, K7	5	E21	V	+I _{IB} = 10 (E16-E21)	ALL	-10	70	"	
	-I _{IB}	4001	28	<u>2/</u>	26 V	-4 V	OPEN	-11 V	K1, K7	5	E22	V	-I _{IB} = 10 (E22-E15)	ALL	-10	50	nA	
			29	<u>2/</u>	15 V	-15 V	OPEN	0 V	K1, K7	5	E23	V	-I _{IB} = 10 (E23-E17)	ALL	-10	50	"	
			30	<u>2/</u>	4 V	-26 V	OPEN	11 V	K1, K7	5	E24	V	-I _{IB} = 10 (E24-E16)	ALL	-10	70	"	
	I _{IO}	4001	31	<u>2/</u>	CALCULATE VALUE USING DATA FROM TESTS 22, 26, and 29. <u>3/</u>							I _{IO} = 10 (2E17-E20-E23)	ALL	-20	20	nA		
	+PSRR	4003	32	----	20 V	-15 V	OPEN	0 V	NONE	5	E25	V	+PSRR = 20 log $\frac{10^4}{(E_{25} - E_{26})}$	ALL	80	----	dB	
					10 V	-15 V	OPEN	0 V	NONE	5	E26	V						
	-PSRR		33	----	15 V	-20 V	OPEN	0 V	NONE	5	E27	V	-PSRR = 20 log $\frac{10^4}{(E_{27} - E_{28})}$	ALL	80	----	dB	
					15 V	-10 V	OPEN	0 V	NONE	5	E28	V						
			34	<u>4/</u>	CALCULATE VALUE USING DATA FROM TESTS 20 and 21.							CMR = 20 log $\frac{22000}{(E_{15} - E_{16})}$	ALL	80	----	dB		
	CMR	V _{IO} ADJ(+)	----	35	<u>5/</u>	15 V	-15 V	OPEN	0 V	K5	5	E29	V	V _{IO} ADJ(+) = (E17 – E29)	01, 02 04, 05	8	----	mV
		V _{IO} ADJ(-)	-----	36	<u>5/</u>	15 V	-15 V	OPEN	0 V	K5, K6	5	E30	V	V _{IO} ADJ(-) = (E17 – E30)	01, 02 04, 05	----	-8	mV
		I _{OS} (+)	3011	37	<u>6/</u>	15 V	-15 V	OPEN	-10 V	NONE	6	I4	mA	I _{OS} (+) = I4	01, 02, 03 04, 05, 06	-40	----	mA
		I _{OS} (-)		38	<u>6/</u>	15 V	-15 V	OPEN	10 V	NONE	6	I5	mA	I _{OS} (-) = I5	01, 02, 03 04, 05, 06	----	40	mA
		I _{CC}	3005	39	----	15 V	-15 V	OPEN	0 V	NONE	2	I6	mA	I _{CC} = I6 <u>7/</u>	01, 02, 03 04, 05, 06	----	0.3	mA
																3.5		
3 T _A = -55°C	V _{IO}	4001	40	<u>2/</u>	26 V	-4 V	OPEN	-11 V	NONE	5	E31	V	V _{IO} = E31	ALL	-7	7	mV	
			41	<u>2/</u>	4 V	-26 V	OPEN	11 V	NONE	5	E32	V	V _{IO} = E32	ALL	-7	7	"	
			42	<u>2/</u>	15 V	-15 V	OPEN	0 V	NONE	5	E33	V	V _{IO} = E33	ALL	-7	7	"	
			43	<u>2/</u>	5 V	-5 V	OPEN	0 V	NONE	5	E34	V	V _{IO} = E34	ALL	-7	7	"	
	$\frac{\Delta V_{IO}}{\Delta T}$	4001	44	<u>8/</u>	$\frac{\Delta V_{IO}}{\Delta T} = \frac{[V_{IO}(\text{test 42}) - V_{IO}(\text{test 3})]}{80^\circ\text{C}}$								ALL	-30	30	μV/°C		
	+PSRR	4003	45	----	20 V	-15 V	OPEN	0 V	NONE	5	E35	V	+PSRR = 20 log $\frac{10^4}{(E_{35} - E_{36})}$	ALL	80	----	dB	
10 V					-15 V	OPEN	0 V	NONE	5	E36	V							

See footnotes at end of table.

TABLE III. Group A inspection for all device types – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Notes	Adapter pin numbers				Energized relays	Measured pin			Equation 1/	Device types	Limits		Unit
					1	2	3	4		No.	Value	Unit			Min	Max	
3 T _A = -55°C	-PSRR	4003	46	----	15 V	-20 V	OPEN	0 V	NONE	5	E37	V	$-PSRR = 20 \log \left \frac{10^4}{(E_{37} - E_{38})} \right $	ALL	80	----	dB
				----	15 V	-10 V	OPEN	0 V	NONE	5	E38	V					
	CMR	3011	47	4/	CALCULATE VALUE USING DATA FROM TESTS 40 and 41.								$CMR = 20 \log \left \frac{22000}{(E_{31} - E_{32})} \right $	ALL	80	----	dB
			48	5/	15 V	-15 V	OPEN	0 V	K5	5	E39	V	V _{IO} ADJ(+) = (E33 – E39)	01, 02, 03, 04, 05	8	----	mV
			49	5/	15 V	-15 V	OPEN	0 V	K5, K6	5	E40	V	V _{IO} ADJ(-) = (E33 – E40)	01, 02, 03, 04, 05	----	-8	mV
			50	6/	15 V	-15 V	OPEN	-10 V	NONE	6	I7	mA	I _{OS} (+) = I7	01, 02, 03, 04, 05, 06	-40	----	mA
			51	6/	15 V	-15 V	OPEN	10 V	NONE	6	I8	mA	I _{OS} (-) = I8	01, 02, 03, 04, 05, 06	----	40	mA
			52	----	15 V	-15 V	OPEN	0 V	NONE	2	I9	mA	I _{CC} = I9 Z/	01, 02, 03, 04, 05, 06	----	0.3	mA
																4.0	
4 T _A = +25°C	+V _{OP}	4004	53	----	15 V	-15 V	OPEN	-15 V	K3	6	(EO)1	V	+V _{OP} = (EO)1	ALL	12		V
	-V _{OP}		54	----	15 V	-15 V	OPEN	15 V	K3	6	(EO)2	V	-V _{OP} = (EO)2	ALL		-12	V
	+V _{OP}	4004	55	----	15 V	-15 V	OPEN	-15 V	K4	6	(EO)3	V	+V _{OP} = (EO)3	04, 05, 06	10		V
	-V _{OP}		56	----	15 V	-15 V	OPEN	15 V	K4	6	(EO)4	V	-V _{OP} = (EO)4	04, 05, 06			V
	A _{VS} (+)	4004	57	9/	15 V	-15 V	OPEN	-10 V	K3 K4	5	E41	V	$A_{VS}(+) = \frac{10}{(E3 - E41)}$	01, 02, 03, 04, 05, 06	5 50 ¹⁰		V/mV
	A _{VS} (-)			9/	15 V	-15 V	OPEN	10 V	K3 K4	5	E42	V	$A_{VS}(-) = \frac{10}{(E42 - E3)}$	01, 02, 03, 04, 05, 06	5 50		V/mV
	A _{VS}	4004 58	59	----	5 V 5 V	-5 V -5 V	OPEN OPEN	-2 V 2 V	K3 K3	5 5	E43 E44	V V	$A_{VS} = \frac{4}{(E44 - E43)}$	01, 02, 03, 04, 05, 06	3 20		V/mV
5 T _A = +125 °C	+V _{OP}	4004	60	----	15 V	-15 V	OPEN	-15 V	K3	6	(EO)5	V	+V _{OP} = (EO)5	ALL	12		V
	-V _{OP}		61	----	15 V	-15 V	OPEN	15 V	K3	6	(EO)6	V	-V _{OP} = (EO)6	ALL		-12	V
	+V _{OP}	4004	62	----	15 V	-15 V	OPEN	-15 V	K4	6	(EO)7	V	+V _{OP} = (EO)7	04, 05, 06	10		V
	-V _{OP}		63	----	15 V	-15 V	OPEN	15 V	K4	6	(EO)8	V	-V _{OP} = (EO)8	04, 05, 06			V
	A _{VS} (+)	4004	64	9/	15 V	-15 V	OPEN	-10 V	K3 K4	5	E45	V	$A_{VS}(+) = \frac{10}{(E17 - E45)}$	01, 02, 03, 04, 05, 06	4 25 ¹⁰		V/mV
	A _{VS} (-)			9/	15 V	-15 V	OPEN	10 V	K3 K4	5	E46	V	$A_{VS}(-) = \frac{10}{(E46 - E17)}$	01, 02, 03, 04, 05, 06	4 25		V/mV
	A _{VS}	4004 65	66	----	5 V 5 V	-5 V -5 V	OPEN OPEN	-2 V 2 V	K3 K3	5 5	E47 E48	V V	$A_{VS} = \frac{4}{(E48 - E47)}$	01, 02, 03, 04, 05, 06	3 20		V/mV

See footnotes at end of table.

TABLE III. Group A inspection for all device types – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Notes	Adapter pin numbers				Energized relays	Measured pin			Equation 1/	Device types	Limits		Unit
					1	2	3	4		No.	Value	Unit			Min	Max	
6 T _A = -55°C	+V _{OP}	4004	67	----	15 V	-15 V	OPEN	-15 V	K3	6	(EO)9	V	+V _{OP} = (EO)9	ALL	12		V
	-V _{OP}		68	----	15 V	-15 V	OPEN	15 V	K3	6	(EO)10	V	-V _{OP} = (EO)10	ALL		-12	V
	+V _{OP}	4004	69	----	15 V	-15 V	OPEN	-15 V	K4	6	(EO)11	V	+V _{OP} = (EO)11	04, 05, 06	10		V
	-V _{OP}		70	----	15 V	-15 V	OPEN	15 V	K4	6	(EO)12	V	-V _{OP} = (EO)12	04, 05, 06			V
	A _{VS} (+)	4004	71	9/	15 V	-15 V	OPEN	-10 V	K3 K4	5	E49	V	$A_{VS}(+) = \frac{10}{(E33 - E49)}$	01, 02, 03 04, 05, 06	4 25 ¹⁰		V/mV
	A _{VS} (-)			9/	15 V	-15 V	OPEN	10 V	K3 K4	5	E50	V	$A_{VS}(-) = \frac{10}{(E50 - E33)}$	01, 02, 03 04, 05, 06	4 25		V/mV
	A _{VS}	4004 72	73	----	5 V 5 V	-5 V -5 V	OPEN OPEN	-2 V 2 V	K3 K3	5 5	E51 E52	V V	$A_{VS} = \frac{4}{(E52 - E51)}$	01, 02, 03 04, 05, 06	3 20		V/mV
7 T _A = +25°C	TR _(tr)	----	74	FIG 4	15 V	-15 V	50 mV	OPEN	NONE	6	Δt1	ns	TR _(tr) = Δt1	01, 02, 03 04, 05, 06		400 200	ns
	TR _(os)	----	75	FIG 4	15 V	-15 V	50 mV	OPEN	NONE	6	V _O , ΔV _{O1}	mV	TR _(os) = 100 $\frac{\Delta V_{O1}}{V_{O1}}$	01, 02, 03 04, 05, 06		20 40	%
	SR(+)	4002	76	FIG 4	15 V	-15 V	8/	OPEN	NONE	6	ΔV _O (+)	V	SR(+) = $\frac{\Delta V_{O1}(+)}{\Delta t1(+)}$	01, 02, 03	0.8		V/μs
											Δt1 (+)	μs		04, 05, 06			
	SR(-)	4002	77	FIG 4	15 V	-15 V	8/	OPEN	NONE	6	ΔV _{O1} (-)	V	SR(-) = $\frac{\Delta V_{O1}(-)}{\Delta t1(-)}$	01, 02, 03	0.8		V/μs
											Δt1 (-)	μs		04, 05, 06			
	NI _(BB)	4002	78	FIG 6	15 V	-15 V	OPEN	0 V	NONE	6	(EO)13	mV rms	NI _(BB) = $\frac{(EO)13}{1000}$	ALL		15	mV rms
	NI _(PC)	4002	79	10/	15 V	-15 V	OPEN	0 V	K1, K2	6	(EO)14	mV pk	NI _(PC) = $\frac{(EO)14}{1000}$	ALL		80	μV pk
	CS	4002	80	FIG 7	15 V	-15 V	10 V	0 V	K2, K3	5	E53	V	CS = 20 log $\left \frac{20000}{(E53 - E54)} \right $	02, 03, 05, 06	80		dB
				11/	15 V	-15 V	-10 V	0 V	K2, K3	5	E54	V					
		4002	81	FIG 7	15 V	-15 V	10 V	0 V	K2, K5	5	E55	V	CS = 20 log $\left \frac{20000}{(E55 - E56)} \right $	02, 03, 05, 06	80		dB
				11/	15 V	-15 V	-10 V	0 V	K2, K5	5	E56	V					
		4002	82	FIG 7	15 V	-15 V	10 V	0 V	K2, K7	5	E57	V	CS = 20 log $\left \frac{20000}{(E57 - E58)} \right $	02, 03, 05, 06	80		dB
				11/	15 V	-15 V	-10 V	0 V	K2, K7	5	E58	V					
		4002	83	FIG 7	15 V	-15 V	10 V	0 V	K4, K1	5	E59	V	CS = 20 log $\left \frac{20000}{(E59 - E60)} \right $	02, 03, 05, 06	80		dB
				11/	15 V	-15 V	-10 V	0 V	K4, K1	5	E60	V					

See footnotes at end of table.

TABLE III. Group A inspection for all device types – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Notes	Adapter pin numbers				Energized relays	Measured pin			Equation 1/	Device types	Limits		Unit
					1	2	3	4		No.	Value	Unit			Min	Max	
7 T _A = +25°C	CS	4002	84	FIG 7	15 V	-15 V	10 V	0 V	K4, K5	5	E61	V	CS = 20 log $\frac{20000}{(E61 - E62)}$	02, 03, 05, 06	80		dB
				11/	15 V	-15 V	-10 V	0 V	K4, K5	5	E62	V					
		4002	85	FIG 7	15 V	-15 V	10 V	0 V	K4, K7	5	E63	V	CS = 20 log $\frac{20000}{(E63 - E64)}$	02, 03, 05, 06	80		dB
				11/	15 V	-15 V	-10 V	0 V	K4, K7	5	E64	V					
		4002	86	FIG 7	15 V	-15 V	10 V	0 V	K6, K1	5	E65	V	CS = 20 log $\frac{20000}{(E65 - E66)}$	02, 03, 05, 06	80		dB
				11/	15 V	-15 V	-10 V	0 V	K6, K1	5	E66	V					
		4002	87	FIG 7	15 V	-15 V	10 V	0 V	K6, K3	5	E67	V	CS = 20 log $\frac{20000}{(E67 - E68)}$	02, 03, 05, 06	80		dB
				11/	15 V	-15 V	-10 V	0 V	K6, K3	5	E68	V					
		4002	88	FIG 7	15 V	-15 V	10 V	0 V	K6, K7	5	E69	V	CS = 20 log $\frac{20000}{(E69 - E70)}$	02, 03, 05, 06	80		dB
				11/	15 V	-15 V	-10 V	0 V	K6, K7	5	E70	V					
		4002	89	FIG 7	15 V	-15 V	10 V	0 V	K8, K1	5	E71	V	CS = 20 log $\frac{20000}{(E71 - E72)}$	02, 03, 05, 06	80		dB
				11/	15 V	-15 V	-10 V	0 V	K8, K1	5	E72	V					
		4002	90	FIG 7	15 V	-15 V	10 V	0 V	K8, K3	5	E73	V	CS = 20 log $\frac{20000}{(E73 - E74)}$	02, 03, 05, 06	80		dB
				11/	15 V	-15 V	-10 V	0 V	K8, K3	5	E74	V					
		4002	91	FIG 7	15 V	-15 V	10 V	0 V	K8, K5	5	E75	V	CS = 20 log $\frac{20000}{(E75 - E76)}$	02, 03, 05, 06	80		dB
				11/	15 V	-15 V	-10 V	0 V	K8, K5	5	E76	V					
8 T _A = +125 °C	TR _(tr)	----	92	FIG 4	15 V	-15 V	50 mV	OPEN	NONE	6	Δt2	ns	TR _(tr) = Δt2	01, 02, 03 04, 05, 06	400 200		ns
	TR _(os)	----	93	FIG 4	15 V	-15 V	50 mV	OPEN	NONE	6	V _{O2} , ΔV _{O2}	mV	TR _(os) = 100 $\frac{\Delta V_{O2}}{V_{O2}}$	01, 02, 03 04, 05, 06	20 40		%
	SR(+)	4002	94	FIG 4	15 V	-15 V	12/	OPEN	NONE	6	ΔV _{O2} (+)	V	SR(+) = $\frac{\Delta V_{O2}(+)}{\Delta t2(+)}$	01, 02, 03	0.7		V/μs
											Δt2 (+)	μs		04, 05, 06	5		
	SR(-)	4002	95	FIG 4	15 V	-15 V	12/	OPEN	NONE	6	ΔV _{O2} (-)	V	SR(-) = $\frac{\Delta V_{O2}(-)}{\Delta t2(-)}$	01, 02, 03	0.7		V/μs
											Δt2 (-)	μs		04, 05, 06	5		

See footnotes at end of table.

TABLE III. Group A inspection for all device types – Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Notes	Adapter pin numbers				Energized relays	Measured pin			Equation 1/	Device types	Limits		Unit
					1	2	3	4		No.	Value	Unit			Min	Max	
8 T _A = -55°C	TR(tr)	----	96	FIG 4	15 V	-15 V	50 mV	OPEN	NONE	6	Δt3	ns	TR(tr) = Δt3	01, 02, 03		400	ns
														04, 05, 06		200	
	TR(os)	----	97	FIG 4	15 V	-15 V	50 mV	OPEN	NONE	6	V _{O3} , ΔV _{O3}	mV	TR(os) = 100 $\frac{\Delta V_{O3}}{V_{O3}}$	01, 02, 03		20	%
														04, 05, 06		40	
	SR(+)	4002	98	FIG 4	15 V	-15 V	12/	OPEN	NONE	6	ΔV _{O3} (+)	V	SR(+) = $\frac{\Delta V_{O3}(+)}{\Delta t3(+)}$	01, 02, 03	0.7		V/μs
											Δt3 (+)	μs		04, 05, 06	5		
12 T _A = +25°C	SR(-)	4002	99	FIG 4	15 V	-15 V	12/	OPEN	NONE	6	ΔV _{O3} (-)	V	SR(-) = $\frac{\Delta V_{O3}(-)}{\Delta t3(-)}$	01, 02, 03	0.7		V/μs
											Δt3 (-)	μs		04, 05, 06	5		
	ts(+)	4002	100	FIG 5	15 V	-15 V	10 V	OPEN	NONE	5	ts(+)	ns	See FIGURE 5	01, 02, 03		6,000	ns
	ts(-)		101	FIG 5	15 V	-15 V	-10 V	OPEN	NONE	5	ts(-)	ns	See FIGURE 5.	04, 05, 06		1,500	ns

- 1/ The equations take into account both the closed loop gain of 1,000 and the scale factor multiplier so that the calculated value is in table I units. The measured value units should, therefore, be used in the equation. (For example: If E1 = 2 V and V_{IO} = E1, then V_{IO} = 2 mV.) For devices marked with the "Q" certification mark, the parameters listed herein may be guaranteed if not tested to the limits specified in accordance with the manufacturer's QM plan
- 2/ Each device shall be tested over the common mode range as specified in table III. V_{CM} conditions are achieved by grounding the inputs and algebraically subtracting V_{CM} from each supply. (For example: If V_{CM} = -11 V, then +V_{CC} = +15 V – (-11) = +26 V and –V_{CC} = -15 V – (-11) = -4 V).
- 3/ Input offset current, I_{IO}, may be measured directly. To do so, both K1 and K2 shall be energized. The difference in E values, with and without the relays energized, is multiplied by the proper coefficient to yield the I_{IO} value.
- 4/ Common mode rejection is calculated using the offset voltage values measured at the common mode range end points.
- 5/ V_{IO} ADJ (±) is only tested on device types 01 and 04 certain duals in a 14 pin dual-in-line package.
- 6/ The output shall be shorted to ground for 25 ms, or less.
- 7/ For device types 02, 03, 05, and 06 maximum limit shown is for 1 operating ampere only, this value is double for the dual device (for example: 2 x 3.5 = 7 mA at +25°C and +125°C; for example: 2 x 4.0 = 8 mA at -55°C), quadruple for the quad devices.
- 8/ Tests 24 and 44 which require a read and record measurement plus a calculation may be omitted except when subgroups 2 and 3 are being accomplished for group A sampling inspection and groups C and D end-point measurements.
- 9/ To minimize thermal drift, the reference voltage for the gain measurement (E3, E17, and E33) shall be taken immediately prior to or after the reading corresponding to device gain (E41, E42, E45, E46, E49, and E50).
- 10/ Broadband noise NI(BB) shall be measured using an RMS voltmeter with a bandwidth of 10 Hz to 15 kHz. "Popcorn" noise NI(PC) shall be measured for seconds.
- 11/ Quad devices 03 and 06 shall be tested for all combinations of channel separation (for example: tests 80 through 91). Dual devices are tested for two combinations of channel separation (for example: tests 80 and 83).
- 12/ All device types are tested with a -5 V to +5 V step input as shown on figure 4. The circuit gain is 1 V/V.

TABLE IV. Group C end-point electrical parameters. 1/

Table III tests		Limits		Units
		Min	Max	
V _{IO}	Limit	-5	5	mV
	Delta	-1	1	
+I _{IB}	Limit	-200	200	pA
	Delta	-100	100	
-I _{IB}	Limit	-200	200	pA
	Delta	-100	100	

1/ T_A = +25°C, ±V_{CC} = ±15 V for all device types.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- Tests shall be as specified in table II herein.
- Subgroups 9, 10, and 11 shall be omitted.
- Subgroup 12 shall be added to group A inspection as shown in table III herein. The sample size series number shall be 5 for all classes (accept on 0).

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

- End point electrical parameters shall be as specified in table II herein.
- The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows.

4.5.1 Voltage and current. All voltage values given are referenced to the microcircuit ground terminal of the device under test (DUT). Current values given are conventional current and are positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military's service system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of the specification.
- b. Pin and compliance identifier, if applicable (see 1.2).
- c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirements for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to acquiring activity in addition to notification of the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of MIL-STD-883, method 5003), corrective action and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- i. Requirements for "JAN" marking.
- j. Packaging requirements (see 5.1).

6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43128-3990.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331.

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6.6 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

<u>Military device type</u>	<u>Generic-industry type</u>
01	061
02	062
03	064
04	071, 771, LF151, LF411
05	072, 772, LF153, LF412
06	074, 774, LF147

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
 Army – CR
 Navy - EC
 Air Force - 11
 NASA - NA
 DLA – CC

Preparing activity:
 DLA - CC

 Project 5962-1983

Review activities:
 Army - MI, SM
 Navy - AS, CG, SH, TD
 Air Force – 03, 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://assist.daps.dla.mil>.