

ENGINEERING PRACTICE (EP) STUDY

TITLE: Similar Screening, TCI/QCI and RHA table requirements of MIL-PRF-38535 and TM5004/5005 of MIL-STD-883.

EP study project number: 5962-2011-009

FINAL REPORT

Study conducted by DLA Land and Maritime-VAC

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**EP study on standardization of Screening, QCI/TCI and RHA table requirements for
MIL-PRF-38535 and TM5004/5005 tables of MIL-STD-883**

OBJECTIVE: The purpose of this Engineering Practice (EP) Study was to obtain input and justification from the military services, microcircuit manufacturers, QML microcircuits users and space application microcircuits user communities to generate similar requirements on devices Screening, QCI/TCI and RHA tables to MIL-PRF-38535 and TM5004/5005 of MIL-STD-883.

BACKGROUND: In early 1970's standardized military microcircuits were used under the Joint Army Navy (JAN) program, which was based on general specification MIL-M-38510, and test method 5004/5005 of MIL-STD-883. Later, QML program established to provide a benchmark performance requirement to the device manufacturer and users communities to comply MIL-PRF-38535 requirements. Since MIL-PRF-38535 screening tables, QCI/TCI tables and RHA requirements are different in some instances than MIL-STD-883 screening TM 5004 and QCI/TCI table requirements of TM5005. The JEDEC sub-committee JC-13.2 formed a Task Group (TG 2009-01) for finding the differences between these two documents requirements. Subsequently, TG discussed all findings with microcircuits manufacturer and users communities in several JEDEC meetings and requested to DLA Land and Maritime for EP Study with offering similar requirements in both of tables of MIL-PRF-38535 and TM5004/5005 of MIL-STD-883.

Accordingly, DLA Land and Maritime-VAC conducted EP study which was sent out to the microcircuits manufacturers, test laboratories, OEM, Users, military services and space communities members on August 23, 2011 for obtaining input and comments.

RESULTS: After numerous discussions on initial EP study report with all parties at the JEDEC forum in October, 2011 and February 2012, the task group summarized all received comments and submitted to DLA Land and Maritime for next action. Considering TG's recommendation and all received comments from the manufacturers, users and military services, the DLA Land and Maritime-VAC has prepared a similar tables for MIL-PRF-38535 and TM5004/5005 of MIL-STD-883 that's contains similar screening requirements (see attachment #1), QCI/TCI requirements (see attachment # 2) and RHA test requirements (see attachment # 3).

CONCLUSIONS: DLA Land and Maritime-VAC is preparing similar tables of screening and TCI/QCI requirements and added to the draft revision of MIL-PRF-38535 based on the final EP study report. Similarly, test method 5004 and 5005 of MIL-STD-883 will be updated through next action.

Attachment # 1**Proposed draft of identical table for MIL-PRF-38535 and TM5004 of MIL-STD-883****Table IA : Microcircuits Screening procedure for hermetic QML microcircuits.**

Test	Table IA Test for hermetic QML microcircuits (MIL-PRF-38535)		Table I Test for class level S and B hermetic microcircuits (MIL-STD-883,TM5004)		Proposed identical Table IA Test for QML Hermetic microcircuits to MIL-PRF-38535/TM5004 of MIL-STD-883	
	Class Q	Class V	Class level B (=class Q)	Class level S (=class V)	Class Q (class level B)	Class V (class level S)
1. Wafer lot acceptance <u>1/</u>	TRB plan (see H.3.2.1.4)	TRB plan (see H.3.2.1.4) TM 5007		TM 5007 (All Lots)	QM plan (see H.3.2.1.4)	QM plan (see H.3.2.1.4) or TM 5007 (All Lots)
2. Non destructive bond pull (NDBP) test		TM2023		TM2023 (100%)		TM2023 (100%)
3. Internal visual inspection <u>2/</u>	TM 2010, test condition B (see J.3.3)	TM 2010, test condition A (see J.3.3)	TM 2010, test condition B	TM 2010, test condition A	TM 2010, test condition B (100%)	TM 2010, test condition A (100%)
4. Temperature cycling/ Thermal shock <u>3/</u>	TM 1010, test condition C, 50 cycles minimum	TM 1010, test condition C, 50 cycles minimum	TM 1010, test condition C, 100%	TM 1010, test condition C, 100%	TM 1010, test condition C, 10 cycles minimum (100%)	TM 1010, test condition C , 50 cycles minimum 1(100%)
5. Constant acceleration (High stress test) <u>4/</u>	TM 2001, test condition E (minimum) Y1 orientation only (see J.3.4)	TM 2001, test condition E (minimum) Y1 orientation only (see J.3.4)	TM 2001, test condition E (minimum) Y1 orientation only 100%	TM 2001, test condition E (minimum) Y1 orientation only 100%	TM 2001, test condition E (minimum) Y1 orientation only (100%)	TM 2001, test condition E (minimum) Y1 orientation only (100%)
6. External Visual Inspection <u>5/</u>			100%	100%	(100%)	(100%)
7. Particle Impact Noise Detection (PIND) <u>6/</u>		TM 2020, test condition A on each device		TM 2020, test condition A		TM 2020, test condition A on each device (100%)
8. Serialization <u>7/</u>	In accordance with device specification	In accordance with device specification		100%	In accordance with device specification (100%)	In accordance with device specification (100%)

Table IA : Microcircuits Screening procedure for hermetic QML microcircuits – Continued.

Test	Table IA Test for Hermetic QML microcircuits (MIL-PRF-38535)		Table I Test for Hermetic class level S and B microcircuits (MIL-STD-883 TM5004)		Proposed identical Table IA Test for QML Hermetic microcircuits to MIL-PRF-38535/TM5004 of MIL-STD-883	
	Class Q	Class V	Class level B (=class Q)	Class level S (=class V)	Class Q (class level B)	Class V (class level S)
9. Pre burn-in (Interim) electrical parameters <u>8/</u>	In accordance with device specification	In accordance with device specification	In accordance with device specification 100% <u>9/</u>	In accordance with device specification 100% <u>10/</u>	In accordance with device specification (100%) <u>9/</u>	In accordance with device specification (100%) <u>10/</u>
10. Burn-in test <u>8/</u> <u>11/</u> <u>12/</u>	TM 1015, 160 hours at +125°C minimum (see J.3.5)	TM 1015, 240 hours at +125°C minimum (see J.3.5)	TM 1015, 160 hours at +125°C minimum (100%)	TM 1015, 240 hours at +125°C minimum (100%)	TM 1015, 160 hours at +125°C minimum (100%)	TM 1015, 240 hours at +125°C minimum. (100%) <u>13/</u>
11. Post burn-in (Interim) electrical parameters <u>8/</u>	In accordance with device specification	In accordance with device specification		In accordance with device specification <u>10/</u>	In accordance with device specification (100%) <u>9/</u>	In accordance with device specification (100%) <u>10/</u>
12. Reverse bias Burn-in test <u>11/</u> <u>14/</u>		TM 1015, On each device as specified in the applicable device specification		TM 1015, Condition A or C; 72 hours at +150°C minimum (100%)		TM 1015, Condition A or C; 72 hours at +150°C minimum (100%)
13. Post burn-in (Interim-reverse bias) electrical parameters <u>8/</u>				In accordance with device specification <u>10/</u>		In accordance with device specification (100%) <u>10/</u>
14. Percent defective allowable (PDA) calculation <u>15/</u>	5 percent all lots (TM5004), (subgroup I, table III)	5 percent and 3 percent on functional all lots (TM5004), (subgroup I, table III)	5 percent (see 3.5.1) (All Lots)	5 percent (see 3.5.1) 3 percent functional parameters at 25°C (All Lots)	5 percent PDA (All Lots)	5 percent PDA, 3 percent PDA for functional parameters at 25°C (All Lots)

Table IA : Microcircuits Screening procedure for hermetic QML microcircuits – Continued.

Test	Table IA Test for Hermetic QML microcircuits (MIL-PRF-38535)		Table I Test for Hermetic class level S and B microcircuits (MIL-STD-883 TM5004)		Proposed identical Table IA Test for QML Hermetic microcircuits to MIL-PRF-38535/TM5004 of MIL-STD-883	
	Class Q	Class V	Class level B (=class Q)	Class level S (=class V)	Class Q (class level B)	Class V (class level S)
15. Final electrical tests <u>16/</u> (see table III) a. Static test (1) at 25°C (2) Maximum and Minimum operated temperature b. Dynamic or functional test <u>17/</u> (1) at 25°C (2) Maximum and Minimum operated temperature c. Switching test (1) at 25°C (2) Maximum and Minimum operated temperature	In accordance with device specification (see J.3.6)	In accordance with device specification (see J.3.6)	In accordance with applicable device specification (100%)	In accordance with applicable device specification (100%)	In accordance with applicable device specification (see group A test) (100%)	In accordance with applicable device specification (see group A test) (100%)
16. Seal test <u>18/</u> a. Fine b. Gross	TM 1014 (see J.3.7)	TM 1014 (see J.3.7)	TM 1014 (100%)	TM 1014 (100%)	TM 1014 (100%)	TM 1014 (100%)
17. Radiographic (x-ray) or C-SAM <u>19/</u>				TM 2012, Two views (100%)		TM 2012, Two views (100%)
18. External visual inspection <u>20/ 21/</u>	TM 2009	TM 2009	TM 2009 (100%) <u>22/</u>	TM 2009 (100%) <u>22/</u>	TM 2009 (100%)	TM 2009 (100%)
19. Radiation dose rate induced latch-up test <u>22/</u>			TM 1020 (100%)	TM 1020 (100%)	TM 1020 (100%)	TM 1020 (100%)

Table IA : Microcircuits Screening procedure for hermetic QML microcircuits – Continued.

1/ All wafer lots shall be selected for testing in accordance with the requirements of method 5007 of MIL-STD-883.

2/ Unless otherwise specified, at the manufacturer's option for test samples selection of group B, bond strength test (method 5005) may be randomly selected prior to or following internal visual (method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual exam), and unsealed microcircuits awaiting further processing shall be stored in a dry, inert, controller environment until sealed. Test method 2010 applies in full except when method 5004, alternate 1 or alternate 2 (appendix A) is in effect (see 3.3 method 5007 of MIL-STD-883). For gallium arsenide (GaAs) devices only, TM 5013 of MIL-STD-883 should be used.

3/ For class level B devices, this test may be replaced with thermal shock method 1011, test condition A minimum.

4/ All microcircuits shall be subjected to constant acceleration. For large packages microcircuits which are contained in packages that have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be tested by replacing test condition E with condition D or with test conditions as specified in the applicable device specification. Unless otherwise specified in the acquisition document, the stress level for large, monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this data shall be specified in the QM plan, and available for review by the preparing or acquiring activity. The minimum stress level allowed in this case is condition A. When test condition F of method 1015 for temperature accelerated screening is used for either burn-in or reverse bias burn-in, it shall be used for both. Also, when devices have aluminum/gold metallurgical systems (at either the die pad or package post), the constant acceleration test shall be performed after burn-in and before completion of the final electrical tests (I.e., to allow completion of time limited tests but that sufficient 100 percent electrical testing to verify continuity of all bonds is accomplished subsequent to constant acceleration).

5/ At the manufacturer's option, external visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

6/ See paragraph A.4.6.3 in the appendix A of MIL-PRF-38535. The PIND test may be performed in any sequence after temperature cycling test and prior to post burn-in (interim) electrical parameters test.

7/ Prior to the first recorded electrical measurement in screening each class V (class level S) microcircuit, and when specified, each class Q (class level B) microcircuit shall be marked with a unique serial number assigned consecutively within the inspection lot. This serial number allows traceability of test results down to the level of the individual microcircuit within that inspection lot. For class V (class level S), inspection lot records shall be maintained to provide traceability from the serial number to the specific wafer lot from which the devices originated.

Table IA : Microcircuits Screening procedure for hermetic QML microcircuits – Continued.

8/ Interim (pre and post burn-in) electrical testing shall be performed when specified, to remove defective devices prior to further testing or to provide a basis for application of percent defective allowable (PDA) criteria when a PDA is specified. The PDA shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in all cases where delta parameters are specified) with the parameters, deltas and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class level S the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class level S screening where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or subplot for burn-in shall be used to determine the percent defective for that lot, or subplot and the lot or subplot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA (20 percent) or 2 devices, whichever is greater. This test need not include all specified device parameters, but shall include those measurements that are most sensitive to and effective in removing electrically defective devices (see A.4.6.1.1 of MIL-PRF-38535).

9/ When specified in the applicable device specification, 100 percent of the devices shall be tested for those parameters requiring delta calculations.

10/ For class V (class level S) microcircuit devices delta measurements shall be performed. Pre burn-in or interim electrical parameters shall be read and recorded only when delta measurements have been specified as part of post burn-in electrical measurements, and 100 percent of the devices shall be tested for those parameters requiring delta calculations.

11/ Burn-in shall be performed on all QML microcircuits, except as modified in accordance with device specification (SMD section 4.2), at or above their maximum rated operating temperature (for devices to be delivered as wafer or die, burn-in of packaged samples from the lot shall be performed to a quantity accept level of 10(0)). For microcircuits whose maximum operating temperature is stated in terms of ambient temperature (TA), table I of TM 1015 of MIL-STD-883 applies. For microcircuits whose maximum operating temperature is stated in terms of case temperature (TC), and where the ambient temperature would cause TJ to exceed +175°C, the ambient operating temperature may be reduced during burn-in from +125°C to a value that will demonstrate a TJ between +175°C and +200°C and TC equal to or greater than +125°C without changing the test duration. Data supporting this reduction shall be documented in the QM plan and shall be available to the acquiring and qualifying activities upon request.

12/ When test condition F of method 1015 for temperature accelerated screening is used for either burn-in or reverse bias burn-in , it shall be used for both. Also, when devices have aluminum/gold metallurgical systems (at either the die pad or package post), the constant acceleration test shall be performed after burn-in and before completion of the final electrical tests (i.e., to allow completion of time limited tests but that sufficient 100 percent electrical testing to verify continuity of all bonds is accomplished subsequent to constant acceleration).

13/ Dynamic burn-in only. Test condition F of method 1015 and temperature accelerated test requirement shall not apply. For class level S or class V burn-in test shall perform in accordance with TM 1015 of MIL-STD-883, on each device for 240 total hours at +125°C. For a specific device type, the burn-in duration may be reduced from 240 to 160 hours if three consecutive production lots of identical parts, from three different wafer lots pass percent defective allowable (PDA) requirements after completing 240 hours of burn-in. Sufficient analysis (not necessarily failure analysis) of all failures occurring during the run of the three consecutive burn-in lots shall not reveal a systematic pattern of failure indicating an inherent reliability problem which would require that burn-in be performed for a longer time. Other burn-in conditions may be considered by a class V validation team. The manufacturer's burn-in procedures shall contain corrective action plans, approved by the validation team, for dealing with lot failures (see B.4.1.f of MIL-PRF-38535).

Table IA : Microcircuits Screening procedure for hermetic QML microcircuits – Continued.

14/ The reverse bias burn-in is a requirement only when specified in the applicable device specification and is recommended only for a certain MOS, linear or other microcircuits where surface sensitivity may be of concern. When reverse bias burn-in is not required, interim post burn-in electrical parameter measurements shall be omitted. The order of performing the burn-in test and the reverse bias burn-in test may be inverted.

15/ The percent defective allowable (PDA) shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in all cases where delta parameters are specified) with the parameters, deltas and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class level S the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class level S screening where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or subplot for burn-in shall be used to determine the percent defective for that lot, or subplot and the lot or subplot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA (20 percent) or 2 devices, whichever is greater. This test need not include all specified device parameters, but shall include those measurements that are most sensitive to and effective in removing electrically defective devices (see A.4.6.1.1 of MIL-PRF-38535).

16/ Final electrical testing of microcircuits shall assure that the microcircuits tested and meet the electrical requirements of the device specification and shall include the tests of [table III](#), group A, subgroups 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11, unless otherwise specified in the device specification.

17/ Functional tests shall be conducted at input test conditions as follows: $V_{IH} = V_{IH(min)} + 20$ percent, -0 percent; $V_{IL} = V_{IL(max)} + 0$ percent, -50 percent; as specified in the most similar military detail specification. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.

CAUTION: To avoid test correlation problems, the test system noise (e.g., testers, handlers, etc.) should be verified to assure that $V_{IH(min)}$ and $V_{IL(max)}$ requirements are not violated at the device terminals.

18/ For class level B or class Q devices, the fine and gross seal tests shall be performed separately or together, between constant acceleration and external visual inspection test. For class level S or class V devices, the fine and gross seal tests shall be performed separately or together, between final electrical testing and external visual inspection test. In addition, for class level S or class V and class level B or class Q devices, all device lots (sublots) having any physical processing steps (e.g., lead shearing, lead forming, solder dipping to the glass seal, change of, or rework to, the lead finish, etc.) performed following seal or external visual inspection shall be retested for hermeticity and visual defects. This shall be accomplished by performing, and passing, as a minimum, a sample seal test (method 1014) using an acceptance criteria of a quantity (accept number) of 116(0), and an external visual inspection (method 2009) on the entire inspection lot (subplot). For devices with leads that are not glass-sealed and that have a lead pitch less than or equal to 1.27 mm (0.050 inch), the sample seal test shall be performed using an acceptance criteria of a quantity (accept number) of 15(0). If the sample fails the acceptance criteria specified, all devices in the inspection lot represented by the sample shall be subjected to the fine and gross seal tests and all devices that fail shall be removed from the lot for final acceptance. For class level S devices, with the approval of the qualifying activity, an additional room temperature electrical test may be performed subsequent to seal, but before external visual, if the devices are installed in individual carriers during electrical test.

19/ The radiographic screen may be performed in any sequence after serialization. Only one view is required for flat packages and leadless chip carriers having lead (terminal) metal on four sides.

Table IA : Microcircuits Screening procedure for hermetic QML microcircuits – Continued.

20/ External visual shall be performed on the lot any time after radiographic test and prior to shipment, and all shippable samples shall have external visual inspection at least subsequent to qualification or quality conformance inspection testing.

21/ The manufacturer shall inspect the devices 100 percent or on a sample basis using a quantity/accept number of 116(0). If one or more rejects occur in this sample, the manufacturer may double the sample size with no additional failures allowed or inspect the remaining devices 100 percent for the failed criteria and remove the failed devices from the lot. If the double sample also has one or more failures, the manufacturer shall be required to 100 percent inspect the remaining devices in the lot for the failed criteria. Re-inspection magnification shall be no less than that used for the original inspection for the failed criteria.

22/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible. If radiation dose rate induced latch-up screen test is required, shall be performed screening operation step after seal. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test shall be in accordance with the specified device specification. The PDA for each inspection lot or class level S or class V devices subplot, screened, shall be 5 percent or one device, whichever is greater.

Attachment # 2

Proposed draft of identical TCI/QCI tables for MIL-PRF-38535 and TM5005 of MIL-STD-883

Table II (Group B test shall be performed on each inspection lot for each qualified package type and lead finish)

Test <u>1/</u>	Table II Group B tests for QML microcircuits (MIL-PRF-38535)		Table IIa/IIb group B test for class level S and B microcircuits (TM5005 MIL-STD-883)		Proposed identical Group B tests for QML microcircuits (MIL-PRF-38535/ MIL-STD-883)	
	Class Q	Class V	Class level B (=class Q)	Class level S (=class V)	Class Q (class level B, Table IIb)	Class V (class level S, Table IIa)
Subgroup: 1 a. Physical dimensions <u>2/</u> b. Internal water-vapor content <u>2/ 3/</u>				a.TM 2016 2(0) b.TM 1018 3(0) or 5(1) 5,000 ppm maximum water content at 100°C		a.TM 2016 2(0) b.TM 1018 <u>4/</u> 3(0) or 5(1) 5,000 ppm maximum water content at 100°C
Subgroup : 2 a. Resistance to solvents <u>5/</u> b. Internal visual and mechanical	TM 2015 3(0)	TM 2015 3(0)	a. TM 2015 3(0)	a.TM 2015 3(0) b.TM 2013,2014 2(0) Failure criteria from design and construction requirements of applicable acquisition document	a. TM 2015 3(0)	a.TM 2015 3(0) b.TM 2013,2014 2(0) Failure criteria from design and construction requirements of applicable acquisition document
Sub-group : 3 a. Bond strength <u>6/</u> (1) Thermo compression (2) Ultrasonic (3) Flip-chip (4) Beam lead b. Die shear test or substrate attach strength or stud pull test c. Flip chip pull off test (test perform prior underfill dispense)	a. TM 2011 22(0) (1) condition C or D (2) condition C or D (3) condition F (4) condition H b. TM 2019 or 2027 for the applicable die size 3(0)	a. TM 2011 22(0) (1) condition C or D (2) condition C or D (3) condition F (4) condition H b. TM 2019 or 2027 for the applicable die size 3(0)	a. TM 2011 22(0) (1) condition C or D (2) condition C or D (3) condition F (4) condition H	a. TM 2011 22(0) (1) condition C or D (2) condition C or D (3) condition F (4) condition H b. TM 2019 or 2027 for the applicable die size 3(0)	a. TM 2011 22(0) (1) condition C or D (2) condition C or D (3) condition F (4) condition H b. TM 2019 or 2027 for the applicable die size 3(0) c. TM 2031 2(0)	a. TM 2011 22(0) (1) condition C or D (2) condition C or D (3) condition F (4) condition H b. TM 2019 or 2027 for the applicable die size 3(0) c. TM 2031 2(0)

Table II (Group B test shall be performed on each inspection lot for each qualified package type and lead finish)-continued.

Test <u>1/</u>	Table II Group B tests for QML microcircuits (MIL-PRF-38535)		Table IIa/IIb group B test for class level S and B microcircuits (TM5005 MIL-STD-883)		Proposed identical Group B test for QML microcircuits (MIL-PRF-38535/ MIL-STD-883)	
	Class Q	Class V	Class level B (=class Q)	Class level S (=class V)	Class Q (class level B, Table IIb)	Class V (class level S, Table IIa)
<u>Sub-group : 4</u> Solderability <u>7/</u>	TM 2003 22(0) 11 leads/devices Solder temperature +245°C ±5°C	TM 2003 22(0) 11 leads/devices Solder temperature +245°C ±5°C	TM 2003 22(0) Solder temperature +245°C ±5°C	TM 2003 22(0) Based on leads from 3 devices minimum Solder temperature +245°C ±5°C	TM 2003 22(0) (22 leads from 3 devices minimum) Solder temperature +245°C ±5°C	TM 2003 22(0) (22 leads from 3 devices minimum) Solder temperature +245°C ±5°C
<u>Subgroup: 5</u> <u>2/</u> a. Lead integrity <u>8/</u> b. Seal test (1) Fine (2) Gross c. Lid torque <u>9/</u>				a.TM 2004 45(0) Test condition B2, lead fatigue b. TM1014, as applicable c. TM2024, as applicable. 5(0)		a.TM 2004 45(0) (45 leads from 3 devices minimum) Test condition B2, lead fatigue b. TM1014, as applicable c. TM2024, 5(0) as applicable
<u>Subgroup: 6</u> a. Temperature cycling b. Constant acceleration c. Seal (a) Fine (b) Gross d. End-point electrical parameters		15(0) a.TM 1010, condition C, 100 cycles minimum. b. TM2001, condition E: Y ₁ -orientation only c.TM1014 d. As specified in the applicable device specification		15(0) a.TM 1010, condition C, 100 cycles minimum. b. TM2001, condition E: Y ₁ - orientation only c.TM1014 d. As specified in the applicable device specification		15(0) a.TM 1010, condition C, 100 cycles minimum. b. TM2001, condition E: Y ₁ - orientation only c.TM1014 d. As specified in the applicable device specification
<u>Subgroup: 7</u> <u>10/</u> Electrostatic discharge (ESD) sensitivity (For initial qualification only)		ESD testing specified in appendix A of MIL-PRF-38535.		ESD testing specified in appendix A of MIL-PRF-38535	TM 3015	TM 3015

Note: Steady state life test (Ex Sub-group 6 of group B) has been moved to table IV group C. Since, group C widely known as “Steady state life test”.

Table II (Group B test shall be performed on each inspection lot for each qualified package type and lead finish)-continued.

1/ Electrical reject devices from that same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electrical and provided the rejects are exposed to the full temperature/ time exposure of burn-in. Group B test shall be performed on each inspection lot as a condition for lot acceptance for delivery. Group B test shall be performed also each qualified package type and lead finish.

2/ Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot.

3/ This test is required only if it is a glass-frit-sealed package. Unless handling precautions for beryllia packages are available and followed method 1018, procedure 3 shall be used. See Subgroup 6 of table IV.

4/ Test three devices; if one fail, test two additional devices with no failures. At the manufacturers option, if the initial test sample (i.e., 3 or 5 devices) fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot. If sample size (accept number) of 5(1) is used to pass the lot, the manufacturer shall evaluate his product to determine the reason for the failure and whether the lot is at risk.

5/ Resistance to solvents testing required only on devices using inks or paints as a marking medium.

6/ Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in method 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see method 2011).

7/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number applies to the number of leads inspected except in no case shall less than 3 (three) devices be used to provide the number of leads required.

8/ The sample size number of 45 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test and lid torque test, if applicable, (see 9/) in order to meet the requirements of subgroup 4. For pin grid array leads and rigid leads, use method 2028. For leaded chip carrier packages, use condition B1. For leadless chip carrier packages only, use test condition D and a sample size number of 15 based on the number of pads tested taken from 3 devices minimum. Seal test (subgroup 4b) need be performed only on packages having leads exiting through a glass seal.

9/ Lid torque test shall apply only to glass-frit-sealed packages.

10/ The requirements for ESD testing are specified in paragraph 4.2.3 and appendix A of MIL-PRF-38535.

TABLE III. Group A (Electrical tests) 1/

Test	Table II group A electrical test for QML microcircuits (MIL-PRF-38535)		Table I group A electrical tests for class level S and B microcircuits (MIL-STD-883, TM5005)		Proposed identical group A test for QML microcircuits (MIL-PRF-38535/MIL-STD-883) 2/ 3/ 4/ 5/	
<u>Sub-groups :</u>	Class Q	Class V	Class level B (=class Q)	Class level S (=class V)	Class Q (class level B)	Class V (class level S) 6/
1-Static tests at +25°C 2-Static tests at +125°C 3- Static tests at -55°C	116(0)	116(0) or 100 percent/ 0 sample (see B.4.2.a)	116(0)	116(0) or 100 percent/ 0 sample	116(0)	116(0) or 100 percent/ 0 sample
4-Dynamic tests at +25°C 5-Dynamic tests at +125°C 6-Dynamic test at -55°C	116(0)	116(0) or 100 percent/ 0 sample (see B.4.2.a)	116(0)	116(0) or 100 percent/ 0 sample	116(0)	116(0) or 100 percent/ 0 sample
7-Functional test at +25°C 8a- Functional at +125°C 8b- Functional at -55°C	116(0)	116(0) or 100 percent/ 0 sample (see B.4.2.a)	116(0)	116(0) or 100 percent/ 0 sample	116(0)	116(0) or 100 percent/ 0 sample
9- Switching tests at +25°C 10- Switching tests at +125°C 11- Switching test at -55°C	116(0)	116(0) or 100 percent/ 0 sample (see B.4.2.a)	116(0)	116(0) or 100 percent/ 0 sample	116(0)	116(0) or 100 percent/ 0 sample

NOTES:

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2/ At the manufacturer's option, the applicable tests required for group A testing (see 1/) may be conducted individually or combined into sets of tests, subgroups (as defined in table III), or sets of subgroups. However, the manufacturer shall pre-designate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.

3/ The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as pre-designated in 2/, shall be 116/0.

4 A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For class level S or class V : if this testing results in a percent defective allowable (PDA) greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

6/ For class V (class level S) group A additional requirements see paragraph 4.2 of appendix B of MIL-PRF-38535.

TABLE IV. Group C tests (Die and package related test).

Test	Table IV group C die related test for QML microcircuits (MIL-PRF-38535)		Table III group C die related test for class level S and B microcircuits (MIL-STD-883 TM5005)		Proposed identical group C test for QML microcircuits (MIL-PRF-38535/MIL-STD-883) <u>1/</u> <u>2/</u>	
	Class Q	Class V	Class level B (=class Q)	Class level S (=class V)	Class Q (class level B)	Class V (class level S) <u>3/</u> <u>4/</u>
<u>Sub-group 1 :</u> a. Steady-state life test b. End-point electrical parameters	a. TM 1005 45(0) 1000 hrs @125°C b. As specified in the applicable device procurement specification	TM 1005 22(0) 2000 hrs @125°C or 1000 hrs @125°C 45(0) As specified in the applicable device procurement specification	a. TM 1005 1000 hrs @125°C 45(0) b. As specified in the applicable device procurement specification		a. TM 1005 45(0) 1000 hrs @125°C b. As specified in the applicable device procurement specification	a. TM 1005 22(0) 2000 hrs @125°C b. As specified in the applicable device procurement specification

NOTES:

1/ Group C test shall be performed on each SEC/actual device on a periodic basis (at least every 3 months) as a condition for acceptance for delivery.

2/ The quantity (accept no.) for all group C tests shall be 45/0, unless otherwise specified in the acquisition document.

3/ Life test shall be performed on a quantity (accept) criteria of 22(0) for 2000 hours @ 125°C or equivalent per TM 1005 to attain 44,000 device hours. The criteria of 45(0) for 1000 hours are also acceptable. For lot greater than 200, actual devices shall be used. For lot less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22 unless acceptable group C data from the SEC is available for the previous 3 months. The SEC shall have been produced under equivalent conditions as the production lot and as close in time as feasible, but not to exceed a 3-month period.

4/ Group C life tests shall be performed on the initial production lot of actual devices from each wafer lot, in accordance with [table IV](#). Group C life tests are not required to be performed on subsequent production lots when all the following conditions are met:

- (a) Subsequent production lots utilize die from the same wafer lot as the initial production lot.
- (b) Wafers or die remaining from the initial production lot are to be stored in dry nitrogen or equivalent controlled storage, and in covered containers.
- (c) No major changes to the assembly processes have occurred since the group C test was performed on the wafer lot.

Note: For ASICs, a sample size of 5 actual devices may be used with the balance being made up of the SEC.

TABLE V. Group D tests (Package related test) .

Test <u>1/</u>	Table V group D package related test for QML microcircuits (MIL-PRF-38535)		Table IV group D package related test for class level S and B microcircuits (MIL-STD-883, TM5005)		Proposed identical group D package related Test for QML microcircuits (MIL-PRF-38535/MIL-STD-883)	
	Class Q	Class V	Class level B (=class Q)	Class level S (=class V)	Class Q (class level B)	Class V (class level S)
Sub-group: 1 <u>2/</u> Physical dimensions	TM 2016 15(0)	TM 2016 15(0)	TM 2016 15(0)	TM 2016 15(0)	TM 2016 15(0)	TM 2016 15(0)
Sub-group 2: <u>2/</u> a. Lead integrity <u>3/</u> b. Seal <u>4/</u> (1) Fine (2) Gross c. Ball shear for BGA and column pull test for CGA package	a.TM 2004 15(0) lead fatigue B2 or applicable for the package technology style. b.TM 1014 15(0) Test condition as applicable	a.TM 2004 15(0) lead fatigue B2 or applicable for the package technology style. b.TM 1014 15(0) Test condition as applicable	a.TM 2004 45(0) Test condition B2 (lead fatigue) b.TM 1014 45(0) Test condition as applicable	a.TM 2004 45(0) Test condition B2 (lead fatigue) b.TM 1014 45(0) Test condition as applicable	a.TM 2004 45(0) (45 leads from 3 devices minimum) Test condition B2 (lead fatigue) or applicable for the package technology style. b.TM 1014 45(0) Test condition as applicable c. BGA-JESD22-B117 (ball shear) and For CGA-TM2003	a.TM 2004 45(0) (45 leads from 3 devices minimum) Test condition B2 (lead fatigue) or applicable for the package technology style. b.TM 1014 45(0) Test condition as applicable c. BGA-JESD22-B117 (ball shear) and For CGA-TM2003
Sub-group : 3 <u>5/</u> a. Thermal shock b. Temperature cycling c. Moisture resistance <u>6/</u> d. Seal (1) Fine (2) Gross <u>7/</u> e. Visual examination f. End-point electrical parameters <u>8/</u>	15(0) a.TM1011 test condition B, 15 cycles b TM1010 Test condition C, 100 cycles c.TM1004 d.TM1014 as applicable e.TM1004,TM1010 f. As specified in the applicable device	15(0) a.TM1011, test condition B, 15 cycles. b TM1010, test condition C, 100 cycles c.TM1004 d.TM1014 as applicable e.TM1004,TM1010 f. As specified in the applicable device specification	15(0) a.TM1011 Test condition B as a minimum, 15 cycles minimum. b TM1010 Test condition C, 100 cycles minimum. c.TM1004 d.TM1014 as applicable e.TM1004,TM1010 In accordance with visual criteria of method 1004 and 1010 f. As specified in the applicable device	15(0) a.TM1011 Test condition B as a minimum, 15 cycles minimum. b TM1010 Test condition C, 100 cycles minimum. c.TM1004 d.TM1014 as applicable e.TM1004,TM1010 In accordance with visual criteria of method 1004and 1010 f. As specified in the applicable device specification	15(0) a.TM1011 Test condition B as a minimum,15 cycles minimum. b TM1010 Test condition C, 100 cycles minimum. c.TM1004 d.TM1014 test condition as applicable e. TM1004, TM1010 In accordance with visual criteria of method 1004 and 1010 f. As specified in the applicable device	15(0) a.TM1011 test condition B as a 15 cycles minimum. b TM1010, test condition C, 100 cycles minimum. c.TM1004 d.TM1014 test condition as applicable e. TM1004, TM1010 In accordance with visual criteria of method 1004 and 1010 f. As specified in the applicable device specification

TABLE V. Group D tests (Package related test) - continued.

Test <u>1/</u>	Table V group D package related test for QML microcircuits (MIL-PRF-38535)		Table IV group D package related test for class level S and B microcircuits (MIL-STD-883 TM5005)		Proposed identical group D package related Test for QML microcircuits (MIL-PRF-38535/MIL-STD-883)	
	Class Q	Class V	Class level B (=class Q)	Class level S (=class V)	Class Q (class level B)	Class V (class level S)
Sub-group: 4 <u>5/</u> a. Mechanical shock b. Vibration, variable frequency c. Constant acceleration <u>9/</u> d. Seal (1) Fine (2) Gross e. Visual examination f. End-point electrical parameters	15(0) a.TM 2002 condition B min b.TM 2007 condition A min c.TM 2001 Test condition E minimum Y1 orientation only d.1014 condition as applicable e. In accordance with visual criteria of method 2007 f. As specified in the applicable device specification	15(0) a.TM 2002 condition B min b.TM 2007 condition A min c.TM 2001 Test condition E minimum Y1 orientation only d.1014 condition as applicable e. In accordance with visual criteria of method 2007 f. As specified in the applicable device specification	15(0) a.TM 2002 condition B min b.TM 2007 condition A min c.TM 2001 Test condition E minimum Y1 orientation only d.1014 condition as applicable e. In accordance with visual criteria of method 2007 f. As specified in the applicable device specification	15(0) a.TM 2002 condition B min b.TM 2007 condition A min c.TM 2001 Test condition E minimum Y1 orientation only d.1014 condition as applicable e. In accordance with visual criteria of method 2007 f. As specified in the applicable device specification	15(0) a.TM 2002 condition B minimum b.TM 2007 condition A minimum c.TM 2001 Test condition E minimum Y1 orientation only d.1014 condition as applicable e. In accordance with visual criteria of method 2007 f. As specified in the applicable device specification	15(0) a.TM 2002 condition B minimum b.TM 2007 condition A minimum c.TM 2001 Test condition E minimum Y1 orientation only d.1014 condition as applicable e. In accordance with visual criteria of method 2007 f. As specified in the applicable device specification
Sub-group: 5 <u>2/</u> a. Salt atmosphere <u>7/</u> b. Seal (1) Fine <u>7/</u> (2) Gross c. Visual examination	15(0) a.1009 Test condition A minimum b.1014 condition as applicable c.1009 In accordance with visual criteria of method 1009	15(0) a.1009 Test condition A minimum b.1014 condition as applicable c.1009 In accordance with visual criteria of method 1009	15(0) a.1009 Test condition A minimum b.1014 condition as applicable c.1009 In accordance with visual criteria of method 1009	15(0) a.1009 Test condition A minimum b.1014 condition as applicable c.1009 In accordance with visual criteria of method 1009	15(0) a.1009 Test condition A minimum b.1014 condition as applicable c.1009 In accordance with visual criteria of method 1009	15(0) a.1009 Test condition A minimum b.1014 condition as applicable c.1009 In accordance with visual criteria of method 1009

TABLE V. Group D tests (Package related test) - continued.

Test <u>1/</u>	Table V group D package related test for QML microcircuits(MIL-PRF-38535)		Table IV group D package related test for class level S and B microcircuits (MIL-STD-883) TM5005		Proposed identical group D package related Test for QML microcircuits (MIL-PRF-38535/MIL-STD-883)	
	Class Q	Class V	Class level B (=class Q)	Class level S (=class V)	Class Q (class level B)	Class V (class level S)
Sub-group: 6 <u>2/</u> Internal water vapor (cavity packages) <u>10/</u>	TM 1018 3(0) or 5(1) 5,000 ppm maximum water content at 100°C	TM 1018 3(0) or 5(1) 5,000 ppm maximum water content at 100°C	TM 1018 3(0) or 5(1) 5,000 ppm maximum water content at 100°C	TM 1018 3(0) or 5(1) 5,000 ppm maximum water content at 100°C	TM 1018 3(0) or 5(1) 5,000 ppm maximum water content at 100°C	TM 1018 3(0) or 5(1) 5,000 ppm maximum water content at 100°C
Sub-group: 7 <u>2/</u> Adhesion of lead finish <u>11/ 12/</u>	TM 2025 15(0) Based on leads from 3 devices minimum	TM 2025 15(0) Based on leads from 3 devices minimum	TM 2025 15(0) Based on leads from 3 devices minimum	TM 2025 15(0) Based on leads from 3 devices minimum	TM 2025 15(0) (15 leads from 3 devices minimum)	TM 2025 15(0) (15 leads from 3 devices minimum)
Sub-group: 8 <u>2/</u> Lid torque <u>13/</u>	TM 2024 5(0) Glass frit seal only	TM 2024 5(0) Glass frit seal only	TM 2024 5(0) Glass frit seal only	TM 2024 5(0) Glass frit seal only	TM 2024 5(0) Glass frit seal only	TM 2024 5(0) Glass frit seal only
Sub-group: 9 a. Soldering heat <u>14/</u> b. Seal (1) Fine (2) Gross c. External Visual examination d. End-point electrical	3(0) a. TM2036 b. TM1014 condition as applicable c. TM2009 d. As specified in the applicable device specification	3(0) a. TM2036 b. TM1014 condition as applicable c. TM2009 d. As specified in the applicable device specification	3(0) a. TM2036 b. TM1014 condition as applicable c. TM2009 d. As specified in the applicable device specification	3(0) a. TM2036 b. TM1014 condition as applicable c. TM2009 d. As specified in the applicable device specification	3(0) a. TM2036 b. TM1014 condition as applicable c. TM2009 d. As specified in the applicable device specification	3(0) a. TM2036 b. TM1014 condition as applicable c. TM2009 d. As specified in the applicable device specification

NOTES:

1/ Group D test shall be performed on each SEC/actual device at every 6 months. In-line monitor data may be substituted for subgroups D1, D2, D6, D7, and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. The in-line monitor data shall be traceable to the specific inspection lot(s) represented (accepted or rejected) by the data.

TABLE V. Group D tests (Package related test) - continued.

- 2/ Electrical reject devices from that same inspection lot may be used for samples.
- 3/ The sample size number of 45, $C = 0$ for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test if applicable (see 4/) in order to meet the requirements of subgroup 2. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads, use method 2028. For leadless chip carrier packages only, use test condition D and a sample size number of 15 ($C = 0$) based on the number of pads tested taken from 3 devices minimum.
- 4/ Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.
- 5/ Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
- 6/ Lead bend stress initial conditioning is not required for leadless chip carrier packages. For fine pitch packages (25 mil pitch) using a nonconductive tie bar, preconditioning shall be required on 3 devices only prior to the moisture resistance test with no subsequent electrical test required on these 3 devices. The remaining 12 devices from the sample of 15 devices do not require preconditioning but shall be subjected to the required endpoint electrical tests.
- 7/ After completion of the required visual examinations and prior to submittal to method 1014 seal tests, the devices may have the corrosion by-products removed by using a bristle brush.
- 8/ At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.
- 9/ Microcircuits which are contained in packages that have an inner seal or cavity perimeter of two inches or more in total length, or have a package mass of five grams or more, may be tested by replacing condition E with condition D method 2001. For packages that cannot tolerate the stress level of condition D, the manufacturer shall have data to justify a reduction in the stress level. The reduced stress level shall be specified in the manufacturers QM plan. The minimum stress level allowed in this case is condition A.
- 10/ Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with 5 additional devices from the same lot. If sample size (accept number) of 5(1) is used to pass the lot, the manufacturer shall evaluate his product to determine the reason for the failure and whether the lot is at risk.
- 11/ The adhesion of lead finish test shall not apply for leadless chip carrier packages.
- 12/ Sample size number based on number of leads with zero failure.
- 13/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (i.e., wherever frit seal establishes hermeticity or package integrity).
- 14/ This test is performed at qualification/re-qualification of design changes, which may affect this test. The manufacturer shall determine, for each package, the applicable conditions from test method 2036 that are appropriate for the mounting conditions, and assure by testing, or through their assembly processes, that the part is subjected to an equivalent time/temperature stress.

Attachment # 3

TABLE V: Group E tests (Radiation hardness assurance test)

Test <u>1/</u>	Table C-I group E RHA test for QML microcircuits (MIL-PRF-38535)		Table V group E RHA test for class level S and B microcircuits (MIL-STD-883)		Proposed identical group E RHA tests for QML microcircuits (MIL-PRF-38535/MIL-STD-883)	
	Class Q	Class V	Class level B (=class Q)	Class level S (=class V)	Class Q (class level B)	Class V (class level S)
Subgroup :1 <u>2/ 3/</u> Neutron irradiation test (Displacement Damage test) a. Initial qualification b. QCI c. Endpoint electrical parameters	TM 1017 @25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/ inspection lot	TM 1017 @25°C 2(0) devices/wafer or 11(0) devices /wafer lot	a.TM 1017 @25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0)devices/inspection lot b. TM 1017 2(0) devices/wafer or 11(0) devices/wafer lot c. As specified in accordance with device specification	a.TM 1017 @25°C 2(0) devices/wafer or 11(0) devices/wafer lot b. TM 1017 2(0) devices/wafer or 11(0) devices/ wafer lot c. As specified in accordance with device specification	a.TM 1017 @ 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11 devices/ inspection lot b. TM 1017 2(0) devices/wafer or 5(0) devices/wafer lot 11(0) devices/ inspection lot <u>4/</u> c. As specified in accordance with device specification	a.TM 1017 @ 25°C 2(0) devices/wafer or 11(0) devices/wafer lot b. TM 1017 2(0) devices/wafer or 11(0) devices/wafer lot <u>5/</u> c. As specified in accordance with device specification
Subgroup : 2 <u>3/ 6/ 8/</u> Total ionization dose(TID) test a. Initial qualification b. QCI c. Endpoint electrical parameters	a.TM 1019 @ 25°C 2(0) devices/wafer or 5(0) devices/wafer lot 22(0) devices/inspecti on lot	a.TM 1019 @ 25°C 2(0) devices/wafer or 22(0) devices/wafer lot 1(0)devices/waf er + 4(0) SEC/wafer or 5(0)devices/waf er lot+ 4(0) SEC/wafer	a.TM 1019 @ 25°C at maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot 22(0) devices/inspection lot b. TM 10197 @25°C at maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot 22(0) devices/inspection lot c. As specified in accordance with device specification	a.TM 1019 @ 25°C at maximum supply voltage 4(0) devices/wafer or 2(0) devices/wafer 22(0) devices/wafer lot b. TM 10197 @25°C at maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot 22(0) devices/ inspection lot c. As specified in accordance with device specification	a.TM 1019 @ 25°C at maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/ inspection lot b. TM 10197 @25°C at maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/ inspection lot <u>7/</u> c. As specified in accordance with device specification	a.TM 1019 @ 25°C at maximum supply voltage 2(0) devices/wafer or 22(0) devices/wafer lot or 1(0) device/wafer + 4(0) SEC/wafer or 5(0) devices/wafer lot+ 4(0) SEC/wafer b.TM 1019 @25°C <u>9/</u> 2(0) devices/wafer or 22(0) devices/wafer lot or 1(0) device/wafer + 4(0) SEC/wafer or 5(0) devices/wafer lot+ 4(0) SEC/wafer c. As specified in accordance with device specification

TABLE V. Group E tests (Radiation hardness assurance test) – Continued.

Test <u>1/</u>	Table C-I group E RHA test for QML microcircuits (MIL-PRF-38535)		Table V group E RHA test for class level S and B microcircuits (MIL-STD-883)		Proposed identical group E RHA tests for QML microcircuits (MIL-PRF-38535/MIL-STD-883)	
	Class Q	Class V	Class level B (=class Q)	Class level S (=class V)	Class Q (class level B)	Class V (class level S)
<u>Subgroup: 3 10/</u> a. Dose rate upset test (Transient ionizing irradiation test) b. End point electrical parameters		For Digital TM1021 For Linear TM1023 at 25°C 2(0) devices/wafer 11(0) devices/wafer lot	a. For Digital TM1021 For Linear TM1023 at 25°C 2(0) devices/wafer 11(0) devices/inspection lot b. As specified in accordance with device specification	a. For Digital TM1021 For Linear TM1023 at 25°C 2(0) devices/wafer 11(0) devices/wafer lot b. As specified in accordance with device specification	a. For Digital TM1021 For Linear TM1023 at 25°C 2(0) devices/wafer or 11(0) devices/inspection lot <u>7/</u> b. As specified in accordance with device specification	a. For Digital TM1021 For Linear TM1023 at 25°C 2(0) devices/wafer 11(0) devices/wafer lot <u>5/</u> b. As specified in accordance with device specification
<u>Subgroup: 4 11/</u> Radiation dose rate induced latch-up test		TM 1020 As specified in the device specification	TM 1020 As specified in the device specification	TM 1020 As specified in the device specification	TM 1020 As specified in the device specification	TM 1020 As specified in the device specification
<u>Subgroup: 5 12/</u> Single event effects (SEE) test		ASTM F-1192 or JESD57 4(0) devices		ASTM F-1192 or JESD57 4(0) devices As specified in the device specification		ASTM F-1192 or JESD57 4(0) devices As specified in the device specification

NOTES:

1/ Group E tests may be performed prior to device screening. Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. End point electrical parameters as specified in accordance with device specification.

2/ This test is to be conducted only when specified in the purchase order or contract. Neutron irradiation test (Displacement damage test) is not required for MOS devices unless bipolar elements are included by design.

3/ The radiation hardness assurance capability level (RHACL)/radiation assurance in the SPEC level is the ratio of the capability level to the specification level of devices fluence. Subgroups shall be invoked when radiation hardness assurance capability level (RHACL) specification requirements are not met. For an example if RHACL/SPEC ratio is > 10 then this test may not be required, but if the RHACL/SPEC ratio falls within > 1 and ≤ 10 then the subgroup test is required.

TABLE V. Group E tests (Radiation hardness assurance test) – Continued.

4/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 27(1).

5/ In accordance with wafer lot. If one part fails, 7 additional parts may be added to the test sample with no additional failures allowed, 18(1).

6/ Parts used for one subgroup test may not be used for other subgroups, but may be used for higher levels in the same subgroup. For subgroup 2, total dose exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.

7/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).

8/ Traceability to the specific wafer is required.

9/ In accordance with wafer for device types with greater than or equal to 100,000 equivalent transistors/chip selected from the wafer. The manufacturer shall define and document sampling procedures. The test structures shall be randomly selected from the wafer. An X-ray source may be used on test structures at the wafer level provided correlation has been established between the X-ray and the Cobalt-60 source and shall be documented in the QM plan.

10/ Radiation dose rate upset (Transient irradiation test) test shall be conducted during qualification on first QCI when specified in purchase order or contract.

11/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible. If radiation dose rate induced latch-up screen test is required, shall be performed screening operation after seal. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test shall be in accordance with the specified device specification. The PDA for each inspection lot or class level S or class V devices subplot, screened, shall be 5 percent or one device, whichever is greater.

12/ Single event effects (SEE) test shall be performed during initial qualification and after any design or process change that may affect SEE response. When single event effects (SEE) testing is specified in the purchase order or contract the SEE test shall be performed according to ASTM F-1192 or JESD57. For destructive SEE (SEB and SEGR) test shall be performed in accordance to JESD57.