ENGINEERING PRACTICE STUDY

TITLE : Preparing a new class Y (ceramic non-hermetic flip chip device) standard microcircuit drawings (SMD) boilerplate under MIL-PRF-38535.

June 12, 2017

STUDY PROJECT 5962-2017-004

FINAL REPORT

Study Conducted by DLA Land and Maritime
Document Standardization Division (VA)
Active Devices Branch

Prepared by:

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ENGINEERING PRACTICE STUDY
for

Preparing a new class Y (ceramic, non-hermetic, flip chip, ball grid array (BGA) and column grid array (CGA) device) standard microcircuit drawings (SMD) boilerplate under MIL-PRF-38535.

I. OBJECTIVE: The purpose of this Engineering Practice (EP) Study is to obtain input from the military services, microcircuit manufacturers, and space user communities for the preparing of standard microcircuit drawings (SMD) **boilerplate** for new **class Y** ceramic, non-hermetic, flip chip, ball grid array (BGA) and column grid array (CGA) devices under MIL-PRF-38535. This standard boilerplate will help to generate a procurement document (SMD) for class Y flip chip device, and shall include all necessary reliability test and requirements to meet the governing specification MIL-PRF-38535.

II. BACKGROUND: Design requirements of modern electronics warfare/space monitoring systems are growing faster and moving forward to complex technologies with new packaging construction. Considering complexity of new technologies and device packaging techniques DLA Land and Maritime along with NASA and Space community members explored the class Y concept and developed the requirements for qualification and screening of flip chip ceramic non-hermetic microcircuits packages for space applications.

The class Y journey started in 2009 with numerous engineering studies, meetings and teleconferences to evaluate class Y devices many subcomponents, test developments and requirements. In December 2013, governing performance specification MIL-PRF-38535 was approved adding class Y devices requirements that lead to the start of class Y devices manufacturing process qualification and QML certification.

Currently DLA Land and Maritime, along with Space communities, are working with manufacturers for supplying QML class Y ceramic, non-hermetic, flip chip, ball grid array (BGA) and column grid array (CGA) devices for space applications.

DLA Land and Maritime-VAC launched an EP study project for preparing a new boilerplate for class Y ceramic, non-hermetic, flip chip, BGA/CGA device SMD to meet MIL-PRF-38535 requirements. DLA Land and Maritime-VAC is also requesting military services, microcircuits manufactures, and space communities to review the attached draft boilerplate requirements and provide comments/feedback to DLA Land and Maritime within 30 days from the date of this letter.

III. RESULTS: The EP Study initial draft was posted on the web and coordinated with military services, microcircuit manufacturers, original equipment manufacturers, and user communities in March 13, 2017 for review and comments. All received comments were discussed at Colorado JEDEC joint JC-13.2/G-12 meeting in May, 2017. DLA Land and Maritime-VAC has prepared a final report for standardization of standard microcircuit drawings (SMD) **boilerplate** for new **class Y** ceramic, non-hermetic, flip chip, ball grid array (BGA) and column grid array (CGA) devices under MIL-PRF-38535 (see attachment # 1).

IV. CONCLUSIONS: The outcome of this EP study for QML class Y ceramic, non-hermetic, flip chip devices SMD boilerplate will be published to the DLA Land and Maritime website, and boilerplate shall be used for generating all new QML class Y SMDs.

(Attachment # 1)

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Class Y SMD Boilerplate

(Class Y Ceramic non hermetic flip chip LGA/BGA/CGA devices)

REV																				
SHEET																				
REV																				
SHEET	15	16	17																	

REV STATUS	REV														
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Your name here	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
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AMSC N/A	REVISION LEVEL	SIZE **A** / CAGE CODE **67268** / **5962-XXXXX**
		SHEET 1 OF XX

DSCC FORM 2233
APR 97

5962-EXXX-XX

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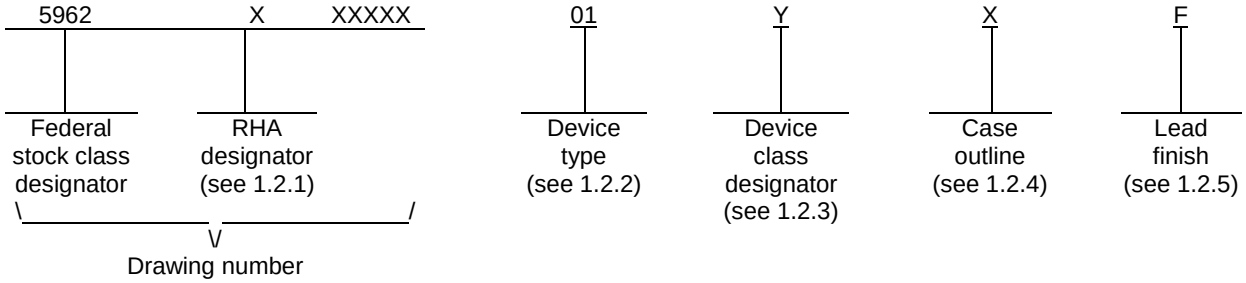
1. SCOPE

1.1 Scope. This drawing documents product assurance class level consisting of high reliability space application device class Y ceramic non-hermetic flip chip device. A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device class Y:



1.2.1 RHA designator. Device class Y RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	XXXXXX	XXXXXXXXXXXXXXXXXXXXXXXXXX

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below.

Device class	Device requirements documentation
Y	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 or as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure X	XXX	Ceramic Column Grid Array (CCGA)
X	See figure X	XXX	Ceramic Ball Grid Array (CBGA)
X	See figure X	XXX	Ceramic land Grid Array (CLGA)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device class Y. X/

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x/ Terminal lead finish F is tin lead alloy with copper spiral column. Package case outline X solder columns material is Sn= xx and Pb=xx and wrapped with copper spiral coil. A layer of eutectic solder plated over the surface of the Cu spiral.

Or (if no Cu spiral)

xx/ Terminal lead finish F is tin lead alloy. Package case outline Y solder columns material is Sn= xx and Pb=xx .

For BGA packages:

x/ Terminal lead finish F is tin lead alloy with bismuth. Package case outline K solder balls material is Sn= xx and Pb=xx and Bi= xx.

Or (if no Bi or alloy)

xx/ Terminal lead finish F is tin lead alloy. Package case outline K solder balls material is Sn= xx and Pb=xx .

1.3 Absolute maximum ratings. 1/

1.4 Recommended operating conditions.

1.5 Radiation features. XX/

Maximum total dose available (high dose rate = 50 – 300 Rad(Si)/s)..... xx Rad(Si)

Maximum total dose available (low dose rate ≤ 10m Rad(Si)/s) ..... xx Rad(Si)

Heavy ion single event phenomenon (SEP):

No single event latch-up (SEL) occurs at effective LET (see 4.4.4.xx) ..... ≤ xxx Mev-cm^2/mg

No single event upset (SEU) occurs at effective LET (see 4.4.4.xx) ..... ≤ xx Mev-cm^2/mg

Single event transient (SET) observed at onset LET (see 4.4.4.xx) ..... xx Mev-cm^2/mg

For Proton test:

No proton upset error occurs ..... ≤ xx MeV

Single event upset (SEU) error rate (SER)..... xx upsets/bit-day

Neutron irradiation /displacement damage test ..... xx neutrons/cm^2

Prompt dose upset/latch-up test.....xx Rad(Si)/sec

Dose rate survivability (DRS) test .....xx Rad(Si)/sec

Applicable RHA information shall be provided in this section 1.5

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

XX/ For devices with solder terminations BGA/CGA devices RHA group E subgroups test may be performed without balls and Columns in accordance with MIL-PRF-38535. Total ionizing dose(TID) test shall be performed per test method 1019 of MIL-STD-883. Heavy ion single event phenomenon (SEP) test shall be performed per ASTM F1192 or JESD57.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD57 - Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation

J-STD-020 - Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices

JEP163 - Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits

JESD22-B117 - Solder ball shear test method

JESD471 - Symbol and Label for Electrostatic Sensitivity Devices.

JESD625 - Requirements for Handling Electrostatic Discharge Sensitive (ESDs) Devices

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for class Y devices shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device class Y.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and **figure** ___ .

3.2.2 Terminal connections. The terminal connections shall be as specified on **figure** ___.

3.2.3 Truth table(s). The truth table(s) shall be as specified on **figure** ___.

3.2.4 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on **figure** ___.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table IA.

3.4.1 Solderability test for BGA/CGA packages: Solderability test for case outline XX for CGA/BGA package has been verified during solder column or ball attachment process in accordance with method 2003 of MIL-STD-883.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For class Y packages where marking of the entire SMD PIN number is required (see herein 1.2). For RHA product, the RHA designator shall still be marked. Marking for device class Y shall be used ink or laser mark in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device class Y shall be a "QML" or "Q" as required in MIL-PRF-38535.

A.5.1.1 Electrostatic discharge (ESD) sensitivity mark. ESD marking on devices and, on container/carriers are required as specified in MIL-PRF-38535. All of the markings shall appear on the carrier, unit pack (e.g., individual foil bag), unit container, or multiple carriers (e.g., tubes, rails, magazines) for delivery. An industry standard symbol for identifying ESD sensitive items (e.g., JESD471 symbol) shall be marked on the carrier or container.

A.5.1.1.1 Moisture sensitivity level (MSL) mark. Non-hermetic devices such as class Y can exhibit sensitivity to moisture-induced stress and must be handled, packaged, and stored in a proper manner to avoid potential damage during assembly solder reflow attachment and/or repair operations. Moisture sensitivity levels are defined as a rating identifying a component's susceptibility to damage due to absorbed moisture when subjected to reflow soldering. The manufacturer shall be required to define the moisture sensitivity level (MSL) for each non-hermetic device in accordance with J-STD-020.

3.5.2 Lot date code. Flip chip devices lot date code shall be assigned after underfill cured to identify the device with the assembly processing and assembly location. Devices will be traceable through the lot date code to the assembly year, underfill sealing week and assembly location.

3.6 Certificate of compliance. For device class Y, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets for device class Y and the requirements of MIL-PRF-38535.

3.7 Certificate of conformance. A certificate of conformance as required for device class Y in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	

See footnotes at end of table.

TABLE IB. SEP Test Limits 1/ 2/ 3/

Device Type	Ion Type	Memory pattern	Bias V_{DD} = xx V SEU Rate 7/	Bias V_{DD} = x V No latch-up (SEL) Effective LET
All	Heavy ion	4/	Xxx upsets/bit-day 5/	LET ≤ xx MeV/mg/cm^2
All	Proton	4/	Xx upsets/bit-day 6/	-

1/ For SEP test conditions, see xxx herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ For SEL worst case temperature T_A = +125°C± 10°C and for SEU worst case temperature T_A = +25°C±10°C.
4/ Testing shall be performed using checkerboard and checkerboard bar test patterns.
5/ Weibull parameters are available from the vendor upon request.
6/ The proton test is performed at the energy level xx MeV and CRÈME 96 with Weibull parameters. Weibull parameters are available from the vendor upon request.
7/ Based on CREME96 (or other SER calculating programs) results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield using Weibull parameters derived from test results and analysis. Weibull parameters are available from the vendor upon request to calculate upset rates for other orbits and space environments.

Applicable RHA information shall be provided in this SEP table IB

FIGURE 1. Case outline.

FIGURE 2. Terminal connections.

FIGURE 3. Truth table.

FIGURE 4. Block diagram.

FIGURE 5. Timing waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For class Y device, sampling and inspection procedures shall be performed in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For class Y device, screening test shall be performed in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Burn-in criteria for class Y device.

a. The manufacturers shall be provide appropriate burn-in information herein table II in accordance with JEDEC publication JEP163. The burn-in test duration, test condition and test temperature shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table III herein.

c. Additional screening for device class Y shall be required as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device class Y. Qualification inspection for device class Y shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for class Y shall be performed in accordance with MIL-PRF-38535 including groups A, B, C, D, and E (RHA test) and as specified.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Devices induced latch-up tests are required for device class Y. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up tests, test all applicable pins on five devices with zero failures.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JESD20 and table IA herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

d. For device class Y, subgroups 7 and 8 tests shall be sufficient to verify the truth table on figure 2 herein or verifying the functionality of the device.

4.4.2 Group B inspection.

a. For class Y flip chip devices with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures of lid shear test for approval.

b. For ball grid array (BGA) packages, ball shear test shall be performed in accordance with JESD22-B117.

c. For column grid array (CGA) packages, solder column pull test shall be performed in accordance with TM 2038 of MIL-STD-883.

4.4.3. Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein. For device class Y steady-state life tests circuit shall be maintained by the manufacturer and shall be made available to the acquiring or preparing activity upon request.

4.4.2.1 Additional criteria for device class Y. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class Y, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5K Rad (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Y devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 or C JESD57 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be adequate to detect latch-up, because the relevant junction is often buried deep below the active chip. Range of the ion which shall be sufficiently penetrate well beyond the deepest part volume of the devices to of the sensitive detect latch-up.

e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

4.4.4.5 Neutron irradiation/displacement damage testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25 °C ±5 °C after an exposure of 1 x 10^{12} neutrons/cm^2 .

TABLE II. Electrical test requirements.

Test requirements (in accordance with MIL-PRF-38535, screening table IA, group A, B, C, D, E and MIL-STD-883 test method)	Subgroups (in accordance with MIL-PRF-38535, table III)
	Device class Y
Interim electrical parameters, (screening table IA)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Static burn-in I, method 1015 (see 4.2.1a)	Required 1/
Static burn-in II method 1015 (see 4.2.1a)	Required 1/
Dynamic burn-in , method 1015 (see 4.2.1a)	Required 1/
Final electrical parameters, (screening table IA)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4.1)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group B end point electrical parameters, (see 4.4.2)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters, (see 4.4.3)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group D end-point electrical parameters, (see 4.4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group E end-point electrical parameters, (see 4.4.5) 3/	1,7,9
Post-column attach electrical parameters test (see 4.2) 3/	1

1/ The manufacturers shall be provide appropriate burn-in information herein table II in accordance with burn-in publication JEP163.
2/ PDA applies to subgroups 1 and 7.
3/ For flip chip class Y BGA/CGA devices, screening and group A, B, C, D and RHA test group E shall be preformed at land grid array (LGA) level. i.e. before ball or column attached to the devices. After ball or column attach, electrical test shall be performed at 25°C (Group A, subgroup 1) as a minimum to verify that no electrical/mechanical damage has been introduced due to the column attach process.
x/ For flip chip Class Y device, Nondestructive bond pull (NDBP) test is not required.
x/ For devices without a cavity such as class Y or flip chip devices with underfill, Particle impact noise detection (PIND) test is not applicable.
x/ For flip chip technology C-SAM inspection is required. C-SAM inspection shall be performed on each flip chip device in accordance with TM 2030 of MIL-STD-883.
x/ C-SAM test shall be performed on each device when a heat sink or lid is attached directly to the back side of the flip chip die in accordance with TM 2030 of MIL-STD-883.
x/ Seal test (TM 1014) is not required for class Y non-hermetic devices.

TABLE III. Burn-in and operating life test delta parameters (+25°C).

All critical parameter 1/ 2/	Symbol	Device types	Delta limits
For example: Supply current	I_{CC}		
Input current low level	I_{IL}		
Input current high level	I_{IH}		
Output voltage low level	V_{OL}		
Output voltage high level	V_{OH}		

1/ These parameters shall be recorded before and after the required burn-in to determine delta drift limits.

2/ Manufacturer shall be specified in table III all critical parameters that have delta drift values during burn-in test.

4/ The delta drift limit shall be computed with reference to the previous interim electrical parameters. The delta drift limit shall be specified in table III.

4.5 Delta measurements for device class Y. Class Y devices, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with MIL-PRF-38535, table III. Delta limits shall be required on class Y devices, and shall be recorded before and after the required burn-in screens and steady-state life tests to determine delta limit compliance. The electrical parameters to be measured, with associated delta limits are listed in table III.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device class Y.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device class Y. Sources of supply for device class Y are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Package integrity demonstration test plan (PIDTP). For class Y microcircuits, the PIDTP must address issues unique to non-hermetic construction and materials, such as potential materials degradation, moisture absorption, and resistance of active devices, passive devices and interconnects to environmental effects and processing stresses. Flip chip PIDTP also shall address the materials and processes unique to solder bump interconnect attach, underfill and thermal interface materials (TIM). The QA approved PIDTP shall be documented in the product QM plan and shall be available upon requested in the purchase order or contract.

6.8 CGA packages lead finish: Microcircuits devices for column grid array (CGA) packages are supplying to this drawing with terminal lead finish mark “F”. Terminal lead finish F is tin (Sn) and lead (Pb) alloy with copper spiral column, and solder column material contains compositions of Sn= xx and Pb=xx and wrapped with copper spiral coil. A layer of eutectic solder plated over the surface of the Cu spiral.

6.9 BGA packages lead finish: Microcircuits devices for ball grid array (BGA) packages are supplying to this drawing with terminal lead finish mark “F”. Terminal lead finish F is tin (Sn) and lead (Pb) and Bismuth (Bi) alloy, and solder ball material contains compositions of Sn= xx and Pb=xx and Bi=xx .

6.10 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

a. RHA test conditions of SEP.

b. Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latchup (SEL).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: XX-XX-XX

Approved sources of supply for SMD 5962-XXXXX are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-XXXXXXXXXX	XXXXX	XXXXXXXXX
5962-XXXXXXXXXX	XXXXX	XXXXXXXXX

1/ Microcircuits devices for column grid array (CGA) or ball grid array (BGA) packages are supplied to this drawing with terminal lead finish mark “F” which are a tin (Sn) and lead (Pb) or Bismuth (Bi) alloy or other . The solder column material contains compositions of Sn= xx% and Pb=xx% or Bi= % or other.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.