

ENGINEERING PRACTICE (EP) STUDY

TITLE: Evaluation and test requirements of Pb free bump for flip chip devices under MIL-PRF-38535.

May 01, 2021

EP Study Project Number: 5962-2021-001

Final Report

**Study Conducted by DLA Land and Maritime
Document Standardization Division (VA)
Active Device Branch (VAC)**

Prepared by:

**Rodney Chambers
DLA Land and Maritime -VAC
Email: Rodney.Chambers@dla.mil
Phone: 614-692-9460**

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EP study of Evaluation and test requirements of Pb free bump for flip chip devices under MIL-PRF-38535.

- I. **OBJECTIVE:** The purpose of this Engineering Practice (EP) Study is to obtain input/feedback from the military services, microcircuit manufacturers, package assembly houses and user communities concerning Pb free bump use into flip chip devices and its test requirements to be added to MIL-PRF-38535 documents.
- II. **BACKGROUND:** Design requirements of modern electronics systems are growing faster and moving forward with an advance in complex package technologies like flip chip. Flip-chip design have been developed with Controlled Collapse Chip Connection (C4) compared with conventional packaging using wire-bonding technology, flip-chip offers many advantages such as high I–O density, short interconnects, self-alignment, better heat dissipation through the back of the die, smaller footprint, lower profile, high throughput, etc. The outstanding merits of flip-chip have made it one of the most attractive techniques in modern electronic packaging.

MIL-PRF-38535 requires Sn/Pb bump but environmental and EU regulations on the use of certain substances, including Lead (Pb), have resulted in a continuing global transition to Pb-free electronics. Flip chip manufacturers are experiencing a changing primary market in worldwide consumer electronics due to the conversion to Pb-free. However, DLA Land and Maritime with Aerospace and Defense electronics sector has been more cautious to the adoption of Pb-free bump technologies into flip chip devices.

Considering the current situation of Sn/Pb bumps inaccessibility, DLA Land and Maritime-VA along with flip chip manufacturers, Aerospace and Defense community proposed to conduct an EP study for developing a consensus in test requirements for using Pb free solder bumps to MIL-PRF-38535 flip chip devices.

- III. **RESULTS:** The Ep Study project initial draft posted to DLA Land and Maritime website on December 18, 2020 and distributed to military services, microcircuit manufacturers, original equipment manufacturers, and user communities for review and comments. All received comments/responses were compiled and discussed internally within DLA-VAC. From the feedback received, 25 comments are appended within the original proposal (see attachment #1). The DoD requirement of at least 3% Lead (Pb) by weight has been successful in providing high reliability and maintainability applications. The 3% Lead (Pb) requirement has also been successful at suppressing Tin Whisker growth. The proposal within this ep study refers to Pb-free as Tin alloyed solders such as Tin-Silver (SnAg), Tin-Silver-Copper (Sn-Ag-Cu, also known as SAC), or any tin alloy containing less than 3% lead (Pb) content by weight. The use of pure unalloyed Tin is prohibited. Mitigation techniques called out in this EP Study refer to mitigating risk of failure and should not be confused with assurance against whisker growth.

Not determined within this EP Study:

- Are there affects to die passivation / glassivation areas when using higher temperature profile solders such as SnAg and Sn-Ag-Cu (SAC) type solders?
 - How to handle identifiers for devices that contain (Pb-free) solder (i.e. defining the alloy composition in the Standard Microcircuit Drawing (SMD)?
 - Do we have verifiable, (i.e., acoustic microscopy), voiding requirements to assure all bumps have encapsulation?
- IV. **CONCLUSIONS:** This EP study focuses on the allowance of Pb-free solder bumps with underfill used internal to flip chip devices and subject across all package technologies of MIL-PRF-38535. Manufacturer shall document a Lead Free Control Plan (LFCP) in the PIDTP for QA approval. Long-term reliability is unknown in varying applications and environments upon allowing any tin alloy bump containing less than 3% lead (Pb) content by weight. The user is cautioned to review the Standard Microcircuit Drawing (SMD) to assure the part being acquired meets the requirements/reliability of the system application. Two separate ongoing JEDEC task groups are coordinating qualification and screening requirements specific to flip chip applications and class Y expansion to organic substrates. DLA-VAC will coordinate with these working groups to help address any overlaps in proposed changes. If no other EP study is determined necessary, the next draft revision to MIL-PRF-38535 will have all proposed changes together in a single document for review and comment prior to implementation.

ATTACHMENT # 1

Evaluation and test requirements of Pb free bump for flip chip devices under MIL-PRF-38535

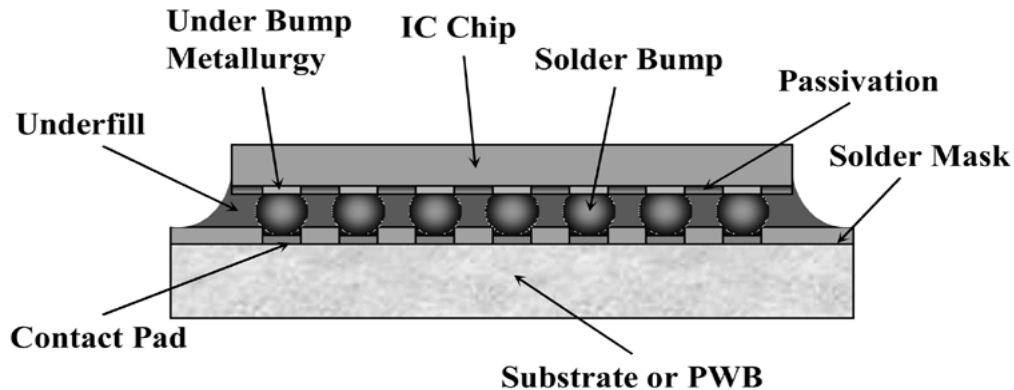


Figure 1: Typical flip chip layout

Issues/concerns for Pb free bump in flip chip devices:

There are two concerns to be addressed with the Pb-free transition: tin whiskers and Pb-free joint integrity and durability.

The goal of this EP study is to find out standard practices for high reliability part manufacturers and use them to mitigate the Pb-free risks in the parts. SAE ARP6537 document shall be used as a guideline to qualify and provide risk mitigation of Pb free bump to MIL-PRF-38535 flip chip devices.

#	Comments	BY:
*1	Currently does not build any Class Y as it is defined in MIL-PRF-38535. Thus, we have no feedback regarding Class Y as it is currently defined with a ceramic header.	13.2 MFG

Proposed Pb-free bump verbiage to MIL-PRF-38535 Section A.3.5.6.3 ***2 *3 *4**

A.3.5.6.3 Microcircuit finishes. Finishes of all external leads or terminals and all external metal package elements shall conform to either A.3.5.6.3.2 or A.3.5.6.3.3, as applicable. The use of pure tin, as an underplate or final finish, is prohibited both internally and externally. The tin content of solder shall not exceed 97 percent. Tin shall be alloyed with a minimum of 3 percent lead by weight. **However, the use of lead-free solder bumps used internal to device with underfill or encapsulation and mitigated per SAE ARP6537 are allowed. Pb-free solders allowed by IPC J-STD-001DS are also allowed in limited amounts for high temperature solder needs.** The lead finish designator (see A.3.6.2.7) shall apply to the finish of the leads or terminals. The leads or terminals shall meet the applicable solderability and corrosion resistance requirements. The other external metallic package elements (including metalized ceramic elements) shall meet the applicable corrosion resistance requirements. Finishes on interior elements (e.g., bonding pads, posts, tabs) shall be such that they meet the lead bonding requirements and applicable design and construction requirements. The use of strike plates is permissible to the maximum thickness of 10 microinches (0.25 micrometer). All plating of finishes and undercoats shall be deposited on clean, nonoxidized metal surfaces. Suitable deoxidation or cleaning operations shall be performed before or between plating processes. All parts shall be capable of meeting the following requirements of MIL-STD-883:

- a. Test method 2004, lead integrity, test condition B1, B2, or D, or test method 2028, pin-grid package destructive lead pull test, as applicable.
- b. Test method 1009, salt atmosphere.
- c. Test method 2003, solderability (plus time/temperature exposure of burn-in except for devices which have been hot solder dipped or have undergone tin fusing after burn-in).
- d. Test method 2025, adhesion of lead finish.

#	Comments	BY:
*2	Regarding SAE ARP6537, does this spec have any specific alloy composition requirement or underfill requirements?	13.2 MFG
	ARP6537 does not specify bump alloy composition requirements. The use of underfill is a requirement. Solder alloy and underfill composition details should be documented in the PIDTP. The Pb-free bump qualification test along with screening and QCI test are used to bound the reliability risk for any materials. The use of pure unalloyed Tin is prohibited. The PIDTP will be used to determine acceptable solder bump compositions with matching underfill.	DLA:
*3	suggestion IPC J-STD-001 (space addendum)	13.2 MFG
	Agree to remove the revision designation and just state (space addendum).	DLA:
*4	What does limited amounts mean?	13.2 MFG
	The proposed wording in the EP-study is as originally proposed to DLA. The term "limited amounts" is used in reference to cases where a high temperature solder, e.g., SN96.3Ag3.7, is required inside the part (which is believed to be limited). High temperature solder alloys, e.g., SN96.3Ag3.7, shall only be used where specifically indicated by approved Standard Microcircuit Drawing (SMD). The verbiage here will need adjustment regarding the use of materials called out in the J-STD-001 space addendum. Recommend the following change in verbiage. From: Pb-free solders allowed by IPC J-STD-001DS are also allowed in limited amounts for high temperature solder needs. To: Pb-free solders shall have a Lead Free Control Plan (LFCP) and shall be documented in the PIDTP for QA approval.	DLA:

- Proposed update to Appendix H:**

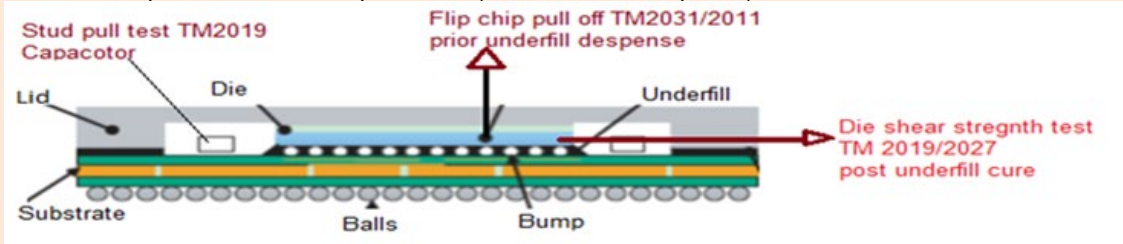
H.3.4.4.1.2.1 Pb free bump qualification for Flip-chip devices : For microcircuit devices containing Pb-free solder bumps with Underfill/Encapsulation. Manufacturer shall perform the following test for Pb free bump initial qualification for risk mitigation: ***5**

Screen	Test Method	Condition *6	Sample Size
Thermal Cycling	MIL-STD-883, TM1010	Cond C, 1000 Cycles *7	22 pieces
HAST *8	JESD22-A110 (Biased HAST)	130°C/85% relative humidity for 96 hours Or 110°C/85% relative humidity for 264 hours	16 pieces
Thermal Shock *9	MIL-STD-883, TM1011	Cond B, 15 cycles	22 pieces
Shock and Vibe *10	MIL-STD-883, TM2002, 2007, and 2001 similar to MIL-PRF-38535 Group D, Subgroup 4 (without hermeticity)	TM2002: Cond B TM2007: Cond A TM2001: Cond D	15 pieces
Bump Shear Test	JESD22-B117 or JESD22-B109B *11		Minimum of 30 bumps on each of 3 different die
Die Attach Bond Strength	MIL-STD-883, TM2011	Cond F	3 pieces
Die Shear Strength	MIL-STD-883, TM2019		3 pieces
Die Pull Off	MIL-STD-883, TM2031		3 pieces
Destructive Part Analysis(DPA) bump sample post-thermal cycle and thermal shock test	See DPA see 4.1.1		1 piece

***12**

#	Comments	BY:
*5	New section added to 38535 outlining the following test requirements for initial bump qualification for risk mitigation. Proposing the following update: H.3.4.4.1.2.1 <u>Pb free bump qualification for Flip-chip devices</u> : For microcircuit devices containing Pb-free solder bumps with Underfill/Encapsulation. Manufacturer shall document a Lead Free Control Plan (LFCP) in the PIDTP for QA approval. Manufacturer shall perform The following test shall be performed for Pb free bump initial qualification for risk mitigation:	DLA
*6	H.3.4.4.1.2.1, Table – there should be separate requirements for Space (Class Level S) vs Non-Space (Class Level B) per table in ARP6537. This proposal for Pb free bump is intended to apply across flip-chip packages of all classes of MIL-PRF-38535. However, to your point we may have to consider that conditions may vary with respect to temperature constraint of the package technology used, (i.e ceramic vs organic substates, or plastic encapsulated devices). We may need to consider separate columns and or footnotes to assure the requirements in this table address qualification for solder bump alloys in accordance with their appropriate package technology.	13.2 MFG DLA

#	Comments	BY:
<u>*7</u>	Recommend adding a footnote: "Parts with organic substrate containing Pb-free Solder Bumps with Underfill use MIL-STD-883, TM 1010 condition B" This footnote agrees with SAE ARP6537 which calls out the following for thermal cycling test: Group 1A - Parts with ceramic substrate containing Pb-free Solder Bumps with Underfill/Encapsulation - condition C Group 1B Parts with organic substrate containing Pb-free Solder Bumps with Underfill/Encapsulation - condition B	DLA:
<u>*8</u>	If package is ceramic hermetically seal, I don't think HAST should be applied since there is no moisture inside the cavity and enhance this test will not test anything. I agree for a non-hermetically seal package, this test is needed.	13.2 MFG
	HAST is performed for this one-time initial qualification of the Pb-free solder. HAST test will provide inspection for durability of the Pb-free solder joint against whisker growth, cracks, and defects.	DLA
<u>*9</u>	Table H – Thermal Shock – Is this absolutely necessary?	13.2 MFG
	This test is listed in ARP 6537. This test can expose weaknesses at the Ball Grid Array (BGA) level, external to devices. This test will be used here to bound any risk of failure internally for flip chip solder bumps. DLA would like to receive additional justification regarding this test and are reluctant to remove this requirement at this time. Manufacturers may consider test optimization per approval by the DLA qualifying activity, provided the product is still capable of meeting the screening and Technology Conformance Inspection (TCI) testing.	DLA
<u>*10</u>	Table H – Shock & Vibe – TI believes this is not applicable for organic flip chip. Do you agree?	13.2 MFG
	This test is listed in ARP 6537. This test can expose weaknesses at the Ball Grid Array (BGA) level, external to devices. This test will be used here to bound any risk of failure internally for flip chip solder bumps. DLA would like to receive additional justification regarding this test and are reluctant to remove this requirement at this time. Manufacturers may consider test optimization per approval by the DLA qualifying activity, provided the product is still capable of meeting the screening and Technology Conformance Inspection (TCI) testing.	DLA
<u>*11</u>	H.3.4.4.1.2.1, Table – "JESD22-B109" should remove the "B" which is the rev level.	13.2 MFG
	Agree to remove the revision designation.	DLA:

#	Comments	BY:
*12	Table H – Die Attach Bond Strength, Die Shear Strength, Die Pull Off – Which of these do we really need? Can you clarify the difference between them? TI has seen no issues with die attach/shear strength and believe the die will crack if we try to pry the die off the die attach.	13.2 MFG
	These are all one-time qualifications/characterization test. Die Attach Bond Strength - For bond strength testing, the forces at the time of failure and the failure category, or the minimum and maximum readings of the microcircuits if no failures occur. See Test Method 2011 condition F Die Shear Strength - TM 2019 or TM 2027 (after underfill cured) For die shear or stud pull strength testing, the forces at the time of the failure and the failure category, or the die shear or stud pull reading if no separation occurs. Die Pull Off - pull off test shall be performed (before underfill dispense) in accordance with TM 2031 	DLA:

4.1.1 MIL-STD-1580 DPA Procedure

- Decapsulation and part opening

If the package is fully molded then MIL-STD-1580 Requirement 16 for chemical procedures shall be used to decapsulate the part.

If device employs a metal lid with epoxy attach the following process may be used: Place the part lid side down on a hot plate heated to 150C for 45 minutes. Carefully remove the lid by gently prying around all sides of the device. Ensure the tool used to pry off the lid does not extend into the cavity to the extent it may damage internal features. Use caution as this technique may not work for all metal lidded devices.

Post decapsulation or opening, MIL-STD-883 TM 2010 and 2013 shall be performed for internal visual.

- Cross Sectioning

Cross section shall be used to verify any voiding or delamination of the under-fill.

Cross section through at least one row of internal solder bumps shall be performed to examine the intermetallics and check for voids in the bumps.

- **Flip Chip void inspection:** Manufacturer shall perform Acoustic Microscopy inspection on each flip chip device in accordance with the methodology defined within TM 2030 of MIL-STD-883 for flight products or IPC/J-STD-035 for other products. Visual Inspection shall be conducted at low magnification in the range of 30X to 60X. The device may be examined at an angle other than perpendicular to the die surface in order to facilitate the inspection.

Acceptance criteria is defined below:

- Inspection criteria (using Acoustic Microscopy and Visual Inspection)
- 100% inspection on space grade flight hardware; sampling per ANSI/ASQ Z1.4 with AQL = 4.0 for other hardware
- Maximum 1% total allowable voiding/missing underfill material under the entire die area using acoustic microscopy ***13**
- No delamination between the underfill and device surface or substrate allowed, this includes no evidence of either cohesive or adhesive separation ***14**
- Underfill must surround all of the peripheral solder joints (0% voiding on device perimeter) using acoustic microscopy and visual inspection ***15**
- No cracks in underfill fillet; no holes, chip outs, or voids in the underfill material at the die corners using acoustic microscopy and visual inspection ***16**
- No evidence of chip outs, cracks, or damage to the device or substrate, such as those caused by the dispensing process, using acoustic microscopy and visual inspection. ***16**

NOTE: The level of acceptable voiding under flip chip devices is dependent on end use reliability. In some cases, lower percent voiding may be required. Voiding under the device is not recommended in order to meet most reliability requirements. Two adjacent solder bumps that have a connected void may bridge during subsequent thermal processing. If possible, no voids should connect adjacent solder bumps. ***17**

#	Comments	BY:
*13	Regarding "Maximum 1% allowed voiding/missing in underfill...", Our current criteria is 5%. We would need to assess capability to meet 1% requirement.	13.2 MFG
	Pb-free taskgroup has received feedback from other suppliers stating that they are using < 0.5% voiding. Continued discussion may be needed to provide guidance. Also TM 2030 will need to be reviewed for possible updates.	DLA
*14	Regarding "No delamination between the underfill and device surface or substrate allowed, this includes no evidence of either cohesive or adhesive separation" – This can be done in-line, as cannot do it on finished goods. SAM cannot be done as sound waves will not yield valid results when passing through metal lid.	13.2 MFG
*15	Propose to remove line: "Underfill must surround all of the peripheral solder joints (0% voiding on device perimeter) using acoustic microscopy and visual inspection".	13.2 MFG
*16	Further discussion is desired.	13.2 MFG
*17	Most of the suppliers said 0% voiding is achievable. However, equipment limitations could make it difficult to specify 0%. The note at the bottom was created to address that concern. The manufacturers felt that 1% voiding may be too much since a void between bumps allows for a point to point short. It was agreed that this note will make the criteria confusing. Question was asked if a visual image could be added that could resolve this issue and clarify the requirements. DLA mentioned that TM2030 needed to be updated too.	GWG notes
	DLA will take action item to discuss this item with DLA-VQ and possibly reach out to main suppliers to request them to review the study and provide feedback and/or images to make the requirement clearer.	DLA

- **Managing durability risk: *18**

After qualification of the Pb free bump packages the manufacturer shall perform group B and D as production lot tests. Group B test shall be performed on each inspection lot as a condition for lot acceptance for delivery. Group B test shall be performed on each qualified package type and lead finish.

The following test performed in group B (lot acceptance test) and D (package qualification test):

- 1) Group B2: (Mechanical and environmental test)
 - a. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0)
 - b. Flip chip pull off test TM 2031 or TM 2011 2(0)

#	Comments	BY:
*18	ARP6537 document Table #3 list a table detailing lot testing for space applications. These tests are all covered within MIL-PRF-38535 as: • Group B tests (Mechanical and environmental test) • Group D (Package related test) tests of MIL-PRF-38535.	DLA

2) MIL-PRF-38535 Table displaying Group D2/D3/D4 test done (Package related test) ***19**

Subgroups test	Tests 1/	MIL-STD-883 test method and conditions
Subgroup 2 sample size 45(0) 2/ 3/	a. Lead/terminal integrity test b. Seal test 4/ (1) Fine leak (2) Gross leak c. For BGA/CGA packages (i) Ball shear test for BGA package (ii) Solder column pull test for CGA package	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style b. TM 1014 Test condition as applicable c. For BGA/CGA packages (i) For BGA package - JESD22-B117 45(0) (45 balls from 2 devices minimum) (ii) For CGA package - TM 2038 45(0) (45 columns from 2 devices minimum)
Subgroup 3 sample size 15(0) 6/ 7/	a. Thermal shock b. Temperature cycling *20 c. Moisture resistance d. Visual examination e. Seal test 9/ *22 (1) Fine leak (2) Gross leak f. End-point electrical parameters 10/	a. TM 1011 Test condition B, 15 cycles minimum b. TM 1010 Test condition C, *21 100 cycles minimum c. TM 1004 8/ d. In accordance with visual criteria of TM 1004 or TM 1010 e. TM 1014 test condition as applicable f. As specified in the applicable device
Subgroup 4 *23 sample size 15(0) 6/ 7/	a. Mechanical shock b. Vibration, variable frequency c. Constant acceleration 11/ *24 d. Seal test *22 (1) Fine leak (2) Gross leak e. Visual examination f. End-point electrical parameters	a. TM 2002 condition B minimum b. TM 2007 condition A minimum c. TM 2001 Test condition E, Y1 orientation only d. TM 1014 condition as applicable e. In accordance with visual criteria of TM 2007 f. As specified in the applicable device specification

#	Comments	BY:
*19	Regarding Groups D2/D3/D4 package related tests: Comment received that we may need to look at how a 38535 testing for Sn/Pb bump testing compares to these tables. You are checking the mechanical robustness so is there something unique about Pb-free that calls for different or additional testing.	GWG notes
	For Sn/Pb, we are not doing extra quality tests. That is why there are extra tests for Pb-free including DPA to initially qualify.	DLA
	End of the line/screening will leverage off the initial qualification to determine if additional testing is needed based on those results.	
	(GWG/DLA will need to address how this should be documented if this is the case.)	GWG
*20	Regarding D3 Temp Cycle: For Pb-free bumps on organic substrates, need TM1010 Condition B (-55C-125C), not Condition C (-65C-150C), as organic substrates may be overstressed at extreme temps. Could create reliability risk.	13.2 MFG
	Agree The actual Group D tables listed in MIL-PRF-38535 will list columns per class. For example, Temp cycle for class Y (ceramic will apply condition C for 100 cycles min) Temp cycle for class Y (organic will propose alternate condition B for 150 cycles). (also refer to comment *21)	DLA
*21	ARP 6537 calls out the following: Group 1A - Parts with ceramic substrate containing Pb-free Solder Bumps with Underfill/Encapsulation condition C Group 1B Parts with organic substrate containing Pb-free Solder Bumps with Underfill/Encapsulation condition B ~~Group 2 Parts containing Other Pb-free Solder and Finishes Under Encapsulation Condition B~~ Group 2 parts are not considered acceptable for QML devices at this time.	DLA
*22	D3/D4 seal test – Need note to exclude Class Y?	13.2 MFG
	Agree The actual group D tables listed in MIL-PRF-38535 will list columns per class. For example, class Y does not require seal.	DLA
*23	D4 NA for non-hermetic packages.	13.2 MFG
	The actual group D tables listed in MIL-PRF-38535 will list columns per class. For example, class Y does not require seal. Also, constant acceleration is not required for all flip chip devices.	DLA
	All other test listed in Group D subgroup 4 are applicable.	
*24	Since device is flip chip, constant acceleration will not test anything, but only going to damage the package (particularly for LGA package), also, it is not able to test anything in organic flip chip substate.	13.2 MFG
	Agree: constant acceleration is not required for flip chip devices.	DLA

- **For managing secondary risk, MIL-PRF-38535 has the below requirements as a part of PIDTP.**

The following should also be considered when selecting an underfill or encapsulation material. Most of these and other best practices for underfill selection are covered in J-STD-030 and MIL-PRF-38535, Appendix H.

- Coefficient of Thermal Expansion (CTE) Mismatch
- Ability to withstand installation process ***25**
- Ability to withstand temperature and other environmental impacts
- Moisture sensitivity level characterization
- Outgassing and other material requirements, such as MIL-STD-883 TM 5011 and ASTM E595

#	Comments	BY:
*25	For secondary risk, can you please clarify the definition of "installation process"	13.2 MFG
	Installation process is about the assembly and packaging technology certification test as called out in Appendix H of MIL-PRF-38535.	DLA
	Recommend update "Ability to withstand ~~installation~~ assembly process."	