

ENGINEERING PRACTICE (EP) STUDY

**TITLE: EP study of non-hermetic microcircuit class N military, avionics & terrestrial (also suitable for small satellite/space program) applications under MIL-PRF-38535.
(Phase 2)**

Study project number: 5962-2020-002

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FINAL REPORT

**Study Conducted by DLA Land and Maritime
Document Standardization Division (VA)
Active Devices Branch (VAC)**

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EP study of non-hermetic microcircuit class N military, avionics & terrestrial (also suitable for small satellite/space program) applications under MIL-PRF-38535.

1. **OBJECTIVE:** The purpose of this Engineering Practice (EP) Study is to obtain input and justification from the military services, microcircuit manufacturers, and space application user's communities, concerning the update/addition of non-hermetic class N military, avionics & terrestrial (also suitable for small satellite/space program) applications under MIL-PRF-38535.
2. **BACKGROUND:** MIL-PRF-38535 offered non-hermetic class N (plastic package). In table IB, class N has an inclusive table that comprises screening and QCI tests requirement, which called tests/monitors for plastic package. However, this inclusive table fails to distinguish between screening and QCI test flows that creates confusion with periodic QCI test monitoring issue as well as product reliability.

Accordingly, to bring advancement and adopting new package technologies into QML system to MIL-PRF-38535, DLA Land and Maritime-VAC is conducting an EP study (phase 2) which includes:

- (1) Update class N with separating screening and QCI tables to make robust high reliability plastic encapsulated microcircuits (PEM) devices for military, avionics & terrestrial (also suitable for small satellite/space program) applications.

DLA Land and Maritime-VAC is requesting review of the following attachments:

Attachment #1 - Survey questionnaire

Attachment #2 - Overview of proposed class N non hermetic devices flow update under MIL-PRF-38535.

Attachment #3 - Screening and QCI table comparison.

Please send comments/feedback to DLA within the stipulated time for discussion and further development.

3. **RESULTS:** The Ep Study project initial draft posted to DLA Land Maritime website on August 24, 2020 and distributed to military services, microcircuit manufacturers, original equipment manufacturers, and user communities for review and comments. From the feedback received, 44 comments are appended within the original proposal (see attachments #1, #2, and #3). All received comments/responses were compiled and discussed at JEDEC JC-13.2 subcommittee meeting on January 26, 2021.
4. **CONCLUSIONS:** The findings of this EP study were sufficient to support proposing 2 separate PEM classes; class N for military, terrestrial and avionics application, and create a new device class P (PEMs for space). Class P will be coordinated through bi-weekly teleconference meetings of a JEDEC JC 13.2 task group working to develop screening, QCI/TCI, and RH/RT requirements for space applications. Continuous developments for updating PEM devices class N will be revised pending coordination progresses from class P. DLA Land and Maritime-VAC will conduct a new EP study phase 3 proposing updates to class N and class P for review prior to updating MIL-PRF-38535.
 - a. EP study phase 2: The comment compilation appended to the proposed changes of class N screening and QCI tables will aid in future coordination for making robust PEM devices class N (military, terrestrial and avionics application). Review of these comments may also be discussed in coordination efforts for class P (PEMs for Space) task group meetings. Final update to Class N will come after Class P requirements for Screening and QCI test are determined.
 - b. EP study phase 3: Create a new non-hermetic Class P for plastic encapsulated microcircuits (PEM) package technology requirements for space applications. EP study phase three will be used to review a side-by-side proposal of an updated class N and Class P requirements. All received comments will be discussed and coordinated, final comments on this study will be published and may result as changes in the next revision of MIL-PRF-38535.

Attachment # 1

Survey questionnaire

Questionnaire:

1. What are your comments / views concerning the update to class N to make robust high reliability plastic encapsulated microcircuit (PEM) devices for military, avionics & terrestrial (also suitable for small satellite/space program) applications under MIL-PRF-38535? ***1**

#	Comments	BY:
*1	Please remove verbiage regarding Class N being suitable for space applications. A new QML class should be created for non-hermetic space parts. Use in small satellite/space programs must be assessed by the user to determine if it is appropriate for use in users' application.	13.2 MFG

2. Would you support the proposed definition to class N into MIL-PRF-38535?

Current definition of class N

6.4.28 Class N. Items which have been subjected to and passed all applicable requirements of this specification including qualification testing, screening testing, and TCI/QCI inspections, and are encapsulated in plastic. This product must be assessed by the user to determine if it is appropriate for use in users' application.

Proposed definition of 6.4.28 Class N ***2 *3 *4**

A microcircuit employing a non-hermetic plastic package, which meets all applicable requirements of this specification including qualification, screening and TCI/QCI inspections. This product is intended for Military, avionics & terrestrial (also suitable for small satellite/space program) applications.

#	Comments	BY:
*2	<u>Proposed definition of 6.4.28 Class N</u> A microcircuit employing a non-hermetic plastic package, which meets all applicable requirements of this specification including qualification, screening and TCI/QCI inspections. This product is intended for Military, avionics & terrestrial (~~also suitable for small satellite/space program~~) applications.	13.2 MFG
*3	Replace " ~~non-hermetic~~ " and insert "encapsulated plastic or non-encapsulated plastic"	DLA- VQ
	Class N is for encapsulated plastic only.	DLA- VAC
*4	Add the below sentence back into the new definition. "This product must be assessed by the user to determine if it is appropriate for use in users' application. "	DLA- VQ
	Update the proposed definition to the following for review: "A microcircuit employing a non-hermetic plastic package, which meets all applicable requirements of this specification including qualification, screening and TCI/QCI inspections, and are encapsulated in plastic. This product is intended for military, avionics & terrestrial (~~also suitable for small satellite/space program~~) applications. This product must be assessed by the user to determine if it is appropriate for use in users' application."	DLA- VAC

3. Would you support proposing wording for existing class N devices to be given a grandfather approval?

Proposed wording: *5 *6 *7

Note: Existing class N microcircuits with QML certification successfully completed prior to the implementation date of this specification are permitted and shall follow the requirements in MIL-PRF-38535 at the time certification was approved.

#	Comments	BY:
<u>*5</u>	yes	13.2 MFG
<u>*6</u>	Yes, if and only if each device specification drawing indicates that it only meets the Class N requirements of the last 38535 rev that has the old requirements. This way a potential configuration management nightmare can be avoided.	GWG
	Need to discuss further for possibility of distinguishing the product level rev thru the CofC or SMD.	DLA- VAC
<u>*7</u>	Why do we have an optional grandfather allowance, now manufacturers will have two flows? How do we identify parts built to the old requirements versus the new proposed requirements?	DLA-VQ
	All new class N products as of the implementation date of the revised spec will build product to the latest Class N requirements. The grandfather clause allows for those legacy items to remain as is.	DLA- VAC
	This would only involve 2 manufactures one of which only have ASIC products.	

4. There are several existing PEM product assurance standards such as, MIL-PRF-38535, AEC Q100, SAE SSB-1, MSFC-STD-3012, AS6294/1 and AS6294/2 all provide approaches for product assurance of Plastic Encapsulated Microcircuits (PEMs).

In comparison to these standards or other internal manufacturer PEM flows, are there any requirements that should be considered for addition or omission as listed in the proposed updates and tables for Class N QML microcircuits.

Attachment # 2

Overview of proposed class N non hermetic devices flow update under MIL-PRF-38535

- ❖ **Purpose:** Class N devices will be updated. Proposed changes will improve quality, reliability, cost saving and availability as a QML SMD PEM device for military, avionics & terrestrial (also suitable for small satellite/space program) applications.

- ❖ **MIL-PRF-38535 main text need update of the following items:**

1. **Plastic/organic molding compound characterization:** TRB shall review plastic/organic molding compound characterization during device package technology qualification by analysis of flowing items and shall be documented to QM plan for QA review and approval: ***7**

#	Comments	BY:
<u>*7</u>	TRB review is typically associated with Class level S requirement.	DLA-VAC

- a) **Glass Transition (Tg) temperature:** Manufacturer shall review/characterization glass transition temperature (Tg) in accordance with ASTM E1640 during the construction analysis of molding material/compound. Glass transition temperature measurements are recommended prior to Burn-in if usage of low Tg (Tg< 120 °C) molding compound. ***8**

#	Comments	BY:
<u>*8</u>	Tg characterization needs to be performed on samples that have not seen elevated temperature and those that have, since Tg may decrease after exposure to high temp.	GWG

- b) **Coefficient of thermal expansion (CTE).** Manufacturer shall review/characterization coefficient of thermal expansion (CTE) molding material/compound per TM5011 of MIL-STD-883. ***9**

#	Comments	BY:
<u>*9</u>	Class N are encapsulated packages only. There are concerns in regards with molding material variations between lot to lot. Parameters for CTE may still need to be evaluated by users according to mission.	DLA-VAC

- c) **Outgassing:** Manufacturer shall review/characterization of outgassing compound materials in accordance with ASTM E595. ***10**

#	Comments	BY:
<u>*10</u>	This is a one-time characterization test of the molding compound material. This is to benefit the customer. It would help to guarantee the material used to assure that it meets the criteria of the QML temperature range specified.	DLA-VAC

Attachment # 2

Overview of proposed class N non hermetic devices flow update under MIL-PRF-38535

- d) **Moisture sensitivity level (MSL) characterization:** Non-hermetic devices such as class N can exhibit sensitivity to moisture-induced stress and must be handled, packaged, and stored in a proper manner to avoid potential damage during assembly solder reflow attachment and/or repair operations. Moisture sensitivity levels are defined as a rating identifying a component's susceptibility to damage due to absorbed moisture when subjected to reflow soldering. The manufacturer shall be required to define the moisture sensitivity level (MSL) for each non-hermetic device package in accordance with JEDEC J-STD-020 ***11 *12**

#	Comments	BY:
*11	There is the Preconditioning Test on page 6 & 7 of SAE AS6294/2 but that test does not call out on the EP study.	Custodian
*12	Another consideration is the long-term storage of plastics in military depots must strictly be controlled. Plastic packages are highly susceptible to moisture ingress (especially on the larger, thinner packages that are common for more leading-edge products) therefore strict moisture controls (e.g., dry bag, etc.) must be adhered to.	DLA-VQ

2. QML class N audit:

- a) **DLA QA will audit for certification/qualification of class N manufacturers.** Device manufacturers initial site audit shall be performed. No other DLA QA site audit is required unless there is process/design changes or other issue arises. Manufacturers shall perform internal audit of their on-shore/off-shore facilities each year and report shall be submitted to QA for review. ***13 *14 *15**

#	Comments	BY:
*13	The lack of periodic DLA audits for Class N is not recommended, unless Class N is to be considered, as no better than, high risk.	GWG
*14	Propose the following verbiage: "DLA QA will audit for certification/qualification of class N manufacturers. Device manufacturers initial site audit shall be performed. ~~No other DLA QA site audit is required unless there is process/design changes or other issue arises.~~ Manufacturers shall perform internal audit of their on-shore/off-shore facilities each year and report shall be submitted to QA for review. Upon approval from the QA, the frequency of re-audit may be extended." Would we use MIL-PRF-38535 Table A-I to declare what we consider process/design changes and whether to require reaudit or redoing Group C as currently proposed? Change control is not straightforward as well due to commercial fabs are not interested in small volumes which military and space are and always will be. Major and minor changes in the commercial world may be different than what is critical in the military world. Most commercial change notices are restricted to major OEM accounts.	DLA-VQ

Attachment # 2

Overview of proposed class N non hermetic devices flow update under MIL-PRF-38535

#	Comments	BY:
<u>*15</u>	Audits are necessary because a company in the commercial world may source die/wafers from multiple wafer fabs and are usually designed to commercial or industrial temperature range (0 °C to 70 °C temp range or -40 °C to 85 °C industrial). - DLA QA audits should not be limited to initial & design/process changes. Should set reaudit frequency of 3 years and go from there. This would help alleviate the need of tracking what design & process changes would merit a reaudit. If this were to happen as proposed and a company did not inform DLA of a design/process change, this could trigger GIDEP with large impact of industry and negative view of VQ. Allowing VQ to establish audit cycles would leverage our expertise to better judge needed audit frequency. Do not handicap auditors out of the gate. - Does “No other DLA QA site audit is required” mean that No other DLA QA site audit is allowed”? There are countless “process/design changes” including changes to QM plans, locations, procedures, mil spec requirements, operating personnel, new or repaired equipment, training systems and even company ownership. DLA audits are needed to determine the status of “process/design changes” that that should be maintained but may not have been. This includes critical equipment that is broken and not replaced/ repaired or calibrated, procedures and/or training that are not adequately updated to reflect the latest spec requirements etc... It is not at all clear what is meant by “unless... other issues arises” Should we be able to go to investigate the closure of the manufactures audit results? Will we be allowed to audit in order to validate the manufactures audit process for completeness? Would we be allowed a second audit second audit when needed to verify the completion of a DLA initial findings prior to issuing certification? If we cannot, would this be grounds to withhold certification? - Seems like the rule “No other DLA site audit is required unless there is a process/design changes or other issue arises” is a catch 22. The reason we perform regular scheduled audits is because there are often process changes and other “issues arises” that we are either not made aware of and/or cannot fully assess the impact of unless we do a physical site audit. This rule if implemented seems short sighted and does not comprehend the need for site audits to maintain the system.	DLA-VQ

Attachment # 2

Overview of proposed class N non hermetic devices flow update under MIL-PRF-38535

3. Wafer acceptance plan: *16 *17

- a. **QML or Non QML Wafer:** TRB shall be reviewed by wafer die characterization via controlled baseline, reliability and electromigration check, over electrical performance and temperature range test. All wafer die inspection reports shall be documented to QM plan for QA review and approval. Non QML wafer die shall be evaluated and characterization per TM 5007 of MIL-STD-883 as a wafer acceptance test and shall be documented to QM plan for QA approval.

#	Comments	BY:
<u>*16</u>	proposed verbiage ~~QML or Non QML~~ Wafer: TRB shall be reviewed by wafer die characterization via controlled baseline, reliability and electromigration check, over electrical performance and temperature range test. All wafer die inspection reports shall be documented to QM plan for QA review and approval. ~~Non QML~~ wafer die shall be evaluated and characterization per TM 5007 of MIL-STD-883 as a wafer acceptance test and shall be documented to QM plan for QA approval.	DLA-VQ
<u>*17</u>	“QML vs Non QML wafer” was proposed for gathering feedback if the consideration of allowing this would increase interest for more manufacturers into the QML program. This proposal would apply TM 5007 to both QML and non-QML wafers. However, the acceptance of non-QML wafers would be new for MIL-PRF-38535. TM 5007 comes with some concerns for example, how to know if any rework, reprocessing, or repair has been performed. More justification is needed to assure that by allowing non QML Wafer would not jeopardize maintaining essential quality and reliability requirements. Note: Separately from the QML program that DLA currently offers Vendor Item Drawing (VID) program for such devices using non-QML die.	DLA-VAC

4. **100% Screening test shall be performed per class N column of Table I of this EP study:**
 (See attachment #3 Screening and QCI table comparison sections for proposed updates to class N based on comparison to AS6294 /1 and AS6294/2)

Attachment # 2

Overview of proposed class N non hermetic devices flow update under MIL-PRF-38535

5. **QCI test:** Updated class N device will be offered as a QML SMD device with wider device characterization and QCI type test that provide robust quality, reliability, cost saving and availability compared to limited lot acceptance type test.
- a. **Group A :** Electrical test shall be performed for static, dynamic, functional and switching test conditions at room/low/high temperature per MIL-PRF-38535. (sample size 116/0).
 - b. **Group B :** Group B test shall be performed on each inspection lot as a condition for lot acceptance for delivery. Group B test shall be performed on each qualified package type and lead finish. ***18**
 - 1. Resistance to solvent test.
 - 2. Bond strength test.
 - 3. Solderability test.

#	Comments	BY:
*18	Do we need die sheer? May be difficult to do die sheer since mold compound is applied prior to singulation	13.2 MFG
	Considering encapsulation this may be difficult to perform die sheer. This needs further discussion.	DLA-VAC

- c. **Group C life test :** Burn-in life test shall be performed based on device technology and shall be documented to the QM plan for QA review and approval. One time sample from 3 wafers or wafer lot shall be tested unless process and design is changed. Sample size 45/0 for 1000 hours at 125°C or equivalent per TM 1005. ***19 *20 *21**

#	Comments	BY:
*19	Need clarification on what "based on device technology" would mean	13.2 MFG
	Based on device technology refers to whether static or dynamic burn in test. For example, a voltage regulator may only undergo static test and no dynamic (no condition D).	DLA-VAC
*20	proposed verbiage: "One time sample from 3 ~~wafers~~ or wafer lot shall be tested..."	DLA-VQ
	Change control is not straightforward as well due to commercial fabs are not interested in small volumes which military and space are and always will be. Major and minor changes in the commercial world may be different than what is critical in the military world. Most commercial change notices are restricted to major OEM accounts.	
	Manufacturers in the commercial world do not perform 100 % burn-in. Other screens are not 100 % but sample only (e.g., internal visual, external visual, temp cycle etc.) and are usually based on sample sizes based on AQLs. Lead finish is either pure tin (lead free) or at best palladium. In some cases, screens such as burn-in may actually degrade the lead finish such as palladium.	
*21	Group C life test: 1) Do not recommend a one-time life test. 2) Recommend that each diffusion run have a 45(0) life test performed, or performed per the requirements for Class Q/B.	GWG

Attachment # 2

Overview of proposed class N non hermetic devices flow update under MIL-PRF-38535

- d. **Group D:** Package related qualification test for class N shall be performed per table V (as proposed per attachment #3 of this EP Study). In line monitors test shall be performed by package family type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. The in-line monitor data shall be traceable to the specific inspection lot(s) represented (accepted or rejected) by the data. Group D test shall be performed each year unless design and process is changed.
- e. **Group E :** Radiation hardness assurance (RHA) test shall be performed as specified in the devices specification SMD per TM1019/883 on each wafer or wafer lot per MIL-PRF-38535 appendix C table .
*22 *23

#	Comments	BY:
<u>*22</u>	Group E should be removed for class N.	13.2 MFG
<u>*23</u>	RHA: 1) TID per 883/1019 is inadequate. 2) RHA needs to meet all the requirements in 38535, Appendix C, just like RHA for classes V/S, Y, and Q/B should be meeting.	GWG
	Further discussion is needed for capability of PEMs detecting / pass heavy ion test. Appendix C may be more applicable for Class P (space).	DLA VAC
	Group E is required per wafer/wafer lot. Group E does not appear to be per device technology. I think Group C and Group E should line up for Class N. Either only done at qual (or major change), or have it done per wafer lot. Prefer done per wafer lot or annually for high volume production, limit to worst case package configuration. Clarify usage of microcircuit group tables.	DLA VQ

6. **Existing class N devices:** Existing class N devices requirement and manufacturing process will be given as a grandfather approval unless manufacturers are willing to accept new updated requirement.

Attachment # 3 Screening and QCI table comparisons

TABLE I. Screening procedure comparison for class N, class Y, AS6294/1 and AS6294/2 microcircuits. ***24**

Screening Tests	Non-hermetic microcircuit devices test requirements MIL-STD-883, test method (TM) and conditions			
	Class N (high reliability) *25 *26	Class Y (class level S)	AS6294/1 (space)	AS6294/2 (military)
1. Wafer lot acceptance test	TRB QM plan (see MIL-PRF-38535 H.3.2.1.4) *27	QM plan (see MIL-PRF-38535 H.3.2.1.4) 1/ or TM 5007 of MIL-STD-883 (all lots)	----	----
2. Nondestructive bond pull (NDBP) test 2/	NA	TM 2023	----	----
3. Internal visual inspection 3/	TM 2010, condition A *28	TM 2010, condition A	----	----
4. Temperature cycling 4/	TM 1010, condition B, -55 to 125 °C 10 cycles minimum	TM 1010, condition C, 10 cycles minimum	TM 1010 condition B (or to the manufacturer's T _{storage} , whichever is less). Temperature cycles, 20 cycles minimum.	MIL-STD-883, Method 1010, Condition B, -55 to 125 °C Cycles, minimum
5. Constant acceleration 5/	NA	TM 2001, condition E (minimum), Y1 orientation only	----	----
6. Visual inspection 6/	100%	100%	MIL-STD-1580 for PEMS	JESD22-B101
7. Particle Impact Noise Detection (PIND) test 7/ 8/	NA	TM 2020, test condition A on each device	----	----
8. Serialization 9/	In accordance with device specification (100%) *29 *30	In accordance with device specification (100%)	MIL-STD-1580 for PEMS	----
9. Pre burn-in (Interim) electrical parameters test 10/, 11/	In accordance with device specification. Refer to JEP163 12/	In accordance with device specification 12/	-Per device specification, Read and Record Refer to JEP163 -Measure at 25 °C, minimum and maximum rated operational temperatures.	----

#	Comments	BY:
*24	Most commercial parts (PEMS) are only tested/screened at room temperature for electrical test.	DLA-VQ
*25	Class N not for space	13.2 MFG
*26	Class N (high reliability) 1) Referring to Class N as "(high reliability)" is a misnomer. 2) Recommend using the term "enhanced reliability" instead, since high reliability should be reserved for Class V/S/Y.	GWG
*27	remove since suggest to remove reference to usage for space	13.2 MFG

Attachment # 3

Screening and QCI table comparisons

#	Comments	BY:
<u>*28</u>	Condition B	13.2 MFG
	Current Class N this is evaluated in accordance with manufactures internal procedures Agree to evaluate to condition B for Class N. -Will propose condition A (class level S) or we can determine later	DLA- VAC
<u>*29</u>	remove since suggest removing reference to usage for space	13.2 MFG
<u>*30</u>	screen step 8: Recommend moving step 8 up in the table to be performed prior to temp cycling.	GWG

Attachment # 3 Screening and QCI table comparisons

TABLE I. Screening procedure comparison for class N, class Y, AS6294/1 and AS6294/2 microcircuits. - Continued.

Screening Tests	Non-hermetic microcircuit devices test requirements MIL-STD-883, test method (TM) and conditions			
	Class N (high reliability)	Class Y (class level S)	AS6294/1 (space)	AS6294/2 (military)
10. Burn-in test: <u>10/ 13/ 14/</u>	TM 1015 160 hours at 125°C , Refer to JEP 163 *31 (a) static BI condition A or B (b) Dynamic BI Condition D <u>15/</u>	TM 1015 240 hours at 125°C , condition D <u>15/</u>	Static (steady-state) Burn-in (BI) test at 125°C ambient or at max junction temperature 7/ MIL-STD-883, Method 1015 for Class level S Refer to JEP163 Condition A or B Dynamic burn-in test at 125°C ambient or at maximum junction temperature MIL-STD-883, Method 1015 for Class level S Refer to JEP163 Condition D	----
11. Post burn-in (Interim) electrical parameters test <u>10/</u>	In accordance with device specification <u>12/</u>	In accordance with device specification <u>12/</u>	-Per device specification. Read and Record Refer to JEP163 -Measure at 25 °C	----
12. Reverse bias burn-in test (Static burn-in) <u>13/ 14/ 16/</u>	NA	TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum		----
13. Post burn-in (Interim- reverse bias) electrical parameters test <u>10/</u>	NA	In accordance with device specification <u>12/</u>		---

#	Comments	BY:
*31	clarify that this follows BI requirements for Class Q (perform Static OR Dynamic)	13.2 MFG
	For Class Q it is either Static or Dynamic however, JEP163 should be used as a guide to determine which is necessary. We will update this proposal to match the same requirement as class Q.	DLA-VAC
	-updated static BI to include condition A or B (based on AS6294) Test condition A: Steady-state, reverse bias. Test condition B: Steady-state, forward bias.	

Attachment # 3

Screening and QCI table comparisons

TABLE I. Screening procedure comparison for class N, class Y, AS6294/1 and AS6294/2 microcircuits. - Continued.

Screening Tests	Non-hermetic microcircuit devices test requirements MIL-STD-883, test method (TM) and conditions			
	Class N (high reliability)	Class Y (class level S)	AS6294/1 (space)	AS6294/2 (military)
14. Percent defective allowable (PDA) calculation <u>17/</u>	5 percent PDA (all lots) *32	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)	Maximum acceptable PDA. Calculate delta at 25 °C. Refer to JEP163 <5%	*33
15. Final electrical tests <u>18/</u> (see table III) a. Static test : (1) at 25°C (2) Maximum and Minimum operating temperature b. Dynamic or functional test : <u>19/</u> (1) at 25°C (2) Maximum and Minimum operating temperature c. Switching test : (1) at 25°C (2) Maximum and Minimum operated temperature	In accordance with applicable device specification (see group A test)	In accordance with applicable device specification (see group A test)	-Per device specification, Read and Record Refer to JEP163 -Measure at 25 °C, minimum and maximum rated operational temperatures.	Per device specification Measure at 25 °C, min. and max. rated temperatures
16. Seal test <u>20/</u> a. Fine leak b. Gross leak	NA	Not applicable	Not applicable	Not applicable
17. Radiographic (X-ray) and/or C-SAM test <u>21/</u>	X-ray: TM 2012, C-SAM TM 2030 *34 *35	X-ray: TM 2012, Two views; C-SAM TM 2030	MIL-STD-1580 for PEMs Acoustic Microscopy inspection J-STD-020, J-STD-035	-Acoustic Microscopy -All parts -J-STD-035 (method), J-STD-020 acceptance criteria
18. External visual inspection <u>22/ 23/</u>	TM 2009	TM 2009	MIL-STD-1580 for PEMs	JESD22-B101
19. Qualification or quality conformance inspection/TCI test sample selection	NA	<u>24/</u>	----	----
20. Radiation dose rate latch-up test <u>25/</u>	JESD78 *36 *37	TM 1020	MIL-HDBK-814	----

Note: AS6294/1 provides a baseline screening flow to apply in cases where PEMs do not meet required quality levels. AS6294/2 JEP121 provides a methodology to support test optimization and JESD16 defines quality level estimation.

Attachment # 3

Screening and QCI table comparisons

#	Comments	BY:
<u>*32</u>	Change this back to current class N requirement of "1% PDA or manufacturer's QM plan" This also aligns with AS6294/2	DLA-VAC
<u>*33</u>	The Destructive Physical Analysis on page 6 & page 7 of AS6294-2, it's called out for Test Method MIL-STD-1580 but in the EP Study Table I row 14. Percent defective allowable (PDA) calculation on page 8, Column AS6294/2 (military), it's blank.	Custodian
<u>*34</u>	Should not have 100% CSAM or Xray requirement, as this is not for space	13.2 MFG
	Due to these being encapsulated devices X-ray or acoustic microscopy should be used to examine for voids.	DLA-VAC
	TM 2030 may need to be reviewed and updated.	
<u>*35</u>	Recommend requiring both x-ray and CSAM.	GWG
<u>*36</u>	remove since suggest removing reference to usage for space	13.2 MFG
<u>*37</u>	Not clear what the technical justification for specifying JESD78 instead of TM 1020?	GWG
	JESD78 is not for radiation latch up. This was a mistake and will be removed.	DLA-VAC
	JESD78 should apply for Electrical overstress latch up test or IC latch up test.	

Attachment # 3

Screening and QCI table comparisons

TABLE I. Screening procedure comparison for class N, class Y, AS6294/1 and AS6294/2 microcircuits – Continued.

- 1/ Testing per manufacturer's QM plan. See paragraph H.3.2.1.4 of MIL-PRF-38535 or TM 5007 of MIL-STD-883.
- ~~2/~~ (Not applicable to Class N for this EP Study)
- 3/ Unless otherwise specified, at the manufacturer's option for test samples selection of group B, bond strength test (method 5005) may be randomly selected prior to or following internal visual (method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual exam), and unsealed microcircuits awaiting further processing shall be stored in a dry, inert, controller environment until sealed. Test method 2010 applies in full except when method 5004, alternate 1 or alternate 2 (appendix A) is in effect (see 3.3 method 5004 of MIL-STD-883). For gallium arsenide (GaAs) devices only, TM 5013 of MIL-STD-883 should be used. For flip chip devices, internal visual inspection shall be performed in accordance with TM 2010 and C-SAM TM 2030.
- 4/ For devices with solder terminations, Temperature cycling test may be performed without balls and columns upon approval of PIDTP and QM plan.
- 5/ (Not applicable to Class N for this EP Study)
- 6/ At the manufacturer's option, external visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.
- ~~7/~~ (Not applicable to Class N for this EP Study)
- ~~8/~~ (Not applicable to Class N for this EP Study)
- 9/ Class V or class Y (class level S) devices shall be serialized prior to the first recorded electrical measurement in screening. Class N and class Q (class level B) microcircuits shall be serialized if delta calculations or matching characteristics are a requirement of the device specification. Each microcircuit shall be assigned a unique serial number in order to trace the data back to an individual device within the inspection lot which shall, in turn, be traceable to the wafer lot from which the device originated.
- 10/ Interim (pre and post burn-in) electrical testing shall be performed when specified, to remove defective devices prior to further testing or to provide a basis for application of percent defect allowable (PDA) criteria when PDA is specified (Ref. test step 14: PDA calculation, and footnote 17 herein). If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or standard microcircuit drawing (SMD). This test need not include all specified device parameters, but shall include those measurements that are most sensitive to the time and temperature effects of burn-in and the most effective in removing electrically defective devices.
- 11/ When specified in the applicable device specification, 100 percent of the devices shall be tested and the results recorded for those parameters requiring delta calculations.
- 12/ For class V and class Y (class level S) microcircuit devices, delta measurements shall be performed. The specific delta parameters shall be as defined in the applicable device specification. Pre burn-in and post burn-in interim electrical parameters shall be read and recorded when delta measurements have been specified as part of post burn-in electrical measurements, 100 percent of the devices shall be tested and the results shall be recorded for those parameters requiring delta calculations.

Attachment # 3

Screening and QCI table comparisons

TABLE I. Screening procedure for hermetic classes Q, V and non-hermetic class N and Y microcircuits- Continued.

- 13/ Burn-in shall be performed on all QML microcircuits, except as modified in accordance with SMD section 4.2, or above their maximum rated operating temperature (for devices to be delivered as wafer or die, burn-in of packaged samples from the wafer lot shall be performed to a quantity accept level of 10(0)). For microcircuits whose maximum operating temperature is stated in terms of ambient temperature (T_A), table I of TM 1015 of MIL-STD-883 applies. For microcircuits whose maximum operating temperature is stated in terms of case temperature (T_C), and where the ambient temperature would cause T_J to exceed $+175^{\circ}\text{C}$, the ambient operating temperature may be reduced during burn-in from $+125^{\circ}\text{C}$ to a value that will demonstrate a T_J between $+175^{\circ}\text{C}$ and $+200^{\circ}\text{C}$ and T_C equal to or greater than $+125^{\circ}\text{C}$ without changing the test duration. Data supporting this reduction shall be documented in the QM plan and shall be available to the acquiring and qualifying activities upon request.
- 14/ When test condition F of method 1015 for temperature accelerated screening is used for either burn-in or reverse bias burn-in, it shall be used for both. Also, when devices have aluminum/gold metallurgical systems (at either the die pad or package post), the constant acceleration test shall be performed after burn-in and before completion of the final electrical tests (e.g. to allow completion of time limited tests but that sufficient 100 percent electrical testing to verify continuity of all bonds is accomplished subsequent to constant acceleration).
- 15/ Where applicable, dynamic burn-in test shall be performed, and test condition F of method 1015 and temperature accelerated test requirement shall not apply. For class V or class Y (class level S), burn-in test shall be performed in accordance with TM 1015 of MIL-STD-883, on each device for 240 total hours at $+125^{\circ}\text{C}$. For a specific device type, the burn-in duration may be reduced from 240 to 160 hours if three consecutive production lots of identical parts, from three different wafer lots pass percent defective allowable (PDA) requirements after completing 240 hours of burn-in. Sufficient analysis (not necessarily failure analysis) of all failures occurring during the run of the three consecutive burn-in lots shall not reveal a systematic pattern of failure indicating an inherent reliability problem which would require that burn-in be performed for a longer time. The manufacturer's burn-in procedures shall contain corrective action plans, approved by the qualifying activities for dealing with lot failures.
- ~~16/~~ (Not applicable to Class N for this EP Study)
- 17/ The percent defective allowable (PDA) shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in all cases where delta parameters are specified) with the parameters, deltas and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class V or class Y (class level S) the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class level S screening where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or subplot for burn-in shall be used to determine the percent defective for that lot, or subplot and the lot or subplot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA (10 percent) or 2 devices, whichever is greater. This test need not include all specified device parameters, but shall include those measurements that are most sensitive to and effective in removing electrically defective devices (see A.4.6.1.1 and A.4.6.1.2 of MIL-PRF-38535).
- 18/ Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the device specification and shall include the tests of [table III](#), group A, subgroups 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11, unless otherwise specified in the device specification.

Attachment # 3

Screening and QCI table comparisons

TABLE I. Screening procedure for hermetic classes Q, V and non-hermetic class N and Y microcircuits – Continued.

19/ Functional tests shall be conducted at input test conditions as follows: $V_{IH} = V_{IH(min)} + 20$ percent, -0 percent; $V_{IL} = V_{IL(max)} + 0$ percent, -50 percent; as specified in the most similar military detail specification. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.

CAUTION: To avoid test correlation problems, the test system noise (e.g., testers, handlers, etc.) should be verified to assure that $V_{IH(min)}$ and $V_{IL(max)}$ requirements are not violated at the device terminals.

~~20/~~ (Not applicable to Class N for this EP Study)

21/ The radiographic and/or C-SAM screening test may be performed in any sequence after serialization. Only one view is required for flat packages and leadless chip carriers having lead (terminal) metal on four sides. For flip chip technology, only C-SAM inspection is required. C-SAM inspection may be performed in any sequence after underfill cure for flip chip technology. For additional requirements for this test, see appendix B paragraph B.4.1 of MIL-PRF-38535.

22/ External visual inspection shall be performed on the lot any time after radiographic test and prior to shipment, and all shippable samples shall have external visual inspection at least subsequent to qualification or quality conformance inspection testing.

23/ The manufacturer shall inspect the devices 100 percent or on a sample basis using a quantity/accept number of 116(0). If one or more rejects occur in this sample, the manufacturer may double the sample size with no additional failures allowed or inspect the remaining devices 100 percent for the failed criteria and remove the failed devices from the lot. If the double sample also has one or more failures, the manufacturer shall be required to 100 percent inspect the remaining devices in the lot for the failed criteria. Re-inspection magnification shall be no less than that used for the original inspection for the failed criteria.

~~24/~~ (Not applicable to Class N for this EP Study)

25/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible such as SOI, SOS and dielectrically isolated technology devices. If radiation dose rate induced latch-up screen test is required, it may be performed at any screening operation step after seal test, at the manufacturer's option. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test shall be in accordance with the device specification. The PDA for each inspection lot for class V or class Y (class level S) subplot submitted for radiation latch-up test shall be 5 percent or one device, whichever is greater.

Attachment # 3
Screening and QCI table comparisons

TABLE II. Group B tests (Mechanical and environmental test)

Subgroups <u>1/</u>	Group B tests for QML non-hermetic microcircuits (MIL-PRF-38535)			
	Class N	Class Y	AS6294/1 (space)	AS6294/2 (military)
Subgroup 1	Resistance to solvents <u>2/</u> TM 2015 3(0)	Resistance to solvents <u>2/</u> TM 2015 3(0)	----	----
Subgroup 2 <u>6/</u> , <u>7/</u>	a. Bond strength TM 2011 22(0) (1) Thermo compression Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H For flip chip devices: b. Flip chip pull off test (test perform prior to underfill dispense) TM 2031 2(0) c. Die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or 2027 3(0) d. Die shear test or substrate attach strength or stud pull test for passive elements TM 2019 or 2027 3(0)	a. Bond strength TM 2011 22(0) (1) Thermo compression Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H For flip chip devices: b. Flip chip pull off test (test perform prior to underfill dispense) TM 2031 2(0) c. Die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or 2027 3(0) d. Die shear test or substrate attach strength or stud pull test for passive elements TM 2019 or 2027 3(0)	----	----

Attachment # 3 Screening and QCI table comparisons

TABLE II. Group B tests (Mechanical and environmental test). – Continued.

Subgroups <u>1/</u>	Group B tests for QML non-hermetic microcircuits (MIL-PRF-38535)			
	Class N	Class Y	AS6294/1 (space)	AS6294/2 (military)
Subgroup 3 sample size 22(0) (22 leads from 3 devices) <u>8/</u>	Solderability TM 2003 Solder temperature +245°C ±5°C	----	----	----
Subgroup 4 <u>3/</u>	----	----	----	----
Subgroup 5	----	----	----	----
Subgroup 6 Sample size 15(0) <u>13/</u>	----	----	----	----
Subgroup 7 Electrostatic discharge (ESD) sensitivity test <u>14/</u>	TM3015 3(0) or JS-001 or JS-002 *38	TM 3015 3(0)	----	----

Note: The class N update requirement is not applicable for existing class N product. The existing class N product shall meet the requirements of MIL-PRF-38535 revision L or previous revisions.

#	Comments	BY:
*38	ESD testing performed at initial qualification.	13.2 MFG
	Agree: Group B test shall be performed on each inspection lot as a condition for lot acceptance for delivery. Group B test shall be performed on each qualified package type and lead finish.	DLA-VAC

Attachment # 3

Screening and QCI table comparisons

TABLE II. Group B tests (Mechanical and environmental test) – Continued.

1/ Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electrical and provided the rejects are exposed to the full temperature/ time exposure of burn-in. Group B test shall be performed on each inspection lot as a condition for lot acceptance for delivery. Group B test shall be performed on each qualified package type and lead finish.

2/ Resistance to solvents testing required only on devices using inks or paints as a marking medium. For devices with solder terminations, Resistance to solvents test shall be performed with balls/columns.

~~3/~~—(Not applicable to Class N for this EP Study)

~~4/~~—(Not applicable to Class N for this EP Study)

~~5/~~—(Not applicable to Class N for this EP Study)

6/ For flip chip packages, a bump shear test shall be performed in accordance with JEDEC JESD22-B117 to determine the shear strength of solder bumps. For solder termination devices, subgroup 2 test can be performed without balls and columns.

7/ Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in table IA herein or TM 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see TM 2011).

8/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number applies to the number of leads inspected except in no case shall less than 3 (three) devices be used to provide the number of leads required. For BGA/CGA packages, solderability test shall be verified after solder ball or solder column attachment processes per TM 2003. For CGA packages, solder temperature shall be maintained in accordance with table 1 of TM 2003.

~~9/~~—(Not applicable to Class N for this EP Study)

~~10/~~—(Not applicable to Class N for this EP Study)

~~11/~~—(Not applicable to Class N for this EP Study)

~~12/~~—(Not applicable to Class N for this EP Study)

~~13/~~—(Not applicable to Class N for this EP Study)

~~14/~~—(Not applicable to Class N for this EP Study)

Attachment # 3

Screening and QCI table comparisons

TABLE III. Group A (electrical tests). 1/

Subgroups	Tests	Non-hermetic microcircuits devices Minimum sample size quantity (accept no.) <u>2/ 3/ 4/ 5/</u> MIL-STD-883 test method and conditions			
		Class N (High reliability)	Class Y <u>6/</u> (class level S)	AS6294/1 (space)	AS6294/2 (military)
1	Static tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	----	*39 ----
2	Static tests at maximum rated operating temperature				
3	Static tests at minimum rated operating temperature				
4	Dynamic tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	----	----
5	Dynamic tests at maximum rated operating temperature				
6	Dynamic tests at minimum rated operating temperature				
7	Functional tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	----	----
8A	Functional tests at maximum rated operating temperature				
8B	Functional tests at minimum rated operating temperature				
9	Switching tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	----	----
10	Switching tests at maximum rated operating temperature				
11	Switching tests at minimum rated operating temperature				

#	Comments	BY:
*39	According to the Electrical Measurements on page 6 of SAE AS6294-2, it use 77(0) or 100 percent/ 0 sample but in the EP Study Table III on page 15, Column AS6294/2, it's blank.	Custodian

Attachment # 3

Screening and QCI table comparisons

- 1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.
- 2/ At the manufacturer's option, the applicable tests required for group A testing (see 1/ herein) may be conducted individually or combined into sets of tests, subgroups (as defined in table III), or sets of subgroups. However, the manufacturer shall pre-designate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.
- 3/ The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as pre-designated in 2/ herein, shall be 116/0.
- 4/ A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For those lots having a quantity of less than 116 devices, the test shall be imposed on a 100 percent basis with zero failure.
- 5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For device class V or class Y (class level S), if the testing results in a percent defective allowable (PDA) greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.
- 6/ For class V and class Y, group A electrical tests additional requirements see paragraph B.4.3 appendix B of MIL-PRF-38535.

Attachment # 3 Screening and QCI table comparisons

TABLE IV. Group C life tests.

Subgroup	Tests	Non-hermetic microcircuits devices MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		*samples required based on lot size	
		Class N (High reliability) <u>1/</u> <u>2/</u>	Class Y (class level S) <u>1/</u> <u>2/</u>	AS6294/1 (space) *40	AS6294/2 (military)
Subgroup 1	a. Steady-state life test b. End-point electrical parameters	a. TM 1005 45(0) 1000 hours at 125°C b. As specified in the applicable device procurement specification	a. TM 1005 45(0) 1000 hours at 125°C b. As specified in the applicable device procurement specification	High Temperature Operational Life Testing (HTOL), 125°C 5/ MIL-STD-883, Method 1005, Condition D. 2000 hours minimum Electrical measurement (per device specification) Read and Record Measure at 25 °C, minimum and maximum rated temperatures.	Sequential Testing, Highly Accelerated Stress Test (HAST) and Temperature Cycling

#	Comments	BY:
*40	Life test in AS62941/1 is part of LAT. The AS6294/1 requirements shown here have been taken out of context from the 6294/1 LAT requirements, resulting in an inaccurate comparison of Class N shortfalls against 6294/1.	GWG

1/ Life test may be performed on a quantity (accept) criteria of 22(0) for 2000 hours at 125°C or equivalent per TM 1005 to attain 44,000 device hours. For lots greater than 200, actual devices shall be used. For lots less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22 unless acceptable group C data from the same lot of SEC is available for the previous 3 months. The SEC shall have been produced under equivalent conditions as the production lot and as close in time as feasible, but not to exceed a 3-months period.

2/ Group C life tests shall be performed on the initial production lot of actual devices from each wafer lot, in accordance with [table IV herein](#). Group C life tests are not required to be performed on subsequent production lots when all the following conditions are met:

- (a) Subsequent production lots utilize die from the same wafer lot as the initial production lot.
- (b) Wafers or die remaining from the initial production lot are to be stored in dry nitrogen or equivalent controlled storage, and in covered containers.
- (c) No major changes to the assembly processes have occurred since the group C test was performed on the wafer lot.

Note: For ASICs, a sample size of 5 actual devices may be used with the balance being made up of the SEC.

Attachment # 3

Screening and QCI table comparisons

TABLE V. Group D tests (Package related test).

Subgroups test	Tests <u>1/</u>	Non-hermetic microcircuits device MIL-STD-883 test method and conditions		*Samples Required Based on Lot Size	
		Class N (High reliability)	Class Y (class level S)	AS6294/1 (space)	AS6294/2 (military)
Subgroup 1 sample size 15(0) <u>2/</u>	Physical dimensions	TM 2016	TM 2016	*Can be required / recommended test Physical dimensions, weight	
Subgroup 2 sample size 45(0) <u>2/ 3/</u>	a. Lead/terminal integrity b. Seal <u>4/</u> (1) Fine leak (2) Gross leak 1. c. For BGA/CGA packages (i) Ball shear test for BGA package (ii) Solder column pull test for CGA package	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style b. NA c. For BGA/CGA packages (i) For BGA package - JESD22-B117 45(0) (45 balls from 2 devices minimum) (ii) For CGA package - TM 2038 45(0) (45 columns from 2 devices minimum)	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style b. <u>5/</u> c. For BGA/CGA packages (i) For BGA package - JESD22-B117 45(0) (45 balls from 2 devices minimum) (ii) For CGA package - TM 2038 45(0) (45 columns from 2 devices minimum)	*Can be required / recommended test a. Terminal-related characterization Solderability Terminal finishing materials (addressing tin whiskers problems) Mechanical integrity of leads b. NA c. ---	
Subgroup 3 sample size 15(0) <u>6/ 7/</u>	a. Thermal shock b. Temperature cycling c. Moisture resistance d. Visual examination e. Seal <u>9/</u> (1) Fine leak (2) Gross leak f. End-point electrical parameters <u>10/</u>	a. TM 1011 Test condition B, 15 cycles minimum b. TM 1010 Test condition B, 100 cycles minimum c. HAST in accordance with JESD22-A118, condition B d. In accordance with visual criteria of TM 1004 or TM 1010 e. NA f. As specified in the applicable device	a. TM 1011 Test condition B, 15 cycles minimum b. TM 1010 Test condition C, 100 cycles minimum c. HAST in accordance with JESD22-A118, condition B d. In accordance with visual criteria of TM 1004 or TM 1010 e. <u>5/</u> f. As specified in the applicable device	a. --- b. MIL-STD-883, Method 1010, Condition B, -55 °C to 125 °C, 500 Cycles, minimum c. Biased HAST JESD22-A110, with continuous bias. (96 hours, +130 °C, 85% RH). 16(0) *samples required based on lot size d. External Visual Inspection MIL-STD-1580 for PEMs e. --- f.---	a. b. c. Biased HAST JESD22-A110, with continuous bias. (+130 °C, 85% RH) Hours, minimum OR Unbiased HAST JESD22-A118, Condition A (+130 °C, 85% RH) d. --- e. --- f.

Attachment # 3

Screening and QCI table comparisons

TABLE V. Group D tests (Package related test). - Continued.

Subgroups	Test <u>1/</u>	Non-hermetic microcircuits device MIL-STD-883 test method and conditions		*Samples Required Based on Lot Size	
		Class N (High reliability)	Class Y (class level S)	AS6294/1 (space)	AS6294/2 (military)
Subgroup 4 sample size 15(0) <u>6/ 7/</u>	a. Mechanical shock b. Vibration, variable frequency c. Constant acceleration <u>11/</u> d. Seal (1) Fine leak (2) Gross leak e. Visual examination f. End-point electrical parameters	NA	a. TM 2002 condition B minimum b. TM 2007 condition A minimum c. TM 2001 Test condition E, Y1 orientation only d. <u>5/</u> e. In accordance with visual criteria of TM 2007 f. As specified in the applicable device specification	----	----
Subgroup 5 sample size 15(0) <u>2/</u>	a. Salt atmosphere b. Visual examination c. Seal <u>9/</u> (1) Fine leak (2) Gross leak	a. TM 1009 Test condition A minimum b. In accordance with visual criteria of TM 1009 c. NA	a. TM 1009 Test condition A minimum b. In accordance with visual criteria of TM 1009 c. <u>5/</u>	----	----
Subgroup 6 <u>2/ 12/</u>	Internal water vapor test (cavity packages)	NA	<u>5/</u>	----	----
Subgroup 7 sample size 15(0) <u>2/ 13/ 14/</u>	Adhesion of lead finish	Where applicable TM 2025	Where applicable TM 2025	*Can be required / recommended test Mechanical integrity of leads	----

Attachment # 3

Screening and QCI table comparisons

TABLE V. Group D tests (Package related test). - Continued.

Subgroups	Test <u>1/</u>	Non-hermetic microcircuits device MIL-STD-883 test method and conditions		*Samples Required Based on Lot Size	
		Class N (High reliability)	Class Y (class level S)	AS6294/1 (space)	AS6294/2 (military)
Subgroup 8 sample size 5(0) <u>2/</u>	Lid torque <u>15/</u>	NA	Where applicable TM 2024	----	----
Subgroup 9 sample size 3(0) (3 leads minimum) <u>16/</u>	a. Soldering heat b. Seal (1) Fine leak (2) Gross leak c. External Visual examination d. End-point electrical	NA	Where applicable a. TM 2036 b. <u>5/</u> c. TM 2009 d. As specified in the applicable device specification	----	----

Note: The class N update requirement is not applicable for existing class N product. The existing class N product shall meet the requirements of MIL-PRF-38535 revision L or previous revisions.

- 1/ In-line monitor data may be substituted for subgroups D1, D2, D6, D7, and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. The in-line monitor data shall be traceable to the specific inspection lot(s) represented (accepted or rejected) by the data.
- 2/ Electrical reject devices from that same inspection lot may be used for samples. For devices with solder terminations, subgroups 1, 2, 5, 6 (only hermetic devices) and 8 tests shall be performed with balls and columns.
- 3/ The sample size number of 45, C = 0 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test if applicable (see 4/) in order to meet the requirements of subgroup 2. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads, use TM 2028. For leadless chip carrier packages only, use test condition D and a sample size number of 15 (C = 0) based on the number of pads tested taken from 3 devices minimum. For LGA/BGA/CGA packages, TM 2004 does not apply.
- 4/ Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.
- 5/ This test is not applicable for class Y non-hermetic microcircuits devices.
- 6/ Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".

Attachment # 3

Screening and QCI table comparisons

TABLE V. Group D tests (Package related test). - Continued.

- 7/ For devices with solder terminations, subgroups 3 and 4 tests may be performed without balls and columns.
- 8/ Lead bend stress initial conditioning is not required for leadless chip carrier packages or BGA/CGA packages. For fine pitch packages (≤ 25 mil pitch) using a nonconductive tie bar, preconditioning shall be required on 3 devices only prior to the moisture resistance test with no subsequent electrical test required on these 3 devices. The remaining 12 devices from the sample of 15 devices do not require preconditioning but shall be subjected to the required endpoint electrical tests.
- 9/ After completion of the required visual examinations and prior to submittal to TM 1014 seal tests, the devices may have the corrosion by-products removed by using a bristle brush.
- 10/ At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.
- 11/ For flip chip packages Constant acceleration test is not required.
- 12/ Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (e.g., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with 5 additional devices from the same lot. If sample size (accept number) of 5(1) is used to pass the lot, the manufacturer shall evaluate his product to determine the reason for the failure and whether the lot is at risk.
- 13/ The adhesion of lead finish test shall not apply for leadless chip carrier, land grid array (LGA), ball grid array (BGA), and column grid array (CGA) packages.
- 14/ Sample size number 15 leads from 3 devices minimum are based on number of leads with zero failure.
- ~~15/~~-(Not applicable to Class N for this EP Study)
- ~~16/~~-(Not applicable to Class N for this EP Study)

Attachment # 3

Screening and QCI table comparisons

TABLE C-I. Group E (RHA) TCI/QCI test comparison for class N, class Y, AS6294/1 and AS6294/2.

Subgroups	Tests <u>1/</u> <u>2/</u>	Non-hermetic microcircuits device MIL-STD-883 test method and conditions			
		Class N (High reliability)	Class Y (class level S)	AS6294/1 (space)	AS6294/2 (military)
Subgroup 1 <u>3/</u> <u>4/</u>	Neutron irradiation test (Displacement Damage test) a. Qualification test and QCI/TCI test b. Endpoint electrical parameters test	a. TM 1017 at 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/inspection lot <u>5/</u> b. As specified in accordance with device specification	a. TM 1017 at 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/inspection lot <u>5/</u> b. As specified in accordance with device specification	DDD testing shall be performed in accordance with MIL-STD-883 Test Method 1017 *41	----
Subgroup 2 <u>3/</u> <u>7/</u> <u>9/</u> <u>10/</u>	Total ionization dose (TID) a. Qualification test and QCI/TCI test b. Endpoint electrical parameters test	a. TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot <u>8/</u> b. As specified in accordance with device specification	a. TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot <u>8/</u> or 1(0) devices/wafer + 4(0) SEC or test structures/wafer or 5(0) devices/wafer lot + 4(0) SEC or test structures/wafer b. As specified in accordance with device specification c. As specified in accordance with device specification	TID high dose rate and low dose rate TID shall be performed in accordance with Test Method 1019 of MIL-STD-883 and guidance from ASTM 1892 *42	----

#	Comments	BY:
*41	AS6294/1 DDD: AS6294/1 also requires statistical analysis of endpoint electrical parameter test per MIL-HDBK-814.	GWG
	Class N should not require this, maybe consider DDD for class P.	DLA- VAC
*42	AS6294/1 TID: AS6294/1 also requires statistical analysis of endpoint electrical parameter test per MIL-HDBK-814.	GWG

Attachment # 3

Screening and QCI table comparisons

TABLE C-I. Group E (RHA) TCI/QCI test comparison for class N, class Y, AS6294/1 and AS6294/2. –continued.

Subgroups	Tests 1/ 2/	Non-hermetic microcircuits device MIL-STD-883 test method and conditions			
		Class N (High reliability)	Class Y (class level S)	AS6294/1 (space)	AS6294/2 (military)
Subgroup 3 11/	a. Dose rate upset test (Transient irradiation test) b. End point electrical parameters test	*43 ----	a. For Digital TM1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0) devices/wafer lot 6/ b. As specified in accordance with device specification	----	----
Subgroup 4 12/	Radiation dose rate induced latch-up test	*44 ----	TM 1020 As specified in the device specification	----	----
Subgroup 5 13/	Single event effects (SEE) test	ASTM F-1192 or JESD57 4(0) devices or As specified in the device specification	ASTM F-1192 or JESD57 4(0) devices or As specified in the device specification	SEE testing shall be performed in accordance with ASTM F-1192, JESD57, and JESD234	----

Note: The class N update requirement is not applicable for existing class N product. The existing class N product shall meet the requirements of MIL-PRF-38535 revision L or previous revisions.

#	Comments	BY:
*43	Not clear why the same Class Y requirements are not required for Class N?	GWG
	Class N should not require this. This can be reviewed for consideration in Class P for space. Normally these tests are for nuclear environment.	DLA-VAC
*44	Not clear why the same Class Y requirements are not required for Class N?	GWG
	Class N should not require this. This can be reviewed for consideration in Class P for space. Normally these tests are for nuclear environment.	DLA-VAC

- 1/ Group E tests may be performed prior to device screening. Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. End point electrical parameters as specified in accordance with device specification.
- 2/ For devices with solder terminations, group E subgroups test may be performed without balls and columns.
- 3/ The radiation hardness assurance capability level (RHACL)/radiation assurance in the SPEC level is the ratio of the capability level to the specification level of devices fluence. Subgroups shall be invoked when the radiation hardness assurance capability level (RHACL) specification requirements of > 10 are not met. For an example, if RHACL/SPEC ratio is > 10 then this test may not be required, but if the RHACL/SPEC ratio falls within > 1 and ≤ 10 then the subgroup test is required.
- 4/ This test is to be conducted only when specified in the purchase order or contract. Neutron irradiation test (Displacement damage test) is not required for MOS devices unless bipolar elements are included by design.

Attachment # 3

Screening and QCI table comparisons

TABLE C-I. Group E (RHA) TCI/QCI test comparison for class N, class Y, AS6294/1 and AS6294/2. –continued.

- 5/ In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
- 6/ In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
- 7/ Parts used for one subgroup test may not be used for other subgroups, but may be used for higher levels in the same subgroup. For subgroup 2, total dose exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.
- 8/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).
- 9/ Traceability to the specific wafer is required.
- 10/ In accordance with wafer for device types with greater than or equal to 4,000 equivalent transistors/chip selected from the wafer. The manufacturer shall define and document sampling procedures. The test structures shall be randomly selected from the wafer. An X-ray source may be used on test structures at the wafer level provided correlation has been established between the X-ray and the Cobalt-60 source and shall be documented in the QM plan.
- 11/ Radiation dose rate upset (Transient irradiation test) test shall be conducted during qualification on first QCI when specified in purchase order or contract.
- 12/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible such as SOI, SOS and dielectrically isolated technology devices. If radiation dose rate induced latch-up screen test is required, shall be performed screening operation after seal. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test in accordance with the specified device specification. The PDA for each inspection lot for class V or class Y (class level S) devices subplot, screened, shall be 5 percent or one device, whichever is greater.
- 13/ When single event effects (SEE) testing is specified in the purchase order or contract, the SEE test shall be performed during initial qualification and after any design or process change that may affect SEE response. Destructive SEE (SEB and SEGR) testing shall be performed accordance with JEDEC JESD57.