

ENGINEERING PRACTICE STUDY

TITLE: Propose changes for Electrostatic Discharge (ESD) requirements to MIL-PRF-38535

March 01, 2017

STUDY PROJECT 5962-2016-008

FINAL REPORT

**Study Conducted by DLA Land and Maritime
Document Standardization Division (VA)
Active Devices Branch (VAC)**

Prepared by:

**Muhammad Akbar
DLA Land and Maritime -VAC**

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

- I. **OBJECTIVE:** The purpose of this Engineering Practice (EP) Study is to obtain input from the military services, microcircuit manufacturers, and user communities to update ESD requirements in MIL-PRF-38535 documents. Microcircuits may be damaged by electrostatic discharge (ESD) due to a deficiency of proper ESD protection, controlling, handling and training programs in place during the manufacturing process. The ESD test method needs to be updated for high pin count devices and advanced packages for new technology devices, which will lead to change MIL-PRF-38535 documents.
- II. **BACKGROUND:** Advanced microcircuits packaging in smaller footprints with higher pin counts lead to issues of appropriate design for ESD protection circuits, testing method for ESD classification and handling of microcircuits. Microcircuits damage from ESD can cost of time, money and potentially mission risk. Currently, MIL-PRF-38535 states that ESD classification shall be identified based on the human body model (HBM) and test method 3015 of MIL-STD-883 and/or ANSI/ESDA/JEDEC JS-001.

Microcircuit part production, handling, and shipping has changed rapidly and Automatic Handling Equipment (AHE) is being added to safely process these devices. Proper grounding and material requirements of ESD controls in AHEs are very important for prevention of charged device model (CDM) and machine model (MM) type damage to ESD sensitive devices.

MIL-PRF-38535 paragraph A.4.4.2.8, Electrostatic Discharge Sensitivity, states that, "ESD classification shall be done in accordance with TM 3015 of MIL-STD-883 (the testing procedure defined within ANSI/ESDA/JEDEC JS-001.may be used as an alternate with acceptable correlation data)". However, these two documents have differences in their test methods.

- TM3015 states that each device shall be tested using three positive and three negative pulses using each of the pin combinations as shown in the table II in the document. A minimum of 1 second delay shall separate the pulses.
- Wherein, ANSI/ESDA/JEDEC JS-001.states that each sample shall be stressed using one positive and one negative pulse with a minimum of 300 milliseconds between pulses per pin for all pin combinations specified in table 2 of the document.

Recently, manufactures raised an issue for using TM3015 for high count pin devices because testing times increased dramatically which caused repeated stressing of the same path and increasing influence of tester parasitic losses and parasitic charge can lead to false-positive failures.

Considering the above issues DLA Land and Maritime –VAC has launched an EP study to develop appropriate ESD requirements for MIL-PRF-38535 and update test method 3015 of MIL-STD-883.

- III. **RESULTS:** The EP Study project was opened and the initial draft posted on the web and distributed to military services, microcircuit manufacturers, original equipment manufacturers, and user communities on September 07, 2016 for review and comments. All received comments/response (see attachment # 1) were compiled and discussed at the JEDEC joint JC-13/G-12 meeting at San Antonio, Texas, on January 2017. After reviewing all comments, DLA Land and Maritime-VAC prepared a proposal of ESD requirements for MIL-PRF-38535 (see attachment #2) which needed to be discussed at the JEDEC JC-13 ESD task group.
- IV. **CONCLUSIONS:** The findings of this EP study were sufficient to support the required update to the ESD requirements in MIL-PRF-38535. The manufacturing industry voluntarily has adopted automation process and testing CDM as an important risk mitigation factor for microelectronic parts. DLA Land and Maritime-VAC will update all documents per JEDEC JC-13 ESD task group recommendations.

Attachment # 1

Received comments on EP study for Electrostatic Discharge (ESD) requirements to MIL-PRF-38535

Considering three HBM/CDM/MM model, the following questionnaire responses or feedback is required for update MIL-PRF-38535 ESD requirements:

Comments/response	Commentators/organization
1) What is your comment to update ESD requirements to MIL-PRF-38535 paragraphs?	
RESPONSE: MIL-PRF-38535 should align to the ANSI/ESDA/JEDEC document JS-001. Note that JS-001 replaced JEDEC JESD22-A114 for HBM ESD testing in April 2010. ESD classification levels should align with the JEDEC classification. MIL-STD-883, Method 3015 should point to the JS-001 as acceptable alternate without demonstrated correlation, or eliminate 3015 and replace completely with JS-001. Right now ESD testing is buried in the text and in Appendix H. Suggest that ESD testing be added to the qualification tables as required for new products. Note that there is ESDA/JEDEC JTR001-01-12, which is a user guide for ANSI/ESDA/JEDEC JS-001 and provides additional guidance for HBM ESD testing as well as a historical background of the standard in the foreword section. Also, CDM ESD testing per ANSI/ESDA/JEDEC document JS-002 should be added to MIL-PRF-38535 as initial qualification test at same time as HBM ESD testing. Note that JS-002 replaced JEDEC JESD22-C101 for CDM ESD testing in August 2014. Machine Model ESD testing is not required [it is not required for commercial ESD testing – only HBM and CDM ESD testing is required by JESD47]. In general, the industry has not adopted Machine Model ESD testing for two main reasons: (1) the MM test results are highly variable across parts and test setups, and (2) the failure modes (due to similar rise times) are the same as HBM testing so the designers do not gain any new information. JEDEC JEP172 is a JEDEC position paper that discusses discontinuing use of machine model testing. ESD marking identifiers should be matched to lowest classification between HBM and CDM levels (e.g., if HBM is Class 2 [2000-3999V] and CDM is Class C2a [500-749V], then marking should be to 500V level). JEDEC JEP155 gives some background on ESD testing and guidance on recommended design level targets. We are not familiar with the history of 3 zaps vs 1 zap. There appears to be some concerns that multiple zaps on packages with high pin-counts may cause an undue over stress on some paths and as a result, the reported failure voltages may be pessimistic. When the HBM testing was first being done, there were not many pins on the packages. The delay times have been shortened (and this may also go along with the reduction in zap number going to 1), driven by pin count and test times and that the extra delay is not needed.	G-12/JC-13

The MIL-STD-38535 should align with the industry standard JS-001 and JS-002 for HBM and CDM testing respectively. JS-001 in particular specifies optimized pin combinations to reduce HBM test time for large pin count devices which should be of interest to the MIL-STD community to greatly reduce the not-realistic "cumulative zapping". MM has been discontinued as a qualification test from the ESDA, JEDEC, AEC and JEITA, so it should not be specified in the MIL-STD.	JC-13
MIL-PRF-38535 § A.3.4.1.4 -> possibility to use TM3015 and/or JESD22-A114	JC-13
Handling and ESD mitigation requirements for Class 0, i.e. < 250V should be the same whether the ESD sensitivity is below 250V, 124V, or 100V. Therefore, do not recommend definitizing Class 0 levels with letters to account for the 124V & 100V levels.	G-12
Missing Class 2, 3A and 3B per MIL-PRF 38535 paragraph A.3.4.1.4, and Table III of TM3015 of MIL-STD-883. Currently MII-PRF-38535. See attached. We concur with Aerospace responses.	AF-85
• CDM is the most relevant and representative ESD test of ST commercial products environments. • HBM remained relevant for our industry especially when human manipulation is involved in the production flow. • MM test is no longer performed in ST as systematic test except if specific requirement from customers.	JC-13
Updating is necessary to align with other ESD industry standards.	JC-13/ESD/ANSI
Replace JESD22-A114 with ANSI/ESDA/JEDEC JS-001 in the document. A114 is no longer supported by JEDEC.	EOS/ESDA

Comments/response	Commentators/organization
2) What ESD models are using in your IC manufacturing process including design, wafer fabrication process, assembly, testing and packaging process to classify ESD sensitivity? Please explain details.	
<u>RESPONSE:</u> Both HBM and CDM ESD classification testing is performed for each new BAE Systems product during qualification. Currently, we use T3015 for HBM testing and JS-002 for CDM testing.	G-12/JC-13
S-001 and JS-002 for HBM and CDM testing	JC-13
We use TM 3015 and/or JESD22-A114A and/or ESCC No. 23800, depending customer requirements and/or quality level objectives and/or package types Military –TM3015-HBM Space-TM3015/ESCC23800-HBM CDM/HBM use in automotive parts	JC-13
This is not applicable for Aerospace since we do not fabricate wafers.	G-12
ESD Model used for: o Qualification/design/ Wafer Fab process are : ▪ HBM : ANSI/ESDA/JEDEC JS-001-2014. ▪ MM: ANSI/ESD STM5.2-2012 (used even if not mandatory). ▪ CDM : JESD22-C101F. o Assy, Test & Packaging: HBM & CDM models are used.	JC-13
IC manufacturing not performed at my facility.	JC-13/ESD/ANSI

Comments/response	Commentators/organization
3) Currently, MIL-PRF-38535 is required for classification of ESD based on HBM (see MIL-PRF-38535 paragraph A.3.4.1.4). What is your comment regarding incorporate other ESD model Charge device model (CDM) and Machine model (MM) requirement for ESD classification to MIL-PRF-38535?	
<u>RESPONSE:</u> I would like to see CDM classifications done on a routine basis by chip manufactures and reported in the data sheets. There is no need for MM testing or classification. See question 1 above for recommendations on classifications.	G-12/JC-13
Agree to add CDM but MM has been discontinued and should not be added.	JC-13
1) Ok if it is not a requirement ! 2) Ok if it is only suggested for initial qualification 3) Ok if that do not impact periodical QCI	JC-13
Classification for ESD should be based on the worst-case model, i.e. the model that results in the lowest ESD voltage sensitivity. should also include at least the CDM which is also proving very sensitive for new technology devices	G-12

• CDM can be incorporated as it is the most representative ESD model. • MM is not relevant in ST commercial products environment. • MM is used for automotive industry where automation is well deployed in manufacturing.	JC-13
CDM needs to be added. Most ESD failures that occur today are either CDM, CBE (Charged Board Event), or CDE (Cable Discharge Event). Additionally, ANSI/ESD S20.20-2014 has explicitly added 200 volts CDM for a limit to the ESD control program. Machine Model needs to be dropped, in my opinion.	JC-13/ESD/ANSI
The industry has concluded that machine model (MM) is not an appropriate stress for qualifying devices for ESD.	EOS/ESDA

Comments/response	Commentators/organization
4) Currently ESD marking and classification on microcircuits device are based on HBM model, If CDM and MM are incorporated how these 2 models will be implemented? it should be just information purposes in the devices specification?	
<u>RESPONSE:</u> As stated above CDM would be an additional set of classification. It should be reported in the datasheets and stamped on the part (or shipping container) when possible. This should be carried over to MIL-HDBK-103 and/or QML-38535.	G-12/JC-13
Suggest the CDM level could be added to the DLA website cross reference and not included on marking.	JC-13
with package integration, there is less and less available place on devices to mark all needed or required information. ESD HBM indicator is enough ! Other models, if useful and tested, could be given in SMD.	JC-13
The model used to determine the class should be specified in the QML listing and represent the worst-case.	G-12
• In ST rules both CDM & HBM are conducted. - o For HBM we can adapt to what is already mentioned in MIL-PRF-38535 as below table, and target CLASS 1C as requirement: • For CDM we can adapt to what is already mentioned in MIL-STD-1686 as below table, and target CLASS C3 as requirement:	JC-13
Missing Class 2, 3A and 3B per MIL-PRF 38535 paragraph A.3.4.1.4, and Table III of TM3015 of MIL-STD-883. Currently MII-PRF-38535. See attached. We concur with Aerospace responses.	AF-85
Marking of the individual parts is not important as long as the packaging identifies the sensitivities accurately. Current packaging does not provide this information. Both HBM and CDM sensitivity would be good to know. Device specifications (datasheets) rarely provide HBM and CDM information. Another issue is that currently under MIL-STD-883 and MIL-STD-750-1, withstand voltages are not required for Class 0 components. JS-001 & JS-002 both require the determination of the withstand voltage (highest passing voltage).	JC-13/ESD/ANSI

Comments/response	Commentators/organization
5) Should the MIL standards be expanded to include charge device model (CDM) and Machine model (MM) testing method?	
<u>RESPONSE</u> : There is value in having CDM measured and reported. Industry data shows that the majority of ESD failures are due to CDM related issues as most manufacturers have good controls in place for HBM events. MM testing is not required and controls are covered by existing procedures.	G-12/JC-13
Point to JS-002 for CDM testing rather than try to write it into the MIL std. MM should not be added.	JC-13
1) see 3 2) ok if test methods can be standardized	JC-13
yes	G-12
We recommend to include CDM method only. We refer to JEDEC JESD22-A115 (page 4) for argument to avoid MM testing method as part of the requirement. • JESD22-A115 is a reference document; it is not a requirement per JESD47 (Stress Test Driven Qualification of Integrated Circuits). • Machine Model as described in JESD22-A115 should not be used as a requirement for integrated circuit ESD qualification. • Only HBM and CDM are the necessary ESD qualification test methods as specified in JESD47.	JC-13
Yes to CDM and no to MM.	JC-13/ESD/ANSI
The MM stress may find failures, but these failures are not unique to MM stress and should be generated by either HBM and/or CDM.	EOS/ESDA

Recently, manufactures are raised an issue for using TM3015 for high count pin devices wherein products can cause severe problems because of testing times increase dramatically which caused repeatedly stressing the same path and the increasing influence of tester parasitic losses and parasitic charge can lead to false-positive failures. MIL-PRF-38535 paragraph A.4.4.2.8, Electrostatic Discharge Sensitivity, states that, "ESD classification shall be done in accordance with TM 3015 of MIL-STD-883 (the testing procedure defined within JESD22-A114 may be used as an alternate with acceptable correlation data)". However, the two documents have differences in their test methods.

- TM3015 states that each device shall be tested using **three positive and three negative pulses** minimum of 1 second delay shall separate the pulses.
- Whereas, JESD22-A114 states that each sample shall be stressed using **one positive and one negative** pulse with a minimum of 300 milliseconds.

Comments/response	Commentators/organization
6) What is your comment to use TM3015 and/or JESD22-A114 for microcircuits devices with high count pin for ESD sensitivity characterization/classification?	
<u>RESPONSE</u> : JS-001 [replaces JESD22-A114 as noted above] outlines a methodology of testing parts with high pin counts in groups of cloned device/circuit types. TM 3015 has not kept up with design complexity changes; JS-001 is a joint standard approved by ANSI, ESDA, and JEDEC. Commercial manufacturers use JS-001 testing.	G-12/JC-13
Same as 1. above JS-001 in particular specifies optimized pin combinations to reduce HBM test time for large pin count devices which should be of interest to the MIL-STD community to greatly reduce the not-realistic "cumulative zapping".	JC-13
With modern high count devices, we observe that cumulative stress combinations in accordance with TM3015 can damage devices and distort the ESD level result. The use of JESD22-A114 is less restricting.	JC-13
Use TM3015, since it represents a worst case scenario. Classification of a part's ESD sensitivity should insure that it is not damaged by voltages below the specified test voltage. use TM3015 unless the manufacturer can show the two methods produce the same results	G-12

For the simplification of testing configuration suggested by JESD22-A114: - Each IC supplier should be held responsible to verify each possible ESD path of a device. Depending on the confidence level and the design knowledge of the device, different approach can be used in order to achieve the goal. - In JESD22-A114, the simplify configuration is an alternative for verification when false failure is suspected due to accumulative effect. For the number of zap requirement: - JS-001-2014 which is the replacement of JESD22-A114, stated that each pins should be zapped at least 1 positive and 1 negative pulse, it does not forbid to have 3 zaps. - The argument to have 1 zap on each pin, is because we believe the probability for any pin to see 2 ESD pulses in its whole device lifetime is very low, and keeping 1 zap is also to avoid any possible false failure due to accumulative effect. But if there is any special circumstances, it is up to the IC supplier to make their best choice. For the duration between each zap: - The IC supplier is responsible that pins are properly grounded after each zap, to avoid false failure due to accumulative effect on the subsequent pin. The duration is suggested by the standard, but it is up to IC supplier to determine what the needed grounding duration according to their machine is.	JC-13
--	--------------

Comments/response	Commentators/organization
7) Should DLA need to update MIL-PRF-38535 paragraph A.4.4.2.8 for use JESD22-A114 as an alternate with acceptable correlation data requirements?	
<u>RESPONSE:</u> TM 3015 should point to the JS-001 as acceptable alternate without a need for demonstrated correlation, or eliminate TM 3015 and replace completely with JS-001. Additional, this paragraph should add requirement for CDM ESD testing and controls.	G-12/JC-13
JESD22-A114 has been Superseded by ANSI/ESDA/JEDEC JS-001	JC-13
Isn't it already the case ? (The testing procedure defined within JESD22-A114 may be used as an alternate with acceptable correlation data.)	JC-13
Not at this time. If suitable test data can be provided that illustrates that JESD22-A114 is acceptable, then it may be considered as an alternate method with ACCEPTABLE correlation data.	G-12
Yes, and please refer to ANSI/ESDA/JEDEC JS-001-2014 .	JC-13
Probably. This standard is an ANSI approved joint standard by JEDEC and the ESD Association and should be considered acceptable.	JC-13/ESD/ANSI

Comments/response	Commentators/organization
8) Do we want a standard or test method for reducing the number of pin combinations required for testing?	
<u>RESPONSE</u> : Yes, the approach in JS-001 seems reasonable.	G-12/JC-13
Use ANSI/ESDA/JEDEC JS-001	JC-13
Yes ! we would want a new method including : - 3 devices ok to determine the ESD level with for example following method : 1) stress 3 devices respectively at 500V, 1000V, 2000V; 2) Electrical test of the 3 devices 3) Confirm the first lower good result with 2 devices stressed at same level - This method allows us to reduce : a) Scrapped devices : 5 vs 9 ! b) Test costs - Possibility to use 1 or 2 representatives pins for each group , example: 1) for Gnd or power group when all pins are connected in the package or in the die 2) for I/O when all lines are identicals (design = same length, same thickness .. often the case in ADC or DAC devices) - This possibility allows us to reduce : a) Stress cumulative effects b) Test costs (equipments charge / stress combination qty)	JC-13
Yes. However, the standard/method needs to definitize the criteria for reduction of pins to be tested.	G-12
No because it's more time consuming to analyze pin combinations and to save test on few pins rather than to test each pin. ST is performing test on each pins.	JC-13

Comments/response	Commentators/organization
9) Would statistical pin testing be a good approach?	
<u>RESPONSE</u> : Yes, the approach in JS-001 seems reasonable.	G-12/JC-13
Same as 8 above/ Use ANSI/ESDA/JEDEC JS-001	JC-13
Not in of itself. The various circuit elements that are stressed as a function of each device pin also needs to be assessed.	G-12
ST is performing test on each pins. On the statistical pin testing approach, ST would need more details.	JC-13

Comments/response	Commentators/organization
10) How do the new 2.5D and 3D configurations affect ESD testing?	
<u>RESPONSE</u> : Good question. There are papers that deal with the layout and marriage of the die to the interposer. I have not looked into if the test set ups were altered. Our current approach is to perform ESD testing (HBM and CDM) using the final package pinout configuration.	G-12/JC-13/
CDM testing can only be performed if the device "package" is planar in the dead-bug (upside down) configuration. Otherwise, CDM cannot be performed.	JC-13
These configurations can cause complications for ESD testing due to the magnitude and duration of propagated pulses to chips that do not interface with the device pins directly during ESD testing. May want to consider exposing each chip in the device to separate ESD testing. since each configuration use with 2.5D/3D structures is different, then ESD testing will be required to be evaluated for each device	G-12
No such Package Technology used in ST Space Products yet.	JC-13

ESD protection, control, handling and training programs are very important key points to mitigate ESD damage at the design, wafer fab, AHEs, packaging and handing level. Recent audits and NASA/JPL EEE parts bulletin (January–July, 2016 • Volume 8, Issue 1) revealed that microcircuits product manufacturers need to establish well management ESD control program at the component level. i.e. die design, wafer fabrication, wafer bumping, package design, assembly, column attached process, testing and screening, radiation testing, transport by franchise distributor, board level test and verification, and final box level assembly. MIL-PRF-38535 paragraph 3.12 ESD control: require "QML microcircuits shall be handled in accordance with JESD625 or other industry standard practices, to safeguard against discharge damage."

Comments/response	Commentators/organization
11) JESD625 is a requirements documents for handling ESD sensitivity devices and has an extensive ESD protection and control requirements other than ANSI ESD20.20. Should MIL-PRF-38535 be updated as required documents JESD625 for ESD handling and control program?	
<u>RESPONSE</u> : I believe that there is effort to merge JESD625 with ANSI S20.20 so that there is one industry standard. My understanding is that these two standards are similar with only difference being that JESD625 gives more guidance. MIL-PRF-38535 should reference both of these until they get merged.	G-12/JC-13
Recommend ANSI/ESD S20.20 instead.	JC-13
OK to integrate the content of the JESD625-A in the MIL-PRF-38535. e2v comment: in page 9 of the JESD625-A (December 1999) paragraph 6.1 "Minimum requirements" the requirement 4 precises some controls with a quarterly frequency -> e2v suggests to have a semi-annually frequency.	JC-13

This should be considered after a detailed study identifies the differences between these two requirements docs and whether JESD625 needs to be incorporated. Recommend taking this up at JEDEC so a task group can address this. I agree that a comparison of the 2 documents be performed and then determine which document has the most stringent requirements and incorporate or change one of the documents and impose it	G-12
Yes it should. ANSI/ESD S20.20-2014 is used in manufacturing ST Assembly and Test sites.	JC-13
Yes. Either JESD625 or ANSI/ESD S20.20. Some suppliers work to JESD625 and some work to ANSI/ESD S20.20. At the ESD Symposium, earlier this month, I participated in a meeting with the goal of harmonizing these two standards.	JC-13/ESD/ANSI
Don't recommend a comparison to JESD625 and ANSI/ESD S20.20 in "11)". It is true that JEDEC has some sections where the requirements are more stringent than S20.20, but it is less stringent in other areas. Would eliminate (or re-write) the first sentence in "11)".	ESD/ESDA

Comments/response	Commentators/organization
12) JESD625 section 11 stated "Recommended ESD audit checklist" which is comprising 33 check points. What is your comment to implement these 33 points' checklist ESD program for each component level of ICs manufacturing steps?	
<u>RESPONSE:</u> The ESD audit checklist in JESD625 is recommended but not required. Most of the checklist items are good but internally we have our own checklist that is more detailed as I would assume most manufacturers do. I would not make this checklist a requirement in MIL-PRF-38535. I believe that self-audit paragraphs A.4.9.3.7 and A.4.9.3.8 cover the requirement adequately; with the checklist details left to the manufacturer.	G-12/JC-13
Recommend ANSI/ESD S20.20 instead.	JC-13
The JESD625 audit checklist can be used as a guideline but not in a requirement. It's difficult to implement the checklist in all manufacturing steps every year.	JC-13
JESD625 checklist is a good start and some of the items included in the checklist are not included anywhere else. The task of reviewing the checklist should be done either by DLA with inputs from JEDEC and G-12 or by a G-12/JEDEC task group	G-12
Most of the points is already part of the control performed in ST. ST Space Assembly and Test is using and referring to: • IEC61340-Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements. • IEC61340-Part 5-2: Protection of electronic devices from electrostatic phenomena – User guide.	JC-13
No comment. Not involved in the IC manufacturing process	JC-13/ESD/ANSI

Attachment # 2

DLA Land and Maritime- VAC proposed following ESD requirements need to update/change into MIL-PRF-38535 based on EP study received comments.

3.6.7.2 Electrostatic discharge (ESD) sensitivity identifier. Individual microcircuit ESD classification marking is ~~optional~~ **not required**. The manufacturer shall have an option of no ESD marking, marking a single ESD triangle or marking in accordance with the ESD device classification defined in test method TM 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 for human body model (HBM) or ANSI/ESDA/JEDEC JS-002 for charge device model (CDM). Because it may no longer be possible to determine the ESD classification from the part marking, the device discharge sensitivity classification shall have to be obtained through MIL-HDBK-103 or QML-38535. **If manufacturer is using the CDM ESD classification, it shall be reported in the device specification or standard microcircuits drawings(SMD).**

3.6.9 Marking on container. All of the markings specified in 3.6, except the index point, shall appear on the die container/package (e.g., waffle pack, etc.), carrier, unit pack (e.g., individual foil bag), unit container, or multiple carriers (e.g., tubes, rails, magazines) for delivery. For ESD sensitive devices, an industry standard symbol used to identify ESD sensitivity **based on CDM and HBM classification**, (e.g., JESD471 symbol) shall be marked on the carrier or container. However, if all the marking specified above is clearly visible on the devices and legible through the unit carrier or multiple carriers, or both, then the ESD marking only (MIL-STD-1285) shall be required on the multiple carriers. These requirements apply to the original or repackaged QML microcircuits by the manufacturer or distributor.

3.12 ESD control. ESD protection, control, grounding procedures and training programs are very important key points to mitigate ESD damage at the design, wafer fabrication, automatic handling equipment's, assembly, testing, packaging and handing level. QML microcircuits manufacturers/suppliers shall establish an ESD mitigation program to safeguard against discharge damage at all steps in accordance with JESD625 or ANSI/ESD S20.20 ~~other industry standard practices.~~

4.2.3 Electrostatic discharge (ESD) sensitivity. ESD sensitivity testing shall be **performed** ~~done~~ in accordance with TM 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 for human body model (HBM) and/or ANSI/ESDA/JEDEC JS-002 for charge device model (CDM) for product initial qualification or product redesign as a minimum. ~~and the device specification. The testing procedure defined within JESD22-A114 may be used as an option in lieu of TM 3015 provided the manufacturer is able to demonstrate correlation between the two methods.~~ In addition, the reported sensitivity classification levels shall be the ones defined in HBM model in accordance with ~~within~~ TM 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 (see 3.6.7.2). ~~In addition, unless otherwise specified, tests shall be performed for initial qualification and product redesign as a minimum.~~

Definition:

6.4.xx Electrostatic Discharge (ESD): The transfer of electrostatic charge between bodies or surfaces that are at different electrostatic potentials. Electronics industry has three most common ESD Models (1) Human body model (HBM), (2) Charge device model (CDM) and (3) Machine model (MM) are used for classification of ESD and protection of failure analysis.

6.4.xx Human Body Model (HBM): A source of ESD damage is the charged human body, as modeled by HBM standards. The human body model is the oldest and well known ESD model using for characterization of ESD

6.4.xxx Charged Device Model (CDM): A source of damage for the CDM is the rapid discharge of energy from a charged device. CDM is increasingly important reliability issue in the semiconductor industry due to automation in IC's process flow.

6.4.18 Electrostatic discharge (ESD) sensitivity . ESD sensitivity is defined as the level of susceptibility of a device to damage by static electricity. The level of susceptibility of a device is found by ESD classification testing and is used as the basis for assigning an ESD class.

ESD references:

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD471 - Symbol & Label for Electrostatic Sensitive Devices.

JESD541 - Packaging Material Standards for ESD Sensitive Items.

~~JESD22-A114 – Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).~~

ANSI/ESDA/JEDEC JS-001: Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).

ANSI/ESDA/JEDEC JS-002: Electrostatic Discharge (ESD) Sensitivity Testing Charge Device Model (CDM).

JESD625 - Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices.

~~A.3.1.3.27 Electrostatic discharge (ESD) sensitivity. Electrostatic discharge sensitivity is defined as the level of susceptibility of a device to damage by static electricity. The level of susceptibility of a device is found by ESD classification testing and is used as the basis for assigning an ESD class (see A.3.4.1.4).~~

A.3.4.1.4 Qualification to ESD classes. Initial qualification to an ESD class, or requalification after redesign, shall consist of qualification to the appropriate quality and reliability level (class level S or B) plus ESD classification in accordance with test method 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 for human body model (HBM) and/or ANSI/ESDA/JEDEC JS-002 for charge device model (CDM). ~~The test procedure defined within JESD22-A114 (see A.4.4.2.8) may optionally be used provided the manufacturer is able to demonstrate correlation with test method 3015 of MIL-STD-883.~~ However, the device shall be marked based on HBM ESD classification designator only. The ESD classification levels defined below shall be reported.

(a) ESD classification levels are defined based on Human body model(HBM) as follows:

Current ESD classification designator (see note)	Optional individual device marking	Devices package/ container marking	ESD voltage (V)
0	$\Delta 0$	$\Delta 0$	< 250
1A	ΔA	ΔA	250 to < 500
1B	ΔB	ΔB	500 to < 1000
1C	ΔC	ΔC	1000 to < 2000
2	$\Delta \Delta$	$\Delta \Delta$	2000 to < 4000
3A	$\Delta \Delta \Delta A$	$\Delta \Delta \Delta A$	4000 to < 8000
3B	$\Delta \Delta \Delta B$	$\Delta \Delta \Delta B$	≥ 8000

(b) ESD classification levels are defined based on Charge device model (CDM) as follows:

CDM ESD classification level (see note f)	CDM ESD classification test condition (V) (see note g)
C0A	< 125
C0B	125 to < 250
C1	250 to < 500
C2A	500 to < 750
C2B	750 to < 1000
C3	≥ 1000 (see note h)

NOTE: ESD class designator 1 has been replaced with designators 0, 1A, 1B, and 1C as of 15 March 2006. The manufacturer shall test and may mark the tested level obtained under "Optional individual part marking" and the optional individual part marking may be used as the pin one identifier. Also, ESD class designator 3 has been replaced by 3A and 3B ESD class designators. ESD class designation 3 may continue to be used for devices tested before 15 March 2006. After 15 March 2006, for newly developed products, the 3A and 3B designators shall be used. Prior designation category devices previously classed by test as category A may be marked as class 1 (Δ) and devices previously classified as category B may be marked as class 2 ($\Delta\Delta$).

- a. Devices existing prior to 30 September 1989 that were not ESD classification tested shall be marked as class 1 until classified. Devices previously classified by test as category A shall be marked class 1. Devices previously classified by test as category B shall be marked as class 2. If it can be shown that test results obtained using TM 3015.3 of MIL-STD-883 correlate with results using TM 3015.6 of MIL-STD-883 (or later versions) or ANSI/ESDA/JEDEC JS-001 JESD22-A114 (see A.4.4.2.8) and give correct ESD classification, retesting of previously tested devices is not required except where redesign has occurred.
- b. Beginning no later than 31 December 1988 but prior to 15 March 2006, all newly designed or redesigned device types shall have been classified as ESD class 1, 2, or 3 in accordance with TM 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 JESD22-A114 (see A.4.4.2.8). After 15 March, 2006 the device types shall be classified as above.
- c. After 30 September 1989, in order to be compliant with this appendix or 1.2.1 of MIL-STD-883, all other device types for use in new system or equipment designs or system or equipment redesigns shall have completed classification in accordance with test method 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 JESD22-A114 (see A.4.4.2.8). All devices of existing design (e.g., not subject to A.3.4.1.4b above) shall be marked class 1 except when known by test to be, in fact, class 2 or better, in which case they shall be correctly identified for ESD.
- d. Although little variation due to case outline is expected, if a device type is available in more than one package type or case outline, ESD testing and classification shall be applied to at least that one package type shown by experience to be worst case for ESD.
- e. ESD testing classification results (or class one marking assigned without test) shall be submitted to DLA Land and Maritime-VA for all SMD devices built in compliance to this appendix. ESD testing classification results for non-SMD devices built in compliance to this appendix shall be retained by the manufacturer and made available to the acquiring or preparing activity upon request.
- f. Use the "C" prefix to indicate a CDM classification level.
- g. The classification test condition is not equivalent to the actual set voltage of the tester. Please see section 6.5.1 and Annex G of ANSI/ESDA/JEDEC JS-002 for charge device model (CDM) for further details.
- h. For CDM test Conditions above 1,000 volts, depending on geometry of the device package, corona effects may limit the actual pre-discharge voltage and discharge current.

[FYI NOTE: Some paragraphs text in Appendix A is duplicate with some text in main paragraphs for adopting old legacy 883 part requirement to meet appendix A of MIL-PRF-38535]

A.3.6.9.2 Electrostatic discharge (ESD) sensitivity identifier. Microcircuits shall be ESD classified in accordance with A.3.4.1.4, however, ESD classification marking is optional ~~not required~~. The manufacturer shall have an option of no ESD marking, marking a single ESD triangle or marking in accordance with the ESD device classification defined in test method 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 for human body model (HBM) and/or ANSI/ESDA/JEDEC JS-002 for charge device model (CDM). Because it may no longer be possible to determine the ESD classification from the part marking, the device Discharge Sensitivity Classification shall be as listed in MIL-HDBK-103 or QML-38535. If manufacturer is using the CDM ESD classification, it shall be reported in the device specification or standard microcircuits drawings(SMD).

A.4.4.2.8 Electrostatic discharge (ESD) sensitivity. ESD sensitivity testing shall be performed ~~done~~ in accordance with TM 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 for human body model (HBM) and/or ANSI/ESDA/JEDEC JS-002 for charge device model (CDM) for product initial qualification or product redesign as a minimum. ~~and the device specification. The testing procedure defined within JESD22-A114 may be used as an option in lieu of TM 3015 provided the manufacturer is able to demonstrate correlation between the two methods.~~ In addition, the reported sensitivity classification levels shall be the ones defined in HBM model in accordance with ~~within~~ TM 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 (see 3.6.7.2). ~~Devices shall be handled in accordance with the manufacturer's in-house control documentation, which shall be maintained by the manufacturer. Guidance for device handling is available in JESD625.~~

A.4.8.1.1.14 ESD handling control program. ESD protection, control, grounding procedures and training programs are very important key points to mitigate ESD damage at the design, wafer fabrication, automatic handling equipment's, assembly, testing, packaging and handling level. QML microcircuits manufacturers/suppliers shall establish an ESD mitigation program to safeguard against discharge damage at all steps in accordance with JESD625 or ANSI/ESD S20.20

~~The ESD handling control program documentation shall be under document control. This includes methods, equipment and materials, training, packaging, handling, and procedures for handling ESD sensitive devices.~~

A.5.2.2 Marking of container. All of the markings specified in A.3.6, except the index point and serialization, shall appear on the carrier, unit pack (e.g., individual foil bag), unit container, or multiple carriers (e.g., tubes, rails, magazines) for delivery. An industry standard symbol for identifying ESD sensitive ~~based on the CDM and HBM classification items~~ (e.g., JESD471 symbol) shall be marked on the carrier or container. However, if all the marking specified above is clearly visible on the devices and legible through the unit carrier or multiple carriers, or both, then the ESD marking only (in accordance with MIL-STD-1285) shall be required on the multiple carriers. These requirements apply to the original or repackaged product by the manufacturer or distributor.

TABLE H-IIA. Technology characterization testing for hermetic and non-hermetic packages .

5. Susceptibility to electrostatic discharge (ESD) sensitivity 2/ == MIL-STD-883 test method and condition or JEDEC test method

ESD TM 3015 or **ANSI/ESDA/JEDEC JS-001** ~~JESD-22-A114~~

2/ ESD classification level is as defined within test method 3015.

TABLE H-IIB. Technology characterization testing for plastic packages.

9. Susceptibility to electrostatic discharge (ESD) sensitivity 4/ == MIL-STD-883 test method and condition or JEDEC test method

ESD TM 3015 or **ANSI/ESDA/JEDEC JS-001** ~~JESD-22-A114~~

4/ ESD classification level is as defined within test method 3015.

H.3.4.8 Product qualification (extension from existing qualified technology) .

b. Product qualification for multi-product wafer (MPW):

3(iv) Electrostatic Discharge (ESD) sensitivity test shall be performed in accordance with TM 3015 or **ANSI/ESDA/JEDEC JS-001**; Capacitance in accordance with TM 3012; and Electrical Latch-up: Each buffer type shall be tested for initial qualification or buffer design changes.