

ENGINEERING PRACTICE (EP) STUDY

**TITLE: EP study on update of non-hermetic microcircuits class N (military, terrestrial and avionics application) and class Y (Space application) to MIL-PRF-38535.
(Phase 1)**

Study project number: 5962-2019-002

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FINAL REPORT

**Study Conducted by DLA Land and Maritime
Document Standardization Division (VA)
Active Devices Branch (VAC)**

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**EP study on
Update of non-hermetic microcircuits class N (military, terrestrial and avionics application
and class Y (Space application) to MIL-PRF-38535.**

- I. **OBJECTIVE:** The purpose of this Engineering Practice (EP) Study is to obtain input and justification from the military services, microcircuit manufacturers, and space application user's communities, concerning the update/addition of non-hermetic class N (military, terrestrial and avionics application) and class Y (non-hermetic Space application) microcircuits to MIL-PRF-38535.
- II. **BACKGROUND:** MIL-PRF-38535 offered non-hermetic class N (plastic package) and class Y (ceramic substrate non-hermetic device for space application). In table IB, class N has an inclusive table that comprises screening and QCI tests requirement, which called tests/monitors for plastic package. However, this inclusive table fails to distinguish between screening and QCI test flows that creates confusion with periodic QCI test monitoring issue as well as product reliability.

On the other hand, design requirement of modern electronics satellite/warfare systems are growing faster and moving forward with an advance and complex package technologies. Considering complexity of new technologies and device packaging techniques, JEDEC CE-12 formed a task groups (TG) for exploring the state of the art class Y concept to develop a new organic substrate flip chip devices, and 2D, 2.5D and 3D package technology requirements for qualification and screening of non-hermetic microcircuits packages for space applications.

Accordingly, to bring advancement and adopting new package technologies into QML system to MIL-PRF-38535, DLA Land and Maritime-VAC is conducting an EP study (phase 1) which includes:

- (1) Update class N with separating screening and QCI tables to make robust high reliability plastic encapsulated microcircuits(PEM) devices for military, terrestrial and avionics application;
- (2) Update/create a new appendix K (Next Gen) with other appendix/sections update for non-hermetic microcircuits devices that includes organic/ceramic substrate flip chip devices, 2D, 2.5D and 3D package technology requirements for space applications.

DLA Land and Maritime-VAC is requested to review all attachment (Survey questionnaire attachment #1, Screening and QCI requirement attachment #2, Appendix H PIDTP requirement attachment #3 and next Gen appendix K requirement attachment #4) and send comments/feedback to DLA within the stipulated time for discussion and further development.

- III. **RESULTS:** The EP Study project was open and initial draft posted on the DLA Land and Maritime website and distributed to military services, microcircuit manufacturers, original equipment manufacturers, and user communities on March 11, 2019 for review and comments. All received comments/responses (see attachment # 1) were compiled and discussed at JEDEC joint JC-13/CE-12 PEM subcommittee meeting in Memphis, TN on May 2019 and Columbus, Ohio on September 16, 2019. After reviewed all comments, DLA Land and Maritime-VAC is proposing to conduct separate EP study phase 2: Update class N with screening and QCI tables to make robust high reliability plastic encapsulated microcircuits(PEM) devices for military, terrestrial and avionics application; and EP study phase 3: Update/create a new appendix K (Next Gen) for non-hermetic microcircuits devices that includes organic/ceramic substrate flip chip devices, 2D, 2.5D and 3D package technology requirements for space applications.
- IV. **CONCLUSIONS:** The findings of this EP study was sufficient to support for continues development by updating plastics devices class N for military, terrestrial and avionics application and updating class Y devices including a new appendix K (Next Gen) new technology requirements for space applications. DLA Land and Maritime-VAC will conduct EP study phase 2 for class N and phase 3 for class Y updating to MIL-PRF-38535.

Attachment-# 1

Survey questionnaire and received comments

Questionnaire:

1. What are your comments / views concerning the update class N to make robust high reliability plastic encapsulated microcircuits(PEM) devices for military, terrestrial and avionics application to MIL-PRF-38535?

JC-13.2 MFGR: In table IA, the Class N screening flow should closer match to applicable Class Q requirements [to match its current intent], not Class V/Y. Class Y would need to include organic as well as non-organic parts.
JC-13.2 MFGR : Welcomes the update of class N to flip chip package. This could expand our customer portfolio.
Test lab: I think we need to make it robust. The current way that is defined in the Mil PRF 38535 is very ambiguous and does not allow for clear understanding of what the screening and qualification requirements are
JC-13.2 MFGR : MIL-PRF-38535 revision L Class N is significantly out of date for use in high reliability applications and leaves much of the screening up to the manufacturer (not standardized). The attempt in this EP Study was to ask questions about Class N (military, terrestrial and avionics applications), not Class N (space). However, similar to what was discussed in AS6294/1 or /2, terrestrial and space were broken out into 2 different requirements/levels. The attached update of the tables only addressed "high reliability" which mirrored Class V/Y in most of the tables which we equated to "Space" applications. We have provided inputs on Class N in question 5 and 10 of this questionnaire.

2. How would you define the proposed class N into MIL-PRF-38535? Do you support proposed definition of class N?

Current definition of class N:

6.4.28 Class N. Items which have been subjected to and passed all applicable requirements of this specification including qualification testing, screening testing, and TCI/QCI inspections, and are encapsulated in plastic. This product must be assessed by the user to determine if it is appropriate for use in users' application.

Proposed definition of 6.4.28 Class N: A microcircuit employing a non-hermetic plastic package, which meets all applicable requirements of this specification including qualification, screening and TCI/QCI inspections, and are not limited to encapsulated in plastic.

JC-13.2 MFGR: The Class definitions in MIL-PRF-38535, paragraphs 6.4.27-6.4.34 should be clarified to indicate which are for space, high reliability applications and which are for non-space, military applications. I believe that the original intent for Class N was non-space, military applications.
JC-13.2 MFGR: Agrees with the proposed class N definition.
TEST Lab: I support the below definition. (proposed definition) WE have to have a clear guidance with sample sizes for screening, qual and TCI/QCI for class N to work
JC-13.2 MFGR : The red text below under the proposed definition doesn't make any sense and conflicts with the 1 st sentence. End the sentence after "inspections". Proposed definition of 6.4.28 Class N. A microcircuit employing a non-hermetic plastic package, which meets all applicable requirements of this specification including qualification, screening and TCI/QCI inspections.

3. What are your comments / views concerning the addition of **organic substrate** to class Y flip chip non-hermetic devices for space level application into MIL-PRF-38535?

JC-13.2 MFGR: Remove "flip chip" from question as Class Y can be flip chip or wirebond. As we have been discussing in the Class Y task group, I support the addition of organic substrates to Class Y. Also as discussed, we need some way to indicate use profiles and organic vs ceramic substrates in the final product definitions.

JC-13.2 MFGR : This is a positive point. Te2v agrees as we could widen our range of products

TEST Lab: We should do so after defining requirements specific to Class Y using organic substrates

JC-13.2 MFGR: Acceptable to use organic substrate to class Y Flip Chip non hermetic, however careful considerations shall be made on:

- Coefficient of thermal expansion (CTE)
- Glass transition temperature (Tg) if appropriate
- Substrate core and build-up layer materials
- Solder mask material and thickness; SMD versus NSMD landing pads
- Via plugging
- Conductor material and landing pad construction
- Moisture absorption and outgassing characterization

4. How would you define the proposed class Y into MIL-PRF-38535? Do you support proposed definition of class Y?

Current definition of class Y:

6.4.31 Class Y. A microcircuit employing a ceramic non-hermetic package, which meets all applicable requirements of this specification including qualification, screening and TCI/QCI requirements, and all applicable requirements of Appendix B herein.

Proposed definition of class Y: "A microcircuit employing a ~~ceramic~~ non-hermetic package, which meets all applicable requirements of this specification including qualification, screening and TCI/QCI requirements, and all applicable requirements of Appendix B and Appendix K (Next Gen) herein.

JC-13.2 MFGR: See our proposed definition below. Appendix K doesn't make sense as a separate appendix. Individual paragraphs within could be incorporated into the existing spec sections.

Proposed definition of class Y: "A microcircuit employing a ~~ceramic~~ non-hermetic package, which meets all applicable requirements of this specification including qualification, screening and TCI/QCI requirements, and all applicable requirements of Appendix B (Space Applications) and Appendix K (Next Gen) herein.

JC-13.2 MFGR: Agrees with the proposed class Y definition.

As per 2. there is one slight note of caution: in the case the fabrication is subcontracted (at NXP for example) we must ensure that the screening is done according to the 38535 requirements.

Test Lab: We will have to also re-define Appendix B and Appendix K (Next Gen). Once that is done; this definition can be supported

JC-13.2 MFGR : No comments.

5. What are your general comments on the update class N ?

JC-13.2 MFGR: Class N should be equivalent to Class Q for non-hermetic parts. Class Y should be equivalent to Class V but for non-hermetic parts.

JC-13.2 MFGR : It is a good point to introduce this new class in order to provide to customers a new line/range of product.

Test lab: Need to have separate tables for screening; quals and QCI/TC with samples sizes

JC-13.2 MFGR : More measurements can be included to ensure high reliability of plastic encapsulated packages.

- 1) Process selection:
 - a) Wire bond with intermetallic compound (IMC) > 75%.
 - b) Inline monitor on bond cratering.
 - c) Include CSAM in every mold setup.
- 2) Assembly Inspection: 100% optical inspection before encapsulation (Condition B) and 100% at final outgoing.
- 3) Outgassing test should be added (appendix H) one time in accordance with ASTM E595 or MIL-STD-883 test method 5011 as applicable.

6. What are the technical/engineering issues for 2D/2.5D and 3D packages ?

JC-13.2 MFGR: May want to move these into 38534 with element evaluation of the different pieces.

JC-13.2 MFGR : Not currently used by Te2v.

JC-13.2 MFGR: Abstains from comment, no involvement in 2.5D – 3D package technology.

7. Do you have any technical suggestions for flip chip/2D/2.5D/3D packages with BGA/CGA board level testing? Please provide your comments.

JC-13.2 MFGR: Mixing too many things in this question. Each should be considered separately: flip chip, 2D/2.5D/3D packaging, BGA packages and CGA packages. Resistance to Soldering test or board level testing should be include during the initial characterization and qualification. Problem for some manufacturers is that they do not know the next level assembly/board level conditions to test to. There has been discussion at JEDEC for Aerospace (Larry) to provide example use profiles so that manufacturers can test to them.

JC-13.2 MFGR : No.

JC-13.2 MFGR : Flip Chip with Cu pillar are higher reliable in solder extrusion within package compared to ball flip chips. A multiple reflow test (at least 3x of IR reflow) is recommended for characterization.

8. Do you have any technical issue with **Pb-free micro bump of flip chip packages** ? What are the advantages of Pb-free bump instead of tin-lead bump?

JC-13.2 MFGR: Advantages of Pb-free flip chip is availability. As commercial industry moves away from leaded products, availability becomes an issue. Pb-free has different issues that need to be evaluated vs leaded bumps such as materials, sizes, tin whiskers (unknown if this is an issue for flip chip but expected to not be and to be mitigated by underfill).

JC-13.2 MFGR :L Our experience is that C4 lead free have better reliability results that C4 leaded. In particular for temperature cycling results are better. We have the case of products that failed temperature cycling tests with C4 leaded and passed the same tests with C4 lead free.

JC-13.2 MFGR : None detected on our selected material of Pb-free alloy. Advantage of Pb free: Compliant to European Union (EU) legislation passed on the Waste from Electrical and Electronic Equipment (WEEE) and the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directives in 2002. However careful selection of Sn based alloy composition is required to have good soldering and to prevent Sn migration. Typically Sn-Ag-Cu based alloys are recommended.

9. For 2D/2.5D/3D package uses copper filler TSV interposer technique, are this copper filler has long term reliability issue ?

JC-13.2 MFGR: We haven't used this yet so no opinion.

JC-13.2 MFGR : No experience

JC-13.2 MFGR : Abstains from comment, no involvement in 2.5D – 3D package technology.

10. DLA Land and Maritime-VAC proposed draft Screening and TCI/QCI requirements for class N and class Y (see attachment # 2), please review those tables and provide your comments/feedback.

JC-13.2 MFGR: In table IA, the Class N screening flow should closer match to applicable Class Q requirements [to match its current intent], not Class V/Y. Class Y would need to include organic as well as non-organic parts.

JC-13.2 MFGR: About screening table :

- ❖ TM2030 for CSAM is not suitable for TIM or underfill inspection. This TM refers to a die attach which is not the same. TM2030 should be revised or another TM should be proposed for replacement.
- ❖ Static BI : Specific method of TM1015 should be detailed or more precise to avoid any question/discussion
- ❖ Comment 8/ : precision has to be added on flipchip with capacitors on which the PIND test is mandatory (on the contrary to flipchip alone)
- ❖ CSAM TIM is requested by appendix B but not mentioned in the screening table : it should be added for cohesion

About QCI tables :

- ❖ Subgroup D8 refers to TM2024 and is not appropriate, it is dedicated to silver glass package. Instead, internally we use TM2027 which is more relevant.

JC-13.2 MFGR :

- a. The attached EP Study was not modified from the existing MIL-PRF-38535, assume that any changes to this document other than specifically to address class Y or N will not be included (i.e. table II note 5).
- b. **Table IA: Screening test:**
 - a. 1. Wafer lot acceptance test: Add note 1/ to Class N
 - b. 3. Internal visual inspection: recommend Condition B, 100% inspection prior to encapsulation.
 - c. 14. PDA: Add "(all lots)" to the table for Class N
 - d. 17. Remove from the screening table and move to Group B.
 - i. When moved to Group B, also change and/or in the 1st cell to "and" and change x-ray to 1 view (top).
 - ii. C-SAM is written as SAM and C-SAM – should be consistent. Also C-SAM should be in accordance with J-STD-20.
 - e. External Visual TM2009 doesn't take plastic encapsulated devices into consideration and should be enhanced with additional criteria related to plastic packages.
 - f. Notes 9, 12, 15, 17 should also reference Class N
 - g. Note 21/ will need to be removed and restated in Group B.
- c. **Table II: (Group B)**
 - a. Add screening table item 17 to Group B requirements (see Table IA bullet d above)
 - b. Bond Strength should be allowed to be done "In-line" during mfg processing. Note 7/ talks about pre-seal but doesn't adequately address Class N mold process (encapsulation is a better term)
- d. **Table III: (Group A)**
 - a. Note 6 should include Class N.
- e. **Table IV (Group C)**
 - a. No comments
- f. **Table V: (Group D)**
 - a. Subgroup 1 TM 2016 should be allowed to be performed inline (similar to Bond strength)
 - b. Subgroup 3a (Thermal shock): doesn't apply to class N and should be deleted.
 - c. Subgroup 3c (Moisture resistance): should allow Condition A or B depending on package style.
 - d. Subgroup 5 (Salt Atmosphere): Not applicable and should be removed.
 - e. Subgroup 8 (Lid torque): Not applicable and should be removed.

11. Please review the proposed changes of MIL-PRF-38535 appendix H (PIDTP) (see attachment # 3), and new appendix K (Next Gen) (see attachment # 4) and provide your comments.

JC-13.2 MFGR:

- Under H.3.4.4.1.2.1) remove flip chip from sentence: For organic substrate flip-chip devices, the following factors shall be evaluated and documented in PIDTP and move the organic section under H.3.4.4.1.1 for non-hermetic packages.
- Tables H-IA and H-IIA: should Class N be added with Class Y columns?
- Appendix K doesn't make sense as a separate appendix. Individual paragraphs within could be incorporated into the appropriate existing spec sections. Akbar had mentioned that this appendix was supposed to show screening an qual deltas for non-hermetic parts but you already show these in the tables in Attachment #2.

JC-13.2 MFGR : Class Y and class N are different while their QCI are identical.

- Appendix B and K are very similar. Do you think appendix B will be maintained?

JC-13.2 MFGR Appendix H

- a. Too many “and” in the sentence.
 - b. H.3.4.1.1 Process technology validation. The manufacturer shall perform sufficient technology qualification testing to assure the devices supplied meet the minimum class N **and** class Y, **and** class level B or S performance requirements as described herein. The manufacturer shall maintain documentation of qualification testing for review by the preparing or acquiring activity upon request.
 - c. H.3.4.4.1.2 Section 8: Change “Copper filer to Copper filler” a) Copper filer TSV interposer geometry.
 - d. H.3.4.4.1.2 Section 8.1: Why are cycles including in HTOL?
- 8.1) Long-term reliability test 2D or 2.5D or 3D package devices:
- 1) High-temperature operating life (HTOL) test shall be performed with a maximum voltage at $T_j = 125^{\circ}\text{C}$ on samples size 5(0) **for 1500 cycles**.
 - e. H.3.4.4.1.2 Section 8.1 (4): Change “perfumed” to performed
 - 4) Power cycling test shall be **perfumed** at 125°C on samples size 5(0) for 1500 cycles.
 - f. Table H-IB
 - (1) Group 2, should either have OR for x-ray (1 view) or SAM. Recommend having both however SAM should be in accordance with J-STD-20 (looking for delamination).
 - (2) Group 3, change 1000 cycles to 500 cycles in accordance with JESD 47
 - (3) Group 4, delete as not applicable.
 - g. H.3.4.4.1.2 Section Change to allow for 500 cycles for non-ceramic substrates as shown below
 - 5.1) Underfill long term reliability test: Manufacture’s shall perform following long term underfill reliability test
 - (1) Temperature cycling test: Cured underfill with solder bump temperature cycling test shall be performed for 1,000 cycles (ceramic substrate) **or 500 cycles (non-ceramic substrate)** in accordance with TM1010 condition C (-65 to 150°C)

JC-13.2 MFGR Appendix K

- a. K.1.1 Does this scope include Class N? Class V – both are referenced within the body of the appendix.
- b. K.2.1 change “specified” to “specific”, not sure the 2nd sentence makes any sense. Last sentence of this paragraph needs work too.
- c. K.2.4 so this appendix supersedes the main body of MIL-PRF-38535 or Appendix H?
- d. K.3.1 invokes Appendix C for Class N & Y products, it shouldn’t.
- e. K.3.14 Organic with mold compound? Class Y should not have mold compound.
- f. K.3.15 Class Y 2D, 2.5D, 3D have mold compounds? Is this correct?
- g. K.3.2 – change paragraph to reflect Appendix A.3.1.2.
- h. K.4.3 Group A exemption/addition of Group A for all classes is blank – why have (a) – (c)
- i. K.4.3 Table II, Group B – why is class V included in the exceptions? Does this paragraph apply to Class N?
- j. K.4.3 Table V, Group D – (a) – (c) are all empty, why have them in the spec?
- k. K.4.3 Group E – (a) – (c) are all empty, why have them in the spec?

JC-13.2 MFGR :

- 1. Attachment #1 Survey Questionnaire, I have no comments and Q1 and Q3 and we can support Q2 and Q4
- 2. Attachment #2, Note #5 should be updated to include class N
- 3. Attachment #3, since we are not a fab house, how do we control process technology validation per page 29.
- 3a. Since we do not do plastic package assembly how do we the information needed for assembly and packaging technology certification as required on page 40 and 44?
- 3b. Flip Chip, if we are to enter this assembly technology, we must be prepared to supply the information required on page 48 sec H.3.4.4.1.2

JC-13.7/CE-12 Task Group 2018-02

- ❖ p.2, note 1. Heat sink is covered under flip-chip PIDTP category, item 6. Passive attach might be a separate PIDTP category, but should be generalized to apply to an ancillary component, not just capacitors. This was discussed in original EP study.
- ❖ p.2, note 2. As currently defined, PIDTP is only required for space applications, so does not apply to Class N.
- ❖ p.4. This list is where this TG should focus, if limited to expanding Class Y to organic substrates. Of course, the word “ceramic” would have to be removed from the Class Y definition. Note particularly that the issue of CTE is mismatch to the die.
- ❖ p5, note 2. Perhaps 2.5D could just be treated as just another type of substrate – the silicon interposer.
- ❖ p5, note 3. I suggest that TSV, which enables 3D, could be just another PIDTP “nonstandard assembly technology” category.
- ❖ p9, note 1. I don’t see why BGA and CGA must be separated. We went through this in drafting the current PIDTP requirements, and found most to be common to any solder termination.
- ❖ H.3.4.4.1.2 Flip-Chip Assembly. For space microcircuits employing flip-chip assembly technologies either **class V or class Y (class level S)**, the PIDTP must address the **materials and processes unique to solder bump interconnect attach, underfill and lid-to-die attach**. The plan shall demonstrate as a minimum, how the following are evaluated and monitored including a corresponding package level reliability demonstration:
 - 1) **Substrate materials**. The substrate materials shall be documented in the PIDTP, and shall include landing pad composition.
 - i) Coefficient of thermal expansion (CTE)
 - ii) Glass transition temperature (Tg) if appropriate
 - iii) Substrate core and build-up layer materials
 - iv) Solder mask material and thickness; SMD versus NSMD landing pads
 - v) Conductor material and landing pad construction
 - vi) Moisture absorption and outgassing characterization
- ❖ H.3.4.4.1.3 Solder Terminations. For space use microcircuits employing solder terminations (**class V or class Y**), the PIDTP shall address the **materials and processes unique to solder terminations, such as ball/column integrity, attachment integrity, damage due to test, protection for shipment and shelf life**. The manufacturer shall perform **post column attachment electrical characterization over temperature and compare data with pre-column attachment** process to assess any changes due to the column attachment process.
 - i) BGA solder ball or CGA solder column composition
 - ii) BGA solder ball or CGA solder column attach process
 - iii) Landing pad construction and dimensions
 - iv) BGA solder ball diameter or CGA solder column diameter and length

Notes:

- Consider separate paths for BGA solder balls versus CGA solder columns so as not to conflate the two different termination technologies
- Need to review sections other than PIDTP for accommodations for Class Y extensions to flip chip on organic, 2.5D, 3D, etc.; look at class definitions, screening and qualification tests, etc.

JC-13.7/CE-12 Task Group 2018-02

- ❖ **Question 1.** I would like to see N look as much like Y as Q looks like V, with the only difference being the non-space application, which drives less stringent qualification and screening.
- ❖ **Question 2.** I suggest dropping references to plastic from the N definition, and focusing on nonhermeticity. This makes it more parallel to N. Of course, I similarly advocate expanding Y to include the option of organic encapsulation (via another PIDTP category, as I proposed in 2016).
- ❖ **Question 3.** Drop “ceramic” from the Y definition, and expand the PIDTP section on flip-chip substrate materials.
- ❖ **Question 4.** I don’t see why Appendix K is required. Rather, I would expand the PIDTP requirements to cover the additional “non-standard” technologies to which Appendix K is aimed.
- ❖ **Question 5.** 2.5D silicon interposers seem like just another flip-chip substrate material. TSVs, which enable 3D, do have many unique issues. I would handle this with another PIDTP category.
- ❖ **Question 6.** As discussed in the original EP study, board level testing seems out of scope for 38535.
- ❖ **Question 7.** There are various issues, but the most significant concern has been whisker growth.
- ❖ **Advantages** include higher density, higher performance, and more sources of supply.
- ❖ **Question 8.** Various, but primarily stress and extrusion due to thermal cycling (especially in-process).

Custodian :

- ❖ **Page 6, Table IA: Regarding Test #14**, under the Class N column, is 5 percent PDA the only requirement? There’s a stray comma in this block, so unsure if there’s some information missing here or if the comma was inserted by mistake.
- ❖ Page 14, Table III: There may have been a document conversion issue which converted some of the degree (°) symbols to small boxes throughout the document. This was initially discovered in Table III, where +25°C showed a small box where the degree symbol is supposed to be located. In addition, this issue was also discovered in: paragraph H.3.1.9.c.1.iv and v (page 29); paragraph H.3.2.1.2.1b(2) (page 34); and paragraph H.3.4.1 (page 45).
- ❖ Page 24, Paragraph H.2.3: In ASSIST, DoD withdrew their adoption of EIA557. As a result, confirm that this is still an appropriate document to reference.
- ❖ Page 27-28, Figures H-1 and H-2: Some of the wording in the boxes in these figures got accidentally cut out. Recommend re-sizing the appropriate boxes to ensure the full text fits.
- ❖ Page 37, Paragraph H.3.2.1.3.2.a.3: It appears the numbering scheme is off as there are two paragraphs labelled #3.
- ❖ Page 59, Paragraph K.2.1: There appears to be something missing in the first sentence of this paragraph between “specified” and “of this appendix”. Should it say, “.....specified in sections K3 and K4 of this appendix”?
- ❖ Page 63, Paragraph K.3.15: It should read as “2.5D” instead of “2,5D”.
- ❖ Page 67: Reference is made to a “table H-IX” near the top of this page; however, this table doesn’t seem to exist. Confirm the appropriate table number to reference here.
- ❖ **Custodian :** Concur in Update of non-hermetic microcircuits class N (military, terrestrial and avionics application and class Y (Space application) to MIL-PRF-38535. It’s necessary to update/addition on the Class N for military, terrestrial and avionics application use. 38535. It’s necessary to update/addition on the Class N for military, terrestrial and avionics application use.
- ❖ **Reviewer :** The Naval Air Systems Command (AS) has no comments to offer on the study. However, we would like to be provided with a copy of the results of the study

Attachment # 2

TABLE IA. Screening procedure for hermetic class Q and V and non-hermetic class N and Y microcircuits

Screening Tests	Hermetic microcircuit devices test requirements MIL-STD-883, test method (TM) and conditions		Non-hermetic microcircuit devices test requirements MIL-STD-883, test method (TM) and conditions	
	Class Q (class level B)	Class V (class level S)	Class N (high reliability)	Class Y (class level S)
1. Wafer lot acceptance test	QM plan (see H.3.2.1.4) <u>1/</u>	QM plan (see H.3.2.1.4) <u>1/</u> or TM 5007 of MIL-STD-883 (all lots)	TRB QM plan (see H.3.2.1.4)	QM plan (see H.3.2.1.4) <u>1/</u> or TM 5007 of MIL-STD-883 (all lots)
2. Nondestructive bond pull (NDBP) test <u>2/</u>		TM 2023		TM 2023
3. Internal visual inspection <u>3/</u>	TM 2010, condition B	TM 2010, condition A	TM 2010, condition A	TM 2010, condition A
4. Temperature cycling <u>4/</u>	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum
5. Constant acceleration <u>5/</u>	TM 2001, condition E (minimum), Y1 orientation only	TM 2001, condition E (minimum), Y1 orientation only		TM 2001, condition E (minimum), Y1 orientation only
6. Visual inspection <u>6/</u>	100%	100%	100%	100%
7. Particle Impact Noise Detection (PIND) test <u>7/ 8/</u>		TM 2020, test condition A on each device		TM 2020, test condition A on each device
8. Serialization <u>9/</u>	In accordance with device specification (100%)	In accordance with device specification (100%)	In accordance with device specification (100%)	In accordance with device specification (100%)
9. Pre burn-in (Interim) electrical parameters test <u>10/</u>	In accordance with device specification <u>11/</u>	In accordance with device specification <u>12/</u>	In accordance with device specification <u>12/</u>	In accordance with device specification <u>12/</u>
10. Burn-in test: <u>10/ 13/ 14/</u>	TM 1015 160 hours at +125°C minimum	TM 1015 240 hours at 125°C, condition D <u>15/</u>	TM 1015 240 hours at 125°C , condition D <u>15/</u>	TM 1015 240 hours at 125°C , condition D <u>15/</u>
11. Post burn-in (Interim) electrical parameters test <u>10/</u>		In accordance with device specification <u>12/</u>	In accordance with device specification <u>12/</u>	In accordance with device specification <u>12/</u>
12. Reverse bias burn-in test (Static burn-in) <u>13/ 14/ 16/</u>		TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum	TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum	TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum
13. Post burn-in (Interim- reverse bias) electrical parameters test <u>10/</u>		In accordance with device specification <u>12/</u>	In accordance with device specification <u>12/</u>	In accordance with device specification <u>12/</u>

TABLE IA. Screening procedure for hermetic class Q and V and non-hermetic class N and Y microcircuits - Continued.

Screening Tests	Hermetic microcircuit devices test requirements MIL-STD-883, test method (TM) and conditions		Non-hermetic microcircuit devices test requirements MIL-STD-883, test method (TM) and conditions	
	Class Q (class level B)	Class V (class level S)	Class N (high reliability)	Class Y (class level S)
14. Percent defective allowable (PDA) calculation <u>17/</u>	5 percent PDA (all lots)	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)	5 percent PDA,	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)
15. Final electrical tests <u>18/</u> (see table III) a. Static test : (1) at 25°C (2) Maximum and Minimum operating temperature b. Dynamic or functional test : <u>19/</u> (1) at 25°C (2) Maximum and Minimum operating temperature c. Switching test : (1) at 25°C (2) Maximum and Minimum operated temperature	In accordance with applicable device specification (see group A test)	In accordance with applicable device specification (see group A test)	In accordance with applicable device specification (see group A test)	In accordance with applicable device specification (see group A test)
16. Seal test <u>20/</u> a. Fine leak b. Gross leak	TM 1014	TM 1014	Not applicable	Not applicable
17. Radiographic (X-ray) and/or C-SAM test <u>21/</u>		X-ray: TM 2012, Two views; C-SAM TM 2030	X-ray: TM 2012, Two views; C-SAM TM 2030	X-ray: TM 2012, Two views; C-SAM TM 2030
18. External visual inspection <u>22/ 23/</u>	TM 2009	TM 2009	TM 2009	TM 2009
19. Qualification or quality conformance inspection/TCI test sample selection	<u>24/</u>	<u>24/</u>	<u>24/</u>	<u>24/</u>
20. Radiation dose rate induced latch-up test <u>25/</u>	TM 1020	TM 1020	TM 1020	TM 1020

Note: The class N update requirement is not applicable for existing class N product. The existing class N product shall meet the requirements of table IB of MIL-PRF-38535.

TABLE IA. Screening procedure for hermetic class Q and V and non-hermetic class N and Y microcircuits - Continued.

- 1/ Testing per manufacturer's QM plan. See paragraph H.3.2.1.4 of MIL-PRF-38535 or TM 5007 of MIL-STD-883.
- 2/ For flip chip packages Nondestructive bond pull (NDBP) test is not required.
- 3/ Unless otherwise specified, at the manufacturer's option for test samples selection of group B, bond strength test (method 5005) may be randomly selected prior to or following internal visual (method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual exam), and unsealed microcircuits awaiting further processing shall be stored in a dry, inert, controller environment until sealed. Test method 2010 applies in full except when method 5004, alternate 1 or alternate 2 (appendix A) is in effect (see 3.3 method 5004 of MIL-STD-883). For gallium arsenide (GaAs) devices only, TM 5013 of MIL-STD-883 should be used. For flip chip devices, internal visual inspection shall be performed in accordance with TM 2010 and SAM TM 2030.
- 4/ For devices with solder terminations, Temperature cycling test may be performed without balls and columns upon approval of PIDTP and QM plan.
- 5/ All microcircuits shall be subjected to constant acceleration. For microcircuits which are contained in packages that have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be tested by replacing test condition E with condition D or with test conditions as specified in the applicable device specification. Unless otherwise specified in the acquisition document, the stress level for large, monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this deviation shall be specified in the QM plan, and data available for review by the preparing or acquiring activity. The minimum stress level allowed in this case is condition A. For flip chip devices, Constant acceleration test is not required.
- 6/ At the manufacturer's option, external visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.
- 7/ See paragraph A.4.6.3 of appendix A and paragraph B.4.1 of appendix B of MIL-PRF-38535. The PIND test may be performed in any sequence after temperature cycling test and prior to post burn-in (interim) electrical parameters test.
- 8/ For device without a cavity or for flip chip devices with underfill, PIND test is not applicable.
- 9/ Class V or class Y (class level S) devices shall be serialized prior to the first recorded electrical measurement in screening. Class N and class Q (class level B) microcircuits shall be serialized if delta calculations or matching characteristics are a requirement of the device specification. Each microcircuit shall be assigned a unique serial number in order to trace the data back to an individual device within the inspection lot which shall, in turn, be traceable to the wafer lot from which the device originated.
- 10/ Interim (pre and post burn-in) electrical testing shall be performed when specified, to remove defective devices prior to further testing or to provide a basis for application of percent defect allowable (PDA) criteria when PDA is specified (Ref. test step 14: PDA calculation, and footnote 17 herein). If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or standard microcircuit drawing (SMD). This test need not include all specified device parameters, but shall include those measurements that are most sensitive to the time and temperature effects of burn-in and the most effective in removing electrically defective devices.
- 11/ When specified in the applicable device specification, 100 percent of the devices shall be tested and the results recorded for those parameters requiring delta calculations.
- 12/ For class V and class Y (class level S) microcircuit devices, delta measurements shall be performed. The specific delta parameters shall be as defined in the applicable device specification. Pre burn-in and post burn-in interim electrical parameters shall be read and recorded when delta measurements have been specified as part of post burn-in electrical measurements, 100 percent of the devices shall be tested and the results shall be recorded for those parameters requiring delta calculations.

TABLE IA. Screening procedure for hermetic classes Q, V and **non-hermetic class N and Y microcircuits**- Continued.

- 13/ Burn-in shall be performed on all QML microcircuits, except as modified in accordance with SMD section 4.2, or above their maximum rated operating temperature (for devices to be delivered as wafer or die, burn-in of packaged samples from the wafer lot shall be performed to a quantity accept level of 10(0)). For microcircuits whose maximum operating temperature is stated in terms of ambient temperature (T_A), table I of TM 1015 of MIL-STD-883 applies. For microcircuits whose maximum operating temperature is stated in terms of case temperature (T_C), and where the ambient temperature would cause T_J to exceed $+175^{\circ}\text{C}$, the ambient operating temperature may be reduced during burn-in from $+125^{\circ}\text{C}$ to a value that will demonstrate a T_J between $+175^{\circ}\text{C}$ and $+200^{\circ}\text{C}$ and T_C equal to or greater than $+125^{\circ}\text{C}$ without changing the test duration. Data supporting this reduction shall be documented in the QM plan and shall be available to the acquiring and qualifying activities upon request.
- 14/ When test condition F of method 1015 for temperature accelerated screening is used for either burn-in or reverse bias burn-in, it shall be used for both. Also, when devices have aluminum/gold metallurgical systems (at either the die pad or package post), the constant acceleration test shall be performed after burn-in and before completion of the final electrical tests (e.g, to allow completion of time limited tests but that sufficient 100 percent electrical testing to verify continuity of all bonds is accomplished subsequent to constant acceleration).
- 15/ Where applicable, dynamic burn-in test shall be performed, and test condition F of method 1015 and temperature accelerated test requirement shall not apply. For class V or class Y (class level S), burn-in test shall be performed in accordance with TM 1015 of MIL-STD-883, on each device for 240 total hours at $+125^{\circ}\text{C}$. For a specific device type, the burn-in duration may be reduced from 240 to 160 hours if three consecutive production lots of identical parts, from three different wafer lots pass percent defective allowable (PDA) requirements after completing 240 hours of burn-in. Sufficient analysis (not necessarily failure analysis) of all failures occurring during the run of the three consecutive burn-in lots shall not reveal a systematic pattern of failure indicating an inherent reliability problem which would require that burn-in be performed for a longer time. The manufacturer's burn-in procedures shall contain corrective action plans, approved by the qualifying activities for dealing with lot failures.
- 16/ The reverse bias burn-in is a requirement only when specified in the applicable device specification and is recommended only for a certain MOS, linear or other microcircuits where surface sensitivity may be a concern. When reverse bias burn-in is not required, interim post burn-in electrical parameter measurements shall be omitted. The order of performing the burn-in test and the reverse bias burn-in test may be inverted. Static burn-in may be substituted for high temperature reverse bias burn-in based on device technology and must be approved by the QA. Moreover, burn-in time-temperature regression table I of TM 1015 of MIL-STD-883 can be used for determination of reverse bias burn-in time and temperature.
- 17/ The percent defective allowable (PDA) shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in all cases where delta parameters are specified) with the parameters, deltas and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class V or class Y (class level S) the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class level S screening where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or subplot for burn-in shall be used to determine the percent defective for that lot, or subplot and the lot or subplot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA (10 percent) or 2 devices, whichever is greater. This test need not include all specified device parameters, but shall include those measurements that are most sensitive to and effective in removing electrically defective devices (see A.4.6.1.1 and A.4.6.1.2 of MIL-PRF-38535).
- 18/ Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the device specification and shall include the tests of [table III](#), group A, subgroups 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11, unless otherwise specified in the device specification.

TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic class N and Y microcircuits - Continued.

- 19/ Functional tests shall be conducted at input test conditions as follows: $V_{IH} = V_{IH(min)} + 20$ percent, -0 percent; $V_{IL} = V_{IL(max)} + 0$ percent, -50 percent; as specified in the most similar military detail specification. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.

CAUTION: To avoid test correlation problems, the test system noise (e.g., testers, handlers, etc.) should be verified to assure that $V_{IH(min)}$ and $V_{IL(max)}$ requirements are not violated at the device terminals.

- 20/ The fine and gross leak seal tests shall be performed separately or together, between constant acceleration and external visual inspection test. For class level S and class level B devices, all device lots (sublots) having any physical processing steps (e.g., lead shearing, lead forming, solder dipping to the glass seal, change of, or rework to, the lead finish, etc.) performed following seal or external visual inspection shall be retested for hermeticity and visual defects. This shall be accomplished by performing, and passing, as a minimum, a sample seal test (method TM 1014) using an acceptance criteria of a quantity (accept number) of 116(0), and an external visual inspection (method TM 2009) on the entire inspection lot (sublot). For devices with leads that are not glass-sealed and that have a lead pitch less than or equal to 1.27 mm (0.050 inch), the sample seal test shall be performed using an acceptance criteria of a quantity (accept number) of 15(0). If the sample fails the acceptance criteria specified, all devices in the inspection lot represented by the sample shall be subjected to the fine and gross seal tests and all devices that fail shall be removed from the lot for final acceptance. For class level S devices, with the approval of the qualifying activity, an additional room temperature electrical test may be performed subsequent to seal, but before external visual, if the devices are installed in individual carriers during electrical test.
- 21/ The radiographic and/or SAM screening test may be performed in any sequence after serialization. Only one view is required for flat packages and leadless chip carriers having lead (terminal) metal on four sides. For flip chip technology, only C-SAM inspection is required. SAM inspection may be performed in any sequence after underfill cure for flip chip technology. For additional requirements for this test, see appendix B paragraph B.4.1 of MIL-PRF-38535.
- 22/ External visual inspection shall be performed on the lot any time after radiographic test and prior to shipment, and all shippable samples shall have external visual inspection at least subsequent to qualification or quality conformance inspection testing.
- 23/ The manufacturer shall inspect the devices 100 percent or on a sample basis using a quantity/accept number of 116(0). If one or more rejects occur in this sample, the manufacturer may double the sample size with no additional failures allowed or inspect the remaining devices 100 percent for the failed criteria and remove the failed devices from the lot. If the double sample also has one or more failures, the manufacturer shall be required to 100 percent inspect the remaining devices in the lot for the failed criteria. Re-inspection magnification shall be no less than that used for the original inspection for the failed criteria.
- 24/ Samples shall be randomly selected from the assembled inspection lot for testing in accordance with the specific device class and lot requirements of Group A, B, C, D, E and applicable appendices of MIL-PRF-38535 or TM 5005 of MIL-STD-883; after the specified screen requirements herein table IA or TM 5004 have been satisfactorily completed.
- 25/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible such as SOI, SOS and dielectrically isolated technology devices. If radiation dose rate induced latch-up screen test is required, it may be performed at any screening operation step after seal test, at the manufacturer's option. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test shall be in accordance with the device specification. The PDA for each inspection lot for class V or class Y (class level S) sublot submitted for radiation latch-up test shall be 5 percent or one device, whichever is greater.

TABLE II. Group B tests (Mechanical and environmental test)

Subgroups <u>1/</u>	Group B tests for QML Hermetic microcircuits (MIL-PRF-38535)		Group B tests for QML non-hermetic microcircuits (MIL-PRF-38535)		Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Class Q	Class V	Class Y	Class N	Class level B	Class level S
Subgroup 1	Resistance to solvents <u>2/</u> TM 2015 3(0)	Resistance to solvents <u>2/</u> TM 2015 3(0)	Resistance to solvents <u>2/</u> TM 2015 3(0)	Resistance to solvents <u>2/</u> TM 2015 3(0)		a. Physical dimensions <u>3/</u> TM 2016 2(0) b. Internal water vapor content TM 1018 3(0) or 5(1) <u>5/</u> (5,000 ppm maximum water content at 100°C) <u>3/ 4/</u>
Subgroup 2 <u>6/</u>	a. Bond strength <u>7/</u> TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Flip-chip – N/A (4) Beam lead - Test condition H For flip chip devices: b. Flip chip pull off test (test perform prior to underfill dispense) TM 2031 or TM 2011 2(0) c. Die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or 2027 3(0) d. Die shear test or substrate attach strength or stud pull test for passive elements TM 2019 or 2027 3(0)	a. Bond strength TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Flip-chip – N/A (4) Beam lead - Test condition H For flip chip devices: b. Flip chip pull off test (test perform prior to underfill dispense) TM 2031 2(0) c. Die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or 2027 3(0) d. Die shear test or substrate attach strength or stud pull test for passive elements TM 2019 or 2027 3(0)	a. Bond strength TM 2011 22(0) (1) Thermo compression Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H For flip chip devices: b. Flip chip pull off test (test perform prior to underfill dispense) TM 2031 2(0) c. Die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or 2027 3(0) d. Die shear test or substrate attach strength or stud pull test for passive elements TM 2019 or 2027 3(0)	a. Bond strength TM 2011 22(0) (1) Thermo compression Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H For flip chip devices: b. Flip chip pull off test (test perform prior to underfill dispense) TM 2031 2(0) c. Die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or 2027 3(0) d. Die shear test or substrate attach strength or stud pull test for passive elements TM 2019 or 2027 3(0)	Resistance to solvents <u>2/</u> TM 2015 3(0)	a. Resistance to solvents <u>2/</u> TM 2015 3(0) b. Internal visual and mechanical TM 2013, 2014 2(0) c. Bond strength TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Flip-chip – N/A (4) Beam lead - Test condition H For flip chip devices: d. Flip chip pull off test (test perform prior to underfill dispense) TM 2031 2(0) e. Die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or 2027 3(0) f. Die shear test or substrate attach strength or stud pull test for passive elements TM 2019 or 2027 3(0)

TABLE II. Group B tests (Mechanical and environmental test). – Continued.

Subgroups <u>1/</u>	Group B tests for QML Hermetic microcircuits (MIL-PRF-38535)		Group B tests for QML non-hermetic microcircuits (MIL-PRF-38535)		Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Class Q	Class V	Class Y	Class N	Class level B	Class level S
Subgroup 3 sample size <u>22</u> (0) (22 leads from 3 devices) <u>8/</u>	Solderability TM 2003 Solder temperature +245°C ±5°C	Solderability TM 2003 Solder temperature +245°C ±5°C	Solderability TM 2003 Solder temperature +245°C ±5°C	Solderability TM 2003 Solder temperature +245°C ±5°C	Solderability TM 2003 Solder temperature +245°C ±5°C	Solderability TM 2003 Solder temperature +245°C ±5°C
Subgroup 4 <u>3/</u>						a. Lead integrity <u>9/</u> TM 2004 (Test condition B2, lead fatigue) b. Seal test TM 1014, as applicable (1) Fine leak (2) Gross leak c. Lid torque <u>10/</u> TM 2024, as applicable d. For BGA/CGA devices: (i) For BGA package - JESD22-B117 <u>45</u> (0) (45 balls from 2 devices minimum) (ii) For CGA package - TM 2038 <u>45</u> (0) (45 columns from 2 devices minimum)
Subgroup 5					a. Bond strength <u>7/</u> TM 2011 <u>15</u> (0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Flip-chip – condition F (4) Beam lead - condition H	sample size <u>45</u> (0) a. End-point electrical parameters <u>11/</u> - As specified in the applicable device specification b. Steady state life test <u>12/</u> TM 1005 Test condition C, D and E c. End-point electrical parameters <u>11/</u> - As specified in the applicable device specification

TABLE II. Group B tests (Mechanical and environmental test). – Continued.

Subgroups <u>1/</u>	Group B tests for QML Hermetic microcircuits (MIL-PRF-38535)		Group B tests for QML non-hermetic microcircuits (MIL-PRF-38535)		Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Class Q	Class V	Class Y	Class N	Class level B	Class level S
Subgroup 6 Sample size 15(0) <u>13/</u>						a. Temperature cycling TM 1010, condition C, 100 cycles minimum b. Constant acceleration TM 2001, condition E, Y ₁ orientation only c. Seal test TM 1014 (1) Fine leak (2) Gross leak d. End-point electrical parameters - As specified in the applicable device specification
Subgroup 7 Electrostatic discharge (ESD) sensitivity test <u>14/</u>	TM 3015 3(0)	TM 3015 3(0)	TM 3015 3(0)		TM 3015 3(0)	TM 3015 3(0)

Note: The class N update requirement is not applicable for existing class N product. The existing class N product shall meet the requirements of table IB of MIL-PRF-38535.

TABLE II. Group B tests (Mechanical and environmental test) – Continued.

- 1/ Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electrical and provided the rejects are exposed to the full temperature/ time exposure of burn-in. Group B test shall be performed on each inspection lot as a condition for lot acceptance for delivery. Group B test shall be performed on each qualified package type and lead finish.
- 2/ Resistance to solvents testing required only on devices using inks or paints as a marking medium. For devices with solder terminations, Resistance to solvents test shall be performed with balls/columns.
- 3/ Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot. For devices with solder terminations, Physical dimension test shall be performed with balls/columns.
- 4/ This test is required only, if it is a glass-frit-sealed package. Unless handling precautions for beryllia packages are available and followed TM 1018, procedure 3 shall be used (see group D, subgroup 6 of table V). For class Y non-hermetic microcircuits devices Internal water vapor content test is not applicable.
- 5/ Test three devices; if one fail, test two additional devices with no failures. At the manufacturers option, if the initial test sample (e.g., 3 or 5 devices) fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot. If sample size (accept number) of 5(1) is used to pass the lot, the manufacturer shall evaluate their product to determine the reason for the failure and whether the lot is at risk.
- 6/ For flip chip packages, a bump shear test shall be performed in accordance with JEDEC JESD22-B117 to determine the shear strength of solder bumps. For solder termination devices, subgroup 2 test can be performed without balls and columns.
- 7/ Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in table IA herein or TM 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see TM 2011).
- 8/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number applies to the number of leads inspected except in no case shall less than 3 (three) devices be used to provide the number of leads required. For BGA/CGA packages, solderability test shall be verified after solder ball or solder column attachment processes per TM 2003. For CGA packages, solder temperature shall be maintained in accordance with table 1 of TM 2003.
- 9/ The sample size number of 45 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test and lid torque test, if applicable, (see 10/) in order to meet the requirements of subgroup 4. For pin grid array leads and rigid leads, use TM 2028. For leaded chip carrier packages, use condition B1. For leadless chip carrier packages only, use test condition D and a sample size number of 15 based on the number of pads tested taken from 3 devices minimum. Seal test (subgroup 4b) need to be performed only on packages having leads exiting through a glass seal. For LGA/BGA/CGA packages, TM 2004 does not apply.
- 10/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (e.g., wherever frit seal establishes hermeticity or package integrity). Device packages with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures for lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.
- 11/ Read and record group A subgroups 1, 2 and 3.
- 12/ The alternate removal-of-bias provisions of 3.3.1 of TM 1005 shall not apply for test temperature above 125°C.
- 13/ For devices with solder terminations, Temperature cycling and Constant acceleration test may be performed without balls/columns attachment.
- 14/ Electrostatic discharge (ESD) sensitivity test for initial qualification and redesign only. The requirements for ESD testing are specified in paragraph 4.2.3 and A.3.4.1.4 of appendix A of MIL-PRF-38535.

TABLE III. Group A (electrical tests). 1/

Subgroups	Tests	Hermetic microcircuits devices Minimum sample size quantity (accept no.) <u>2/ 3/ 4/ 5/</u> MIL-STD-883 test method and conditions		Non-hermetic microcircuits devices Minimum sample size quantity (accept no.) <u>2/ 3/ 4/ 5/</u> MIL-STD-883 test method and conditions	
		Class Q (class level B)	Class V <u>6/</u> (class level S)	Class Y <u>6/</u> (class level S)	Class N (High reliability)
1	Static tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
2	Static tests at maximum rated operating temperature				
3	Static tests at minimum rated operating temperature				
4	Dynamic tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
5	Dynamic tests at maximum rated operating temperature				
6	Dynamic tests at minimum rated operating temperature				
7	Functional tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
8A	Functional tests at maximum rated operating temperature				
8B	Functional tests at minimum rated operating temperature				
9	Switching tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
10	Switching tests at maximum rated operating temperature				
11	Switching tests at minimum rated operating temperature				

- 1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.
- 2/ At the manufacturer's option, the applicable tests required for group A testing (see 1/ herein) may be conducted individually or combined into sets of tests, subgroups (as defined in table III), or sets of subgroups. However, the manufacturer shall pre-designate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.
- 3/ The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as pre-designated in 2/ herein, shall be 116/0.
- 4/ A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For those lots having a quantity of less than 116 devices, the test shall be imposed on a 100 percent basis with zero failure.
- 5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For device class V or class Y (class level S), if the testing results in a percent defective allowable (PDA) greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.
- 6/ For class V and class Y, group A electrical tests additional requirements see paragraph B.4.3 appendix B of MIL-PRF-38535.

TABLE IV. Group C life tests.

Subgroup	Tests	Hermetic microcircuits devices Minimum sample size quantity (accept no. MIL-STD-883 test method and conditions		Non-hermetic microcircuits devices Minimum sample size quantity (accept no. MIL-STD-883 test method and conditions	
		Class Q (class level B) <u>1/</u>	Class V (class level S) <u>1/ 2/</u>	Class Y (class level S) <u>1/ 2/</u>	Class N (High reliability) <u>1/ 2/</u>
Subgroup 1	a. Steady-state life test	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C
	b. End-point electrical parameters	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification

1/ Life test may be performed on a quantity (accept) criteria of 22(0) for 2000 hours at 125°C or equivalent per TM 1005 to attain 44,000 device hours. For lots greater than 200, actual devices shall be used. For lots less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22 unless acceptable group C data from the same lot of SEC is available for the previous 3 months. The SEC shall have been produced under equivalent conditions as the production lot and as close in time as feasible, but not to exceed a 3-months period.

2/ Group C life tests shall be performed on the initial production lot of actual devices from each wafer lot, in accordance with [table IV herein](#). Group C life tests are not required to be performed on subsequent production lots when all the following conditions are met:

- (a) Subsequent production lots utilize die from the same wafer lot as the initial production lot.
- (b) Wafers or die remaining from the initial production lot are to be stored in dry nitrogen or equivalent controlled storage, and in covered containers.
- (c) No major changes to the assembly processes have occurred since the group C test was performed on the wafer lot.

Note: For ASICs, a sample size of 5 actual devices may be used with the balance being made up of the SEC.

TABLE V. Group D tests (Package related test).

Subgroups test	Tests <u>1/</u>	Hermetic microcircuits device MIL-STD-883 test method and conditions		Non-hermetic microcircuits device MIL-STD-883 test method and conditions	
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)	Class N (High reliability)
Subgroup 1 sample size 15(0) <u>2/</u>	Physical dimensions	TM 2016	TM 2016	TM 2016	TM 2016
Subgroup 2 sample size 45(0) <u>2/ 3/</u>	a. Lead/terminal integrity b. Seal <u>4/</u> (1) Fine leak (2) Gross leak 1. c. For BGA/CGA packages (i) Ball shear test for BGA package (ii) Solder column pull test for CGA package	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style b. TM 1014 Test condition as applicable c. For BGA/CGA packages (i) For BGA package - JESD22-B117 45(0) (45 balls from 2 devices minimum) (ii) For CGA package - TM 2038 45(0) (45 columns from 2 devices minimum)	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style b. TM 1014 Test condition as applicable c. For BGA/CGA packages (i) For BGA package - JESD22-B117 45(0) (45 balls from 2 devices minimum) (ii) For CGA package - TM 2038 45(0) (45 columns from 2 devices minimum)	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style b. <u>5/</u> c. For BGA/CGA packages (i) For BGA package - JESD22-B117 45(0) (45 balls from 2 devices minimum) (ii) For CGA package - TM 2038 45(0) (45 columns from 2 devices minimum)	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style b. <u>5/</u> c. For BGA/CGA packages (i) For BGA package - JESD22-B117 45(0) (45 balls from 2 devices minimum) (ii) For CGA package - TM 2038 45(0) (45 columns from 2 devices minimum)
Subgroup 3 sample size 15(0) <u>6/ 7/</u>	a. Thermal shock b. Temperature cycling c. Moisture resistance d. Visual examination e. Seal <u>9/</u> (1) Fine leak (2) Gross leak f. End-point electrical parameters <u>10/</u>	a. TM 1011 Test condition B, 15 cycles minimum b. TM 1010 Test condition C, 100 cycles minimum c. TM 1004 <u>8/</u> d. In accordance with visual criteria of TM 1004 or TM 1010 e. TM 1014 test condition as applicable f. As specified in the applicable device	a. TM 1011 Test condition B, 15 cycles minimum b. TM 1010 Test condition C, 100 cycles minimum c. TM 1004 <u>8/</u> d. In accordance with visual criteria of TM 1004 or TM 1010 e. TM 1014 test condition as applicable f. As specified in the applicable device	a. TM 1011 Test condition B, 15 cycles minimum b. TM 1010 Test condition C, 100 cycles minimum c. HAST in accordance with JESD22-A118, condition B d. In accordance with visual criteria of TM 1004 or TM 1010 e. <u>5/</u> f. As specified in the applicable device	a. TM 1011 Test condition B, 15 cycles minimum b. TM 1010 Test condition C, 100 cycles minimum c. HAST in accordance with JESD22-A118, condition B d. In accordance with visual criteria of TM 1004 or TM 1010 e. <u>5/</u> f. As specified in the applicable device

TABLE V. Group D tests (Package related test). - Continued.

Subgroups	Test 1/	Hermetic microcircuits device MIL-STD-883 test method and conditions		Non-hermetic microcircuits device MIL-STD-883 test method and conditions	
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)	Class N (High reliability)
Subgroup 4 sample size 15(0) <u>6/ 7/</u>	a. Mechanical shock b. Vibration, variable frequency c. Constant acceleration <u>11/</u> d. Seal (1) Fine leak (2) Gross leak e. Visual examination f. End-point electrical parameters	a. TM 2002 condition B minimum b. TM 2007 condition A minimum c. TM 2001 Test condition E, Y1 orientation only d. TM 1014 condition as applicable e. In accordance with visual criteria of TM 2007 f. As specified in the applicable device specification	a. TM 2002 condition B minimum b. TM 2007 condition A minimum c. TM 2001 Test condition E, Y1 orientation only d. TM 1014 condition as applicable e. In accordance with visual criteria of TM 2007 f. As specified in the applicable device specification	a. TM 2002 condition B minimum b. TM 2007 condition A minimum c. TM 2001 Test condition E, Y1 orientation only d. <u>5/</u> e. In accordance with visual criteria of TM 2007 f. As specified in the applicable device specification	
Subgroup 5 sample size 15(0) <u>2/</u>	a. Salt atmosphere b. Visual examination c. Seal <u>9/</u> (1) Fine leak (2) Gross leak	a. TM 1009 Test condition A minimum b. In accordance with visual criteria of TM 1009 c. TM 1014 condition as applicable	a. TM 1009 Test condition A minimum b. In accordance with visual criteria of TM 1009 c. TM 1014 condition as applicable	a. TM 1009 Test condition A minimum b. In accordance with visual criteria of TM 1009 c. <u>5/</u>	a. TM 1009 Test condition A minimum b. In accordance with visual criteria of TM 1009 c. <u>5/</u>
Subgroup 6 <u>2/ 12/</u>	Internal water vapor test (cavity packages)	TM 1018 3(0) or 5(1) 5,000 ppm maximum water content at 100°C	TM 1018 3(0) or 5(1) 5,000 ppm maximum water content at 100°C	<u>5/</u>	<u>5/</u>
Subgroup 7 sample size 15(0) <u>2/ 13/ 14/</u>	Adhesion of lead finish	Where applicable TM 2025	Where applicable TM 2025	Where applicable TM 2025	Where applicable TM 2025

TABLE V. Group D tests (Package related test). - Continued.

Subgroups	Test 1/	Hermetic microcircuits device MIL-STD-883 test method and conditions		Non-hermetic microcircuits device MIL-STD-883 test method and conditions	
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)	Class N (High reliability)
Subgroup 8 sample size 5(0) 2/	Lid torque 15/	Where applicable TM 2024	Where applicable TM 2024	Where applicable TM 2024	Where applicable TM 2024
Subgroup 9 sample size 3(0) (3 leads minimum) 16/	a. Soldering heat b. Seal (1) Fine leak (2) Gross leak c. External Visual examination d. End-point electrical	Where applicable a. TM 2036 b. TM 1014 condition as applicable c. TM 2009 d. As specified in the applicable device specification	Where applicable a. TM 2036 b. TM 1014 condition as applicable c. TM 2009 d. As specified in the applicable device specification	Where applicable a. TM 2036 b. 5/ c. TM 2009 d. As specified in the applicable device specification	Where applicable a. TM 2036 b. 5/ c. TM 2009 d. As specified in the applicable device specification

Note: The class N update requirement is not applicable for existing class N product. The existing class N product shall meet the requirements of table IB of MIL-PRF-38535.

- 1/ In-line monitor data may be substituted for subgroups D1, D2, D6, D7, and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. The in-line monitor data shall be traceable to the specific inspection lot(s) represented (accepted or rejected) by the data.
- 2/ Electrical reject devices from that same inspection lot may be used for samples. For devices with solder terminations, subgroups 1, 2, 5, 6 (only hermetic devices) and 8 tests shall be performed with balls and columns.
- 3/ The sample size number of 45, C = 0 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test if applicable (see 4/) in order to meet the requirements of subgroup 2. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads, use TM 2028. For leadless chip carrier packages only, use test condition D and a sample size number of 15 (C = 0) based on the number of pads tested taken from 3 devices minimum. For LGA/BGA/CGA packages, TM 2004 does not apply.
- 4/ Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.
- 5/ This test is not applicable for class Y non-hermetic microcircuits devices.
- 6/ Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".

TABLE V. Group D tests (Package related test). - Continued.

- 7/ For devices with solder terminations, subgroups 3 and 4 tests may be performed without balls and columns.
- 8/ Lead bend stress initial conditioning is not required for leadless chip carrier packages or BGA/CGA packages. For fine pitch packages (≤ 25 mil pitch) using a nonconductive tie bar, preconditioning shall be required on 3 devices only prior to the moisture resistance test with no subsequent electrical test required on these 3 devices. The remaining 12 devices from the sample of 15 devices do not require preconditioning but shall be subjected to the required endpoint electrical tests.
- 9/ After completion of the required visual examinations and prior to submittal to TM 1014 seal tests, the devices may have the corrosion by-products removed by using a bristle brush.
- 10/ At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.
- 11/ For flip chip packages Constant acceleration test is not required.
- 12/ Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (e.g., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with 5 additional devices from the same lot. If sample size (accept number) of 5(1) is used to pass the lot, the manufacturer shall evaluate his product to determine the reason for the failure and whether the lot is at risk.
- 13/ The adhesion of lead finish test shall not apply for leadless chip carrier, land grid array (LGA), ball grid array (BGA), and column grid array (CGA) packages.
- 14/ Sample size number 15 leads from 3 devices minimum are based on number of leads with zero failure.
- 15/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (e.g., wherever frit seal establishes hermeticity or package integrity). Device packages with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures for lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.
- 16/ This test is performed at qualification/re-qualification of design changes which may affect this test. The manufacturer shall determine, for each package, the applicable conditions from TM 2036 that are appropriate for the mounting conditions, and assure by testing, or through their assembly processes, that the part is subjected to an equivalent time/temperature stress.

TABLE C-I. Group E (RHA) TCI/QCI test for class Q, class V and class N and class Y.

Subgroups	Tests <u>1/</u> <u>2/</u>	Hermetic microcircuits device MIL-STD-883 test method and conditions		Non-hermetic microcircuits device MIL-STD-883 test method and conditions	
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)	Class N (High reliability)
Subgroup 1 <u>3/</u> <u>4/</u>	Neutron irradiation test (Displacement Damage test) a. Qualification test and QCI/TCI test c. Endpoint electrical parameters test	a. TM 1017 at 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/inspection lot <u>5/</u> b. As specified in accordance with device specification	a. TM 1017 at 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/inspection lot <u>5/</u> b. As specified in accordance with device specification	a. TM 1017 at 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/inspection lot <u>5/</u> b. As specified in accordance with device specification	a. TM 1017 at 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/inspection lot <u>5/</u> b. As specified in accordance with device specification
Subgroup 2 <u>3/</u> <u>7/</u> <u>9/</u> <u>10/</u>	Total ionization dose (TID) a. Qualification test and QCI/TCI test b. Endpoint electrical parameters test	a. TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot <u>8/</u> b. As specified in accordance with device specification	a. TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot <u>8/</u> or 1(0) devices/wafer + 4(0) SEC or test structures/wafer or 5(0) devices/wafer lot + 4(0) SEC or test structures/wafer b. As specified in accordance with device specification	a. TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot <u>8/</u> or 1(0) devices/wafer + 4(0) SEC or test structures/wafer or 5(0) devices/wafer lot + 4(0) SEC or test structures/wafer b. As specified in accordance with device specification c. As specified in accordance with device specification	a. TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot <u>8/</u> b. As specified in accordance with device specification

TABLE C-I. Group E (RHA) TCI/QCI test for class Q, class V and class N and Y. –continued.

Subgroups	Tests <u>1/</u> <u>2/</u>	Hermetic microcircuits device MIL-STD-883 test method and conditions		Non-hermetic microcircuits device MIL-STD-883 test method and conditions	
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)	Class N (High reliability)
Subgroup 3 <u>11/</u>	a. Dose rate upset test (Transient irradiation test) b. End point electrical parameters test	a. For Digital TM 1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0) devices/inspection lot <u>5/</u> b. As specified in accordance with device specification	a. For Digital TM1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0) devices/wafer lot <u>6/</u> b. As specified in accordance with device specification	a. For Digital TM1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0) devices/wafer lot <u>6/</u> b. As specified in accordance with device specification	
Subgroup 4 <u>12/</u>	Radiation dose rate induced latch-up test	TM 1020 As specified in the device specification	TM 1020 As specified in the device specification	TM 1020 As specified in the device specification	
Subgroup 5 <u>13/</u>	Single event effects (SEE) test		ASTM F-1192 or JESD57 4(0) devices or As specified in the device specification	ASTM F-1192 or JESD57 4(0) devices or As specified in the device specification	ASTM F-1192 or JESD57 4(0) devices or As specified in the device specification

Note: The class N update requirement is not applicable for existing class N product. The existing class N product shall meet the requirements of table IB of MIL-PRF-38535.

- 1/ Group E tests may be performed prior to device screening. Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. End point electrical parameters as specified in accordance with device specification.
- 2/ For devices with solder terminations, group E subgroups test may be performed without balls and columns.
- 3/ The radiation hardness assurance capability level (RHACL)/radiation assurance in the SPEC level is the ratio of the capability level to the specification level of devices fluence. Subgroups shall be invoked when the radiation hardness assurance capability level (RHACL) specification requirements of > 10 are not met. For an example, if RHACL/SPEC ratio is > 10 then this test may not be required, but if the RHACL/SPEC ratio falls within > 1 and ≤ 10 then the subgroup test is required.
- 4/ This test is to be conducted only when specified in the purchase order or contract. Neutron irradiation test (Displacement damage test) is not required for MOS devices unless bipolar elements are included by design.

TABLE C-I. Group E (RHA) TCI/QCI test for class Q, class V and class N and Y. –continued.

- 5/ In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
- 6/ In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
- 7/ Parts used for one subgroup test may not be used for other subgroups, but may be used for higher levels in the same subgroup. For subgroup 2, total dose exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.
- 8/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).
- 9/ Traceability to the specific wafer is required.
- 10/ In accordance with wafer for device types with greater than or equal to 4,000 equivalent transistors/chip selected from the wafer. The manufacturer shall define and document sampling procedures. The test structures shall be randomly selected from the wafer. An X-ray source may be used on test structures at the wafer level provided correlation has been established between the X-ray and the Cobalt-60 source and shall be documented in the QM plan.
- 11/ Radiation dose rate upset (Transient irradiation test) test shall be conducted during qualification on first QCI when specified in purchase order or contract.
- 12/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible such as SOI, SOS and dielectrically isolated technology devices. If radiation dose rate induced latch-up screen test is required, shall be performed screening operation after seal. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test in accordance with the specified device specification. The PDA for each inspection lot for class V or class Y (class level S) devices subplot, screened, shall be 5 percent or one device, whichever is greater.
- 13/ When single event effects (SEE) testing is specified in the purchase order or contract, the SEE test shall be performed during initial qualification and after any design or process change that may affect SEE response. Destructive SEE (SEB and SEGR) testing shall be performed accordance with JEDEC JESD57.

APPENDIX H - CERTIFICATION, VALIDATION, AND QUALIFICATION

H.1 SCOPE

H.1.1 Scope. The qualified manufacturers listing (QML) program applies quantifiable measurement techniques that evaluate a manufacturer's ability to define and follow a baseline of its process. This baseline can include innovative and improved processes that result in an equivalent or higher quality product, provided that the methods used to evaluate and document these changes have been reviewed and approved. Once QML status is achieved, the manufacturer's Technical Review Board (TRB) may approve change(s) to the process baseline based on appropriate reliability and quality data upon concurrence with notification of the Qualifying Activity (QA). The approach outlined in this appendix contains a proven baseline that includes details of the certification, validation, and qualification programs. The necessary characterization, screening, and qualification testing applicable to new technologies is also included. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. However, for QML microcircuits the manufacturers may offer approved alternatives that demonstrate a system that achieves at least the same level of quality and reliability as could be achieved by this appendix.

H.2 APPLICABLE DOCUMENTS

H.2.1 General. The documents listed in this section are specified in section H.3. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in section H.3 whether or not they are listed.

H.2.2 Government documents.

H.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-M-38510](#) - Microcircuits, General Specification For.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-883](#) - Test Method Standard Microcircuits.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>)

H.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

SAE International

[EIA557](#) - Statistical Process Control Systems.

(Copies of these documents are available online at <http://www.sae.org/> or from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- | | |
|-----------------------------|--|
| JEP121 | - Requirements for Microelectronic Screening and Test Optimization. |
| JEP163 | - Selection of Burn-in/Life Test Conditions and Critical Parameters for QML Microcircuits. |
| JESD31 | - General Requirements for Distributors of Commercial and Military Semiconductor Devices. |
| JESD78 | - IC Latch-up Test. |
| JESD471 | - Symbol & Label for Electrostatic Sensitive Devices. |
| JESD625 | - Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices. |
| JESD22-B101 | - External Visual. |
| JESD22-A102 | - Accelerated Moisture Resistance - Unbiased Autoclave. |
| JESD22-A104 | - Temperature Cycling. |
| JESD22-A106 | - Thermal Shock. |
| JESD22-A110 | - Highly Accelerated Temperature and Humidity Stress Test (HAST) – biased. |
| JESD22-B117 | - Solder Ball Shear test. |

(Copies of these documents are available online at <http://www.jedec.org/> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

ANSI/ESDA/JEDEC JOINT STANDARD

[ANSI/ESDA/JEDEC JS-001](#) - For Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) – Component Level.

[ANSI/ESDA/JEDEC JS-002](#) - For Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level.

(Copies of these documents are available online at <http://www.jedec.org/> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.) or

(Copies of these documents are available online at <http://www.esda.org/> or from Electrostatic Discharge Association(ESDA)
7900 Turin Road, Bldg. 3, Rome, NY 13440.)

ASTM INTERNATIONAL (ASTM)

- [ASTM D2863](#) - Standard Test Method for Measuring the Minimum Oxygen Concentration to Support Candle-Like Combustion of Plastics (Oxygen Index).
- [ASTM F1269](#) - Test methods for Destructive Shear Testing of Ball Bonds.
- [ASTM G21](#) - Standard Practice for Determining Resistance of Synthetic Polymeric Materials to Fungi.

(Copies of these documents are available online at <http://www.astm.org/> or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

UNDERWRITERSLABORATORIES INC. (UL)

- [UL 94](#) - Tests for Flammability of Plastic Materials for Parts in Devices and Appliances.

(Copies of this document are available online at <http://www.ul.com/> or from Underwriters Laboratories Inc. (UL), 333 Pfingsten Road, Northbrook, IL 60062-2096.)

H.2.4 **Order of precedence.** Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

H.3 REQUIREMENTS

H.3.1 General. The qualifying activity (QA) shall evaluate the manufacturer's approach to the process baseline. The manufacturer shall have a quality management (QM) plan specifying the characterization, certification, and qualification plans of technologies and product (see appendix G). New technologies shall also be included and have a checklist defining the necessary requirements for calculation/evaluation of failure mechanism, activation energy, characterization plan, qualification plan and validation. The QM plan shall be submitted to the QA for approval (see G.3.3.1s). For class level S product, the manufacturer shall evaluate the changes listed in [table A-I](#) in conjunction with the QA to determine if a change should be classified as a new technology.

H.3.1.1. Characterization requirements. Testing performed with the intent to understand the technology part, materials, and processes used to determine an item's capability. The manufacturer should evaluate their process to determine the long term reliability of the product. For class level S product, a detailed characterization plan identifying critical parameters, test conditions, durations, required measurements, sample size, and temperatures shall be documented, including a detailed physics-of-failure analysis considering mechanical, thermal, electrical, and chemical properties that could contribute to failures. A failure modes effects analysis (FMEA) approach must be followed to ensure to the maximum extent possible that all significant failure mechanisms have been defined and appropriate mitigation techniques have been identified.

H.3.1.2 Certification. Validation, by the QA, that the manufacturer has the capability of producing product which meets or exceeds the requirements contained in this specification. The manufacturer shall document the certification plan as documented in their QM plan. The qualifying activity shall be notified if deviations or exception are taken from the approved plan.

H.3.1.3 Validation. Verification by the QA that the manufacturer has met or exceeded the requirements utilizing data, demonstration, other approved techniques, or a combination thereof.

H.3.1.4 Transitional certification. Temporary certification (approximately 2 years maximum) given by the QA to manufacturers working toward full QML certification (see [H.3.3](#)).

H.3.1.5 Qualification requirements. Evidence that the characterization testing and evaluations of failure mechanisms show the technology meets or exceeds documented requirements. The qualification methodology will vary depending upon the technology. The manufacturer shall document the qualification plan that is applicable to each technology. The qualification testing for new technologies shall consist of standard military test methods as outlined in MIL-PRF-38535, MIL-STD-883, or the QM plan as approved by the QA, including any tests deemed necessary by the characterization and physics-of-failure analysis.

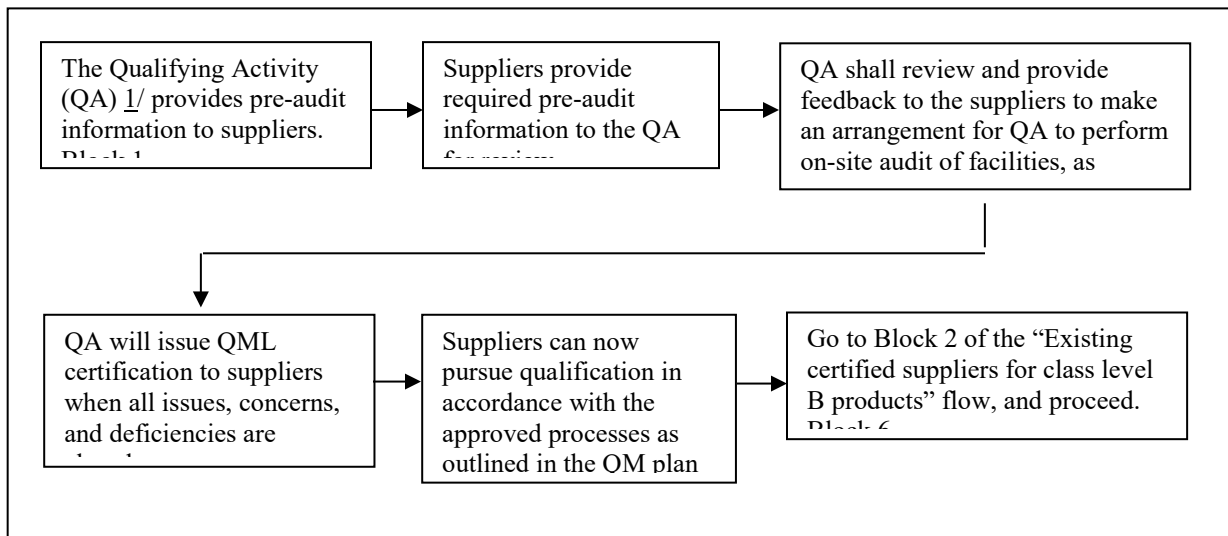
H.3.1.6 New technology requirements. For class level B product, this is a product family, material, or process, that has never been previously characterized and qualified by the manufacturer, and is detailed in the manufacturer's new technology insertion program (see [3.4.1.1.1](#) and [6.4.43](#)).

For class V and class Y (class level S), this is a product family, material, or process, that has never been previously characterized and qualified by the manufacturer for space applications, and is detailed in the manufacturer's new technology insertion program (see [3.4.1.1.1](#), [6.4.43](#) and [B.3.9](#)).

H.3.1.7 Mature technology requirements. A mature technology is one which the manufacturer has previously released to production the techniques, materials, controls, design, and has a continuous reliability monitor plan in place to identify major reliability life-limiting mechanisms and their associated acceleration factors establish activation energy, detect long-term product shifts, and generate process data or established proof of stable process and/or equipment with negligible wear out (see [6.4.44](#)).

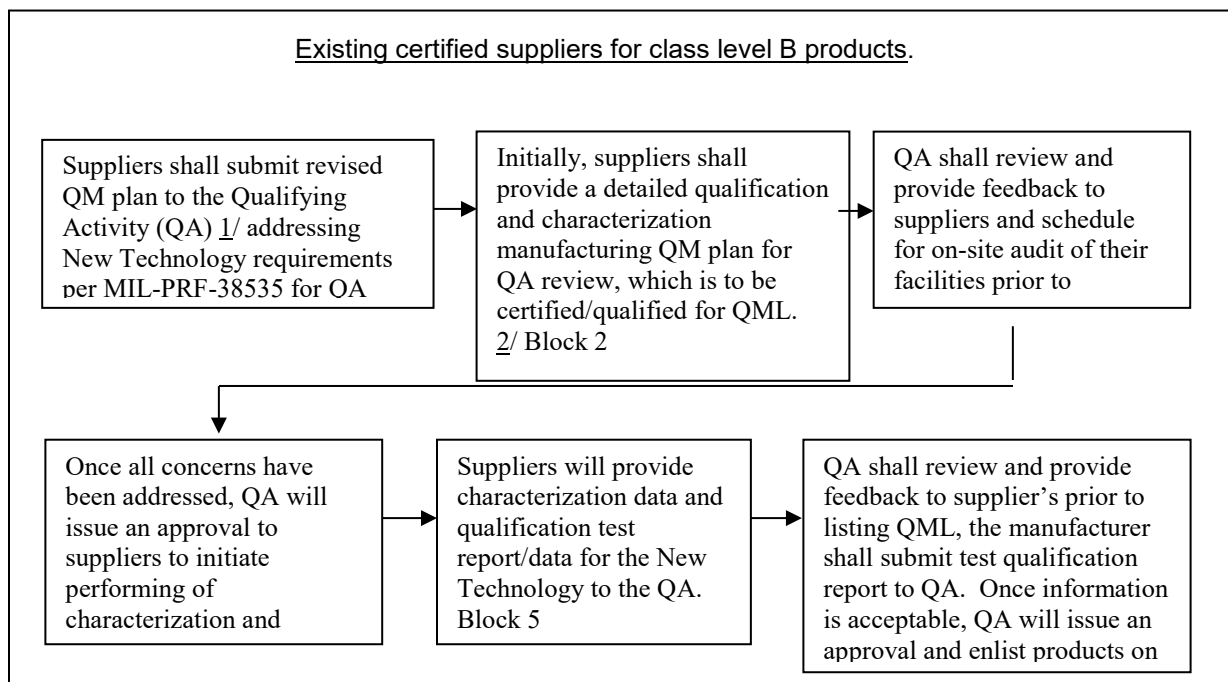
H.3.1.8 General QML process flows. The general QML process flows for new suppliers, and existing certified suppliers, providing class level B products is shown in [figure H-1](#), and for new suppliers, and existing certified suppliers, providing class level S products is shown in [figure H-2](#).

New suppliers for class level B products.



1/ The QA is the DLA Land and Maritime, Columbus.

Existing certified suppliers for class level B products.

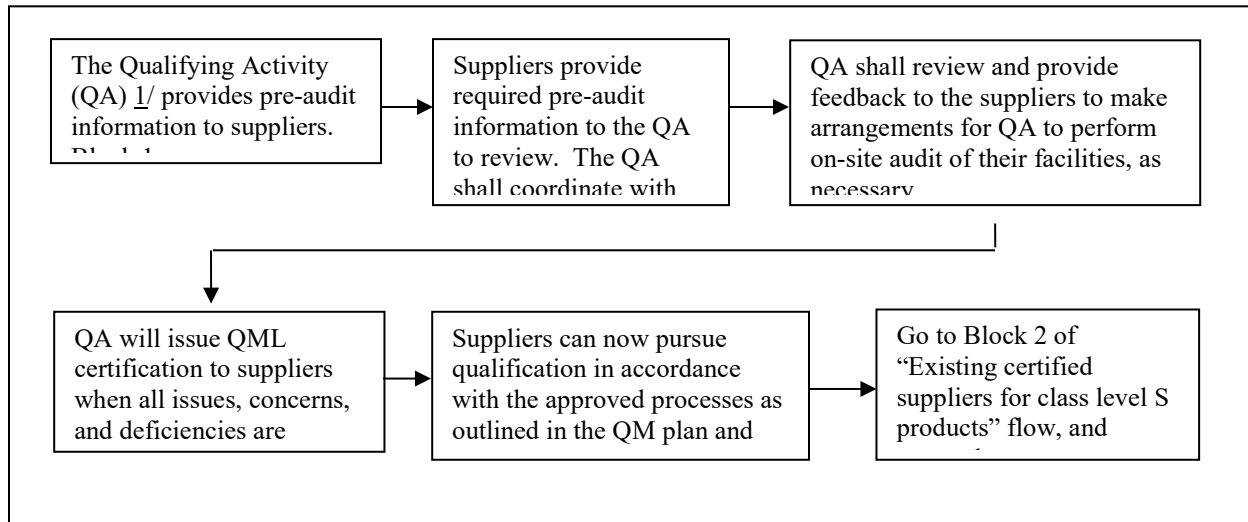


1/ The QA is the DLA Land and Maritime, Columbus.

2/ Any deviation from a previously QA approved plan for new technology shall require again QA approval prior to listing on QML.

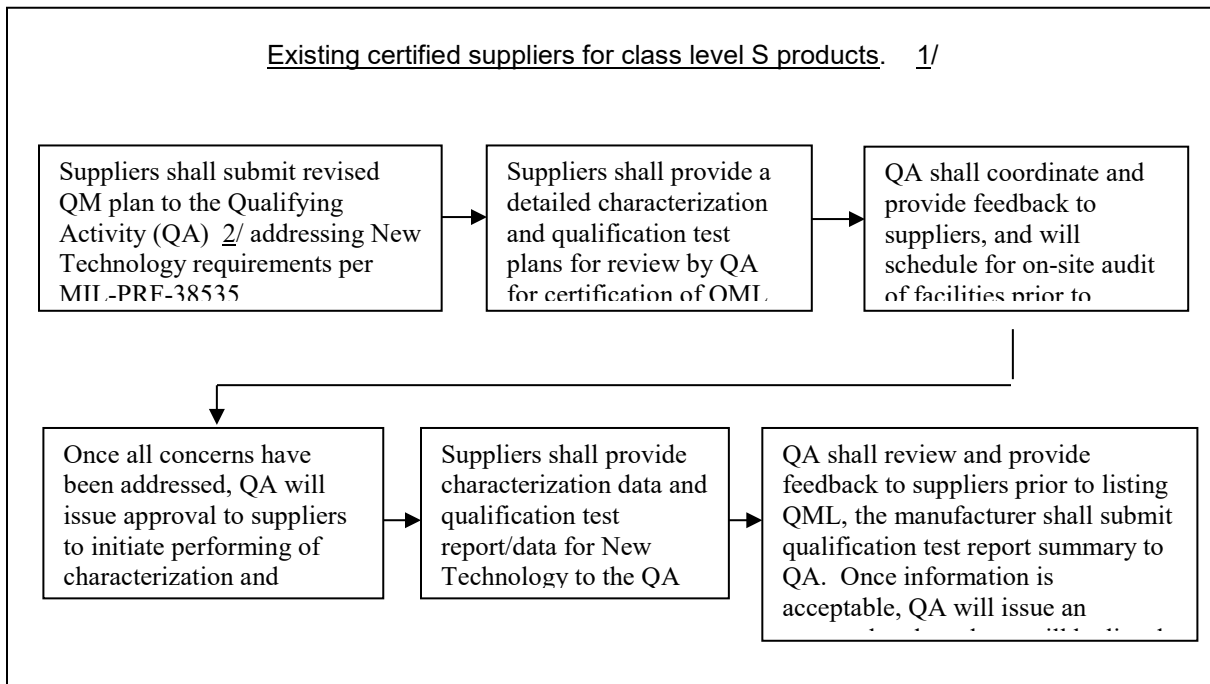
FIGURE H-1. Class level B QML process flows

New suppliers for class level S products.



1/ The QA is the DLA Land and Maritime, Columbus.

Existing certified suppliers for class level S products. 1/



1/ Each block requires coordination with the space community and approval by the QA.

2/ The QA is the DLA Land and Maritime, Columbus.

3/ Any deviation from a previously QA approved plan for new technology shall require again QA approval prior to listing on QML.

FIGURE H-2. Class level S QML process flows.

H.3.1.9 Overview of QML Approval Process. The process for achieving QML approval is outlined below in six basic stages and is further described in detail in the subsequent sections. The stages are listed in the normal sequence to be accomplished; however, several stages may occur concurrently.

- a) Design, wafer fabrication, assembly, and test certification;
 - 1) Design methodologies:
 - i) Reliability and radiation hardness assurance (RHA) design rules.
 - 2) Wafer fabrication/foundry processes:
 - i) SPC controls
 - ii) Metallization controls
 - iii) Reliability monitors
 - 3) Assembly processes
 - 4) Screening and Test Methodologies
 - 5) Audit/approval
- b) Physics-of-failure/TCV reliability assessment;
 - 1) Plan approval
 - i) Electromigration (EM)
 - ii) Time dependent dielectric breakdown (TDDB)
 - iii) Hot carrier injection (HCI)
 - iv) Threshold voltage instability, including Negative Bias Temperature Instability (NBTI) for 130 nm and smaller CMOS technologies.
 - v) Metallization stability over life.
 - vi) Others as applicable
 - 2) Report approval
- c) Process technology validation/SEC qualification;**
 - 1) Plan approval
 - i) Screening flow
 - ii) Process performance characterizations
 - iii) Process qualification tests
 - iv) For class N and class level B products, life test on a minimum of 1 wafer lot for 1000 hrs minimum at 125°C ambient, or equivalent.**
 - v) For class level S products, long term life test shall meet the requirements of paragraph B.3.4, appendix B, or shall meet long term life test on a minimum of 1 wafer lot for 4,000 hours minimum at 125°C ambient, or equivalent.
 - 2) Report approval
- d) Product qualification (From existing qualified process technology)
 - 1) Plan approval
 - i) Screening flow
 - ii) Product performance characterizations
 - iii) Product qualification tests
 - iv) 1,000 hour life test or equivalent
 - 2) Report approval

- e) Standard Microcircuit Drawing (SMD)
 - 1) Draft development
 - 2) User coordination
 - 3) SMD release
- f) QML listing of approved parts.

H.3.1.10 Manufacturer's Responsibility. It is the manufacturer's responsibility to ensure all of the defined systems and controls are fully implemented and operational as defined in this specification, appendices, and applicable standards and specifications. The manufacturer shall provide a focal point representative for the coordination and communication of QML program.

H.3.1.11 Qualifying Activity (QA) Responsibility. The QA is responsible for the coordination between the government agencies in the performance of quality audits and report approvals. The QA shall consolidate concerns and observations from the various agencies to provide a jointly agreed to position to provide to the manufacturer in addressing audit deficiencies and in meeting the specified requirements.

Any request for data, additional testing, or new manufacturing requirements, for a QML manufacturer, that were not part of the QA approved certification, qualification test plan, or DLA Land and Maritime audit results, must be provided to and approved by the QA. Supporting data for the request shall also be provided to the QA. Upon approval by the QA, the QA shall submit the request or requirement to the QML manufacturer. The QA shall arrange any necessary conference calls or site visits with the QML manufacturer.

H.3.2 Certification.

H.3.2.1 Design, Wafer Fabrication, Assembly, and Test Certification. The QA shall perform certification validation of the Design, Wafer Fabrication, Assembly, and Test capabilities of the manufacturer. The QA validation shall include analysis of data, and demonstration of the manufacturer's capability, to meet the requirements for certification in the following areas:

H.3.2.1.1 Design. The manufacturer should address the design methodology for the following areas of design.

NOTE: These are also applicable to third party design centers.

H.3.2.1.1.1 Circuit design. QML microcircuits should address the circuit design requirements and performance characteristics herein:

- a. Model verification. Provide evidence that all models utilized in the design process are functional, predictable, and accurate over the worst case temperature and electrical extremes. Examples of these models are electrical (transistor, passives, interconnect, package), behavioral, logic, fault, timing, signal integrity, power estimation and thermal conductivity.
- b. Layout verification. Demonstrate the capability of the automated or manual procedures routinely used for design, electrical, and reliability rule checking to catch all known errors, singularly and in combination. These rules cover, as a minimum:
 - (1) Design rules check (DRC): Geometric and physical.
 - (2) Electrical rules check (ERC): Shorts and open, connectivity.
 - (3) Reliability rules: Electromigration and current density, IR drops, latch-up, single event upset (SEU), hot carrier injection (HCI), electrostatic discharge (ESD), burnout backgating (for gallium arsenide (GaAs) technology).
- c. Performance verification. The manufacturer should design and construct a chip or set of chips to assess the process capability to perform routing and to accurately predict post-routing performance. The manufacturer should demonstrate that the actual measured performance for each function over temperature and voltage falls between the two worst case performance limits or is covered by statistical models. All critical minimum geometric and electrical design rules should be stressed via devices or structures located on the SEC, TCV, or PMs. The electrical stress requirements for the transistors, passive devices and interconnects on these structures should be determined by worst case circuit conditions. Failure analysis (FA) should be conducted to identify the failure mechanisms occurring in any failed devices and/or structures. Corrections to the design or to the verification/screening method shall be undertaken to mitigate any future occurrences of failures. These changes shall be presented to the QA prior to implementation if part of a new technology test plan. It is allowed that the manufacturer may choose actual product for their TCV or SEC. The manufacturer shall demonstrate burn-in circuits and life test conditions through characterization efforts to ensure proper operation at the device specified frequency.
- d. Testability and fault coverage verification. The manufacturer should demonstrate a design style and a design-for-test (DFT) methodology that, in conjunction with demonstrated CAD for test tools, can provide 99 percent or greater fault coverage on a design of reasonable complexity. The manufacturer should also address their approach for a testability bus to groups such as the Joint Test Action Group (JTAG). The manufacturer should demonstrate the fault coverage measurement (fault simulation, test algorithm analysis, etc.) capability that is used to provide fault coverage statistics of the design using the demonstrated design style, DFT method and CAD for test tools. Measurement of fault coverage should be in accordance with the procedures defined in TM 5012 of MIL-STD-883. For non-digital microcircuits, the fault coverage requirement may not be applicable, but should be supplemented as measures of analog fault coverage become better defined. For microcircuits with both analog and digital functions, this requirement fully applies to the digital portions of the microcircuits.

H.3.2.1.1.2 Design checklist (Class level S) . The following items shall be used as minimum requirements, as applicable for the technology, for the manufacturer and QA in evaluating the new technology for class level S product:

a. Design environment/infrastructure.

- (1) Project schedule.
- (2) Resource management (e.g., designers, hardware, software development).
- (3) Historical factors (e.g., any pertinent information based on previous designs, design rules, lessons learned, etc.).
- (4) Tools and design flow.
- (5) ASIC cell library and design kit.
- (6) Intellectual property (IP, e.g., any pertinent information such as use of 3rd party licensed IP, IP developed by another entity or manufacturer, etc.).
- (7) Models (for those developing their own cell libraries, and ASIC design kits), for analog/signal integrity simulations, and power calculations.

b. Detailed design hardware description language (HDL) coding (first phase of design).

- (1) Specification development guidelines (e.g., what design information must be included in the specification).
- (2) HDL coding guidelines.
- (3) Design for test (DFT) insertion and fault testing.
- (4) Built-in self test (BIST).

c. Validation/verification of modules and top level design.

- (1) Fault coverage percentage.
- (2) Emulation/prototyping.
- (3) Radiation effects mitigation.

d. Synthesis, static timing.

- (1) Foundry synthesis guidelines – Handoff to design team
- (2) Formulation of constraints from specification/requirements.
- (3) Synthesis and statically timed net list – Correlated with original HDL.

e. Physical design.

- (1) Foundry physical design guidelines – Handoff to design team
- (2) Placement based on partitioning, architecture, I/O location.
- (3) Static timing analysis, with iterated placement, cell sizing and routing to achieve timing closure.

f. Release to foundry.

- (1) Foundry run rule checks
- (2) Critical design/final design review, utilizing foundry checklists.

H.3.2.1.1.3 Package Design. Packages used for QML microcircuits should address the design requirements and performance characteristics herein. Characterization may be performed by the microcircuit manufacturer, by an external lab, or by the package supplier. In any case, the manufacturer's assembly of QML microcircuits should address all the testing requirements herein. The manufacturer shall address package design/construction quality and reliability. The manufacturer is responsible to maintain documented validation of all characterization methods used, including all supporting data.

- a. Thermal characterization. The thermal resistance should be determined for all packages used in the manufacture of QML parts. This value may be obtained by direct or indirect measurements, or by simulation tools or calculations. TM 1012 of MIL-STD-883 may be used for this calculation. If the thermal resistance is obtained by a calculation or simulation tool, this procedure should be certified. To certify such a method of theoretical estimation, the manufacturer shall demonstrate a correlation between the theoretically estimated value and the actual measured value for at least one package of the same style with equal or greater pin count.
- b. Electrical characterization. The following electrical characterization parameters should be addressed:
 - (1) Ground and power supply impedance. Packages used in the manufacture of QML microcircuits should be minimal contributors to ground and power supply noise. The above requirement can be met either through the use of documented package design rules or through testing of the packages, either individually or by similarity, in accordance with TM 3019 of MIL-STD-883.
 - (2) Cross-coupling effects. Cross-coupling of wideband digital signals and noise between pins in packages used for digital QML microcircuits should be minimized. The above requirement can be met either through the use of documented package design rules or through testing the packages, either individually or by similarity, in accordance with TM 3017 and TM 3018 of MIL-STD-883.
 - (3) High voltage effects. The voltage applied to a QML package should not produce a surface or bulk leakage between adjacent package conductors (including leads or terminals). The above requirement can be met either through the use of documented high voltage package design rules aimed at minimizing bulk or surface leakage, or through testing of the high voltage packages, either individually or by similarity, in accordance with TM 1003 of MIL-STD-883.
- c. Mechanical characterization. The manufacturer shall perform package mechanical characterization tests which includes evaluation for shock and vibration to demonstrate the capability to withstand impacts due to moisture ingress, contamination, corrosion, etc.

H.3.2.1.2 Wafer fabrication. This includes the manufacturer's in-house fabrication or the subcontractor's fabrication. The wafer fabrication quality systems and controls include statistical process control (SPC) and in-process monitoring programs including the technology characterization vehicle (TCV) program or the Standard Evaluation Circuit (SEC) and parametric monitors (PMs) or alternate assessment procedure with the approval of qualifying activity (QA).

As part of certification, the manufacturer should identify a specific technology or technologies for the wafer fabrication. A technology consists of the fabrication sequence, design rules and electrical characteristics. Demonstration of wafer fabrication capability consists of the fabrication sequence, design rules, electrical characteristics, and process information. All supporting documentation and data shall be made available to the qualifying activity before or during the management and technology validation (see [G.3.2.2.1](#)).

A plan shall also be presented that provides for an on-going reliability monitor and failure rate calculations.

H.3.2.1.2.1 Wafer fabrication checklist (Class level S) . The following items shall be used as minimum requirements, as applicable for the technology, for the manufacturer and QA in evaluating the new technology for class level S product:

- a. Process development
 - (1) Design of experiments (This information may not be readily available for older technologies especially when a process is transferred from another facility).
 - (2) Process sensitivity (This will define what parameters within the process would identify if the process is stable or marginal. Process variation is different and shows the process can yield even when the parameters are at minimum or maximum).
 - (3) Modeling and simulation.
 - (4) Producibility and yield analysis.
- b. Process characterization.
 - (1) Voltage.
 - (2) Temperature (Minimum range of -55°C to +125°C, otherwise provide justification).
 - (3) Process variability.
 - (4) Best and worst case or statistical simulation models considering independent variation of device types (e.g. NFET and PFET).
 - (5) Frequency (Defined by the electrical requirements of the device specification).
 - (6) Radiation (see appendix C), if applicable.
 - (7) Performance margins (until failure).
 - (8) Process optimization.
 - (9) Process maturity assessment.

- c. Process qualification.
 - (1) Test vehicle.
 - (2) Single or 1 lot.
 - (3) Environmental conditions (for fabrication, test, assembly, and storage).
 - (4) Accept/reject criteria.
 - (5) Perceptivity of tests (TCV and test programs shall be capable of highlighting the critical parameters and discerning the results that identify accept/reject criteria).
 - (6) Process baselined for qualification (no further changes required after characterization).
 - (7) Qualification by test, similarity, or space heritage (Process or device that has been produced and passed space level testing and has flown in a space environment similar to the environment expected for this process/device).
- d. Fabrication.
 - (1) TRB program (or equivalent) (see [G.3.2.2](#)).
 - (2) SPC and in-process monitoring program (see [H.3.2.1.3](#)).
- e. Radiation hardness assurance (RHA) (see appendix C), if applicable.

H.3.2.1.3 SPC and in-process monitoring program. An in-process monitoring system should be used by the manufacturer to control key processing steps to insure device yield, reliability, and RHA if applicable. The monitoring system can utilize various test structures, methods, and measurement techniques. The critical operations to be monitored should be determined by the manufacturer based on their experience and knowledge of their processes. The resulting data should be analyzed by appropriate SPC methods (in accordance with the requirements of SAE [EIA557](#) to determine control effectiveness. The following should be addressed for the wafer fabrication process, as a minimum, by the manufacturer:

- a. Incoming mask and fabrication process materials.
- b. Equipment used for wafer fabrication.
- c. Doping material concentration.
- d. Cross section diffusion or concentration profile, and epitaxial (EPI) layer.
- e. Passivation or glassivation.
- f. Metallization deposition.
- g. Resultant line width.
- h. Passivation process temperature and time.
- i. Diffusion, implant anneal process temperature, and time, or both.
- j. Sintering or annealing temperature and time.
- k. All reliability test data including the standard evaluation circuit (SEC).
- l. Mask inspection and defect density data.
- m. Parametric monitor test data.
- n. Photoresistive processing (including rework procedures).

- o. Ion implant.
- p. Wafer backside preparation.
- q. Wafer probe acceptance criteria.
- r. Rework policy.
- s. Oxide process.
- t. Gate formation.
- u. Air bridge process.
- v. Via hole process.
- w. Clean room procedures.
- x. Change control system/notification.
- y. Lot travelers (ref. [A.3.4.6](#), [A.3.4.6.1](#))
- z. Equipment calibration and preventive maintenance.
- aa. Wafer traceability.
- ab. Wafer acceptance plan.
- ac. Wafer bump characteristics (height, width etc.,)

H.3.2.1.3.1 SPC and in-process monitor checklist (Class level S) . The following items shall be used as minimum requirements, as applicable for the technology, for the manufacturer and QA in evaluating the new technology for class level S product:

- a. Define SPC monitor points.
- b. Define control limits and absolute limits.
- c. Review of data by the manufacturer and QA.
- d. Out of control (OOC) action plans.
- e. Radiation performance, if applicable.
- f. Process capability (C_{PK}) trigger level.
- g. Sample data for any prime lot reviewed by the manufacturer and QA (Prime lot is defined as a lot meeting all process monitor requirements with no MRB or out of control actions implemented).
- h. SPC controls in place audited by the QA.

H.3.2.1.3.2 Parametric monitor (PM). The manufacturer should have PMs to be used for measuring electrical characteristics of each wafer type in a specified technology. The PM test structures can be incorporated into the grid (kerf), within a device chip, as a dedicated drop-in die or any combination thereof. Location of the PM test structures should be optimally positioned to allow for the determination of the uniformity across the wafer. A suggested location scheme is one near the wafer center and one in each of the four quadrants of the wafer, at least two-thirds of a radius away from the wafer center. The manufacturer should establish, and document, reject limits and procedures for parametric measurements including which parameters shall be monitored routinely and which shall be included in the SPC program. Documentation of the PM should also include PM test structure design, test procedure (including electrical measurement at temperature and the relationship between the measured limits and those determined in the manufacturer's circuit simulations), design rules and process rules. Alternate measurement techniques, such as in-line monitors, are acceptable if properly documented. The following parameters are to be used as a guideline by the manufacturer's TRB in formulating the PM.

a. General electrical parameters.

- (1) Sheet resistance: Structures should be included to measure the sheet resistance of all conducting layers.
- (2) Junction breakdown: Structures should be included to measure junction breakdown voltages for all diffusions.
- (3) Contact resistance: Structures should be included to measure contact resistance of all inter-level contacts.
- (3) Ionic contamination and minority carrier life time: Structures should be included to measure ionic contamination, such as sodium, in the gate, field, and inter-metal dielectrics and minority carrier lifetime.

b. MOS parameters.

- (1) Gate oxide thickness: Structures should be included to measure gate oxide thickness for both "N" and "P" gate oxides as applicable.
- (2) MOS transistor parameters: A minimum set of test transistors should be included for the measurement of transistor parameters. The minimum transistor set should include a large geometry transistor of sufficient size that short channel and narrow width effects are negligible, and transistors that can separately demonstrate the maximum short channel effects and narrow width effects allowed by the geometric design rules. Both "N" and "P" transistors should be included for a complementary metal oxide semiconductor (CMOS) technology. If there is more than one nominal threshold voltage for either the "N" or "P" transistor type the minimum set should be included for each threshold. The transistor parameters to be measured are given below:
 - (a) Threshold voltage: The linear threshold voltage (V_T) for each transistor in the minimum set of transistors should be measured.
 - (b) Linear transconductance: The linear transconductance (g_m) for the full minimum set of transistors should be measured.
 - (c) Effective channel length: The effective channel length for the minimum channel length of each transistor type should be measured.
 - (d) I_{on} : I_{on} for representative transistors in the set.
 - (e) I_{off} : I_{off} for representative transistors in the set.
 - (f) Propagation delay: A test structure should be available in the form of a functional circuit from which propagation delay information can be measured at room temperature.
 - (g) Field leakage: Field transistor leakage for the minimum spaced adjacent transistors at the maximum allowed voltage should be measured.

- c. Bipolar parameters. Care should be taken in the manner and sequence in which all breakdown voltage and current measurements are taken so as to not permanently alter the device for other measurements.
- (1) Sheet resistance: Structures should be included which can be used to measure sheet resistance of all doped regions (e.g., emitter, buried collector.)
 - (2) Schottky diode parameters: The following measurements should be made on Schottky diodes representative of the size used in the technology:
 - (a) Reverse leakage: The reverse leakage current (I_R) should be measured at a specified reverse voltage.
 - (b) Reverse breakdown: The reverse breakdown voltage (BV) should be measured at a specified current.
 - (c) Forward voltage: The forward turn-on voltage (V_f) should be measured at a specified current.
 - (3) Bipolar transistor parameters: The following measurements should be made on bipolar transistors representative of the size and type used in the technology. The types should include NPN, Schottky clamped NPN, vertical PNP, substrate PNP, and lateral PNP transistors as applicable.
 - (a) Transistor gain: The common emitter dc current gain (H_{fe}) should be measured on representative transistors over three decades of collector current, the highest point of which is at the maximum rated current of the device.
 - (b) Leakage currents: The leakage currents (I_{CEO} , I_{CBO} , and I_{EBO}) should be measured on representative transistors at a specified voltage.
 - (c) Breakdown voltages: The breakdown voltages (BV_{EBO} , BV_{CBO} , and BV_{CEO}) should be measured on representative transistors at specified currents.
 - (d) Forward voltages: The forward voltages (V_{BE0} and V_{BC0}) should be measured on representative transistors at the rated currents.
 - (e) Propagation delay: A test structure should be available in the form of a functional circuit from which propagation delay information can be measured at room temperature.
 - (4) Isolation leakage: The isolation leakage current (I_L) between minimum spaced adjacent transistor collectors should be measured at a specified voltage.
- d. GaAs parameters.
- (1) Sheet resistance: Structures should be included which can be used to measure sheet resistance of each of the conducting layers.
 - (2) Metal-insulator-metal (MIM) capacitor: Capacitor test structures should be included so that dc and rf capacitance, leakage, and breakdown can be measured.
 - (3) FATFET: A long gate length FET suitable for measurement of Schottky barrier height and ideality factor, carrier concentration and mobility, and channel depth should be included.
 - (4) Isolation: A structure for use in measuring substrate isolation breakdown should be included.
 - (5) Ohmic contacts: An ohmic contact transmission line structure should be included so that specific contact resistance and transfer length can be measured.
 - (6) GaAs FET parameters: FET test structures should be included, suitable for RF probing, which can be used for measurement of both DC and RF FET parameters. The following parameters should be measured:

- (a) I_{dss} - saturated drain current at zero gate bias.
 - (b) g_m - transconductance at saturation and at 50 percent I_{dss} .
 - (c) Pinch off voltage.
 - (d) Gate-drain leakage and breakdown voltage.
 - (e) Gate-source breakdown voltage.
 - (f) Source and drain resistance.
 - (g) S-parameters of FET over frequency range of technology.
- e. Fast-test reliability structures. Fast-test reliability structures are structures meant to evaluate, within a few seconds of testing, a particular known reliability failure mechanism to insure that the processing which an individual wafer received is consistent with the reliability goals of the technology. The fast-test structures are in general new and, with the exception of hot carrier aging structures, are not sufficiently mature. Development work on them is intense however, and it is intended that these structures when mature, shall become a mandatory part of the PM. For this reason it has been decided to include information regarding fast-test reliability structures in the following paragraphs. Documentation should be available which shows the correlation between fast-tests and the results of the more traditional accelerated aging tests performed on the TCV.
- (1) Hot carrier aging: A fast-test structure should be included to evaluate the susceptibility of MOS transistors to hot electron aging. This structure may be one of the PM test transistors.
 - (2) Electromigration: Worst-case design rule fast-test structures should be included to evaluate the susceptibility of each metal level and the associated contacts to electromigration.
 - (3) Time dependent dielectric breakdown (TDDB): Fast-test structures should be included that can evaluate the long-term reliability of gate oxides.
 - (4) Contact resistance: Fast-test structures should be included that can evaluate the long-term reliability of contacts.
 - (5) Gate diffusion: Fast-test structures should be included that can evaluate the long-term reliability of the gate contact.
 - (6) Threshold voltage instability, including Negative Bias Temperature Instability (NBTI) for 130 nm and smaller CMOS technologies.

H.3.2.1.4 Wafer acceptance plan. The TRB should develop and demonstrate a wafer acceptance plan based on electrical and radiation (if applicable) measurement of PMs. This plan should utilize the PM and should include visual criteria, if applicable.

For wafer lot acceptance tests shall be performed in accordance with TM 5007 of MIL-STD-883 or an alternative which meets the minimum requirements of TM 5007 on each wafer lot producing class V or class Y (class level S) devices. The use of TM 5013 of MIL-STD-883 is encouraged for GaAs technology devices. In addition, this plan should address the concerns detailed in TM 2018 of MIL-STD-883 (e.g., metallization, step coverage). The use of TM 2018 is encouraged, however alternate procedures utilizing PMs and in-line monitors are accepted if approved during validation. PM data should be recorded and made available for review.

This plan can be either a wafer by wafer acceptance plan or a wafer lot acceptance plan, but shall address the following concerns:

- a. Small lots.
- b. Large lots.
- c. Specialty lots.

H.3.2.1.5 Assembly and packaging. The manufacturer shall demonstrate the quality system and controls, including SPC and in-process monitoring programs for both in-house assembly line and any/all of their subcontractors performing assembly processing for SMD products.

H.3.2.1.5.1 Assembly and packaging technology certification. As part of the certification, the manufacturer should identify the specific assembly technologies that are expected to be listed as part of the technology flow for QML and used in QML microcircuits. Those processes shall be qualified by addressing, as a minimum, the test in tables H-IA or H-IB as appropriate. An assembly technology consists of the materials and processes used for wafer saw, die attach, wire bond, flip chip attachment, package sealing, lead attach, solder dipping, marking, and any other process involved with the construction of the product. All supporting documentation and data shall be made available to the qualifying activity before or during the management and technology validation (see [G.3.2.2.1](#)). The following items shall be used as minimum requirements by the manufacturer and the QA in evaluating assembly and packaging for class level S product:

- a. Assembly processes.
 - (1) Die attach.
 - (2) Wire bond/bump.
 - (3) Encapsulation.
 - (4) Process monitors/SPC.
 - (5) Inspections.
 - (6) Tests – Mechanical, thermal, optical.
 - (7) Lead or column attach.
 - (8) Incoming tests or review of accompanying C of C on materials (e. package, die attach material, etc.).
- b. Package processes and technology.
 - (1) Design.
 - (2) Materials selection.
 - (3) Assembly under supplier control.
 - (a) By supplier.
 - (b) Subcontracted.
 - (4) Thermal characterization.
 - (a) Hot spots.
 - (b) Thermal impedance.
 - (5) Electrical characterization.
 - (a) At specification levels including voltage, full temperature range, and other excitation conditions.
 - (b) Beyond specification conditions to determine margin.
 - (c) Plan to address unspecified or untested parameters (Review analysis to ensure critical untested parameters are specified or addressed)
 - (6) Package qualification data.
 - (a) Incoming package tests on bare package.
 - (b) Incoming tests on raw materials (e. die attach, etc.)
 - (c) Mechanical tests.
 - (d) Thermal tests.
 - (e) Electrical tests.
 - (f) Thermal impedance.

- (7) Column attachment.
 - (a) ESD controls.
 - (b) at 25°C electrical validation pre and post column attach.
 - (c) Mechanical integrity.
 - (d) Co-planarity.

H.3.2.1.6 SPC and in-process monitoring program. A process monitoring system should be used by a manufacturer to control key processing steps to insure product yield and reliability. The monitoring system can utilize various test chips, methods and measurement techniques. The critical operations to be monitored shall be determined by the manufacturer based on their experience and knowledge of their processes. The resulting data should be analyzed by appropriate SPC methods to determine control effectiveness. The following should be addressed, as a minimum, by the manufacturer:

- a. Incoming assembly process materials.
- b. Incoming package acceptance.
- c. Equipment used for assembly.
- d. Wafer acceptance criteria.
- e. Die attach.
- f. Chip to package interconnect (wire/ribbon bond, tab, flip chip).
- g. Package seal.
- h. Marking.
- i. Rework.
- j. Lead trim, form, and final finish.
- k. Atmosphere and cleanliness control.
- l. Chip encapsulation/molding.
- m. Encapsulant purity.
- n. Internal gas analysis (IGA).
- o. Flip chip die pull off test shall be performed (before underfill dispense) in accordance with TM 2031 and bump shear test shall be performed for wafer bump technology qualification.
- p. Balls/Columns attach.

H.3.2.1.7 Test capability. The manufacturer shall document test capability to their QM plan, which includes devices screening, qualification and technology conformance test conditions in accordance with the applicable Standard Microcircuits Drawing (SMD), MIL-PRF-38535, and MIL-STD-883, as applicable to the product.

H.3.2.1.8 Certification approval. Upon successful demonstration by the manufacturer of meeting the certification requirements, the QA will issue a certification of approval. This certification will include QA approved alternatives and test optimizations as presented by the manufacturer and listed in the QM plan. Documentation and data presented by the manufacturer during the certification process does not need to be provided as a part of the reliability assessment and qualification stages.

H.3.2.2 Physics-of- failure/TCV reliability assessment.

H.3.2.2.1 Reliability assessment plan. For class level S product, the manufacturer shall provide to the QA a reliability assessment plan for the technology. The plan shall account for all significant failure mechanisms as listed in the following sections.

H.3.2.2.2 TCV program . A TCV program should be implemented by the manufacturer for the technology or process being considered for certification. The program should contain, as a minimum, those test structures needed to characterize a technology's susceptibility to intrinsic reliability failure mechanisms such as electromigration, time dependent dielectric breakdown (TDDB), gate sinking, ohmic contact degradation, sidegating/backgating, hot carrier aging and threshold voltage instability, including Negative Bias Temperature Instability (NBTI). If other wear-out mechanisms are discovered as integrated circuit technology continues to mature, test structures for the new wear out mechanisms should be added to the TCV program. The TCV program shall be used for the following purposes: Certification of the technology; reliability monitoring; radiation hardness assurance and monitoring, when applicable; change control; and the characterization of fast-test intrinsic reliability structures.

NOTE: The test structures necessary to monitor intrinsic reliability failure mechanisms do not have to be a single die or location, but can appear on the PM, the SEC, or the device itself. The TCV program (see [G.3.3.f](#)) should, however, indicate where the structures are located and how they are tested and analyzed.

H.3.2.2.2.1 TCV certification. For initial reliability assessment, sufficient TCV test structures for each wear-out mechanism should be subjected to accelerated aging experiments. The TCV test structures should be randomly chosen from and evenly distributed from three homogeneous wafer lots in the technology to be certified in the fabrication facility to be certified. These wafers shall have passed the wafer or wafer lot acceptance requirements. The accelerated aging experiments should produce an estimate of the mean time to failure (MTTF) and a distribution of the failure times under worst case operating conditions and circuit layout consistent with the design rules for each wear-out mechanism. From the MTTF and distribution of failures a worst case operating lifetime or a worst case failure rate can be predicted. Test structures should be from completed wafers which have been passivated/ glassivated. A summary of the accelerated aging data and analysis should be available for review by the qualifying activity. The initial certification MTTF, failure distribution and acceleration factors should be used as benchmarks for the technology to which subsequent TCV results shall be compared. This includes evaluation of activation energy, acceleration factors based on voltage and temperature for the technology, long term reliability and known failure mechanism (FMEA) and mitigation strategies. The current density and temperature acceleration factors for electromigration should be determined and a MTTF and failure distribution determined for the worst case current, temperature, and layout geometry allowed in the technology. From the MTTF and failure distribution, a failure rate for electromigration in the technology should be calculated.

All of the TCV test structures shall use the same packaging materials and assembly procedures as standard circuits in the technology. The TCV structures need not use a fully qualified package since qualified packages shall tend to have lead counts far in excess of those needed for intrinsic reliability studies. The packaging requirement for the TCV may be waived by the qualifying activity if the manufacturer can supply documentation showing the equivalence of wafer level and packaged accelerated aging results.

NOTE: In those cases where this may not be possible, the TCV should use a suitable package to allow for the evaluation of the chip technology to be qualified, without adversely affecting the outcome of the test.

An example of the requirements of packages for TCV test structure concerns the hydrogen content of a ceramic package and its effect on hot carrier aging, and can differ substantially for packaged and non-packaged devices. The minimum requirements to be addressed for the TCV structures for specific mechanisms are given below.

- a. Hot carrier aging. The TCV should use structures that monitor hot carrier aging applicable to the technology to be used in QML microcircuits. Device degradation is to be characterized in terms of both linear transconductance (g_m) and threshold voltage (V_{TH}) and the resistance to hot carrier aging is to be based on whichever parameter experiences the manufacturers' specified degradation limit for the minimum channel length and width allowed in the technology. A wafer level fast-test screen should be established for technologies that are susceptible to hot carrier aging. This test should be part of the wafer acceptance criteria.
 - (1) Metal oxide semiconductor (MOS). The TCV should have structures to characterize the effects of hot carrier aging as a function of channel length for MOS transistors for each of the nominal threshold voltages used in the technology. Degradation should be characterized in terms of g_m and V_{TH} .
 - (2) Bipolar. The TCV should contain structures for characterizing hot carrier aging of diodes in bipolar technologies.
- b. Electromigration. The TCV should contain structures for the worst case characterization of metal electromigration over:
 - (1) Flat surfaces.
 - (2) Worst case noncontact topography.
 - (3) Through contacts between conductive layers.
 - (4) Contacts to the substrate.
- c. Time dependent dielectric breakdown (TDDB) (MOS). The TCV should contain structures for characterizing TDDB of gate oxides. The structures should have gate oxide area and perimeter dominated structures. Separate perimeter structures should be used for the gate ending on a source or drain boundary and where the gate terminates over the transistor-to-transistor isolation oxide. The electric field and temperature acceleration factors for TDDB should be determined and a MTTF and failure distribution determined for the worst case voltage conditions and thinnest gate oxide allowed in the technology. From the MTTF, a failure rate for TDDB in the technology should be calculated.
- d. TCV fast test structure requirements. The structures to be used for the fast test reliability monitoring of hot electron aging should be included in the TCV program so that correlations of the fast-test measurements with the accelerated aging results may be made.

NOTE: It is strongly recommended that fast test intrinsic reliability structures for electromigration and TDDB be included in the TCV program so that correlations can be made with longer term aging experiments. It is likely that these structures shall be required for wafer acceptance in the future.
- e. Ohmic contact degradation. The TCV should have a structure for assessing the degradation of ohmic contacts with time at temperature, especially for gallium arsenide (GaAs).
- f. Sidegating/backgating. A structure should be included for evaluating sidegating/backgating of field effect transistor's (FET's) in GaAs technology.
- g. Sinking gate. A FET structure should be included for evaluating the sinking gate degradation mechanism and other channel degradation mechanisms of GaAs FET's.

- h. Threshold voltage instability, including Negative Bias Temperature Instability (NBTI) for 130 nm and smaller CMOS technologies. The NBTI test structure evaluates the effect due to interface traps (oxide energy states) in the gate oxide that form under DC inversion stress. Holes in the PMOS devices are known to interact with these traps more easily than electrons, and so this is a PMOS dominated mechanism. These trapped holes cause the threshold voltage (V_{TH}) of the affected transistor to shift lower (more negative) with increasing temperature, degrading device performance.

H.3.2.2.3 Assembly and packaging. The manufacturer should list the assembly and packaging processes (die-attachment, wire/ribbon bonding, seal molding and part marking) that is expected to be listed on the QML and used in QML microcircuit assembly (see [H.3.2.1.5](#)).

H.3.2.2.3.1 Assembly process technology. New assembly process technologies shall be characterized to determine the mechanical and thermal performance. The technology's susceptibility to intrinsic reliability failure mechanisms shall be characterized to determine potential failure modes. The characterizations may include performance of thermal stresses at multiple temperature levels to develop derating curves. Tables H-IA and H-IB identify the assembly process qualification testing which shall be addressed for the technology being used.

H.3.2.2.3.2 Packaging technology. The manufacturer shall address package design/construction quality and reliability. The manufacturer is responsible to maintain documented validation of all characterization methods used, including all supporting data (see [H.3.2.1.1.3](#)). Tables H-IIA and H-IIB identify the key package characteristics for which testing shall be addressed on each QML package technology.

H.3.2.2.4 Reliability assessment report. For class V or class Y (class level S) product, a reliability assessment report shall be submitted to the QA for review and approval which demonstrates the successful completion and results of the assessment.

H.3.3 Transitional certification.

H.3.3.1 Transitional certification and qualification. Manufacturers may be granted transitional certification based on the following requirements:

- a. The manufacturer has qualifying activity (QA) approval that all facilities covered by the transitional certification supply product built to the previously certified and qualified MIL-M-38510 product flows. Facilities not meeting this condition are eligible for transitional certification, but they may require an audit if deemed necessary by the QA.

If the manufacturer has never received MIL-M-38510 certification and qualification, but has been approved by DLA Land and Maritime for class M products only, an audit of the facilities under QML consideration shall be required. If these facilities have been audited by DLA Land and Maritime under the class M (SMD) random audit program, the audit may not be necessary, as determined by the QA.

Facilities that have never been audited by DLA Land and Maritime are eligible for transitional certification and an audit will be required unless the QA determines that an audit is not necessary.

- b. The manufacturer should submit a plan for achieving full QML. The plan should include a self-assessment, quality improvement plan, SPC plan, and a plan to upgrade any DLA Land and Maritime drawing or SMD part to one part-one part number Q level devices.

- c. The manufacturer should comply with all requirements of [appendix A](#) of this specification until the QA has approved the manufacturer for full QML certification at which time the previous MIL-M-38510 (appendix A of MIL-PRF-38535) requirements shall be superseded by the requirements of the main body of this specification and all applicable appendices. As the manufacturer moves toward full QML certification, the QA can allow variations to [appendix A](#) as part of the transition process. For class level S only, the manufacturer should notify the space community (e.g., NASA, NRO, DTRA, and AFSMC) of any proposed major variations to appendix A requirements. Further review by these organizations may be necessary before these variations can be sanctioned.
- d. Any major changes to the transitional certification lines should be approved by the QA until such time as the QA approves the manufacturers TRB system and QM plan. This includes any deletion of test requests.
- e. If any re-qualifications are required they should be in accordance with the guidelines of [appendix A](#) or as approved by the QA.

The QML allowances given by this transitional certification shall be approved after the on-site verification and certification by the QA, but prior to shipment of any product under this specification. In addition, the manufacturer shall make a commitment to becoming QML certified for all portions of the process under transitional certification. If this commitment is not met, the QA reserves the right to remove the transitional certification and all benefits associated with that certification.

NOTE: The transitional certification is not permanent (approximately 2 years maximum, unless extended by the QA) but allows the manufacturer some flexibility while still working toward QML on the remainder of the processes committed to QML. No class level S product shall be shipped until a full QA on-site certification is achieved.

H.3.4 Qualification.

H.3.4.1 Technology qualification. The process for qualification is outlined below and is further described in detail in the subsequent sections.

- a. Plan approval.
 - (1) Screening flow.
 - (2) Process performance characterization plans and data.
 - (3) Process qualification test plans and data.
 - (4) For class level B products, life test on a minimum of 1 wafer lot for 1000 hrs minimum at 125°C ambient, or equivalent.
 - (5) For class level S products, long term life test shall meet the requirements of paragraph [B.3.4](#), appendix B, or shall meet long term life test on a minimum of 1 wafer lot for 4,000 hours minimum at 125°C ambient, or equivalent.
- b. Report approval.

For initial technology qualification, a sufficient number of SEC devices is required, from wafers passing the wafer screen requirements and randomly chosen and evenly distributed from three wafer lots for life testing and total ionizing dose (TID) requirements (RHA products only). The testing shall be performed in accordance with MIL-PRF-38535 Groups A, B, C, D, and E (if applicable) or to the agreed to alternatives and test optimizations defined in the QM plan. The number of SEC device failures shall serve as a qualification benchmark for the technology. Failure analysis (FA) should be done on failed SEC's to determine each failure category and action taken to correct any problems found. The SEC reliability data, including FA results, should be available for review by the QA. For RHA environments, irradiate SEC to demonstrate radiation hardness assurance capabilities limit (RHACL).

For new class level S product, if the technology is mature at other levels, the manufacturer may provide a supplemental/alternative data submittal to the QA for the reliability demonstration above. The alternative data submittal may include, but is not limited to the following:

- a. Historic product shipment summary - total quantity shipped of similar product/family on same process.
- b. Field returns summary. (NOTE: Proprietary information such as program names and individual customer names shall not be revealed.)
- c. Reliability summary data - from the reliability monitor program & Failure rate calculation.
- d. Historic qualification data - from similar product(s) from the same process family.
- e. Examples of process monitors and data showing performance & trends from recent lots.
- f. Examples of wafer lot acceptance reports.

NOTES: For complex devices initial technology qualification, a sufficient number of SEC or actual devices are required, and selected devices must pass wafer screen test requirements. The SEC or actual devices shall be chosen randomly and evenly distributed from multiple wafers or multiple wafer lots or single wafer lot (with the approval of QA) for life testing, and for RHA devices, total ionizing dose (TID) test and samples size shall meet the requirements of [table C-I](#) group E test herein and TM 1019 of MIL-STD-883.

H.3.4.1.1 Process technology validation. The manufacturer shall perform sufficient technology qualification testing to assure the devices supplied meet the minimum **class N and class Y**, and class level B or S performance requirements as described herein. The manufacturer shall maintain documentation of qualification testing for review by the preparing or acquiring activity upon request.

H.3.4.1.2 Technology qualification eligibility. Design, wafer fabrication, assembly, and qualification testing of the demonstration vehicles may begin before certification is granted. However, if deficiencies and concerns found during the validation require changes to the process flows, the design, wafer fabrication, assembly, and testing shall be redone on the new process flows. In all cases, start of the qualification testing should begin no later than 6 months after the letter of certification is received in order to retain the manufacturer's initial certification. Completion should be achieved in a timely manner or recertification may be necessary.

H.3.4.1.3 Demonstration vehicles. Demonstration vehicles shall be produced on the certified manufacturing line as defined in the QM plan submitted during the certification process. These demonstration vehicles should be of such complexity as to be representative of the microcircuits to be supplied by the manufacturer. The demonstration vehicles will be assembled in packages that are representative of manufacturer technology and shall be screened to the appropriate QML classes Q or V or Y flow, including all applicable test alternatives and test optimizations. Each demonstration vehicle shall operate and meet all performance requirements of the device specification and RHACL for a radiation hardened process.

NOTES: For a technology which has a die as its primary product, the demonstration vehicle should be suitably packaged to allow evaluation of the technology without adversely affecting the outcome of the tests.

H.3.4.2 Technology qualification test plan. The manufacturer shall submit a qualification test plan which details the test flow, test limits, test data to be measured, recorded and analyzed, test sampling techniques, and traceability records. The test plan should detail materials, manufacturing construction techniques (including design CAD tools), testing and reporting techniques and should be made available to the qualifying activity at the time of certification. The test plan should include traceability documentation, milestone charts and the proposed demonstration vehicle descriptions. All test limits should be in accordance with the requirements of the SMD. All demonstration vehicles shall be representative of the manufacturing and screening processes. For class level S product new technology items, the plan shall include any screening tests or additional qualification tests required as a result of the characterization and physics-of-failure evaluations.

H.3.4.3 Wafer fabrication technology validation. A manufacturer should have the standard evaluation circuits (SEC) or technology characterization vehicles (TCV) for the technology or process being considered for certification. A manufacturer's SEC should be used to demonstrate fabrication process reliability for the technology. The SEC design documentation should address: The design methodology, the software tools used in the design, the functions it is to perform, its size in terms of utilized transistor or gate count, and simulations of its performance. Documentation procedures for the SEC and standard production devices should be the same so that correlation can be made. The SEC may be designed solely for its role as a quality and reliability monitoring vehicle or it may be a standard product. (For RHA environment, see appendix C.) The SEC should address the following requirements for initial technology characterization/qualifications:

- a. Complexity. The complexity of the SEC for digital microcircuits shall contain, as a minimum, one-half the number of transistors expected to be used in the largest microcircuit to be built on the QML line.

All microcircuits device types shall include one or more test vehicles or SEC that represent all the cell types, including memory and exercise the functionality of the process technology.

For class V or Y (class level S) microcircuit devices, the SEC or multiple devices shall represent all the cell types including memory and shall operate during burn-in at a minimum of 75% of the product frequency, and keeping in mind maximum junction temperature and power dissipation constraints, and shall have electrical tests performed to demonstrate expected product operating capability at the maximum rated frequency without parametric or catastrophic failure. Alternative approaches must be approved by the Qualifying Activity.

- b. Functionality. The SEC shall contain fully functional circuits capable of being tested and screened in a manner identical to the QML microcircuits.
- c. Design. The SEC shall be designed to stress the design capabilities of the process (see H.3.2.1.1.1c). The architecture of the SEC should be designed so that failures can be easily diagnosed.
- d. Fabrication. The SEC shall be processed on a wafer fabrication line that is intended to be, or already is, a certified QML line.
- e. Packaging. The SEC shall be packaged in a package qualified in accordance with requirements in 3.4.1.4.1 herein.

NOTES: A different SEC may be required whenever the design rules, the materials, the basic processes, or the basic functionality of the technology differ.

H.3.4.4 Assembly/Packaging technology validation. The manufacturer shall demonstrate the capability of the assembly and package processes by qualifying the SEC package or actual product to the package certification and qualification procedures. The manufacturer shall document how packages used in the manufacture of QML products are grouped together as a package family for qualification and change control purposes. The technology qualification demonstration shall be conducted on samples pulled from minimum of 3 different assembly lots for assembly/process technology validation. The qualification testing shall be conducted in accordance with MIL-PRF-38535 Groups A, B, and D or to the agreed to alternatives and test optimizations defined in the QM plan.

H.3.4.4.1 Package integrity demonstration test plan (PIDTP) . Manufacturability, test, quality and reliability issues unique to specific non-traditional assembly/package technologies intended for space applications shall be addressed in a Package Integrity Demonstration Test Plan at the start of the package design cycle. The PIDTP shall be approved by QA after consultation with the space community. The technologies requiring such a plan are: a) non-hermetic packages (e.g., class Y), b) flip-chip assembly, and c) solder terminations. Microcircuits employing more than one of these technologies shall include elements for each in the PIDTP.

H.3.4.4.1.1 Non-Hermetic packages. For class Y microcircuits, the PIDTP must address issues unique to non-hermetic construction and materials, such as potential materials degradation, moisture absorption, and resistance of active devices, passive devices and interconnects to environmental effects and processing stresses. Moisture sensitivity level characterization (ref: IPC/JEDEC J-STD-020D) shall be performed for exposed flip-chip underfill or thermal grease/epoxy.

H.3.4.4.1.2 Flip-chip assembly. For space microcircuits employing flip-chip assembly technologies including 2D, 2.5D or 3D package construction technology devices comprises either class V or class Y (class level S), the PIDTP must address the materials and processes unique to solder bump interconnect attach, underfill and lid-to-die attach. The plan shall demonstrate as a minimum, how the following are evaluated and monitored including a corresponding package level reliability demonstration:

1) Substrate materials. The substrate materials (organic or ceramic substrate) shall be documented in the PIDTP, and shall include landing pad composition. For organic substrate flip chip devices the following factors shall be evaluated and documented in PIDTP:

- i) Coefficient of thermal expansion (CTE)
- ii) Glass transition temperature (Tg) if appropriate
- iii) Substrate core and build-up layer materials
- iv) Solder mask material and thickness; SMD versus NSMD landing pads
- v) Conductor material and landing pad construction
- vi) Moisture absorption and outgassing characterization

2) Bump geometry. The solder bump geometry including micro bump shall be documented in the PIDTP, and shall include bump height, bump diameter and bump pitch, as well as a description of the under bump metallurgy (UBM) shape, size and thickness.

3) Solder bump deposition process and materials. The solder bump deposition process shall be documented in the PIDTP (e.g., plated, evaporation, solder paste), along with the solder alloy. In addition, the UBM deposition process (e.g., plated, evaporation, sputtered) and composition shall be documented in the PIDTP.

4) Flux materials. The flux type (e.g., no-clean, water soluble) and materials employed for solder bump interconnect reflow shall be documented in the PIDTP.

5) Underfill materials. Underfill materials shall be documented in the package integrity demonstration test plan (PIDTP). The PIDTP shall address the relevant properties of the underfill and how they are characterized. The properties below shall be included to the PIDTP:

- i) Coefficient of thermal expansion (CTE)
- ii) Glass transition temperature (T_g)
- iii) Viscosity
- iv) Pot life
- v) The shelf life
- vi) Underfill particle size/Filler contents
- vii) Underfill cure time and temperatures
- viii) Bond strength
- ix) Ionic impurities
- x) Underfill Outgassing test: For non-hermetic flip chip devices(e.g. class Y) outgassing test shall be performed in accordance with ASTM E595. Underfill outgassed limits shall be <1% for total mass loss and <0.1% for CVCM.

5.1) Underfill long term reliability test: Manufacture's shall perform following long term underfill reliability test

(1) Temperature cycling test: Cured underfill with solder bump temperature cycling test shall be performed for 1,000 cycles in accordance with TM1010 condition C (-65 to 150°C) and subsequently (2) SAM test shall be performed to verify underfill void and delamination. The sample size 10(0) shall be considered as minimum during underfill package initial qualification.

6) Thermal interface materials (TIM) for Lid attach/adhesive materials.

Devices with lid or heat spreader attached to the back side of a microcircuit die, the lid attach/adhesive thermal interface materials shall be documented in the PIDTP. The following test parametric results may be considered with C of C or initial certification test performed by TIM suppliers/users; and approved by QA:

- a) Viscosity.
- b) Density
- c) Volume resistivity
- d) Lap shear adhesion
- e) Expiration Date
- f) Pot life
- g) Glass transition temperature (T_g)
- h) Dissipation factor
- i) Ionic impurities
- j) Coefficient of thermal expansion (CTE)
- k) Thermal conductivity
- l) Outgassing test: For non-hermetic flip chip devices(e.g. class Y) outgassing test shall be performed in accordance with ASTM E595. TIM outgassed limits shall be <1% for total mass loss and <0.1% for CVCM.

7) Flip chip bump shear test. For flip chip, a bump shear test shall be performed in accordance with JEDEC JESD22-B117 or equivalent to determine the shear strength of the solder bumps for initial qualification as a part of the wafer bump technology qualification and shall be documented to the PIDTP.

8) 2D or 2.5D or 3D package construction methodology. The 2D or 2.5D or 3D package construction methodology shall be documented in the PIDTP.

- a) Copper filler TSV interposer geometry. The copper filler through silicon via (TSV) geometry and materials compositions shall be documented in the PIDTP. Temperature cycle (TC) testing shall be performed under the conditions of –55°C to +125°C for 1000 cycles with sample size 5(0) without intrinsic failure. These tests demonstrate the performance of the through-silicon via (TSV) interposer technology, C4 bumps, and the interposer interconnects.

8.1) Long-term reliability test 2D or 2.5D or 3D package devices:

- 1) High-temperature operating life (HTOL) test shall be performed with a maximum voltage at $T_j = 125^{\circ}\text{C}$ on samples size 5(0) for 1500 cycles.
- 2) High-temperature storage (HTS) testing shall be performed on samples size 5(0) for 1,000 hours at 150°C temperature conditions to demonstrate the long-term reliability of micro-bump solder joints.
- 3) HAST biased (85% RH at 130°C) tests shall be performed 500 hrs per JEDEC JESD22-A110
- 4) Power cycling test shall be performed at 125°C on samples size 5(0) for 1500 cycles.

9) Lot date code for non-hermetic flip chip device. For non-hermetic flip chip devices lot date code shall be assigned upon completion of underfill cure or at lid attach (method to be defined and documented by the manufacturer) to identify the device assembly processing and assembly location. Devices will be traceable through the lot date code to the assembly year, sealing week and assembly location.

H.3.4.4.1.3 Solder terminations. For space use microcircuits employing solder terminations (class V or class Y), the PIDTP shall address the materials and processes unique to solder terminations, such as ball/column integrity, attachment integrity, damage due to test, protection for shipment and shelf life. The manufacturer shall perform post column attachment electrical characterization over temperature and compare data with pre-column attachment process to assess any changes due to the column attachment process.

TABLE H-IA. Assembly process technology testing for hermetic and non-hermetic packages

Group number	Process	MIL-STD-883 test method and condition or JEDEC test method ^{1/}	
		Hermetic packages (device class Q or V or class level B or S)	Non-hermetic packages (device class Y)
1	Die-attach and interconnect	Where applicable a. Thermal shock TM1011 condition C, 100 cycles b. End-point electricals test - In accordance with device specification c. Radiography (X-ray) TM 2012 or SAM - TM 2030 d. Bond strength TM 2011 (die-mount and wire bond) plus Die cracks TM 2010 e. Die shear or stud pull TM 2019 or TM 2027 f. Flip chip die pull off test TM 2031 (before underfill dispense) g. Underfill/epoxy (see H.3.4.4.1.2) h. Flip chip die shear test TM 2019 or TM 2027 (after underfill cured)	Where applicable a. Thermal shock TM1011 condition C, 100 cycles b. End-point electricals test - In accordance with device specification c. Radiography (X-ray) TM 2012 or SAM - TM 2030 d. Bond strength TM 2011 (die-mount and wire bond) plus For die cracks TM 2010 e. Die shear or stud pull TM 2019 or TM 2027 f. Flip chip die pull off test TM 2031 (before underfill dispense) g. Underfill/epoxy (see H.3.4.4.1.2) and ASTM E595 for outgassing. h. Flip chip die shear test TM 2019 or TM 2027 (after underfill cured)
2	Die-attach, interconnect and seal test	Where applicable a. Mechanical shock TM 2002, condition B b. Variable frequency vibration TM 2007, condition A c. Constant acceleration TM 2001 d. Fine and gross leak TM 1014 e. Visual inspection TM 1010, (visual criteria 20X of magnification) f. End-point electricals test - In accordance with device specification	Where applicable a. Mechanical shock TM 2002, condition B b. Variable frequency vibration TM 2007, condition A c. Constant acceleration TM 2001 d. Not applicable e. Visual inspection TM 1010, visual criteria 20X of magnification f. End-point electricals test - In accordance with device specification
3	Lid seal	Internal gas analysis (IGA) test TM 1018 (5,000 ppm maximum at +100°C)	Not applicable
4	Lid seal	Where applicable Lid torque (glass seal) TM 2024	Where applicable Lid torque (glass seal) TM 2024
5	Code marking	Where applicable Resistance to solvents TM 2015	Where applicable Resistance to solvents TM 2015
6	Final package testing	High temperature Storage TM 1008 (1,000 hours at +150°C)	High temperature Storage TM 1008 (1,000 hours at +150°C)
7	Post burn-in lead finish	Where applicable Solderability TM 2003 solder temperature (+245°C ± 5°C)	Where applicable Solderability TM 2003 solder temperature (+245°C ± 5°C)

^{1/} The test methods are listed herein to give the manufacturer an available method to use. Alternate procedures or test methods may be used.

TABLE H-IB. Assembly process technology testing for class N plastic packages. ^{1/}

Group number	Process	Test	MIL-STD-883 test method or industry standard
1	Die-attach and interconnect	a. In-line visual inspection b. In-line bond strength c. In-line ball bond shear d. In-line die shear/stud pull e. Post molding X-ray	a. TM 2010 (die-mount and wire bond) b. TM 2011 c. ASTM F1269 d. TM 2019 or TM 2027 e. TM 2012
2	Die-attach, interconnect, and molding	a. Radiography (X-ray) b. SAM (ultrasonic inspection) etc.	a. TM 2012 (die-mount and wire bond) b. TM 2030
3	Die-attach, interconnect, and molding	a. Temperature cycling (1,000 cycles) b. End-point electricals	a. TM 1010 condition C or JESD22-A104 b. In accordance with device specification
4	Die-attach, interconnect, and molding	a. Thermal shock (100 cycles)	a. TM 1011 condition C or JESD22-A106 condition C
5	Marking	Resistance to solvents	TM 2015
6	Storage conditions	High temperature storage	TM 1008, 1,000 hours at +150°C
7	Post burn-in lead finish	Solderability	TM 2003 solder temperature (+245°C ± 5°C)

^{1/} The test methods are listed herein to give the manufacturer an available method to use. Alternate procedures or test methods may be used.

TABLE H-IIA. Technology characterization testing for hermetic and non-hermetic packages.

Group number	Process	MIL-STD-883 test method and condition or JEDEC test method	
		Hermetic packages (device class Q or V or class level B or S)	Non-hermetic packages (device class Y)
1	Dimension <u>1/</u>	Physical dimension TM 2016	Physical dimension TM 2016
2	Resistance to moisture	Where applicable a. Thermal shocks TM 1011, condition C, 15 cycles b. Temperature cycles TM 1010, condition C, 100 cycles c. Moisture resistance TM 1004, unbiased condition d. Visual inspection TM 1010 and TM 1004 visual criteria e. Fine and gross leak TM 1014	Where applicable a. Thermal shocks TM 1011, condition C, 15 cycles b. Temperature cycles TM 1010, condition C, 100 cycles c. HAST(Biased) JESD22-A110 d. Visual inspection TM 1010 and TM 1004 visual criteria e. Not applicable
3	Susceptibility to corrosion	Where applicable Salt atmosphere TM 1009, condition A	Where applicable Salt atmosphere TM 1009, condition A
4	Leads	Where applicable Lead integrity TM 2004, condition A, B2 or D For pin grid array TM 2028 For BGA (ball shear) - JESD22-B117 For CGA (Column pull test) TM 2038	Where applicable Lead integrity TM 2004, condition A, B2 or D For pin grid array TM 2028 For BGA (ball shear) - JESD22-B117 For CGA (Column pull test) TM 2038
5	Susceptibility to electrostatic discharge (ESD) sensitivity <u>2/</u>	ESD TM 3015 or ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002	ESD TM 3015 or ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002
6	Susceptibility to latch-up	Where applicable Latch-up test JESD78 or Manufacturers internal procedures	Where applicable Latch-up test JESD78 or Manufacturers internal procedures
7	Thermal resistance	Thermal characteristics TM 1012	Thermal characteristics TM 1012
8	Underfill/epoxy materials	(see H.3.4.4.1.2)	(see H.3.4.4.1.2) and For outgassing ASTM E595
9	BGA/CGA packages: Ball/Column attachment	Per approved PIDTP	Per approved PIDTP

1/ Performed as either characterization or as part of qualification.

2/ ESD classification level is as defined within test method 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 for Human Body

Model (HBM) and ANSI/ESDA/JEDEC JS-002 for Charge Device Model (CDM) as applicable..

TABLE H-IIB. Technology characterization testing for class N plastic packages.

Group number	Process	Test	MIL-STD-883 test method or industry standard
1	Dimensions	Physical dimension	TM 2016 <u>1/</u>
2	Resistance to moisture	a. Preconditioning Electrical test b. Biased HAST (500 hours, +130°C , 85% RH) c. End-point electricals test	a. In accordance with device specification. <u>2/</u> b. JESD22-A110 <u>3/</u> c. In accordance with device specification.
3	Susceptibility to corrosion	Salt atmosphere	TM 1009
4	Susceptibility to leakage and corrosion	Autoclave (no bias) (pressure pot) 2 atm., +121°C	JESD22-A102 (data to be provided for 96 hours and 168 hours)
5	Leads	Lead integrity	TM 2004, condition A, B2 or D
6	Susceptibility to moisture induced cracking at reflow soldering for surface mount and applicable through hole packages	a. Moisture intake b. Reflow simulation c. Inspection for Delamination and cracks	a. 168 hours at +85°C/85% RH or bake + minimum guaranteed time at +30°C /60% RH b. Vapor phase (+219°C , no preheat) or Infrared (+240°C maximum) c. Cross-section at 1000X, ultrasonic (SAM) etc. TM 2030
7	Safety	Flammability	UL 94, ASTM D2863
8	Fungus resistance	ASTM G21	Required only if fungus is a concern
9	Susceptibility to electrostatic discharge (ESD) sensitivity	ESD	ESD TM 3015 or ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 <u>4/</u>
10	Susceptibility to latch-up	Latch-up test	JESD78 or manufacturers internal Procedures
11	Thermal resistance	Thermal characteristics	TM 1012

1/ Performed as either characterization or as part of qualification.

2/ The manufacturer shall define a "preconditioning" procedure that simulates board assembly of plastic surface mount devices. This procedure should include moisture intake and reflow simulation. Exposure to soldering fluxes (possible source of corrosiveness) and to board cleaning agents is also recommended for preconditioning the devices.

3/ Five hundred hours of highly accelerated stress testing (HAST) is preferred but the qualifying activity shall consider the manufacturers overall processing and testing to evaluate this requirement. The actual HAST hours or alternate testing shall be included in the QM plan.

4/ ESD classification level is as defined within test method 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 for Human Body Model (HBM) and ANSI/ESDA/JEDEC JS-002 for Charge Device Model (CDM) as applicable.

H.3.4.5 Technology qualification report approval. The technology qualification report that demonstrates successful compliance to the qualification test plan, and shall be submitted to the QA for their review and approval.

H.3.4.6 Qualification test report. The manufacturer should present to the qualifying activity (QA) an analysis of the qualification data. The aim of this analysis is to show that all process variables are under control and repeatable within the certified technology and that parametric monitor, TCV, and SEC data monitoring are adequate and correlatable to the process. The QA should be notified of any improvements/changes to the certified QML technology flow as a result of evaluating the qualification testing data. The following data, if applicable, should be addressed and retained by the manufacturer to support the results:

- a. Simulation results from the design process (can be reviewed during the validation).
- b. Parametric monitor test data.
- c. Results of each subgroup test conducted, both initial and any resubmissions.
- d. Number of devices tested and rejected.
- e. Failure mode and mechanism for each rejected device.
- f. Read and record variable data on all specified electrical parameter measurements.

NOTE: Specified electrical tests from a serialized, random sample (minimum of 22 devices) may be used to satisfy this requirement. The manufacturer may submit variables data in histogram format giving mean and standard deviation or equivalent for passing microcircuits.

- g. Where delta limits are specified, variable data, identified to the microcircuit serial number, should be provided for initial and final measurements.
- h. For physical dimensions, the actual dimension measurements on three randomly selected microcircuits, except where verification of dimensions by calibrated gauges, overlays, or other comparative dimensions verification devices is allowed.
- i. For bond strength testing, the forces at the time of failure and the failure category, or the minimum and maximum readings of the microcircuits if no failures occur.
- j. For die shear or stud pull strength testing, the forces at the time of the failure and the failure category, or the die shear or stud pull reading if no separation occurs.
- k. A copy of the test data on nondestructive bond pull testing as required by TM 2023 of MIL-STD-883.
- l. For RHA testing, pre-test and post-test end-point electrical parameters, transient and single event phenomenon (SEP) response and test conditions (if applicable).
- m. For lid torque strength testing, the forces at the time of failure or the actual torque, if no separation occurs.
- n. For internal gas analysis (IGA) readings, report all gases found.
- o. Copy of burn-in circuits.

H.3.4.7 Qualification test failures. If any particular testing results are not successful, the manufacturer should perform failure analysis and take necessary corrective action. The manufacturer should notify the qualifying activity of any decision not to pursue qualification of any material or manufacturing construction technique previously certified. After corrective actions have been implemented, qualification testing should restart.

H.3.4.8 Product qualification (extension from existing qualified technology) . If the manufacturer wants to qualify additional product types from previously QA approved process technologies, the qualification plan shall reference the process technology information (physics-of-failure, description, etc.) and define the specific characterization, screening, and qualification tests required for the new product including the life test duration, conditions, and rationale.

a. Product Qualification (Extension from existing qualified process technology)

1) Plan approval

- i) Screening flow
- ii) Product performance characterization plans and data
- iii) Product qualification test plans and data
- iv) 1,000 hour life test or equivalent

2) Report approval

b. Product qualification for multi-product wafer (MPW):

- 1) When qualifying product from a multi-product wafer (MPW), the manufacturer's shall determine whether each product design shall receive all qualification testing separately, or whether commonality of designs shall allow extension to the other designs on the MPW. Each microcircuit design to be used as an SEC or product shall receive the full applicable QML approved screening flow.
- 2) If any MPW microcircuit design is to be considered for qualification by extension then a technical analysis of the designs shall be documented and approved by the TRB to determine which design is worst case and representative of the other microcircuit designs on the same wafer. Microcircuit designs with different levels of circuit spacing (e.g., digital logic vs. memory cell) or different functionality (e.g., analog to digital converter vs. transceiver) must be qualified separately.
- 3) The following areas shall be evaluated as a minimum to determine if a worst case design is representative of the MPW for the identified qualification test methods of MIL-STD-883.
 - i) SEM inspection shall be performed in accordance with TM 2018, (class level S only): Worst case representative design only.
 - ii) Life test shall be performed in accordance with TM 1005; Full qualification sample on worst case representative design only and 5 (five) pieces sample on all other designs also be tested.

- iii) Total Ionizing Dose (TID) test shall be performed in accordance with TM 1019; Dose rate Latch-up test shall be performed in accordance with TM 1020, and Dose rate Upset shall be performed in accordance with TM 1021 (If applicable): Full qualification sample on worst case representative design and 5 (five) pieces sample on all other designs.
- iv) Electrostatic Discharge (ESD) sensitivity test shall be performed in accordance with TM 3015; Capacitance in accordance with TM 3012; and Electrical Latch-up: Each buffer type shall be tested for initial qualification or buffer design changes.
- v) Single Event Effects (SEE) test shall be performed in accordance with JESD57 (If applicable): Manufacturer's shall test each cell type potentially susceptible for initial qualification or cell design changes.

H.3.5 Standard microcircuit drawings (SMDs) . SMD depicts the Government's requirements for an existing commercial item, tested for a military application, disclosing applicable configuration, envelope dimensions, mounting and mating dimensions, interface dimensional characteristics, specified performance requirements, and inspection and acceptance test requirements as appropriate for a military environment. The general steps of SMD preparation by the preparing activity (PA) are as follows:

- a. Draft Development
- b. User Coordination
- c. SMD Release

H.3.6 Listing of microcircuits on the Qualified Manufacturer's List (QML) . To be listed on the QML for this specification, the manufacturer shall demonstrate compliance to the QML certification requirements (see 3.4.1), demonstrate compliance to the QML qualification requirements (see 3.4.2), and work with the PA, the DLA Land and Maritime, to develop a SMD describing the candidate QML device(s) (see 3.5).

Upon approval of the final draft of the SMD, the manufacturer shall submit a completed certificate of compliance (C of C) to DLA Land and Maritime. Acceptance of the C of C by the qualifying activity results in the device being listed on the QML and provides authority for the manufacturer to ship the QML devices in accordance with the SMD.

Manufacturers are officially QML qualified to a given SMD when the SMD is dated and the C of C and qualification report is approved by the QA. Manufacturers are able to ship SMD devices upon being QML qualified to the given SMD. Manufacturers will receive notification of approval from the QA.

Attachment #4

NEW Appendix K (Next Gen)

Non-hermetic flip chip/ 2D, 2.5D and 3D technology devices requirement

K.1 SCOPE

K.1.1 Scope. This appendix presents the requirements that are to be used to supplement this specification and the other applicable appendices for non-hermetic microcircuits. The manufacturer's process may include innovative and improved processes that result in an equivalent or higher quality product, provided that the process used to evaluate and document these changes has been reviewed and approved by the qualifying activity after coordination with the government space community (e.g., DTRA, NASA, NRO, and AFSMC). The approach outlined in this appendix is a proven baseline that contains details of the screening and technology conformance inspection (TCI) procedures. Manufacturers are to be able to demonstrate a process control system that achieves at least the same level of quality as could be achieved by complying with this appendix. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

K.2 APPLICABLE DOCUMENTS

K.2.1 General. The documents listed in this section are specified of this appendix. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents.

K.2.2 Government documents.

K.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-M-38510 - Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>)

K.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

<u>JEP121</u>	- Requirements for Microelectronic Screening and Test Optimization.
<u>JEP163</u>	- Selection of Burn-in/Life Test Conditions and Critical Parameters for QML Microcircuits.
<u>JESD31</u>	- General Requirements for Distributors of Commercial and Military Semiconductor Devices.
<u>JESD78</u>	- IC Latch-up Test.
<u>JESD471</u>	- Symbol & Label for Electrostatic Sensitive Devices.
<u>JESD625</u>	- Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices.
<u>JESD22-B101</u>	- External Visual.
<u>JESD22-A102</u>	- Accelerated Moisture Resistance - Unbiased Autoclave.
<u>JESD22-A104</u>	- Temperature Cycling.
<u>JESD22-A106</u>	- Thermal Shock.
<u>JESD22-A110</u>	- Highly Accelerated Temperature and Humidity Stress Test (HAST) – biased.
<u>JESD22-B117</u>	- Solder Ball Shear test.

(Copies of these documents are available online at <http://www.jedec.org/> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

ANSI/ESDA/JEDEC JOINT STANDARD

<u>ANSI/ESDA/JEDEC JS-001</u>	- For Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) – Component Level.
<u>ANSI/ESDA/JEDEC JS-002</u>	- For Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level.

(Copies of these documents are available online at <http://www.jedec.org/> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.) or

(Copies of these documents are available online at <http://www.esda.org/> or from Electrostatic Discharge Association(ESDA)
7900 Turin Road, Bldg. 3, Rome, NY 13440.)

ASTM INTERNATIONAL (ASTM)

<u>ASTM D2863</u>	- Standard Test Method for Measuring the Minimum Oxygen Concentration to Support Candle-Like Combustion of Plastics (Oxygen Index).
<u>ASTM F1269</u>	- Test methods for Destructive Shear Testing of Ball Bonds.
<u>ASTM G21</u>	- Standard Practice for Determining Resistance of Synthetic Polymeric Materials to Fungi.

(Copies of these documents are available online at <http://www.astm.org/> or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

K.2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document shall take precedence. Nothing in this document, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

K.3 REQUIREMENTS

K.3.1 General. Microcircuits supplied to this appendix shall be manufactured and tested in accordance with the approved DLA qualifying activity (QA) baselines and the applicable requirements specified herein. Upon approval from the Technology Review Board (TRB) and the qualifying activity (QA), screening and TCI tests may be modified/optimized for qualified manufacturer listing (QML) class N or class Y (class level S) product, provided substantiating data is submitted to demonstrate that the manufacturer has a defined capability on the manufacturing line which is under control, repeatable and reliable to and produces product that that meets the intent of the original requirements. These changes cannot affect any thermal, mechanical or electrical parameters, which affect form, fit, function or radiation hardness assurance level (when applicable) of the device, defined within the device specification or standard microcircuit drawing (SMD). The space community (e.g., DTRA, NASA, NRO, and AFSMC) and the customer shall be notified of major changes to the manufacturer's quality management (QM) plan. Any optimization proposed by the manufacturer must be presented to the qualifying activity and coordinated with the space community with accompanying supporting data to validate the proposed change. The optimization must be approved by the QA in writing prior to implementation. For class N and class Y product marked with RHA designator required to meet appendix C and table C-I group E tests.

K.3.1.1 Acquiring activity. When specified by the acquisition document (purchase order), the acquiring activity may:

- a. Require prior notification of major changes to the baselined processes, procedures, or testing.
- b. Require independent verification of wafers (unprobed) or packaged devices (technology characterization vehicle (TCV), standard evaluation circuit (SEC), or actual devices) by original equipment manufacturer's (OEM's) or Government agencies.
- c. Request screening and TCI summary data is delivered with the devices.

K.3.2 Conflicting requirements. In the event of conflict between the requirements of this appendix and other referenced documents, the order of precedence shall be as follows:

- a. The acquisition document (order).
- b. Applicable device specification.
- c. This appendix.
- d. MIL-PRF-38535.
- e. Specifications, standards, and other documents referenced in [2.1](#) of MIL-PRF-38535.

NOTE: The acquisition document may specify additional requirements, but shall not reduce or waive any requirements herein

K.3.3 Validation (certification). Validation of a manufacturing line for production of integrated circuits for use in space systems shall be accomplished by a team headed by DLA Land and Maritime with members from the space community (e.g., NASA, NRO, DTRA, and AFSMC), other interested services, and the customer as necessary.

K.3.4 Manufacturing verification. When specified, the manufacturing verification procedure for new technology shall include characterization of actual devices at -55°C and 125°C (or high and low temperature as specified in the device specification) with DC, AC and full functional electrical parameters. Life testing of new technologies shall be determined by the manufacturer based on characterization with full temperature testing and read and record measurements every 1000 hours. Characterization shall also include a complete evaluation of potential failure mechanisms and mitigations strategies, calculation or evaluation of activation energy and acceleration factors for voltage and temperature, and establishment of long term reliability failure rates.

K.3.5 Design verification. When specified, a fully functional VHSIC Hardware Description Language (VHDL) or applicable design model shall be available.

K.3.6 Part or identifying number (PIN). Each class N and class Y level QML microcircuit shall be marked with the device class designator "N" or "Y" designator in the PIN format, see 3.6.2a herein. Devices procured to MIL-M-38510 PINs shall be marked in the format in 3.6.2b herein .

K.3.7 Serialization. Prior to the first recorded electrical measurement in screening, each class N and class Y microcircuit shall be marked with a unique serial number assigned within the level of the individual microcircuit within that inspection lot.

K.3.8 Traceability. For class N and class Y, inspection lot records shall be maintained to provide traceability from the device serial number to the specific wafer lot or to the specific wafer when testing to any group E subgroup (see table C-I), is performed on a wafer by wafer basis.

K.3.9 New technology requirement. For class Y product, this is a product family, material, or process that has never been previously characterized and qualified by the manufacturer for space applications, and is detailed in the manufacturer's new technology insertion program (see 3.4.1.1 and 6.4.42). Existing devices that meet the major change criteria of table A-I are to be evaluated in conjunction with the qualifying activity to determine if the change should be classified as a new technology, as defined in 3.4.1.1 prior to finalized qualification plan implementation.

K.3.10 Package integrity demonstration test plan (PIDTP). Manufacturability, test, quality and reliability issues unique to specific non-traditional assembly/package technologies intended for space applications must be addressed in a PIDTP at the start of the package design cycle. The PIDTP shall be approved by QA after consultation with the space community. The technologies requiring such a plan are: a) non-hermetic packages (e.g., class Y, 2D, 3D), b) flip-chip assembly, and c) solder terminations. Microcircuits employing more than one of these technologies shall include elements for each in the PIDTP (see H.3.4.4.1).

K.3.11 Solder terminated microcircuits. Microcircuits employing solder terminations (e.g., Ball Grid Array-BGA or Column Grid Array- CGA) shall meet all applicable appendices and Appendix K herein and must be addressed in the package integrity demonstration test plan (PIDTP) (see H.3.4.4.1.3).

K.3.12 Assembly materials. For BGA and CGA packages material contents for solder balls, bumps and solder columns shall be specified on device SMDs and QM plan (see H.3.4.4.1.3) and organic materials shall be included in the PIDTP if applicable.

K.3.13 For class N device:

- (a) Evaluation of molding compound for glass transition temperature

K.3.14 For organic substrate class Y devices:

- (a) Evaluation of molding compound for glass transition temperature

K.3.15 For 2D, 2,5D or 3D class Y devices:

- (a) Evaluation of molding compound for glass transition temperature

K.3.16 Moisture sensitivity level (MSL). Non-hermetic devices such as class N and class Y can exhibit sensitivity to moisture-induced stress and must be handled, packaged, and stored in a proper manner to avoid potential damage during assembly solder reflow attachment and/or repair operations. Moisture sensitivity levels are defined as a rating identifying a component's susceptibility to damage due to absorbed moisture when subjected to reflow soldering. The manufacturer shall be required to define the moisture sensitivity level (MSL) for each non-hermetic device in accordance with JEDEC J-STD-020

K.4 VERIFICATION

K.4.1 Screening test for class N and class Y . In addition to the screening tests specified in the main body of this specification, the screening tests specified below shall be performed, unless prior approval for deletion or modification is given by the qualifying activity.

- (a) Exemption/addition of screening requirement for class N devices :

- 1) Burn-in test methodology shall be determine in accordance with JEDEC JEP163 and test shall perform per TM 1015 of MIL-STD-883.

- (b) Exemption/addition of screening requirement for class Y flip chip devices devices :

- 1) Burn-in test methodology shall be determine in accordance with JEDEC JEP163 and test shall perform per TM 1015 of MIL-STD-883.

- 2) For flip chip technology SAM inspection is required.

- i) SAM inspection shall be performed on each flip chip device in accordance with TM 2030 of MIL-STD-883.
- ii) SAM test shall be performed on each device when a heat sink or lid is attached directly to the backside of the flip chip die in accordance with TM 2030 of MIL-STD-883.

- 3) Seal test (TM 1014) is not required for class Y non-hermetic class Y flip devices.

(c) Exemption/addition of screening requirement for class Y 2D, 2.5D and 3D devices :

- 1) Burn-in test methodology shall be determine in accordance with JEDEC JEP163 and test shall perform per TM 1015 of MIL-STD-883.
- 2) For flip chip technology SAM inspection is required.
 - i) SAM inspection shall be performed on each flip chip device in accordance with TM 2030 of MIL-STD-883.
 - ii) SAM test shall be performed on each device when a heat sink or lid is attached directly to the backside of the flip chip die in accordance with TM 2030 of MIL-STD-883.
- 3) Seal test (TM 1014) is not required for class Y non-hermetic class Y 2D, 2.5D and 3D devices.

K.4.2 Screening for solder termination microcircuits of class N and class Y . In addition to the screening tests specified in the main body of this specification for solder terminated microcircuits, the screening tests specified below shall be performed, unless prior approval for deletion or modification is given by the qualifying activity.

K.4.2.1 Ball grid array (BGA) microcircuits . For BGA microcircuits post-assembly screening burn-in test may be performed before the solder balls have been attached to the package. Electrical test shall be performed across the full military temperature range after attachment of the solder balls on the package.

K.4.2.2 Column grid array (CGA) microcircuits . For CGA microcircuits post-assembly screening (including electrical test and burn-in) may be performed before the solder columns have been attached to the package. Electrical test shall be performed across the full military temperature range before attachment of the solder columns on the package.

After column attach, electrical test shall be performed at 25°C (Group A, subgroup 1) as a minimum to verify that no electrical/mechanical damage has been introduced due to the column attach process, and visual inspection shall be performed according to TM 2009 of MIL-STD-883.

K.4.3 Technology conformance inspection (TCI) for class N and class Y. In addition to the TCI tests specified in the main body of this specification (see table II to table V), unless otherwise noted herein, the TCI requirements listed below apply on each lot of deliverable devices. The group and table references correspond to those contained herein. These requirements do not replace the normal TCI testing requirements of this specification. The following additions or exceptions apply to the TCI tests specified in the main body of this specification.

Table III, group A electrical test shall be performed on each deliverable lot using actual devices. For those lots having a quantity of less than 116 devices, the tests shall be imposed on a 100 percent basis and the lot accepted on zero test rejects. If a microcircuit fails a group A test parameter as a result of faulty test equipment or operator error, the cause shall be determined and documented, and corrective action shall be implemented and documented. The affected lot may then be accepted by being resubmitted to the failed test parameters using a 116/0 or 100 percent/0 sample. If a microcircuit fails a group A test due to a previously unscreened parameter, the affected lot may be accepted by screening the lot 100 percent for the failed parameters, and resubmitting a group A sample to the failed subgroup using a 116/0 or 100 percent/0 sample. Any failures resulting from the second screen shall count toward the lot total percent defective. PDA shall be in accordance with table III herein or TM 5005 of MIL-STD-883 for class level S.

Group A electrical tests are not required to be performed when the following conditions are met:

- (1) The final electrical tests of the 100 percent screening test (see [table I](#)) includes all required group A tests (see [table III](#)).
- (2) The test setup and test conditions are verified by a certified monitor other than the test operator.
- (3) Analysis of failures does not indicate a generic or lot related reliability problem.

Note: In no event shall the absence of separate group A testing result in a failure to satisfy the data requirements of section [B.3.1.1c](#).

- (a) Exemption/addition of Group A test requirement for class N devices :
- (b) Exemption/addition of group A test requirement for class Y flip chip devices :
- (c) Exemption/addition of group A test requirement for class Y 2D, 2.5D and 3D devices :

a. **Table II, group B**, shall be performed on actual devices except as noted herein. Empty device packages or electrical rejects may be used for subgroups B-1 and B-3, and electrical rejects that have been subjected to the 100 percent screening tests may be used for subgroup B-2. The electrical rejects and empty packages shall have been produced under equivalent conditions as the production lot. The TRB shall determine that the intent of the tests is not violated.

For classes N, V and Y exceptions and additional requirements are as follows:

1. Resistance to solvents test is not required for laser marked device.
2. Device packages with lid/heat sink attached on the backside of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures of lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.
3. Device with solder terminations:
 - (i) For ball grid array (BGA) packages, ball shear test shall be performed in accordance with JESD22-B117.
 - (ii) For column grid array (CGA) packages, solder column pull test shall be performed in accordance with TM 2038 of MIL-STD-883.

b. Table IV, group C or group B, Subgroup 5 life test requirements shall be met using one of the procedures below.

(1) Life test may be performed on a quantity (accept) criteria of 22(0) for 2000 hours at 125°C or equivalent per TM 1005 to attain 44,000 device hours. For lots greater than 200, actual devices shall be used. For lots less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22 unless acceptable group C data from the same lot of SEC is available for the previous 3 months. The SEC shall have been produced under equivalent conditions as the production lot and as close in time as feasible, but not to exceed a 3 month period.

Note: For ASICs, a sample size of 5 actual devices may be used with the balance being made up of the SEC.

(2) Group C life tests shall be performed on the initial production lot of actual devices from each wafer lot, in accordance with [table IV herein](#). Group C life tests are not required to be performed on subsequent production lots when all the following conditions are met:

(a) Subsequent production lots utilize die from the same wafer lot as the initial production lot.

(b) Wafers or die remaining from the initial production lot are to be stored in dry nitrogen or equivalent controlled storage, and in covered containers.

(c) No major changes to the assembly processes have occurred since the group C test was performed on the wafer lot.

(a) Exemption/addition of Group C life test requirement for class N devices :

(b) Exemption/addition of group C life test requirement for class Y flip chip devices :

(c) Exemption/addition of group C life test requirement for class Y 2D, 2.5D and 3D devices :

c. Table V, group D test requirements for package technology style characterization testing (see [table H-IX](#)), and group D testing on the initial production lot utilizing the package family of interest, shall be in accordance with MIL-PRF-38535 and the manufacturer's approved QM plan. A package family consists of a set of package types with the same package configuration (e.g., BGA, CGA), material type (e.g., alumina, beryllium oxide (BeO)), package construction techniques (e.g., single layer, multilayer), ball (bumps) and column spacing with identical package assembly techniques (e.g., material and type of seal, ball attach, underfill, solder bumps or wire bond method and wire size, die attach method and material). All new alternate sources of package elements shall be qualified to the applicable group D tests and shall meet paragraph H.3.4.4.1.

- (a) Exemption/addition of Group D package test requirement for class N devices :
- (b) Exemption/addition of group D package test requirement for class Y flip chip devices :
- (c) Exemption/addition of group D test requirement for class Y 2D, 2.5D and 3D devices :

d. Group E inspection shall be performed in accordance with [table C-I of appendix C](#). Metal oxide semiconductor (MOS) microcircuits, when specified, shall be tested for time dependent effects post total dose irradiation. When 100 percent latch-up screen is specified, the PDA shall be 5 percent or one device, whichever is greater. The devices used for group E testing shall pass the specified group A electrical tests. An alternate procedure to [table C-I group E test](#) may be used upon approval of the qualifying activity.

- (a) Exemption/addition of RHA Group E package test requirement for class N devices :
- (b) Exemption/addition of RHA group E package test requirement for class Y flip chip devices :
- (c) Exemption/addition of RHA group E test requirement for class Y 2D, 2.5D and 3D devices :