

ENGINEERING PRACTICE STUDY

TITLE: High Frequency Microcircuit Devices Burn-in Clock Frequency Requirements under MIL-PRF-38535.

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FINAL REPORT

**Study Conducted by DLA Land and Maritime
Document Standardization Division (VA),
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**EP study on
High Frequency Microcircuits Devices Burn-in Clock Frequency Requirements**

- I. **OBJECTIVE:** The purpose of this Engineering Practice (EP) Study is to obtain input/feedback from the military services, microcircuit manufacturers, OEM and user communities concerning high frequency microcircuit devices burn-in clock frequency requirements in accordance to MIL-PRF-38535 and JEDEC JEP163 Burn-in guideline.
- II. **BACKGROUND:** The burn-in test is performed for the purpose of screening or eliminating marginal devices, those with inherent defects or defects resulting from manufacturing aberrations, which cause time and stress dependent failures.

DLA Land and Maritime and the Space agency have raised some concerns over high frequency devices burn-in where manufacturers did not use an adequate clock frequency as mentioned in the device specification. This issue has been discussed with the manufacturers and JEDEC JC-13.2 burn-in task group with an example "If, the device specification specifies a speed/frequency 200 MHz but the burn-in performed at 6 MHz frequency, is this an adequate burn-in for clock frequency or not?" However, some manufacturers have stated such high frequency burn-in equipment is not available in the market.

For improvement of QML SMD microcircuit devices burn-in test circuits and test conditions manufacturers must adopt appropriate burn-in/life test stress and test conditions such as high speed clock frequency for demonstrating early failure detection and intrinsic failure rate (IFR) during burn-in/life test.

Considering the above issue and JEDEC JC-13 burn-in task group request, DLA Land and Maritime –VAC was launched an EP study for improvement of burn-in practice by adopting high speed clock frequency during burn-in. DLA Land and Maritime –VAC has prepared a survey questionnaire (see attachment # 1) for gathering burn-in data of high frequency devices.

- III. **RESULTS:** DLA Land and Maritime-VAC released initial draft of EP study for high frequency devices burn-in requirements into MIL-PRF-38535 on August 25, 2017 for comments and review. DLA has received comments from high frequency device manufacturers and DLA certified burn-in test laboratory (see attachment #2). All received comments were coordinated with manufacturers and users communities and discussed to the JC-13.2 burn-in task group teleconference monthly meetings, and also discussed comments to the JEDEC JC-13.2 burn-in task group meeting at Savannah, GA on January 2018. During discussion at the meeting with manufactures, users and space communities, the following issues were highlighted:

- ❖ The high frequency devices (e.g. 20 MHz to GHz level) burn-in chambers/ovens are not available at this time.
- ❖ Testing high frequency devices have some technical difficulties such as device may damage their performance during burn-in with the GHz frequency at production level.
- ❖ To acquire those high frequency burn-in oven/chambers are very costly undertaking that may not yield an adequate return on investment.
- ❖ Manufacturers TRB shall be evaluated acceptable burn-in methodology based on devices technology and JEDEC JEP163 document.

After discussion the above issues, task group and space community's members were agreed; (a) Manufacture(s) need to be performed high frequency devices burn-in per device specification listed clock frequency during product characterization phase for initial product qualification. (b) Manufacturer(s) should not be required for high frequency devices burn-in per devices clock frequency at the devices production level. (c) For high frequency devices burn-in test methodology shall be documented to the product QM plan for QA approval.

- IV. **CONCLUSIONS:** DLA Land and Maritime-VAC will update MIL-PRF-38535 by adding high frequency burn-in requirement to the respective paragraphs.

ATTACHMENT # 1

DLA Land and Maritime –VAC has prepared survey questionnaire see below for gathering burn-in data of high frequency burn-in devices. DLA Land and Maritime-VAC and JEDEC JC-13 burn-in task group are requesting high speed devices manufacturers to review following questionnaire and response submit to DLA for improvement of burn-in practice by adopting high speed clock frequency during burn-in.

Questionnaire:

- a) For High Frequency products, (i.e. GHz range) what burn-in method is typically used?
- b) How are the parts evaluated to ensure High Frequency operation over the lifetime?
- c) Since JEP163 requires manufacturers TRB to evaluate acceptable burn-in conditions based on technology, i.e. dynamic or static BI, what addition should be added to JEP163 to address high speed devices clock frequency?
- d) If it is a memory product, dynamic burn-in would be best fit, but at what frequency should they use in actual burn-in chamber?
- e) How are parts characterized if there are equipment limitations (i.e. high frequency oven/chamber are not available)?
- f) For Burn-in of high-speed devices, how are hot spots addressed on the die?
- g) For Burn-in of high-speed devices, how is Case temperature vs Junction temperature addressed?
- h) Please provide your feedback, when manufactures are producing low volume, *high speed device and high speed chamber/ovens may not be available or practical to acquire, what method do you use?*

ATTACHMENT # 2

Comments were received from the Manufactures and Test lab

Questionnaire and received comments:

a) For High Frequency products, (i.e. GHz range) what burn-in method is typically used?

MFR 1 comments: The burn-in systems are limited to < 10 MHz operation. Typical dynamic burn-in during production is performed between 100 kHz to 10 MHz at functional operating point for the device. During characterization testing at speeds higher than 10 MHz, the burn-in boards require modifications to add circuitry using either oscillators or FPGAs in order to insert clock signals with higher speeds; or there may be internal circuitry inserted into the die that ramps up the clock. The use of external circuits added to the burn-in board design or inserted through external supplies is not simple or inexpensive and must be carefully designed and evaluated to ensure other problems, such as thermal runaway or device overstress, are not introduced.

MFR 2 comments: *No single approach is used on all products. Several alternatives are available:*

- *Run BI at <20MHz using Burn in oven's sources, e.g. 5-10MHz clock and input, going into the internal digital SCAN / BIST logic; output signals at the same frequency as the input Max capability is 20Mhz for the AEHR MAX3.*
- *Run BI at <200MHz using external clock/crystal. Difficult to get to get rated crystals upto 150C*
- *Run Dynamic BI with at-speed clocking using internal PLL. Advanced technology nodes may be sensitive to static ageing effects due to NBTI.*
- *Static/dynamic hybrid BI Make the part functional and power up the gates with an input clock. Keep all other inputs static. Keep power supply lines static at max operating voltage.*

There are alternates to B/I – design margins, VBOX, IDDQ, GOI-Stress, overall WLR, BIST, DFT, etc.

The cost delta for a high speed oven may preclude releasing parts for space. In addition third party upscreening using a high speed burn-in will not be effective as the third party will not have a viable test solution for complex products. For example without the test vectors (trade secret) full internal testing of the devices, for example IDDQ measurements, are not possible.

MFR 3 comments: Our company has not engaged in GHz-range product burn-in activity.

MFR 4 comments: The BI system provides low frequency signals to set the device into a high frequency test mode. Dynamic BI performed at the frequency required for the device using an on device clock generator combined with built in self-test to provide the necessary stimulus and coverage.

MFR 5 comments: Depends heavily on the product type since some parts more stress and more areas activated by static BI while some better with dynamic BI. Converters always have dynamic clock BI while some RF parts are OK with just DC bias static forward biased BI.

MFR 6 comments: MFR 6 products: 1 to 3GHz,. Test condition: MIL-STD-883 TM 1005 cond. D

Oven equipment Frequency: up to 20 MHz. Product Burn-in conditions are agreed with customers. Due to the Burn-In Board (BIB) format (570mm X 440mm), and the high DUT positions integration on BIBs, it is not possible to propagate clocks signal more than 20 MHz along them. As BIB are inserted inside a thermal chamber and exposed to temperatures between 85°C-125°C, all DUT components polarizations are passive (capacitors, resistor, diode ...) to ensure a good BIB reliability along successive bath processed. Stimulate DUT with high frequency require local oscillators / buffers near each DUT. These components reliability should be affected by ambient temperature (85°C-125°C). In this case, the ideal solution should be to have a local DUT temperature regulation, but require a dedicate burn-in platform which can affect DUT prices.

MFR 7 comments: Typically; the lowest frequency under which the device is operational is used for burn-in. Maximum frequency is typically not used if the device can be operational at lower frequency as the cost of high frequency burn-in is very high

- If the device has a frequency step-up function (as many FPGAs do); then the device is subjected to burn-in using the lower step-up frequency as this will allow the device to be internally stepped up to the higher frequency
- For some RF devices; if oscillation is a concern; static burn-in is used

MFR 8 comments: Dynamic burn-in at up to 1MHz.

b) How are the parts evaluated to ensure High Frequency operation over the lifetime?

MFR 1 comments: Design simulations are performed to ensure high frequency operation over the device's lifetime. The simulations rely on reliability mechanism data taken on the device technology node. Characterization life test is performed on subset of parts during the device technology V-qualification per MIL-PRF-38535, H.3.4.3.a. We typically submit 77 devices for long term (4000-5000 hours) life test with 22 of the 55 parts running at 75% maximum operating frequency during this characterization life test burn-in. This gives us a direct comparison to the remaining 55 parts that are run at the lower speed production level burn-in. For our technologies, we have not seen any differences between high speed and lower speed burn-in.

MFR 2 comments: *On newer ADC's, some AC parameters can be measured at-speed. But for other high speed devices like interface serdes and Opamp it is difficult to measure on ATE. these are only specified as typical parameters in SMD or datasheet.*

If a hybrid Static/Dynamic BI is used the clock-tree is functional during BI.

MFR 3 comments: Wear out mechanisms are addressed within the circuit design system by our company. The technology characterization and corresponding wear out models (e.g., hot carrier, electromigration) are used in a holistic approach to "design-in" a wear out time that exceeds the fielded-use condition lifetime target.

- Burn-in is done to cull parts from the population of the "early fail mode" portion of the classical bathtub curve. This is done by time-temperature-electric field activation of latent defects.
- Simultaneously applied high-frequency, high-voltage, high-temperature conditions for burn-in can have detrimental effects without improving the efficacy of latent-defect activation.
- Examples of the above could include:
- Added cost for burn in hardware without a corresponding material benefit to activating latent defects.
- Overly-constrained performance. "Designing to succeed" in an over-zealous burn-in stimulus condition that is not relevant in fielded-use conditions may lead to "over-design" and undue compromise of another dimension in the total design trade space.

MFR 4 comments: Life test is using the same dynamic BI circuit/bias. Monitor the chamber parameters and perform endpoint electrical testing per qualification plan and review deltas and drift.

MFR 5 comments: Like any other product tested for 240 hour BI and Group C under selected BI condition. Space products follow QMLV for delta's, PDA, etc. like any product.

MFR 6 comments: Devices are evaluated, qualified and periodically controlled (QCI) using HTOL up to 4000Hrs. Devices are electrical tested before, after and intermediate step at full speed.

MFR 7 comments: Life test

- Structure testing (such as TDDBD; Electro-migration)
- Statistical analysis of data as seen in manufacturing; specially during fabrication and electrical testing

MFR 8 comments: The parts are operated at the highest frequency we can apply in the burn-in oven (1MHz) for 168 hours, unless otherwise specified, and evaluated for degradation after returning to room temperature

c) Since JEP163 requires manufacturers TRB to evaluate acceptable burn-in conditions based on technology, i.e. dynamic or static BI, what addition should be added to JEP163 to address high speed devices clock frequency?

MFR 1 comments:

- JEP163 and the mil-standard test methods should allow for voltage acceleration (in addition to temperature).
- Burn-in times and conditions should be determined using the technology acceleration factors, not taken from a table [add the equations to the test methods].
- The current time/temperature tables in MIL-STD-883, Methods 1005 and 1015 should be updated to be consistent with industry accepted acceleration factors ($E_a = 0.7\text{eV}$ for older technologies with unknown technology based factors).
- Alternates to burn-in should be allowed based on the technology failure modes [and justification by the manufacturer].

MFR 2 comments: *A note for high frequency devices that would allow running at lower frequencies for dynamic BI.*

MFR 3 comments: We are of the opinion that JEP163 need not be updated. "High frequency" and "burn in activation of latent defects" can remain "orthogonal" to each other in the set of activities that must be addressed to produce high reliability products. (If there are latent defects that are revealed only substantially by high-frequency stimulus, the "physics of failure" mechanisms should be described, and recommended screening test methods and considerations should be added to JEP163.)

MFR 4 comments: Manufacturer needs to have the flexibility to define how they will meet the requirements to cull out infant mortality and wear out mechanisms.

MFR 5 comments: It should clarify that dynamic involves AC forward bias signals and static means on DC bias applied. The DC HTRB (high Temp Reverse Bias) no longer applied to modern complex IC's and can't be used due to ESD circuits that would be damage the IC's in HTRB. The Mfg should determine which BI condition is best and only use both BI circuits if there is some value added. Doing 2 pass BI rarely adds any additional quality value and in fact adds more risk of inducing damage unnecessarily

MFR 6 comments: Nothing specific to add, TRB including "Burn-in conditions based on technology" is a good requirement

MFR 7 comments: JEP163 does not address RF burn-in which are typically high frequency burn-in. It should be addressed in this document.

- JEP163 should address failure modes associated with technologies as it applies to high speed. Just to do high speed burn-in for the sake of doing high speed burn-in; is not practical. Manufacturers should do studies to find what are the potential failure modes associated with their technologies and what burn-in conditions; if any; provided the most optimal infant mortality screening
- Voltage acceleration studies should also be considered along with temperature acceleration if that helps in keeping the frequency of the burn-in reasonable

MFR 8 comments: The primary problem with high-speed dynamic burn-in is the inherent RC filter between the signal generator and the parts under test. The signal generator has a non-zero output impedance, the wiring between the generator and each part is resistive with a parasitic distributed capacitance to adjacent traces, and the input of each part under test has an associated capacitance. The path between the generator and the parts is, in effect, an integrator. A signal that leaves the generator as a square wave with sharp edges is received at each part as, at best, a squarish wave with sloping rising and falling edges and rounded tops and bottoms. As the number of parts increases or the distance from the generator to the parts in the oven lengthens, the problems become more severe. The frequency at which the rise and fall times at the inputs of the parts can't keep up with the rise and fall times at the output of the signal generator is the slew-limit frequency. At some higher frequency, the rising and falling edges at the inputs don't have time to swing all the way from a logic high to a logic low or vice-versa before the signal switches again, and the parts under test no longer see a valid input signal. The input signal is wobbling in the invalid region, causing unpredictable things to happen in the parts and probably greatly increasing the power supply currents in the parts. The frequency at which this occurs is the full-power bandwidth of the signal-forcing system and marks the absolute maximum operating frequency of the burn-in system. It is dependent on the output characteristics of the signal generator, the distance and characteristics of the wiring/traces between the generator and the board(s), the number of boards, the number of sockets on each board, the number of parts in those sockets, and the input characteristics of the parts under test. This can be partly alleviated by having a separate clock driver for each board, or even a separate driver for each subset of sockets on each board. Based on this, JEP163 might specify that the burn-in be performed for a minimum number of clock cycles, rather than a set time, although the two factors probably are not independent. Burning 1GHz parts in for a thousand times as long because only a 1MHz system is available is probably not realistic, but a relationship between cycles and time could likely be determined through experimentation. As a side note, if the burn-in circuit depends on coordinating different input and clock signals, the problem becomes much worse and the maximum operating frequency will almost certainly have to be reduced.

d) If it is a memory product, dynamic burn-in would be best fit, but at what frequency should they use in actual burn-in chamber?

MFR 1 comments: same response as a) above.

MFR 2 comments: *At max speed.*

MFR 3 comments: Technology and product-specific fail modes must be considered. It is incumbent upon any "New Technology" plan is to address this topic. MIL-PRF-38535 already addresses this nicely by defining the "New Technology Certification and Qualification" requirements. The latitude exists to tailor one's qualification plan and qualification criteria according to one's technology and product-specific fail modes. The structure of the reviews and the practice of employing industry subject matter experts to conduct in-depth, critical reviews works well. Any attempts to apply a "one fits all" definition of "requirements" is doomed to fail given the breadth and heterogeneity of subjects. However, for the technologies Honeywell has qualified, high speed burn-in has not been an effective screen for the technology fail modes. Most defect types are not accelerated by frequency. The ones that might be (e.g., electromigration) are not readily exposed in a burn-in environment, and are better addressed by design and process controls.

MFR 4 comments: The manufacturer needs to consider the technology to determine how best to design and burn-in the device.

MFR 5 comments: At whatever frequency and condition that ensures operating stress under normal use, normally at some reasonably high clock to ensure digital switching current and power used like customer application.

MFR 6 comments: N/A

MFR 7 comments: This can only be determined by performing burn-in at various frequencies and by technologies.

- Also; it is important to know what is the failure mode associated with the technology (adjacent bit failures or refresh failures or charge pump related failure mode etc.). There needs to be design of experiment to determine the optimal frequency, temperature and voltage

MFR 8 comments: Whether it is a memory product or a product with a clock and switching inputs, the operating frequency can be no higher than that at which all data transfer and set-up and hold times can be guaranteed. This will differ from part to part.

e) How are parts characterized if there are equipment limitations (i.e. high frequency oven/chamber are not available)?

MFR 1 comments: The technology failure modes should be understood to define the best methods to screen out infant mortality and early failures. If burn-in is effective and since burn-in systems are limited in operation, external circuits may be required to be added to the burn-in board design or through external supplies; this is not simple or inexpensive and must be carefully designed and evaluated to ensure other problems, such as thermal runaway or device overstress, are not introduced.

MFR 2 comments: *The limitation is only in the burn-in oven. Electrical parametric testing and bench testing can be done at full operating frequencies.*

MFR 3 comments: Laboratory (non-production), means are mostly used. Tests, samples and techniques for characterization are addressed to achieve QML Certification. Production tools (automatic test equipment) are also used, but perhaps in a "non-recurring, characterization" mode. Again, the tests, samples and techniques for characterization are addressed to achieve QML Certification.

MFR 4 comments: See a) above.

MFR 5 comments: problem is the limitations from layout and clock distribution. Corrupt RF signals worsen and are hard to maintain so if reduced frequency you can show same biasing, Max J as higher frequency, should accept that. IF switching causing higher power, then that should be considered. Goal of always to stress part under reasonably normal bias, not try to force to abs max Tj

MFR 6 comments: All critical parameters of T-e2v devices are characterized in worst temperature and supply conditions up to or beyond full speed.

MFR 7 comments: Depends upon the failure mode that is being targeted. Sometimes; it is not possible to characterize a device for high speed failure mode if high speed burn-in oven is not available.

- Sometimes; if failure modes are known and understood for high speed burn-in; die transistor level testing is possible to understand if potential to high speed burn-in failure mode exists.

MFR 8 comments: As in b), the parts are operated at the highest frequency we can apply in the burn-in oven (1MHz) for 168 hours, unless otherwise specified, and evaluated for degradation after returning to room temperature.

f) For Burn-in of high-speed devices, how are hot spots addressed on the die?

MFR 1 comments: Design simulation can look at some hot spots or average increases in temperature. There are thermal imaging systems that could be developed but expensive and not very practical [JPL has one]. Typically, characterization parts are run through burn-in at maximum operating or stress conditions (temperature, voltage, and/or frequency) and evaluated by pre- and post-stress electrical test.

MFR 2 comments: *Another reason to go with lower speed if needed to keep die under 150C. it is usually difficult to predict exact temp of a portion of die.*

MFR 3 comments: We have used infrared imaging and simulation techniques to address hot-spot confirmation and/or detection. This is an activity that is best undertaken as a specific study.

MFR 4 comments: Evaluate during die and package design modeling/simulations. Use thermal monitoring and management during burn-in.

MFR 5 comments: thermal analysis or thermal camera data or Finite Element Modeling software to check Max Tj in BI based on hottest die location.

MFR 6 comments: Mainly, the mean DUT temperature cases are considered. If there are special hot spots to consider in the burn-in setup, we refer to product burn-in specification that can notice the temperature gap between the junction and the hot spot that we do not have to exceed. The final burn-in temperature will be set during the temperature evaluation according to these limitations

MFR 7 comments: May be by exercising the device completely at high speed; high temperature and full datasheet voltages; and then performing a post-stress electrical test

MFR 8 comments: If we know the temperature rise of the hottest part of the die, and know how that temperature increase relates to frequency, the burn-in temperature is reduced to avoid exceeding the maximum junction temperature.

g) For Burn-in of high-speed devices, how is Case temperature vs Junction temperature addressed?

MFR 1 comments: Some die contain thermal diodes specifically for this purpose. Case temperature may be measured using a thermal couple. Knowing the package thermal resistance can also be used to determine the case to junction temperature. In any case, the absolute maximum junction temperature for the device must not be violated.

MFR 2 comments: *MFR 2 performs actual measurement of case temp and uses package thermal characteristics to determine the estimated junction temp. Oven temperature is adjusted so Tj does not exceed 175C for space products, or 150C for others.*

MFR 3 comments: We often use case (from a thermocouple or RTD) temperature and junction (from an on-chip diode) temperature tracking to assure a desired state is attained for each hardware configuration.

MFR 4 comments: Our understanding and management of Theta JC through package design techniques allow us to manage the case temperature in burn-in and control the associated junction temperature.

MFR 5 comments: we usually specify T case and check via eng analysis what Max Tj is per MMethod 1015 requirements

MFR 6 comments: Mainly, the DUT temperature case target is fixed to 125°C. During engineering activities, we characterize the case and junction temperatures through different oven chamber set point.

MFR 7 comments: Junction temperature should be measured whenever possible. Many times; the temperature diode within the device is accessed and used to calculate the junction temperature

- Knowing the thermal resistance of the package also will allow to determine the junction temperature
- It is imperative that junction temperature is not violated during burn-in

MFR 8 comments: The air temperature in the oven is controlled to avoid exceeding the maximum junction temperature. The case temperature goes where it will.

h) Please provide your feedback, when manufactures are producing low volume, *high speed device and high speed chamber/ovens may not be available or practical to acquire, what method do you use?*

MFR 1 comments: The better the wafer manufacturing processes are controlled (using SPC controls, reduction/elimination of defects, etc.) and with improved design practices (to eliminate critical failure modes such as electromigration, NBTI, TDDB, hot carriers), then less is the need for burn-in. Alternates to burn-in may be used for failure modes not eliminated by design or process control. Voltage acceleration and/or statistical methods are successful in screening out bad parts. Today, we use combination of these in addition to modified burn-in systems as defined above.

MFR 2 comments: *We have tried to use on board crystal oscillators but our approach is to see if we can run at low freq if possible. An alternative is through process qualification and modeling.*

MFR 3 comments: We have used circuit-design approaches that comprehend the burn-in system stimulus capability, the chip characteristics and the intended application and warranted life. In combination, a “design for burn-in” outcome is realized.

MFR 4 comments: Alternatives are to out-source to a lab with the capability or develop an internal capability.

MFR 5 comments: *IF same bias and stress conditions based on knowledge of product can show good BI conditions to eliminate early life failures and Group C, then OK. IF required, design RF circuits that work over temp which is very expensive and complex adding to cost and lead time for development. This can make products overly expensive if the BI is overkill vs. what is good eng judgement. For non-QML products, ADI will typically dynamically exercise using a low frequency stimulus (low MHz range where RF effects are minimal and may be ignored.*

FR 6 comments: See a)

MFR 7 comments: If the failure mode of the part shows high frequency dependency; then the only way to not do any infant mortality burn-in at high temperature is to make manufacturing process so robust that such failures are eliminated during manufacturing and hence; so; infant mortality would be required. This would require a SPC based monitoring system

MFR 8 comments: When we don't have and can't acquire an appropriate oven we contract with a local company with the necessary equipment to burn the parts in for us per our instructions.

MFR comments: The manufacturer knows how to best ensure the quality and reliability of their product.

- Proper design and development mitigates the need to perform high speed burn-in
- There are other test techniques used that do a better job ensuring individual device reliability.
- There are significant technical hurdles to performing high speed burn-in in production.
- High speed burn-in needs to be evaluated carefully as it can damage devices if not done properly.
- High speed production burn-in is a very costly undertaking that may not yield an adequate return on investment.
- The justification for burn-in conditions used need to be documented in the product release by the manufacturer. Screening used to augment burn-in such as VBOX, GOI, IDDQ, etc. should be part of this justification.

Questions were to the DLA certified labs TM1005/1015 (burn-in) of MIL-STD-883:

1) Currently, do you have capability to perform burn-in of high frequency microcircuit devices (Range 5 MHz to 3 GHz)?

Test Lab 1 Comments: Our standard burn-in system in Singapore plant can support maximum frequency of 25 Mhz. For product requiring beyond 25Mz will have on site crystal or using customise driver to generate required frequency. Most product are burn-in at frequency below 10 MHz . Our burn-in system in Bangkok plant can support maximum frequency of 32 MHz per driver board. So far products run are mostly EPROM with frequency requirement of 500 KHz or 1 MHz only.

Test Lab 2 comments: Yes; we do.

Test Lab 3 comments: No, we currently do not have the capability range. We can reach 20 MHz.

Test Lab 4 comments: Systems at Milpitas are not configured for high frequency now, but could be if \$\$ made sense. Some systems at Wichita are configured for high frequency burn-in. Cost of hardware goes up to support the higher frequencies and part density per board will go down also effecting cost.

2) Currently, TM1015/1005 dynamic burn-in condition D (parallel excitation) required the excitation frequency shall not be less than 60 Hz means no upper limit clock frequency .

Test Lab 1 Comments: :Nearly all product are burn in above 60 Hz except static burn-in device requiring no signal frequency. Upper limit clock frequency should be set in standard for industry to follow product spec requirement.

Test Lab 2 comments: In reality; there is an upper limit and it is technology, device and cost dependent. For example: If we have a device that is 40 GHz; even if we can apply the 40 GHz biasing; we have to worry about potential oscillation or other issues that could potentially damage the device; so; we have to be very careful on what maximum frequency or biasing scheme we apply. At some point; the cost becomes extremely expensive; so; we have to choose the most optimal frequency (still at various GHz level) that will provide very high level of stimulus and still be somewhat cost acceptable

Test Lab 3 comments: 60 Hz is not an issue.

Test Lab 4 comments: Most typical burn in systems and boards can get to 1MHz. Going above this frequency increases the cost of the system and boards. The higher the frequency the higher the cost. Would not be unreasonable for BIBs to start costing \$40K to \$50K US each, if each device on a BIB was required to receive clean signals above 200 MHz. The original purpose of burn-in to use electrical bias and temperature to accelerate the failure mechanism of the device material, not to test the device during burn-in. High frequency should only be required if that is the only way to activate this failure mechanism.

3) What is your comments /feedback to perform burn-in of high frequency microcircuit devices (Range 5 MHz to 3 GHz)? .

Test Lab 1 Comments: :Frequency for burn-in need to follow product spec.

For massive parallel burn-in has to be done well below 25Mhz due to device loading and length of printed wire trace.

If for engineering reason required to perform burn-in at high frequency burn-in, specialise burn-in board and system has to build, driving burn-in cost exponentially.

Test Lab 2 comments: (1) It is expensive, (2) It is doable, and (3) Should have experienced hardware and device people on staff who understand issues associated with high speed burn-in and life test

Test Lab 3 comments: It will be difficult and cost prohibitive to reach such high frequency.

Test Lab 4 comments: Will increase cost of the systems and BIBs. Again, the intent of burn-in is to stress the device under bias to weed out infant mortality failures. If a device has a failure mechanism that requires a high speed/frequency clock to "toggle" some element of the device to force this failure, then it makes sense. Typically most devices only require a much simpler electrical bias under temp. to accelerate the failure mechanisms that are then caught at the post burn-in test, using ATE and hardware that has been designed to test at high speeds.

4) Is it reasonable to update/revision of MIL-PRF-38535 and test method TM1015/1005 of MIL-STD-883 to incorporate high frequency devices burn-in requirement?

Test Lab 1 Comments: Product design reliability engineer to determine external frequency required to test the device. Device may have internal frequency generator to exercise the device.

Burn-In frequency must be at a frequency to maximize the reliability test coverage of device.

It is reasonable to update the standards so that burn-in can screen out devices that do not meet product spec and reliability.

Test Lab 2 comments: Yes; it is reasonable to update these documents. Our fear is that unreasonable requirements will be put into the documents and these new requirements may not technically feasible to implement or become a cost prohibitive issue for the user or the manufacturer. So; it is imperative that the update be well thought out. It should also address detection of potential failure modes associated with various technologies as it applies to high speed. The added requirements should be based on studies that have proven how the potential failure modes associated with their technologies detected.

Test Lab 3 comments: If the specs are amended to these standards, it will be difficult to attain.

Test Lab 4 comments: It is reasonable to do so, if there are legitimate reasons to stress certain devices at high frequency/speed during burn-in. In any event, it should not be a blanket requirement that all devices must be electrically stressed at end application speed during burn-in.