

ENGINEERING PRACTICE STUDY

PROJECT NUMBER: 5961-2025-112

TITLE:

MIL-STD-750-4, TEST METHOD 4086
"THERMAL RESPONSE TESTING OF DIODES"

PROPOSAL TO DEVELOP A NEW METHOD TO ADDRESS
LEGACY THERMAL RESPONSE TEST METHODS
PREVIOUSLY COVERED IN METHOD 3101 OF MIL-STD-750-3

31 JANUARY 2026

FINAL REPORT

STUDY CONDUCTED BY

DLA WEAPONS SUPPORT
Document Standardization Division (VA)
Active Device Branch (VAC)

Prepared by:
David Corbett
Electronics Engineer
Active Devices Branch

Approved by:
Muhammad Akbar
Chief
Active Devices Branch

ATTACHMENTS 1

I. OBJECTIVES: The objective of this Engineering Practice (EP) Study was to obtain input from users (military services, device manufacturers, laboratories, and user community) concerning a proposed new test method 4086 to be added to MIL-STD-750-4.

II. BACKGROUND: The final report for EP Study concentrating on revising method 3101 of MIL-STD-750-3 (project 5961-2021-020) recommended that since the proposed revision was so different than the existing method (3101.5 as it existed in 2021), that a new method be coordinated for addition as method 4086 of MIL-STD-750-4. However, during many JEDEC 13.1 Technical 750 Test Method Review task group meetings, there were discussions that the new testing method proposed by the EP Study draft be merged with the existing method so that no changes would need be made in MIL-PRF-19500 for the test method number (3101). After over 3 years of attempting to implement this request, DLA suggested that this was not possible and that another solution needed to be pursued. During a recent JEDEC 13.1 Technical 750 Test Method Review task group meeting, a new proposal was suggested to move the existing 3101.6 to MIL-STD-750-4 and identify it as method 4086 and if that endeavor was successful, issue the test method draft of EP Study 5961-2021-020 as method 3101.7 in MIL-STD-750-3. DLA agreed that this new course of action would be more realistic and attainable. DLA developed a draft of the proposed "new" method 4086, which is basically a revision of the current 3101.6. This draft of the new method includes a few editorial and format changes from the current 3101.6 that DLA made to clarify requirements and enhance the useability of the method.

III. RESULTS: The draft of the new method was coordinated to military, industry and user community. All comments received from the initial draft during the review period regarding the new method were accepted and have been incorporated into the final report draft method (see attachment 1).

A Key that identifies the changes that were made to the final report draft method due to comments received from the initial draft have been included at the top of the first page of the attachment.

IV. CONCLUSIONS: The final report draft test method should be proposed for incorporation into the next standardization action to MIL-STD-750-4.

V. RECOMMENDATIONS: Prepare an initial draft of MIL-STD-750-4 using the results of this study for the new test method 4086.

The point of contact for this final report is Mr. David Corbett, DLA Weapons Support VAC, P. O. Box 3990, Columbus, OH 43218-3990. Mr. Corbett can also be reached at 614-693-0168/DSN 614-392-0168 or by electronic mail at: 750.TestMethods@dla.mil.

KEY to changes:

Text that was part of the Initial Draft is just plain black text with white background.

Text that was added for the Final Report as a result of comments to the Initial Draft are highlighted in green.

Text that was proposed to be deleted in the Final Report as a result of comments to the Initial Draft are shown as red text with straight-out.

ATTACHMENT 1 TO FINAL REPORT EP STUDY 5961-2025-112
31 JANUARY 2026

METHOD 4086.0

THERMAL RESPONSE TESTING OF DIODES

1. Purpose. The purpose of this test is to determine the thermal response of semiconductor diode devices using legacy methods and apparatus. The tests of this method can be applied to rectifier diodes, transient voltage suppressors, power Zener diodes, and some zener, signal, and switching diodes. All these different types are hereafter referred to as 'device' or 'devices'.

1.1 Scope. The thermal response testing of devices can be done in two ways, steady-state thermal impedance or transient thermal impedance testing. Steady-state thermal impedance (referred to as 'thermal resistance') determines the overall thermal performance of devices. Transient thermal impedance (referred to as 'thermal impedance') determines the time dependent thermal factors of devices. A production-oriented screening process, referred to as thermal transient testing, is a subset of thermal impedance testing and is addressed herein. Thermal response is measured in °C/W. This quotient measures the change in junction temperature in degrees Celsius Centigrade as a result of a known power level in watts applied to the DUT for a specific heating time. The junction temperature measurements are achieved by a temperature sensitive parameter (TSP) or what is often the forward voltage with a known temperature characteristic at a specific measuring current. The thermal response is most often only the measurement of the change in volts of the TSP with a specified power and heating time that can also be equated to a junction temperature change in °C. Thermal response testing of devices determines the ability of the chip-to-package interface to transfer heat from the chip to the package and is a measure of the thermal quality of the chip attachment. It is relevant to designs that use either headers or heat conducting plugs, with mass and thermal conductivity allowing effective discrimination of poor chip attachments. This is particularly true with power devices.

1.2 Applicability. The thermal response tests of this method are intended for incoming inspection, production monitoring, and pre-burn in screening applications. Some Zener constructions, particularly when used with small junction area designs, cool to rapidly from the cessation of heating current to provide accurate measurement when forward direction (diode) current is used for this test. For such devices, a method is provided to apply currents in the zener direction and make a measurement much closer to the termination of the heating current. In this way, no minority carriers are involved, and inductive effects are minimized due to lower test current. This may be considered a laboratory measurement since cable lengths on ATE may prevent accurate measurements so close to cessation of the heating current.

2. Overview.

2.1 Background for thermal response testing. Steady-state thermal impedance and transient thermal impedance of semiconductor devices are sensitive to the presence of these voids in the die attachment material between the semiconductor chip and package since voids impede the flow of heat from the chip to the substrate (package). Due to the difference in the thermal time constants of the chip and package, the measurement of transient thermal response can be made more sensitive to the presence of voids than can the measurement of steady-state thermal response. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the package. Thus, the heating power pulse width can be selected so that only the chip and the chip-to-substrate interface are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant but less than that of the substrate. Heating power pulse widths ranging from 1 ms to 400 ms for various package designs have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with the added advantage of not having to heat sink the DUT. Thus, the transient thermal impedance or thermal response techniques are less time consuming than the measurement of thermal resistance for use as a manufacturing screen, process control, or incoming inspection measure for chip attachment integrity evaluation.

Revision A Change-X resulted in this new test method.

METHOD 4086

2.2 Organization of this method. This test method details methods of measuring the thermal response of devices that ~~is~~ **are** described in section 5. It also offers examples and guidelines for characterizing and testing covered in appendices A through D as follows:

Appendix A covers thermal impedance production screening guidelines.

Appendix B details thermal impedance testing and thermal characterization guidelines.

Appendix C explains the measurement of the TSP.

Appendix D focuses on a backward t_{md} projector calculation method.

3. Abbreviations, and definitions, equations, and symbols. The following abbreviations, definitions, equations, and symbols shall apply for the purpose of this test method in the forward direction.

3.1 Abbreviations. The following abbreviations are used in this test method.

- a. FEA Finite element analysis.
- b. TCZ Temperature compensated Zeners.
- c. VTC Voltage-temperature coefficient.

3.2 Symbols. The symbols common with both the forward and reverse directions of testing of the TSP are listed in 3.2.1. The symbols associated with forward direction testing of the TSP are listed in 3.2.2. The symbols associated with reverse direction testing (using the Zener biased direction) of the TSP are listed in 3.2.3. See 3.2.4 for symbol substitution difference between the forward and reverse direction.

3.2.1 Common symbols. The following symbols are common for both the forward and reverse direction testing:

- a. CU The comparison unit, consisting of ΔV_F divided by V_H , that is used to normalize the transient thermal response for variations in power dissipation.

NOTE: The typical units for CU are mV/V.

- b. K Thermal calibration factor equal to the reciprocal of α_{VF} .

NOTE 1: K must be measured over a temperature range similar to the test temperature range at an I_M that will permit resolution at the highest temperatures reached during the test.

NOTE 2: The typical units for K are °C/mV.

- c. P_H The product of V_H and I_H during the heating pulse.
- d. $R_{\theta JA}$ Thermal resistance from device junction to the ambient T_A .

NOTE: The typical units for $R_{\theta JA}$ are °C/W.

- e. $R_{\theta JC}$ Thermal resistance from device junction to a point on the outside surface of the case immediately adjacent to the device chip.

NOTE: The typical units for $R_{\theta JC}$ are °C/W.

- f. $R_{\theta JX}$ Thermal resistance from device junction to a defined reference point.

NOTE: The typical units for $R_{\theta JX}$ are °C/W.

ATTACHMENT 1 TO EP STUDY 5961-2025-112
31 JANUARY 2026

MIL-STD-750-4

- g. T_A Ambient or free-air temperature, the air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.
- NOTE: Testing has historically been performed in an open laboratory or on the production floor subject to natural convection and air movement produced by HVAC (heating, ventilation and air conditioning) common to all industrial locations. Any air movement in excess of 1.0 m/s must be blocked.
- h. T_{EC} The temperature of the end cap of a surface-mount package.
- i. t_H The duration of P_H applied to the DUT.
- j. θ A term sometimes used in place of the symbol Z_θ in some art and associated text in this document.
- k. T_J The junction temperature of the DUT.
- l. t_{MD} Measurement delay time, the time from the start of P_H removal to the start of the final V_F measurement time (referred to as t_{SW}).
- NOTE: Delay shall be sufficient in length to allow for attenuation of switching transients to occur. The delay time will vary according to the length of the cable to test fixture (short is always better), associated fixture inductances, package magnetic properties and chip charge storage properties. See further clarification of the use of t_{MD} in this method and in [appendix D](#).
- m. TSP The temperature sensitive parameter of V_F or V_Z .
- n. t_{SW} The sample window time during which final V_F measurement is made.
- NOTE: The value of t_{SW} should be small; it can approach zero if an oscilloscope is used for manual measurements.
- o. $Z_{\theta JC}$ Thermal impedance from device junction to a point on the outside surface of the case immediately adjacent to the device chip.
- NOTE 1: $Z_{\theta JC}$ is measured over a time interval equal to the time constant of the device.
- NOTE 2: The typical units for $Z_{\theta JC}$ are $^{\circ}\text{C}/\text{W}$.
- p. $Z_{\theta JX}$ Thermal impedance from device junction to a time defined reference point.
- NOTE 1: The typical units for $Z_{\theta JX}$ are $^{\circ}\text{C}/\text{W}$.
- NOTE 2: Z_θ has been called "theta" in some art and associated text in this document.
- q. α_{VF} The temperature coefficient of V_F with respect to T_J at a fixed value of I_M .
- NOTE: The typical units for α_{VF} are $\text{mV}/^{\circ}\text{C}$.
- r. ΔT_J The change in T_J caused by the application of P_H for a time equal to t_H .

3.2.2 Forward direction. The following symbols and definitions apply for the purpose of this test method in the forward direction.

- a. I_H The current applied to the DUT during the heating time to cause power dissipation.
- b. I_M The measurement current used to forward bias the temperature sensing diode junction for measurement of V_F .

NOTE: See the introductory comments above when using the Zener direction for the TSP.
- c. V_F The forward biased junction voltage of the DUT used for junction temperature sensing or TSP.

NOTE: See introductory comments above when using the zener direction for the TSP.
- d. V_{Ff} The final V_F value after application of heating power (P_H).
- e. V_{Fi} The initial V_F value before application of heating power (P_H).
- f. V_H The heating voltage resulting from the application of I_H to the DUT.
- g. ΔV_F The change in the TSP, V_F , due to the application of P_H to the DUT.

3.2.3 Reverse (Zener biased) direction. The following symbols and abbreviations apply for the purpose of this test method in the reverse direction.

- a. V_Z The Zener voltage.
- b. V_{ZL} The zener voltage of the DUT used for junction temperature sensing or the TSP.
- c. V_{ZLf} The final V_{ZL} value after application of heating power (P_H).
- d. V_{ZLi} The initial V_{ZL} value before application of heating power (P_H).
- e. ΔV_{ZL} The change in the TSP, V_{ZL} , due to the application of P_H to the DUT.

3.2.4 Variable substitutions when using the reverse (Zener bias) direction. When using the reverse (Zener bias) direction as the TSP, instead of the forward direction, the following changes shall further apply to the definitions and formulas in this test method whenever they appear in the text:

Letter symbols	I_F	is replaced by	I_Z
	V_F	is replaced by	V_{ZL}
	V_H	is replaced by	V_{ZH}
	V_{Fi}	is replaced by	V_{ZLi}
	V_{Ff}	is replaced by	V_{ZLf}
	ΔV_F	is replaced by	ΔV_{ZL}
	V_{F1}	is replaced by	ΔV_{Z1}
	V_{F2}	is replaced by	ΔV_{Z2}

Wording: The phrase 'forward bias' is replaced by the phrase 'reverse bias'.

NOTE: ΔV_F , K, and CU parameter values will be substantially different when using the Zener direction. Some difference will be observed between zeners with different nominal voltages.

MIL-STD-750-4

3.3 K factor equation. The K factor is calculated in accordance with the following equation:

$$K = \left| (T_{J2} - T_{J1}) / (V_{F2} - V_{F1}) \right| \text{ } ^\circ\text{C/mV}$$

Where:

- a. T_{J1} = Initial junction temperature in $^\circ\text{C}$
- b. T_{J2} = Final junction temperature in $^\circ\text{C}$
- c. V_{F1} = Initial V_F voltage in mV
- d. V_{F2} = Final V_F voltage in mV

See [appendix C](#) for examples, methods, and procedures of measuring the K factor using the TSP.

4. Apparatus. The apparatus required for this test shall include the following, configured as shown on figure 4086-1, as applicable to the specified test procedure:

- a. A constant current source capable of adjustment to the desired value of I_H and able to supply the V_H value required by the DUT. The current source should be able to maintain the desired current to within ± 2 percent during the entire length of heating time.
- b. A constant current source to supply I_M with sufficient voltage compliance to turn the TSP junction fully on.
- c. An electronic switch capable of switching between the heating period conditions and measurement conditions in a time frame short enough to avoid DUT cooling during the transition; this typically requires switching in the microsecond or tens of microseconds range.

NOTE: A single programmable current source can be used in lieu of the switch and two independent current sources of subparagraphs a, b and c.

- d. A voltage measurement circuit capable of accurately making the V_{Ff} measurement within the time frame with millivolt resolution.

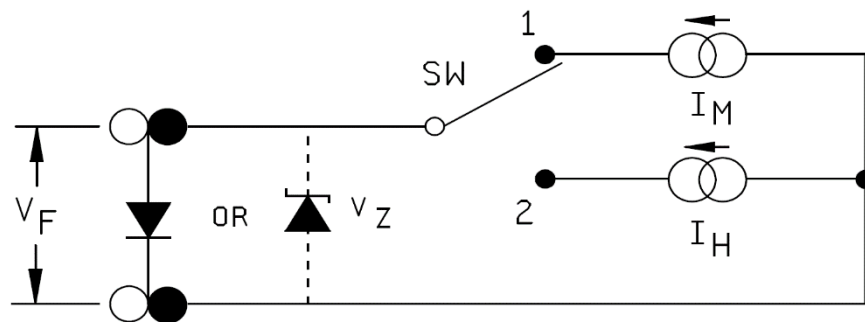


FIGURE 4086-1. Thermal impedance testing setup for diodes.

MIL-STD-750-4

5. Detailed requirements.

5.1 Thermal impedance test operation. The procedure of 5.2 covers single junction chips and the procedure of 5.3 covers chips with multiple junctions. These procedures are considered to be laboratory methods.

5.1.1 Forward direction. The test procedures of 5.2 and 5.3 details the use of discrete test instrumentation of 4 using the forward direction test circuit of figure 4086-1 and waveform on figure 4086-2.

5.1.2 Reverse direction. The test circuit of figure 4086-1 and waveform on figure 4086-3 detail testing in the reverse (Zener bias) direction. When using the reverse direction, correlation assurance shall be provided in the forward production monitoring that thermal impedance in the reverse direction shall not exceed the specified limit.

5.2 Characterization of single junction devices.

5.2.1 General description. The following details the requirements for thermal impedance testing devices with chips that use a single junction design. See appendix B for guidelines on selecting values of I_H , I_M , t_H , and t_{MD} .

5.2.2 Procedure. The testing of single junction devices is summarized as follows: With the DUT in the test circuit (see figure 4086-1), the test begins with the adjustment of I_M and I_H to the desired values (see figures 4086-2 and 4086-3). The value of I_H is usually at least 50 times greater than the value of I_M . Then with the electronic switch in position 1, the value of V_{Fi} is measured. The switch is then moved to position 2 for a length of time equal to t_H and the value of V_H is measured. Finally, at the conclusion of t_H , the switch is again moved to position 1 and the V_{Fi} value is measured within a time period defined by t_{MD} (or $t_{MD} + t_{sw}$ depending on the definitions stated previously). The two current sources are then turned off at the completion of the test.

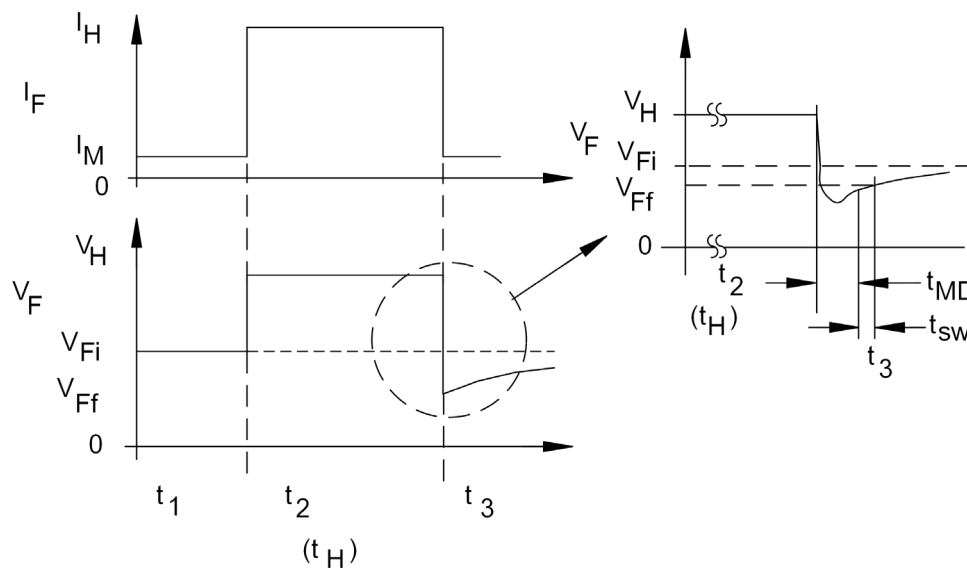


FIGURE 4086-2. Thermal impedance testing waveforms for forward biased methods.

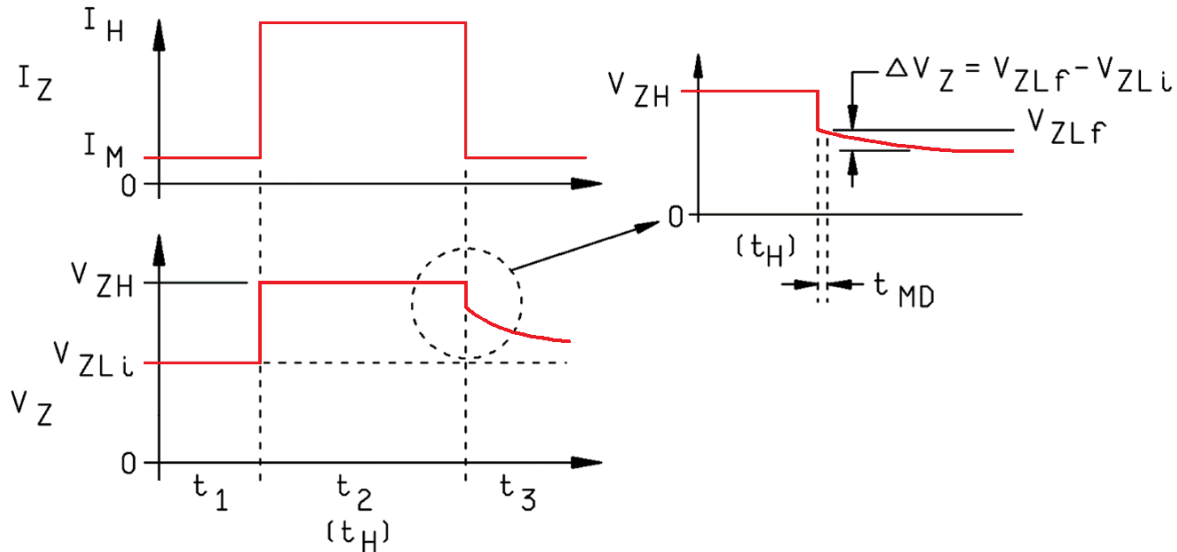


FIGURE 4086-3. Thermal impedance testing waveforms for Zener biased methods.

5.2.3 Limitations of reverse direction testing. This laboratory method is intended on initial Zener device design verification for correlation to subsequent forward direction thermal impedance testing using ATE prior to establishing a production test limit. If testing in the reverse direction exceeds the forward direction testing by 10 percent or more, production monitoring using ATE in the forward direction will require a lower limit, for some devices, than that required by the more accurate laboratory method (see 5.5.1).

5.3 Characterization of dual, quad and diode arrays.

5.3.1 General description. Traditionally, thermal impedance is required in device specification sheets without any clarification as to whether the values are for each element or all elements in parallel. While the assumption has been that the specification limits for thermal resistance apply to all elements in parallel, there has been no procedure on how to perform this. The thermal resistance test setup cannot directly parallel the diodes because the junction with the lower V_F may draw some of the current away from the other elements. Circuitry necessary for measuring thermal resistance and thermal impedance can be prohibitive.

5.3.1.1 Thermal impedance. Thermal impedance shall be measured on each element individually while the other elements are un-powered as it is intended to access chip-to-header bond quality. These individual readings cannot be combined in any way to yield the total rating. This means that there is no universal method to measure the dual or quad as a whole and the individual device specification shall not require such a measurement. Overall, power rating can be derived from similar packages employing single elements or by extensive computer modeling.

5.3.1.2 Thermal resistance. For thermal resistance only, measuring one junction while the other junctions are passively biased at the same power level does work. No power is to be applied until V_{Fi} has been measured; however, V_{Fi} will likely be unaffected if the passively biased junctions are turned off a little late. The thermal resistance value for the measured junction is divided by the total number of junctions being biased to calculate an overall package thermal resistance.

MIL-STD-750-4

5.3.2 Procedure. The testing of multiple junction devices is summarized as follows:

- a. Begin thermal resistance test of one junction while others are off.
- b. Power up remaining junctions to same current as the junction under test.
- c. Power off remaining junctions only after the test junction reading has been acquired.
- d. Calculate total device thermal resistance equals reading of test junction divided by total junctions in array.

5.3.3 Limitations. This technique is not recommended for transient thermal impedance since short readings are not affected much by adjacent junction elements and the switching of the remaining junctions in such short time periods is prohibitive.

5.4 Notes. The following details apply to the testing of 5.2 and 5.3.

- a. Some test equipment may provide a ΔV_F directly instead of V_{FI} and V_{FF} ; this is an acceptable alternative. Record the value of ΔV_F .
- b. Some test equipment may provide $Z_{\theta JX}$ directly instead of V_{FI} and V_{FF} for thermal resistance calculations; this is an acceptable alternative. Record the value of $Z_{\theta JX}$.
- c. Alternative waveforms, as may be generated by ATE using the general principles of this method, may be used upon approval of the qualifying activity.
- d. The zener biased method in figure 4086-3 illustrates a positive TSP when the Zener is in avalanche breakdown. It is also possible to portray a negative TSP for low voltage zeners when they are in the field emission or tunneling mode. A near zero TSP can also result from these two off-setting factors of a specific operating current that shall be avoided by changing to a higher or lower current. Also see appendix C herein for TSP. Note that for Zeners, I_M can be equal to I_H provided the sense time for I_M at the end of t_H is no more than 5 percent of the overall t_H for I_H . This 5 percent value will correlate to a thermal impedance reading that is no more than 5 percent lower than the true value. This is not unlike to the minor errors caused by the measurement delay time associated with the V_F method.
- e. TCZ devices do not normally respond to the Zener biased method of figure 4086-3 since the zener junction is compensated by a forward biased p-n junction diode hereafter referred to as a "stabistor". This compensation results in a near zero-TC for the reference voltage as desired where the TSP becomes ineffective in the normal operating direction for measuring thermal impedance. However, when the stabistor used is another Zener diode with a V_Z higher than the TCZ's own zener, the device can be operated in its reverse direction using the stabistor as both the heat-generating and temperature sensitive element. This is especially true if the two junctions are part of the same chip. When an independent stabistor chip or multiple stabistor chips are employed, the results will be an average of all the chips. Also the K factor used for the thermal impedance measurement becomes the total of the stabistor(s) and the Zener in the TCZ device. Heating test times for TCZ thermal measurement in the range of 10 ms to 30 ms allows all the junctions to be proportionally activated.

MIL-STD-750-4

5.5 Acceptance limit.

5.5.1 General discussion. Variations in diode characteristics from one manufacturer to another cause difficulty in establishing a single acceptance limit for all diodes tested to a given specification sheet. Ideally, a single acceptance limit value for ΔV_F would be the simplest approach. However, different design, materials, and processes can alter the resultant ΔV_F value for a given set of test conditions. Listed below are several different approaches to defining acceptance limits. The ΔV_F limit of 5.5.2 is the simplest approach and is usually selected for screening purposes. The approaches of 5.5.3 through 5.5.6 require increasingly greater detail or effort. In some examples, absolute thermal impedance limits are required for correlation to surge performance such as for zeners. In such examples, setting a limit for Zener diode construction with the forward biased method requires prior evaluation of $Z_{\theta JX}$ (and $R_{\theta JX}$, when desired) by the zener biased method. If the Zener method result is more than 10 percent higher, the limit shall be based on the more accurate zener biased measurement. In such a case, if it is desired to use the forward biased method, the limit (of ΔV_F , $Z_{\theta JX}$, or $R_{\theta JX}$) shall be reduced by the extent (percentage) difference between the two methods.

5.5.2 ΔV_F limit. A single ΔV_F limit is practical if the K factor and V_H values for all diodes tested to a given specification sheet are nearly identical. Since these values may be different for different manufacturers, the use of different limits is likely to more accurately achieve the desired intent. (A lower limit does not indicate a better die bond when comparing different product sources.) The diode specification sheet would list the following test conditions and measurement parameters:

- a. I_H (in A).
- b. t_H (in ms).
- c. I_M (in mA).
- d. t_{MD} (in μs).
- e. t_{sw} (in μs).
- f. ΔV_F (maximum limit value, in mV).

5.5.3 ΔT_J limit. (Much more involved than ΔV_F , but useful for examining questionable devices.) Since ΔT_J is the product of K (in accordance with [appendix C](#) herein) and ΔV_F this approach is the same as defining a maximum acceptable T_J rise for a given set of test conditions.

5.5.4 CU limit. (Slightly more involved than ΔT_J .) The ΔT_J limit approach described in 5.5.3 does not take into account potential power dissipation variations between devices. The V_H value can vary, depending on chip design and size, thus causing the power dissipation during the heating time to be different from device to device. This variation will be small within a lot of devices produced by a single manufacturer but may be large between manufacturers. A CU limit value takes into account variations in power dissipation due to differences in V_H by dividing the ΔV_F value by V_H .

5.5.5 (K•CU) limit. (Slightly more involved but provides greater detail.) This is a combinational approach that takes into account both K factor and power dissipation variations between devices.

5.5.6 $Z_{\theta JX}$ limit. (For full characterization; not required for screening purposes, but preferred if the proper ATE is available.) The thermal impedance approach uses an absolute magnitude value specification that overcomes the problems associated with the other approaches. Thermal impedance is time dependent and is calculated as follows:

$$Z_{\theta JX} = \Delta T_J / P_D = | (K)(\Delta V_F) / (I_H)(V_H) | \text{ } ^\circ\text{C/W}$$

NOTE: See method 3101, MIL-STD-750-3 for further details on using ATE for testing thermal impedance of diodes.

MIL-STD-750-4

5.5.7 R_{θJX} limit. (For thermal resistance specification testing.) The thermal resistance to some defined point, such as the case (R_{θJC}), lead (R_{θJL}), or end cap (R_{θJEC}), is an absolute magnitude value specification used for equilibrium conditions. The t_H heating time shall therefore be extended to longer times (typically 20 to 50 seconds). In the example of R_{θJC}, R_{θJL}, or R_{θJEC} measurements, the case, lead or end cap reference points shall be carefully stabilized and monitored in temperature which requires an infinite heat sink or careful monitoring for optimum results. The ΔT_J in the equation below is the difference in T_J to the case, lead, or end cap reference temperature as applicable by package type.

$$R_{\theta JX} = \Delta T_J / P_D = [(K)(\Delta V_F) / (I_H)(V_H)] \text{ } ^\circ\text{C/W}$$

NOTE: Some ATE designed primarily for thermal impedance testing with short heating times (t_H) may not include capabilities of controlling or monitoring these reference temperatures for an accurate thermal resistance test measurement at long heating times. Also see method 4081, MIL-STD-750-4 for further details on testing thermal resistance of diodes.

5.5.8 General comment for thermal transient testing. One potential problem in using the thermal transient testing approach lies in trying to make accurate enough measurements with sufficient resolution to distinguish between acceptable and nonacceptable diodes. As the DUT current handling capability increases, the thermal impedance under transient conditions will become a very small value. This raises the potential for rejecting good devices and accepting bad ones. Higher I_H values shall be used in this case.

6. Summary. The following test conditions and measurements to be specified and recorded.

6.1 Thermal impedance and equilibrium measurements.

6.1.1 Test conditions. Specify the following test conditions:

- a. I_M measuring current ___mA
- b. I_H heating current ___A
- c. t_H heating time ___ms
- d. t_{MD} measurement time delay ___μs
- e. t_{SW} sample window time ___μs

6.1.2 Data. Record the following data:

- a. V_{FI} initial forward voltage ___V
- b. V_H heating voltage ___V
- c. V_{FF} final forward voltage ___V
- d. NOTE: Some test equipment may provide a ΔV_F instead of V_{FI} and V_{FF}; this is an acceptable alternative. Record the value of ΔV_F.
- e. NOTE: Some test equipment may provide direct display of calculated CU or Z_{θJX}; this is an acceptable alternative. Record the value of CU or Z_{θJX}.

MIL-STD-750-4

6.2 K factor calibration. (Optional for criteria 6.2.1.a or 6.2.1.b, mandatory for 6.2.1.c, 6.2.1.d, or 6.2.1.e.)

6.2.1 Test conditions. Specify the following test conditions:

- a. I_M current magnitude ___ mA
- b. T_{J1} initial junction temperature ___ °C
- c. V_{F1} initial voltage ___ mV
- d. T_{J2} final junction temperature ___ °C
- e. V_{F2} ~~V_{F1}~~ final voltage ___ mV

6.2.2 K factor. Calculate K factor using the K factor equation of 3.3.

K factor ___ °C/mV

6.3 Specification limit calculations. One or more of the following acceptance limits should be measured or calculated, as stated on the device specification sheet (see 5.5 5.6):

- a. ΔV_F ___ mV (For no significant variation in K and V_H among devices).
- b. CU ___ mV/V (For large variation in V_H among devices).
- c. ΔT_J ___ °C (For large variation in K among devices).
- d. $K \bullet CU$ ___ °C/V (For large variation in K and V_H among devices).
- e. $Z_{\theta JX}$ ___ °C/W (For large variation in K, V_H , and I_H among devices, same as $K \bullet CU$ for diodes/rectifiers).
- f. $R_{\theta JX}$ ___ °C/W

MIL-STD-750-4

APPENDIX A

THERMAL IMPEDANCE PRODUCTION SCREENING GUIDELINES

A.1. Applying the thermal impedance test to production screening. The goal of thermal impedance production screening is to detect and remove any devices which have defects that can affect reliability or performance. The key factors for this testing are as follows:

- a. Determine a TSP (K factor) for the DUT as described in [appendix C](#) and calibrate it (usually in mV/°C for 1/K). This parameter is normally measured at a current selected so that it does not affect the accuracy of the thermal impedance test.
- b. Determine a P_T measurement power and t_M measurement pulse time. The measurement pulse time should be sufficient to delineate the package layer being monitored. For example: 10 ms to 30 ms measures the die bond integrity and 100 ms to 300 ms measures both the die bond plus an additional die tab attach to the package header. See [A.3](#) herein. The heating power pulse should be sufficient to heat the junction up at least 50°C unless limited by a maximum power density rating of the junction.
- c. Determine a t_{MD} measurement delay time (time between when power pulse is turned off and the K factor is applied) to provide the junction temperature.
- d. Deploy test equipment capable of applying the pulse determined in A.1.b and providing an output that either directly calculates the peak junction temperature with the supplied K factor and provides a thermal impedance reading in °C/W or provides a delta voltage change that can manually be converted to thermal impedance by dividing by the K factor and the P_T measurement power. This t_{MD} delay time is usually provided by the appropriate specification but extenuating circumstances such as chip storage time or package magnetic resonance may dictate using a longer value of t_{MD} . This is permitted provided a correlation is established between the required value of t_{MD} and the specified value of t_{MD} .

The supplier shall notify DLA Land and Maritime of any specified measurement conditions that might fail to achieve the thermal impedance test method's primary goal of detecting and removing defective devices.

A.2. Logistics of the thermal impedance test. Every semiconductor product type is likely to respond differently in readings to thermal impedance tests. The intent here is not to compare dissimilar product but, rather, to compare product within a single lot to each other (statistical comparison), to a specification maximum limit (when applicable) and, if at all possible, to a design ideal value. The following rules shall be applied:

- a. Any device failing the specification maximum limit (if one exists) is an automatic reject.
- b. Any device falling outside of a normal distribution of thermal impedance readings in a histogram is subject to reject. In order to successfully use thermal impedance to detect and remove any components that have defects that can affect reliability or performance, the histogram for individual lot testing shall be different from that used for end-point testing. For end-point testing, this distribution should be documented over the course of five inspection or screening lots. If each lot has a similar distribution, then the average distribution and pass-fail limits of the combination of all five lots may be used to establish permanent screening limits. If the K factor does not vary more than 10 percent from lot-to-lot, then it is permissible to establish a constant K factor for this particular part number or chip family. Otherwise, the K factor may need to be re-established for every lot. In general, this process should establish a maximum limit for evaluating that particular part type, and while it may not be used to successfully screen manufacturing defects, no individual lot evaluations should allow limits higher than the end-point limit.

MIL-STD-750-4

APPENDIX A

- c. Since a number of factors impact the thermal impedance results, in order to use thermal impedance testing to remove defects, all other influences of thermal impedance shall be held as uniform as possible. This can only be done by evaluating each production or manufacturing lot before these lots are combined into inspection or screening lots. In this case, it is necessary to treat each production or manufacturing lot on a stand-alone basis by calculating a K factor and screening limits from a sample for that specific lot.
- d. Upper and lower pass-fail limits cannot be determined by using ± 3 -sigma. This is because in most cases (except where you have achieved near perfection), the distribution is an asymmetrical histogram bell curve where the right (high-side) of the curve extends farther away from center normal than the left (low-side). This is because making **devices** **devcies** less than perfect (extends right) is easy but making devices better than perfect (extends left) is far less likely. The upper and lower limits can be set one of two ways:
 - 1) Split Histogram curve in half at the center peak value and calculate separate 3-Sigma limits, one for the upper side and one for the lower side.
 - 2) Engineering should visually review the Histogram curve and select appropriate limits based upon what looks normal and what doesn't.

The value of a lower pass-fail limit is to catch changes in the product that might otherwise go undetected. For example: Braze preform is suddenly too thin, chip size was just changed, or package design was changed by package vendor. Since the original design-value for thermal impedance remains the one constant through all testing, this is an excellent tool to confirm that thermal impedance is giving meaningful readings and that the design is being executed correctly by production.

- e. The design-value should fall somewhere in the lower region of the histogram curve or slightly below the curve. Major deviations indicate that one or the other is in error, or that the measurement conditions cannot give an absolute accurate value (though relative values for statistical screening may continue to be usable for screening).

A.3. Heat flow distance versus elapsed time plot. This section is provided to assist in determining the t_m measurement time required to adequately delineate a particular interface. The chart that follows shows effective how far heat travels in the time shown in the X-axis.

The example listed on the graph shows that heat is passing through 10 mils of silicon takes 1.2 ms to reach the back side. During the 1.2 ms, the heat has remained inside the chip, has not passed through the chip bond interface, and is too short a time to measure the chip bond interface, 1.2 ms is too short. Multiply by at least 7 to get a minimum test time.

The example continues to show that it would take 8.7 ms for heat to reach through the silicon chip, across the braze layer that is being evaluated and through but not outside of the tab the chip is mounted on. Based on this, 8.7 ms would work as a t_m that would maximize sensitivity to bad bonds but not be influenced by anything beyond the first tab. This is where the popular default value of 10 ms came from.

MIL-STD-750-4

APPENDIX A

Heat Flow Distance vs Elapsed Time Plot

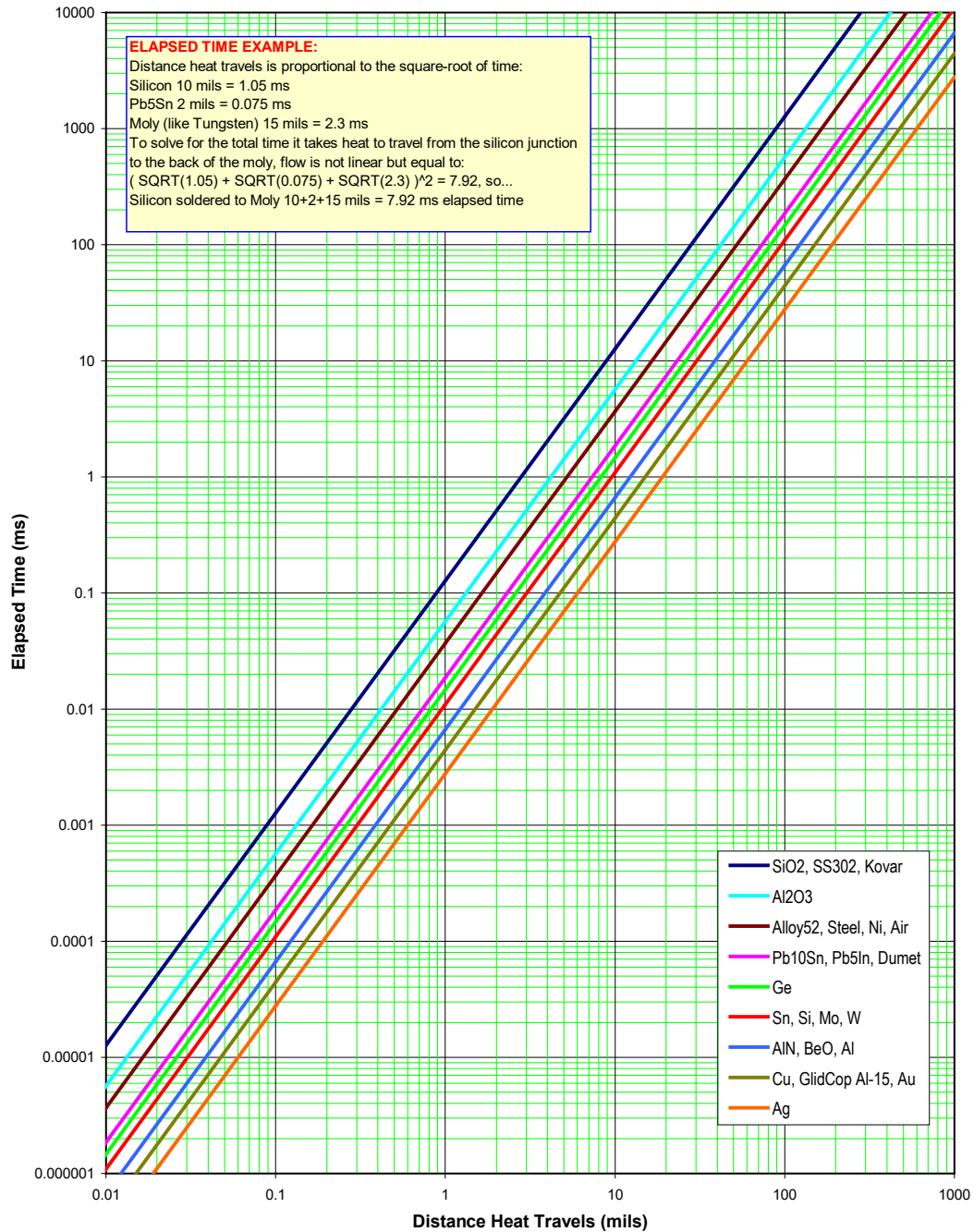


FIGURE 4086-A1 Elapsed time versus distance heat travels vs. elapsed time plot.

METHOD 4086

MIL-STD-750-4

APPENDIX B

THERMAL IMPEDANCE TESTING AND THERMAL CHARACTERIZATION GUIDELINES

B.1 Establishment of test conditions and acceptance limits. The procedure of B.2 describes how to set up the test conditions and determine the acceptance limits for implementing the transient thermal impedance test for chip attachment evaluation using the apparatus and definitions stated [appendix C](#). It can also be used for thermal characterization purposes of various devices. The following details apply:

- a. This procedure thermally characterizes the device out to a point in heating time required to ensure heat propagation through the internal chip attachments. An appropriate heat sink should also be used or the external case or reference point temperature should be also monitored where heating times can be very short for heat propagation to the external mounting point such as for case mounted power devices or very close proximity solder pads to the internal chip element.
- b. When using the procedure for taking thermal resistance measurements, the value for I_H shall be equal to the value specified in the device specification sheets, typically at rated current or higher. The values for t_H , t_{MD} , and heat sink conditions shall be also taken from the device specification sheets. Also, the external reference point temperature shall be measured at the conclusion of the heating time and used in the thermal resistance calculation shown in method 4081.

B.2 Testing procedure. From a sample of 20 to 25 devices, select any one device to start the initial device testing.

Step 1: Set up the test apparatus as follows:

$I_H = 1.0 \text{ A}$	(Or some other desired value near the DUTs normal operating current: Typically higher for power diodes, and lower for Zener diodes, when measured in the Zener direction.)
$t_H = 10 \text{ to } 50 \text{ ms}$	Unless otherwise specified, for most devices rated up to 15 W power dissipation. See figures 4086-B1 and 4086-B2 for best heating time selection.
50 to 100 ms	Unless otherwise specified, for most devices rated up to 200 W power dissipation.
$\geq 250 \text{ ms}$	For steady-state thermal resistance measurement. The pulse shall be shown to correlate to steady-state conditions before it can be substituted for steady-state condition. See test method 4081 of this multipart test method standard for further details on testing thermal resistance of diodes.
$t_{MD} = 100 \text{ } \mu\text{s max}$	For nonmagnetic or noninductive lead/package where inductive delay or stored charge do not influence the reading, $t_{MD} = 70 \text{ } \mu\text{s}$ is a good choice. A larger value may be required on power devices with magnetic/inductive package elements that generate nonthermal electrical transients; unless otherwise specified, this would be observed in the t_3 region on figure 4086-3 . If, however, a value of t_{MD} greater than 300 μs is required in order to be able to test outside of the inductive switching region, then correlation shall be made back to 70 μs from whatever value of t_{MD} is required for a stable test.
Refer to appendix D for a technique for measuring devices that cannot be measured at $t_{MD} = 70 \text{ } \mu\text{s}$ maximum because of stored charge or package magnetic effects. The method will involve measuring at $t_{MD} =$ a higher value and then following a simple calculation to correct the reading. The qualifying activity shall be notified if this alternate t_{MD} method is to be used.	

MIL-STD-750-4

APPENDIX B

$I_M = 10 \text{ mA}$ (Or some nominal value approximately two percent, or less, of I_H .)

IMPORTANT: Diodes like Schottky and gold doped switching rectifiers can have enough saturation current so that the K factor varies with temperature at lower values of I_M . It is safest to have previously measured at least once for each family type, the K factor at 25°C increments from 25°C up to at least 150°C (or T_J max) plus vary the current over a decade. Pick an I_M value where K factor remains fairly consistent over temperature. If K factor is inconsistent, then use the K factor that corresponds with the actual T_J achieved in the thermal impedance test (may require some iterations to calculate this value).

Step 2: Insert device into the apparatus test fixture and initiate a test. (For best results, a test fixture that offers some form of heat sinking would be desirable. Heat sinking is not needed if either the power dissipation during the test is well within the diode's free-air rating or the maximum heating time is limited to less than that required for the heat to propagate through the case.)

Step 3: Based on the value of ΔV_F , proceed forwards or go back using the following criteria:

- a. If ΔV_F is less than 50 mV, return to step 1 and increase heating power into device by increasing I_H .
- b. If ΔV_F is in the 50 to 300 mV range, or ΔV_{ZL} is equivalent to the same ΔT_J , then proceed to step 4. This range approximately corresponds to a junction temperature change of roughly +25°C to +150°C and is sufficient for initial comparison purposes.

EXCEPTION (for when the maximum DUT or test equipment rated I_H has been reached): In this case, the accuracy associated with using a smaller ΔV_F shall be accepted. Test equipment shall have at least 100 μV resolution for ΔV_F . Higher resolution test equipment can easily compensate if ΔV_F is less than 50 mV. If ΔV_F is greater than 150 mV, approximately corresponding to a junction temperature change greater than +75°C, it would probably be desirable to reduce the heating power by returning to step 1 and reducing I_H . Note that some automatic test equipment automatically guards against this problem.

NOTE: The test equipment shall be capable of resolving ΔV_F to within 5 percent. If not, the higher value of ΔV_F shall be selected until the 5 percent tolerance is met. Two different devices can have the same T_J rise even when P_H is different, due to widely differing V_H . Within a given lot, however, a higher V_H is more likely to result in a higher T_J rise. For such examples, this screen can be more accurately accomplished using the CU value. As defined in 2 herein, CU provides a comparison unit that takes into account different device V_H values for a given I_H test condition.

Step 4: Test each of the sample devices and record the data detailed in 6.

Step 5: Select out the devices with the highest and lowest values of CU or $Z_{\theta JX}$ and put the remaining devices aside. These two device will be used to generate data needed to create thermal impedance curves.

The ΔV_F values can be used instead of CU or $Z_{\theta JX}$ if the measured values of V_H are very tightly grouped around the average value.

Step 6: Using the devices with the highest and lowest values from step 5, collect and plot the heating curve data for the two devices in a manner similar to the examples shown on [figure 4086-B1](#).

MIL-STD-750-4

APPENDIX B

Step 7: Interpretation of the heating curves is the next step. Realizing that the thermal characteristics of identical chips should be the same if the t_H is equal to or less than the thermal time constant of the chip, the two curves should start out the same for the low values of t_H . Non-identical chips (thinner or smaller in cross section) will have completely different curves, even at the smaller values of t_H . As the value of t_H is increased, thereby exceeding the chip thermal constant, heat will have propagated through the chip into the chip attachment region. Since the heating curve devices of step 5 were specifically chosen for their difference, the curves of figures 4086-B1 or 4086-B2 diverge after t_H reaches a value where the chip attachment variance has an affect on the device T_J and $Z_{\theta JX}$ as best observed on figure 4086-B2 4086-B1 for a log-log plot. Increasing t_H further will eventually result in a flattening of the curve as the heating propagates in the device package and thermal impedance approaches the thermal resistance value of the device. If the device package has little thermal mass and is not well mounted to a good heat sink, the curve will not flatten very much, but will show a definite change in slope.

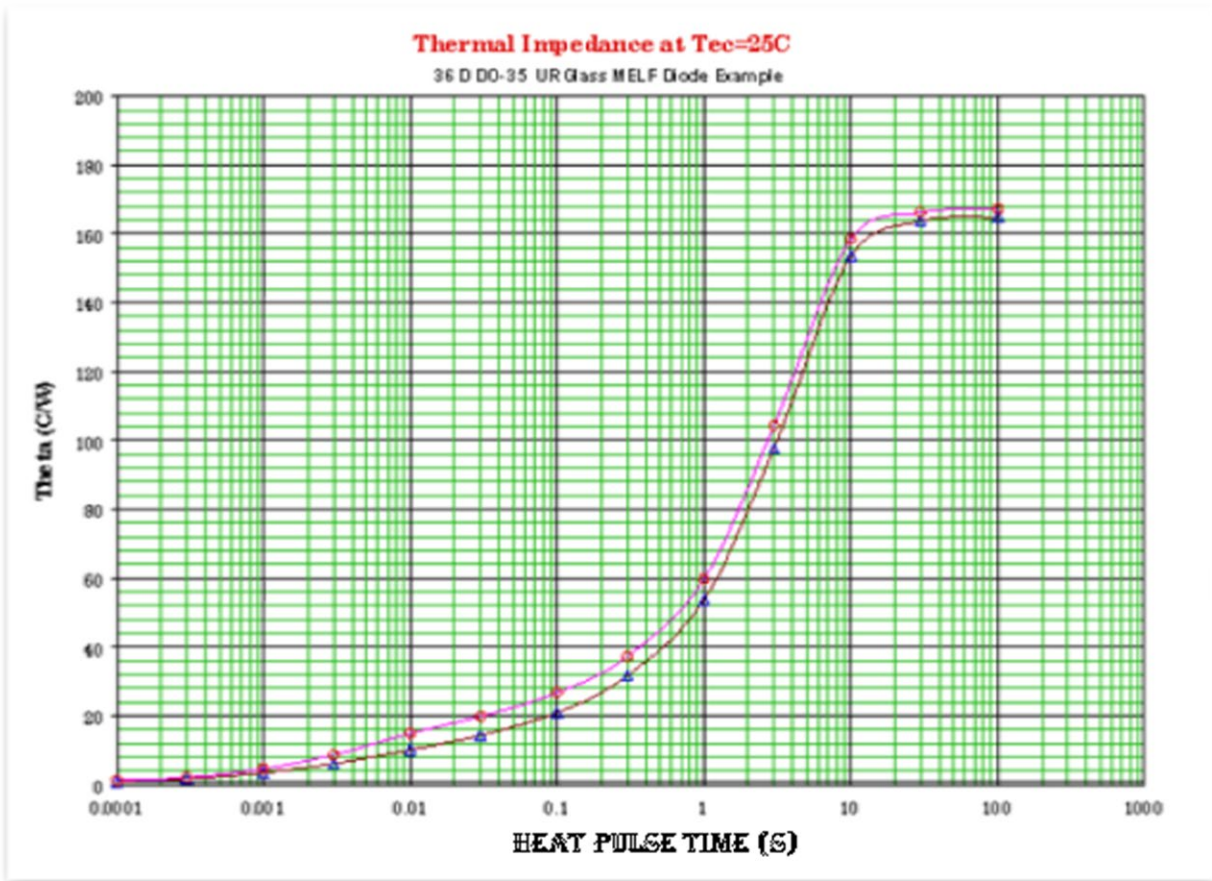
Step 8: Using the heating curve, select the appropriate value of t_H to correspond to the inflection point in the transition region between heat in the chip and heat in the package.

If there are several different elements in the heat flow path (the chip, die attachment material, substrate, substrate attach, and package for example in a hybrid), there will be several plateaus and transitions in the heating curve. An appropriate selection of t_H will optimize evaluation sensitivity to other attachment areas.

Step 9: Return to the apparatus and set t_H equal to the value determined from step 8.

MIL-STD-750-4

APPENDIX B



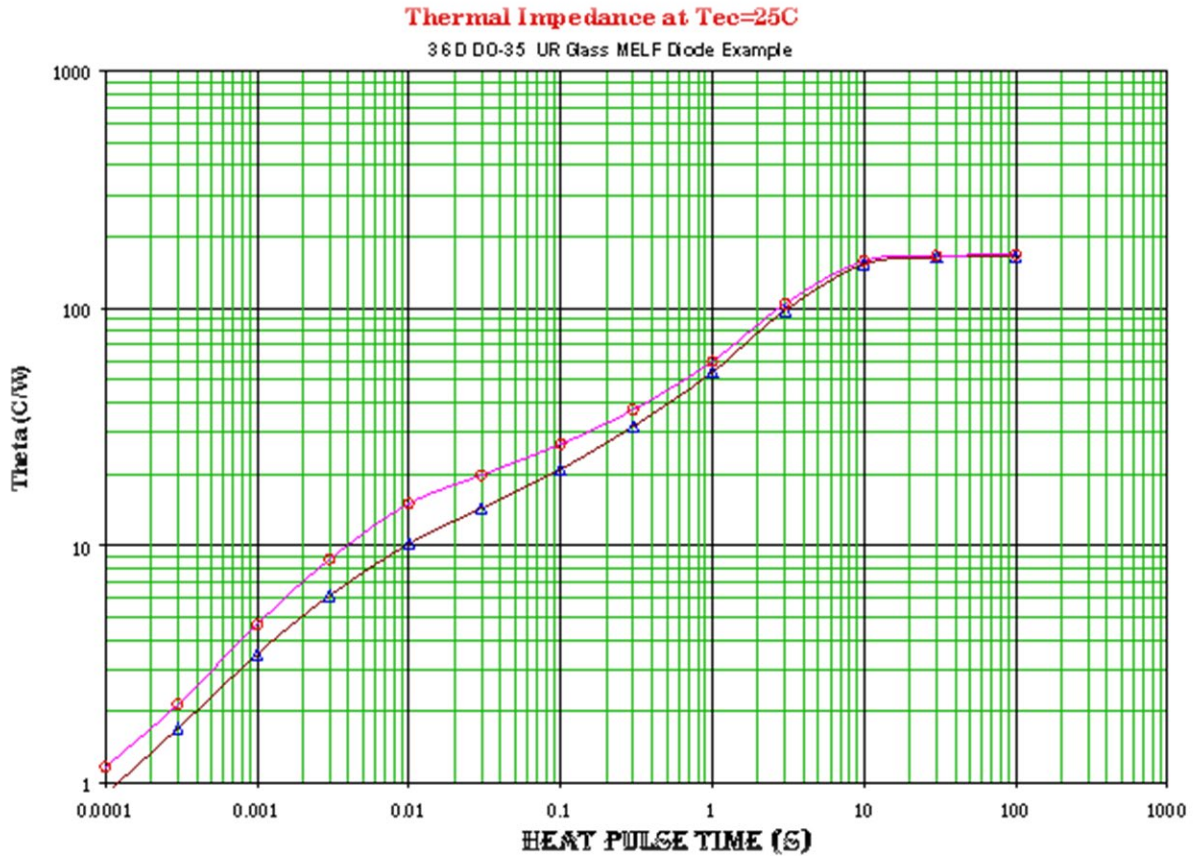
NOTES:

1. Log-linear plot. The time period when the two curves (lower in blue best vs. upper in red worst) are farthest apart is the best heating time to use for thermal impedance die bond testing. Note that since the range from 10 ms to 100 ms in this example are nearly parallel, any place in that region is acceptable; however, 10 ms to 30 ms results in faster testing so that would be the logical choice. While log-log plots are requested for use in the device specification sheet, log-linear plots may be substituted with approval of the Qualifying Activity. See [figure 4086-B2](#) for a log-log example.
2. Both figures 4086-B1 and [4086-B2](#) are of the same data.
3. The log-linear incorrectly leads one to believe that maximum void test sensitivity is available anywhere above 10ms.
4. For tight resolution at long test times, the log-linear can provide better resolution. However, for short pulse operation, the log-log is far superior.

FIGURE 4086-B1. Heating curves for two extreme devices (log-linear plot).

MIL-STD-750-4

APPENDIX B



NOTES:

1. The log-log plot (preferred) illustrates the ability of short test pulses during thermal impedance to detect poor die bonds. The time period when the two curves (lower in blue best vs. upper in red worst) are farthest apart is the best time to use for thermal impedance die bond testing. Note that since the range from 10 ms to 100 ms in this example are nearly parallel, any place in that region is acceptable; however, 10 ms to 30 ms results in faster testing so that would be the logical choice. Each construction design may have a different "sweet zone". For example, many double plug diodes are very near 10 ms for optimum heating times.
2. Both figures 4086-B1 and 4086-B2 are of the same data.
3. The log-log curve deals with resolution accuracy just like any automatic tester. Here the log-log curve makes it clear that you will lose resolution accuracy above 100ms.

FIGURE 4086-B2. Heating curves for two extreme devices (log-log plot).

MIL-STD-750-4

APPENDIX B

Step 10: Because the selected value of t_H is much less than that for thermal equilibrium, it is possible to significantly increase the P_H without degrading or destroying the device. The increased power dissipation within the DUT will result in higher ΔV_F or CU values that will make determination of acceptable and unacceptable devices much easier.

Step 11: The pass/fail limit, the cut-off point between acceptable and nonacceptable devices, can be established in a variety of ways:

- a. Correlation to other chip attachment evaluation methods, such as die shear and X-ray. While these two methods have little actual value from a thermal point of view, they do represent standardization methods as described in various standards.
- b. Maximum allowable junction temperature variations between devices. Since the relationship between ΔT_J and ΔV_F is about $0.5^\circ\text{C}/\text{mV}$ for forward bias testing, or a measurable equivalent for Zener direction testing, the T_J spread between devices can be easily determined. The T_J predicts reliability. Conversely, the T_J spread necessary to meet the reliability projections can be translated to a ΔV_F or CU value for pass/fail criteria.

To fully utilize this approach, it will be necessary to calibrate the devices for exact value of the T_J to V_F characteristic. The characteristic's slope, commonly referred to as K factor, is easily measured on a sample basis using a voltmeter, environmental chamber, temperature monitor, and a power supply setup as described in [appendix C](#) herein. A simple set of equations yield the (T_J) once K and ΔV_F are known:

$$\Delta T_J = (K) (\Delta V_F)$$

$$T_J = T_A + \Delta T_J$$

Where T_A is the ambient or reference temperature. For thermal transient test conditions, temperature is usually equivalent to lead temperature (T_L) for axial lead devices or case temperature (T_C) for case mounted devices.

- c. Statistically, from a 20 to 25 device sample, the distribution of ΔV_F or CU values should be a normal one with defective devices out of the normal range. [Figure 4086-B3](#) shows a ΔV_F distribution for a sample lot of diodes.

NOTE: The left-hand side of the histogram envelope is fairly well defined, but the other side is greatly skewed to the right. This is because the left-hand side is constrained by the absolute best heat flow that can be obtained with a given chip assembly material and process unless a test method error is introduced. The other side has no such constraints because there is no limit as to how poorly a chip is mounted.

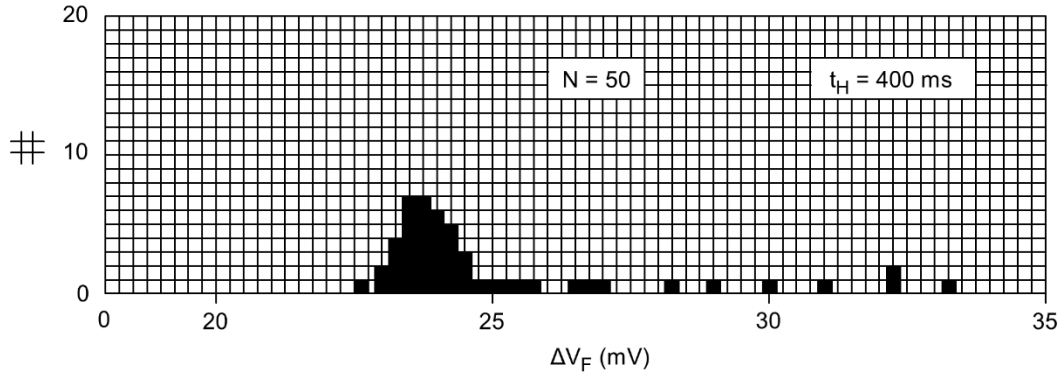


FIGURE 4086-B3. Typical ΔV_F (or $Z_{\theta JX}$) distribution with asymmetrical histogram distribution.

The usual rule of thumb in setting the maximum limit for ΔV_F , CU, or $Z_{\theta JX}$ is to use the distribution average value and three standard deviations (σ). For example:

$$\begin{array}{l} |(\Delta V_F)|_{\text{high limit}} = \overline{\Delta V_F} + X\sigma \end{array}$$

$$\begin{array}{l} |(\text{CU})|_{\text{high limit}} = \overline{\text{CU}} + X\sigma \end{array}$$

$$\begin{array}{l} |(Z_{\theta JX})|_{\text{high limit}} = \overline{Z_{\theta JX}} + X\sigma \end{array}$$

Where $X = 3$ in most cases and $\overline{\Delta V_F}$, $\overline{\Delta \text{CU}}$, and $\overline{\Delta Z_{\theta JX}}$ are the average distribution values.

The statistical data required is obtained by testing 25 or more devices under the conditions of step 11.

The maximum limit determined from this approach should be correlated to the diode's specified thermal resistance. This will ensure that the ΔV_F or CU limits do not pass diodes that would fail the thermal resistance or transient thermal impedance requirements.

Step 12: Once the test conditions and pass/fail limit have been determined, it is necessary only to record this information for future testing requirements of the same device in the same package. It is also recommended that a minimum limit is established to ensure a test method error or other anomaly is investigated.

ATTACHMENT 1 TO EP STUDY 5961-2025-112
31 JANUARY 2026

MIL-STD-750-4

APPENDIX B

Step 13: After the pass/fail limits are established, there shall be verification that they correlate to good and bad bonded devices or the electrical properties such as surge.

B.3 Summary of test procedure steps. The 13 steps listed above are summarized in table 4086-I.

TABLE 4086-I. Summary of test procedure steps.

General description		Steps	Comments
A	Initial setup	1 through 4	Approximate instrument settings to find variations among devices in 10-to-15-piece sample.
B	Heating curve generation	5 through 6	Using highest and lowest reading devices, generate heating curves.
C	Heating curve interpretation	7 through 9	Heating curve is used to find more appropriate value for t_H corresponding to heat in the chip attachment area (for some other desired interface in the heat flow path).
D	Final setup	10	Heating power applied during t_H is increased in order to improve measurement sensitivity to variations among devices.
E	Pass-fail determination	11 through 12	A variety of methods is available such as JEDEC JESD94 or JEDEC JEP148 for setting the fail limit; the statistical approach is the fastest and easiest to implement.
F	Verification	13	Mechanical / electrical correlation

B.4 Routine device thermal transient testing procedure. Once the proper control settings have been determined for a particular device type from a given manufacturing process or vendor, repeated testing of that device type simply requires that the same test conditions be used as previously determined.

MIL-STD-750-4

APPENDIX C

MEASUREMENT OF THE TSP

C.1 Measurement of the TSP. The calibration of V_F versus T_J is accomplished by monitoring V_F for the required value of I_M as the environmental temperature (and thus the DUT temperature) is varied by external heating. It is not required if the acceptance limit is ΔV_F (see 5.5.2), but is relevant to the other acceptance criteria (see 5.5.3 through 5.5.7). The magnitude of I_M shall be chosen so that V_F is a linearly decreasing function over the normal T_J range of the device. I_M shall be large enough to ensure that the device junction is turned on but not large enough to cause significant self-heating.

C.2 Example TSP measurement test circuit setup. An example TSP measurement test circuit setup is shown on figure 4086-C1.

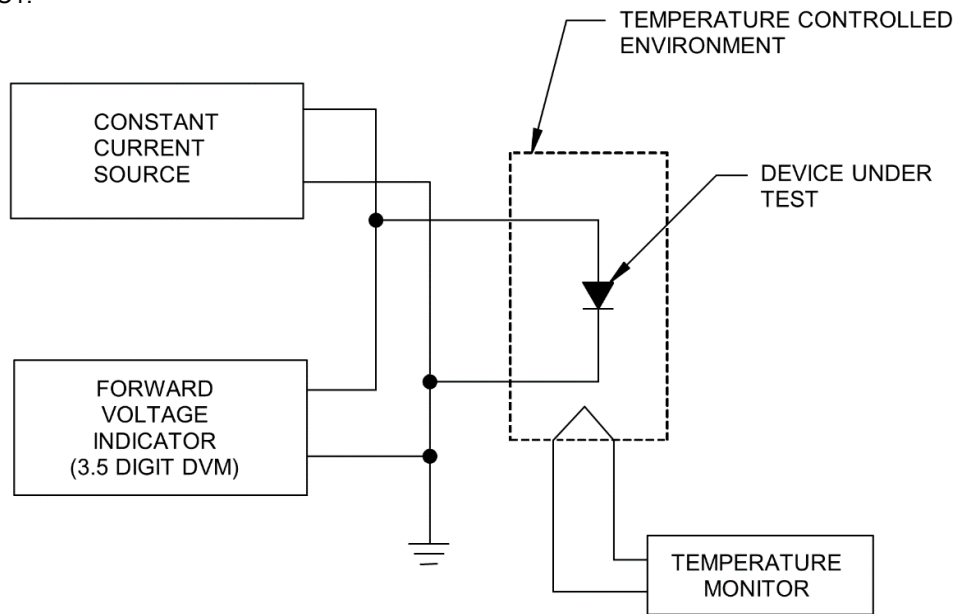


FIGURE 4086-C1 Example TSP test circuit.

C.2.2 Example TSP measurement. An example of the measurement method using the measurement test setup of figure 4086-C1 is as follows: While using a small constant current I_M , decrease the starting value of V_F and increase the starting value of T_J .

Step 1: Measure V_{F1} at T_{J1} using I_M

Step 2: Decrease the starting value of V_F and vary the temperature of the controlled environment to influence T_J

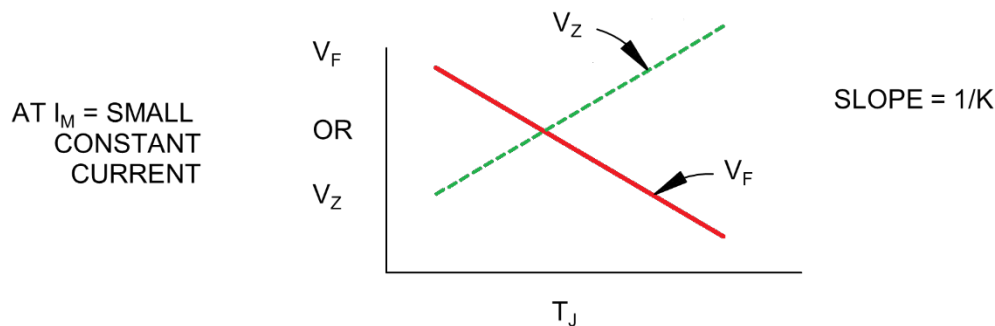
Step 3: Measure V_{F2} at T_{J2} using I_M

Step 4: Calculate the value of the K using the equation of 3.3.

The resulting calibration curve is shown on figure 4086-C2.

MIL-STD-750-4

APPENDIX C A



NOTES:

1. When testing in the forward direction, I_M shall be large enough to overcome surface leakage effects but small enough not to cause significant self-heating.
2. When testing using the reverse (Zener) direction, I_{MZ} may also require adjustment to avoid a near zero TSP where the avalanche breakdown effects are offset by tunneling or field emission (see 5.4.d).
3. T_J is externally applied (e.g., via oven, liquid) environment.

FIGURE 4086-C2. Example calibration curve of V_F (or V_Z) versus T_J .

C.3 K factor.

C.3.1 K factor calculation. A calibration factor K (which is the reciprocal of the slope of the curve on figure 4086-C2 4086-A2) can be calculated using the K factor equation of 3.3.

C.3.2 Temperature considerations. It is required that the range of temperatures that K factor is measured over approximately correlates to the range of temperature used for thermal measurements. It is important to characterize the device at least once over a broad temperature range using increments of 25 °C as well as over several values of I_M . This is especially true for room ambient thermal resistance measurements where the recorded value can be deceptively lower when the device is operated close to its maximum T_J . Some devices, especially gold doped devices, can have a saturation current at these elevated temperatures that can overwhelm the I_M current. Characterization is required as it might reveal that a higher value of I_M will be needed.

C.3.3 Sample size considerations. It has been found experimentally that the K factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 to 12 piece sample from a device lot and determine the average value of K and standard deviation (σ). If σ is less than or equal to 3 percent of the average value of K , then the average value of K can be used for all devices within the lot. If σ is greater than 3 percent of the average value of K , then all the devices in the lot shall be calibrated and the individual values of K shall be used in determining device acceptance.

C.4 Alternative to using individual values of K . As an alternative to using individual values of K , the manufacturer may establish internal limits unique to their product that ensures atypical device removal from the population (lot-to-lot and within-the-lot). The manufacturer shall use statistical techniques to establish the limits to the satisfaction of the Government.

BACKWARD t_{MD} PROJECTOR CALCULATION METHOD

D.1. Backward t_{MD} projector calculation method. While the thermal impedance test method makes allowances for devices that have either magnetic or stored charge issues that hinder using delay times under 100 μs , this "backward projector calculation method" actually gives one method to make the allowance. Generally this correction is only needed for steady-state thermal impedance (a.k.a. thermal resistance) because it is thermal resistance that usually has a specification maximum. Short-pulse-width thermal impedance used for SPC purposes and for screening out poor die bond problems is just as effective regardless of the value of t_{MD} used. However, if absolute thermal impedance accuracy is required, then a minimum delay time is still required for correlation reference.

Figure 4086-D1 illustrates what a thermal impedance tester sees when a test is performed. The first reading (V_F) is always the easiest to take. The second reading (V_F) can be misled by ferromagnetic resonant delay, stored charge, etc. and must be delayed until the device has stabilized. When the device stabilized within the 100 μs t_{MD} period, no further compensation is required.

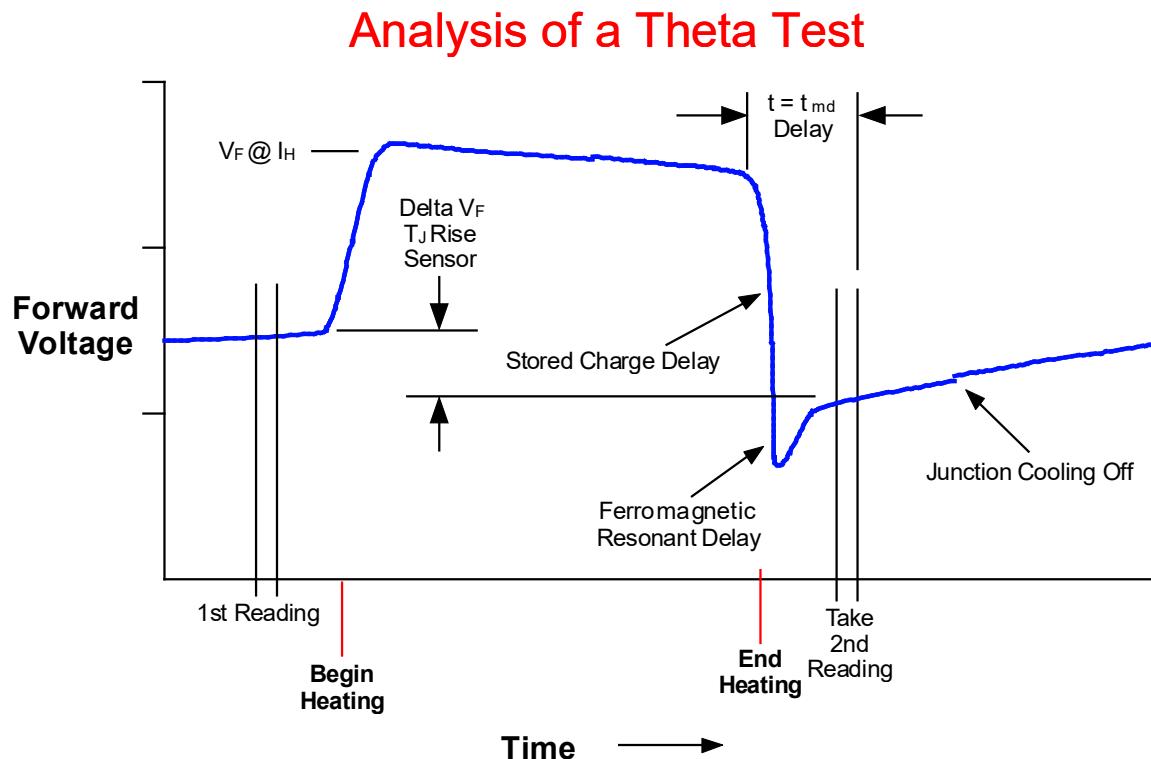


FIGURE 4086-D1. Analysis of theta test.

However, when a much longer t_{MD} is required to avoid the interference caused by magnetics and stored charge, the backward projector calculation method can be used.

D.2. The backward t_{MD} projector calculation.

D.2.1 Definitions. (Any units for t_{MD} and θ can be used, but be consistent throughout).

- a. t_{MD} = Spec delay time for θ (such as 70 μs when it otherwise cannot be measured directly).
- b. t_{MD1} = Delay time that can be measured (such as 1000 μs) for θ_1 .
- c. t_{MD2} = Forced 2nd delay = (approximately 2 to 3 times t_{MD1}) for θ_2 .

D.2.2 Constants.

$$c = (\theta_1 - \theta_2) / [\text{SQRT}(t_{MD1}) - \text{SQRT}(t_{MD2})].$$

$$k = \theta_1 - c * \text{SQRT}(t_{MD1}).$$

Solve: $\theta(t_{MD}) = k + c * \text{SQRT}(t_{MD}).$

NOTE: For ideal θ value, set $t_{MD} = 0$ in the equation, which yields the value of just k .

While it is possible to have a thermal impedance tester programmed to do this automatically, it is also possible to calculate a one-time correction factor that can be applied to the test limit and allow testing using t_{MD1} and θ_1 to adjusted limits.

Calculate the correction factor for a given design and use it instead:

$$\text{Factor} = \theta(t_{MD}) / \theta_1,$$

$$\text{Factor} = [k + c * \text{SQRT}(t_{MD})] / [k + c * \text{SQRT}(t_{MD1})]$$

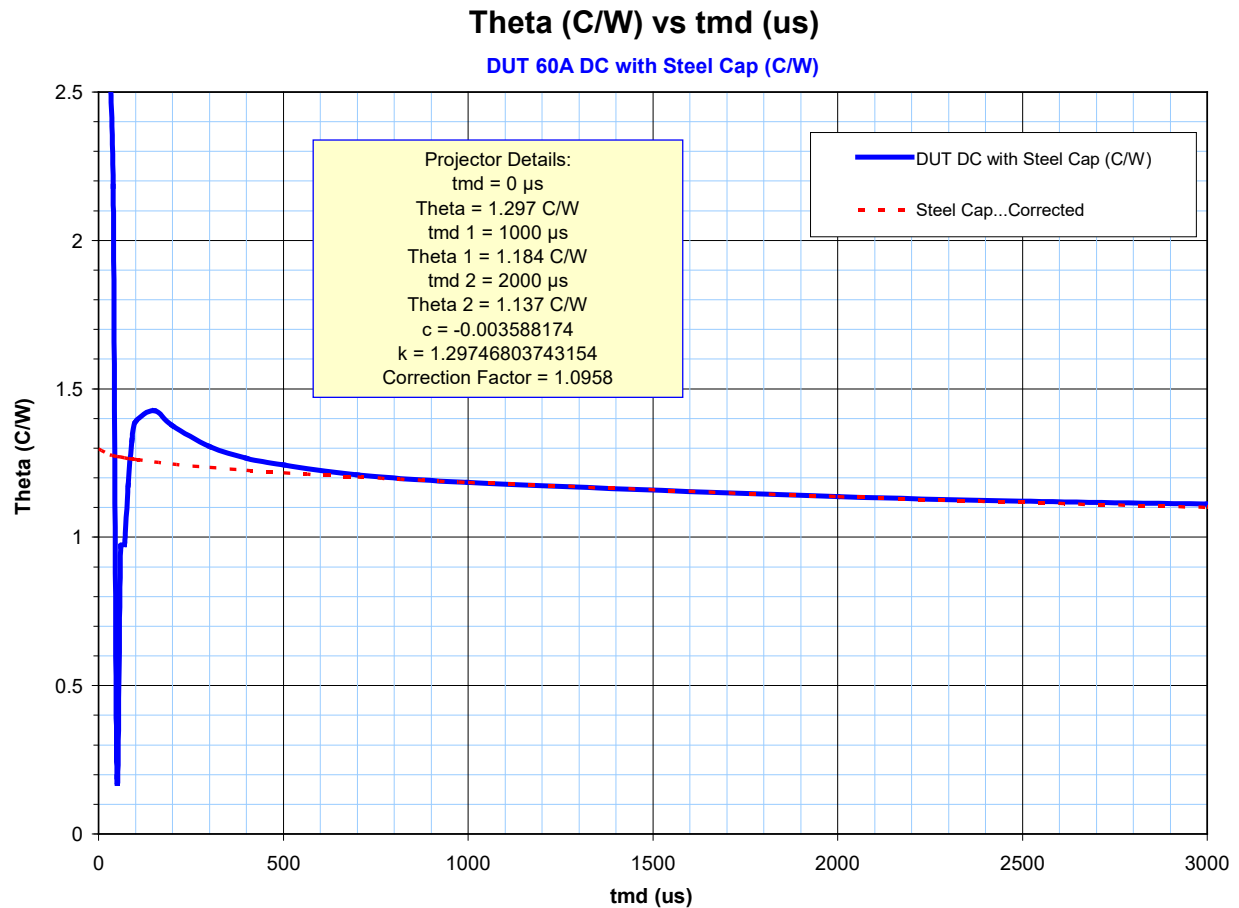
So that the correct $\theta(t_{MD}) = \text{measured } \theta_1 \text{ at } t_{MD1} * \text{Factor}.$

Likewise, the new screening max θ_1 limit using t_{MD1} becomes $\theta(t_{MD}) / \text{Factor}.$

This "Factor" value can be used to apply to any one design (same chip, same package) using the same test setup conditions (I_H , I_M , V_{CE} , etc.) without the need to do any future re-calculations.

Figure 4086-D2 shows examples of a device that benefits immensely from the use of the backward t_{MD} projector (plus the same part with the "trouble maker" removed) and a device that doesn't require the "Projector" at all. Note that using the "Projector" for a device that does not require the "Projector" does not cause any error. The point is also made that the backward t_{MD} projector can work for any semiconductor device including bipolar transistors, field-effect transistors, and diodes:

D.3. Figure 4086-D2. This figure shows a device that is very much in need of correction. This particular example is for a rectifier but this "projector" method works equally well for diodes and bipolar transistors. The dashed line is the output of the "projector" where the value of t_{MD} is varied from zero out to t_{MD2} . The magnetic (due to steel cap) and stored charge perturbations end between 700 μs and 800 μs .



NOTE: Observe closely on the curve above that if the "projector" had not been used, e.g. $t_{MD} = 50 \mu s$ had been used instead, a theta value less than 25 percent of the actual theta value would have been measured. The next measurement would have likely been erratic and your SPC charts would be plotting setup errors and not product integrity.

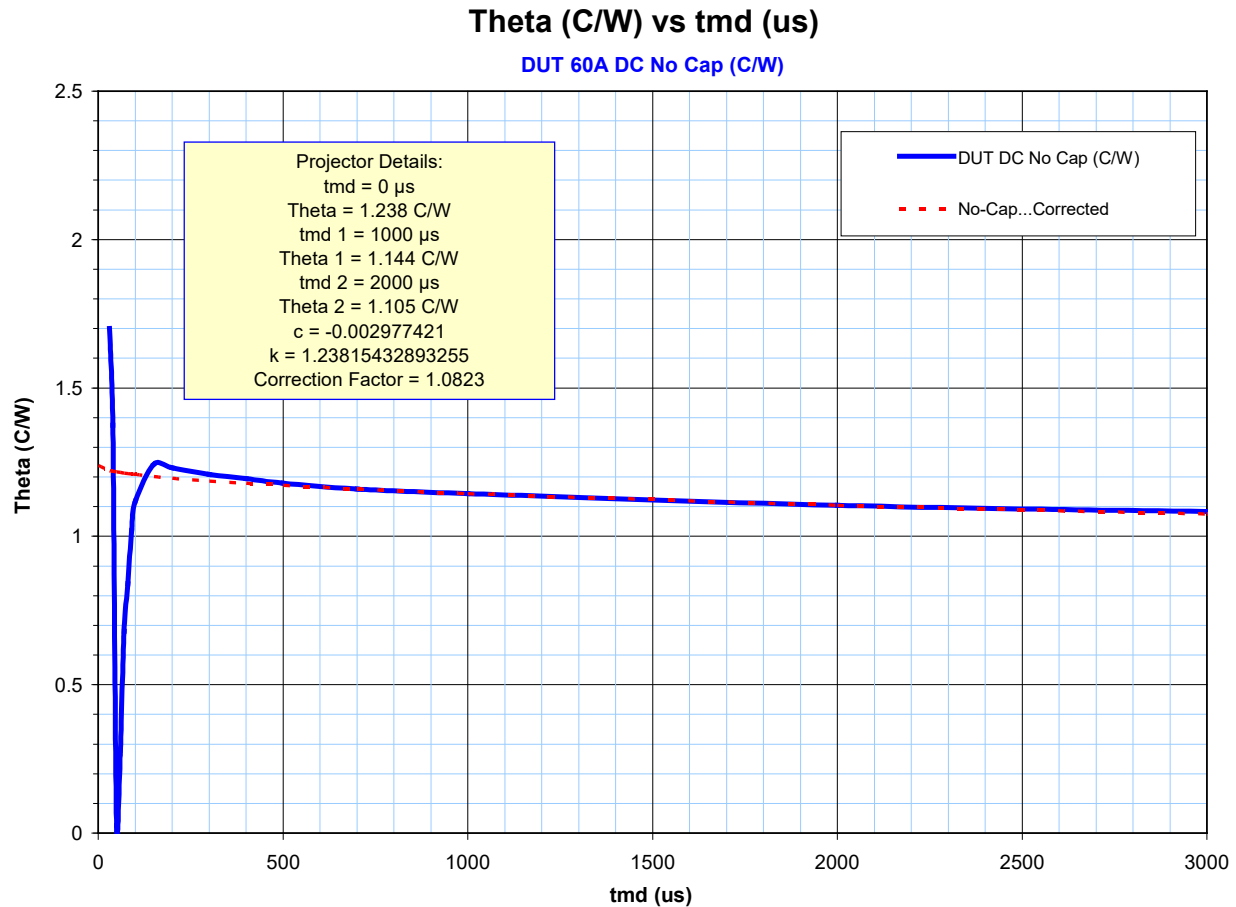
FIGURE 4086-D2. Theta versus t_{MD} .

MIL-STD-750-4

APPENDIX D

D.4. Figure 4086-D3. This figure shows the identical device depicted above except that the steel cap, the cause of much of the magnetic perturbations, has been removed. The perturbations are quite natural since the current carrying terminals pass through the cap creating an artificial magnetic core in which to store energy.

This figure does show that other problems can cause unnatural oscillations (especially at these high currents) where error begins to creep in below 400 μ s.



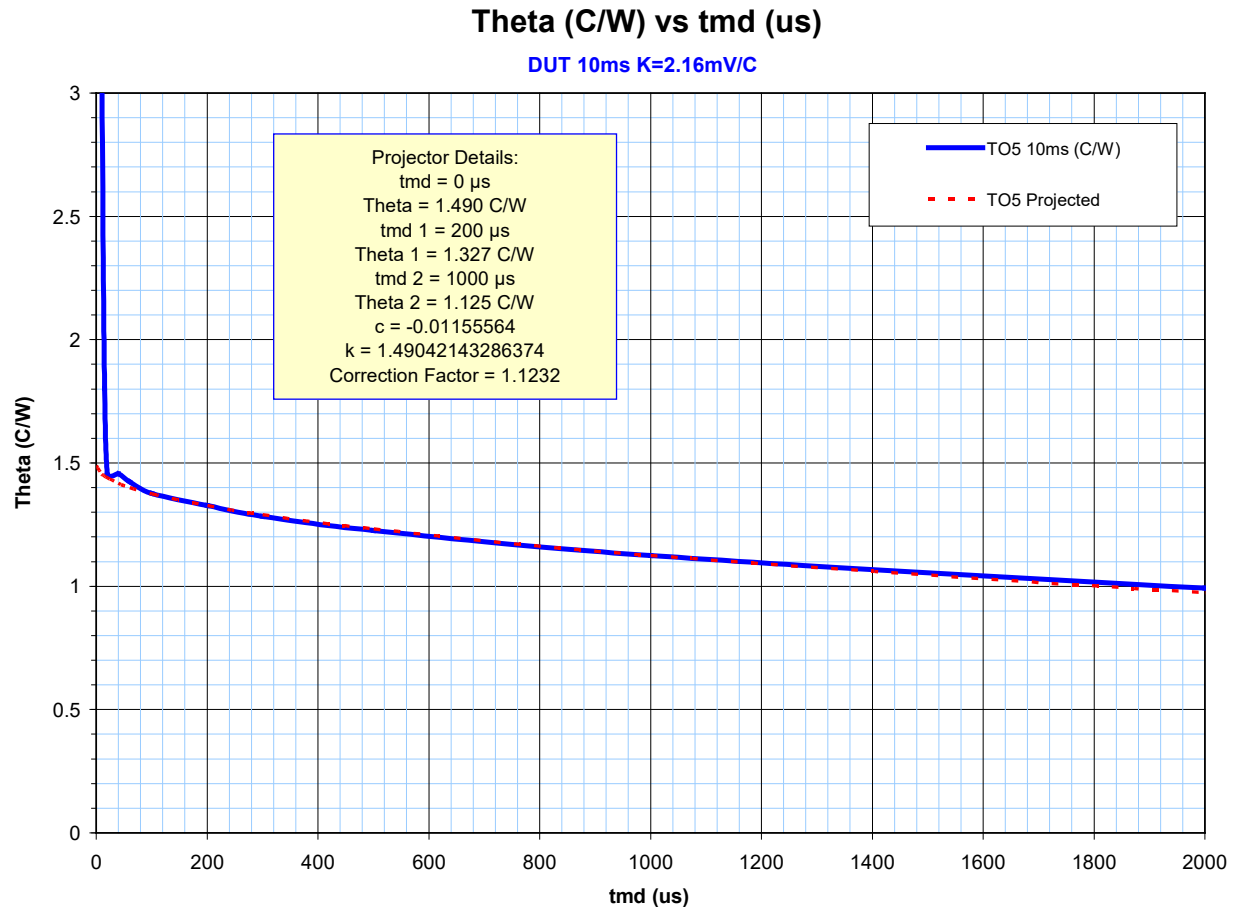
NOTE: The magnetic disturbances removed, there only remains the effects of stored charge and/or recovery delay in the thermal resistance tester as, in this case, the power source shall switch from $I_H = 60$ A to $I_M = 50$ mA.

FIGURE 4086-D3. Theta versus tmd.

MIL-STD-750-4

APPENDIX D

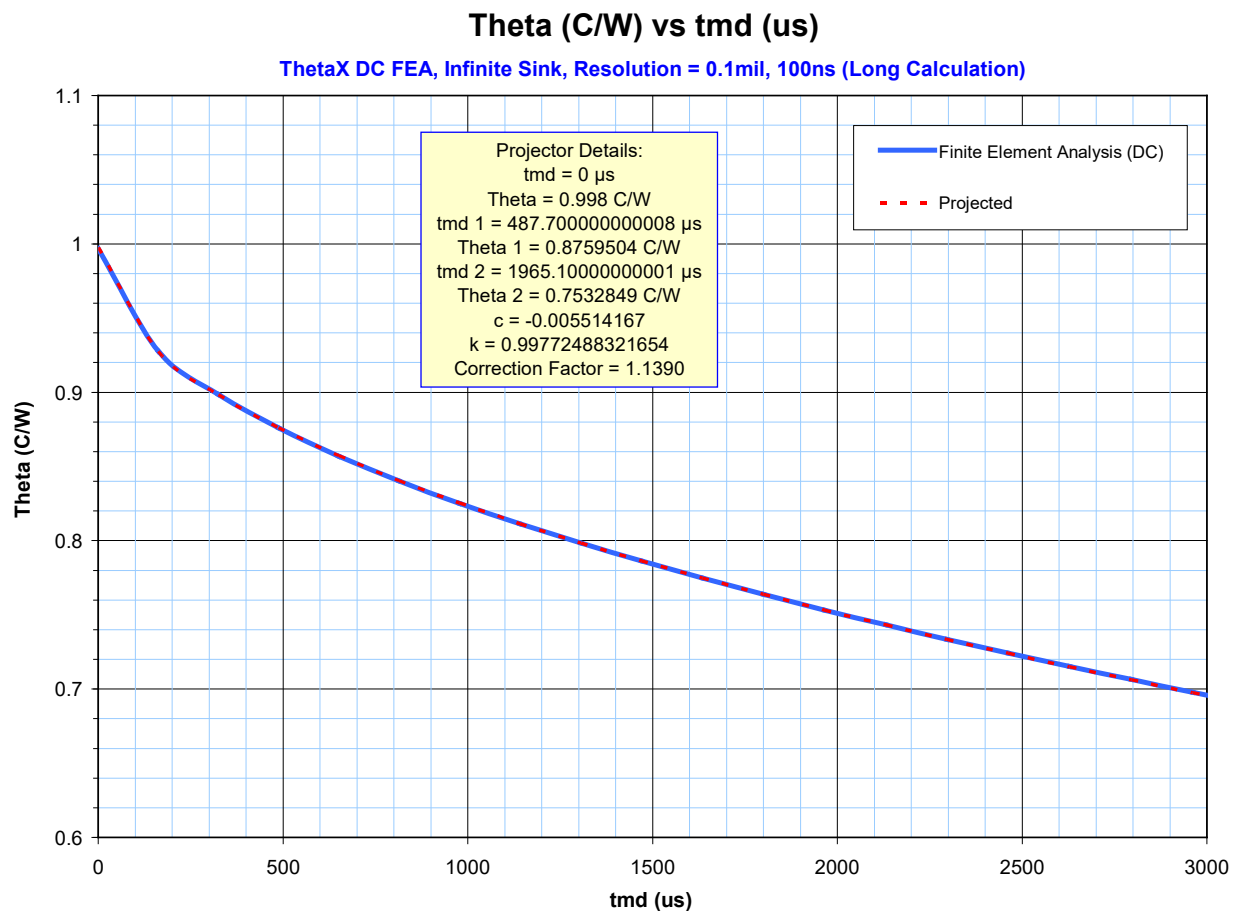
D.5. Figure 4086-D4. This figure shows a device that requires almost no correction at all. The plot shows measured thermal impedance essentially tracking with the "projector" plot. One of the reasons this device performs so well is that the test current is very low (1 A), the chip is very fast, and the case has very little magnetic influence.



NOTE: Knowing exactly how to select t_{MD1} and t_{MD2} is important. Note that t_{MD1} shall be selected just past the point where various perturbations occur and this can be accomplished by making "cooling plots" like the plots used for the figure above. For t_{MD2}, usually pick a value between 2 to 3 times t_{MD1}.

FIGURE 4086-D4. Theta versus t_{md}.

D.6. Figure 4086-D5. A finite element analysis cooling plot, has been prepared for which the thermal resistance at $t_{MD} = 0$ is known by definition. This provides evidence that the "Projector" actually shows what is happening at $t_{MD} = 0$.



NOTES:

1. The selection of "odd" values of t_{MD1} and t_{MD2} is because these were provided by the computer. It can be seen that the FEA output (solid line) and the "Projector" overlay each other perfectly.
2. Be aware that when measuring thermal resistance, the "projector" works very easily with very little guess work. When used for pulsed thermal impedance, some error can creep in if t_{MD1} and/or t_{MD2} is selected carelessly. Again, be prepared with the appropriate cooling plot curve for a given semiconductor family.
3. It has always been believed that measuring theta at $t_{MD} = 0$ was impossible. With this method, it can be done.

FIGURE 4086-D5. Theta versus tmd.