

ENGINEERING PRACTICE STUDY

PROJECT NUMBER: 5961-2019-056

TITLE:

MIL-STD-750-3, TEST METHOD 3402:
PROPOSAL TO CORRECT FIGURES
AND CLARIFY CONTENT

01 AUGUST 2019

FINAL REPORT

STUDY CONDUCTED BY

DLA LAND AND MARITIME
Document Standardization Division (VA)
Active Device Branch (VAC) – VAC

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ATTCH 2

I. OBJECTIVES: The objective of this Engineering Practice (EP) Study was to obtain input from the military services, device manufacturers, laboratories, and user community concerning the proposed revision to test method 3402 of MIL-STD-750-3.

II. BACKGROUND: DLA VAC was informed that test circuit figures in the test method were incorrectly identified. The test circuit figure for condition A was actually for condition B, and vice versa. After performing a review of the content of test method 3402.0, additional consistency, editorial, and organization issues were also noted and have been incorporated in the proposal.

DLA Land and Maritime had requested that military services (custodians and review activities), device manufacturers, OEMs, and laboratories using the subject test method to review a proposed revision. The proposed revision included both format and technical changes.

III. RESULTS: All comments received regarding swapping the figures, proposed content and format changes were resolved and have been incorporated into the final draft of the test method. Both a clean reader draft (see attachment 1) and mark-up source draft with key (see attachment 2) have been included for viewing.

IV. CONCLUSIONS: The highlighted changes to the test method (see attachment 1) should be proposed for incorporation into the next standardization document change action to MIL-STD-750-3.

V. RECOMMENDATIONS: Prepare an initial draft of MIL-STD-750-3 with attachment 1 of this study used for the draft of test method 3402.1.

The point of contact for this final report is Mr. David Corbett, DLA Land and Maritime – VAC, P. O. Box 3990, Columbus, OH 43218-3990. Mr. Corbett can also be reached at 614-692-0526 / DSN 850-0526, or by facsimile at 614-693-642 / DSN 850-1642, or by e-mail to: 750.TestMethods@dla.mil.

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METHOD 3402.1

MOSFET GATE EQUIVALENT SERIES RESISTANCE

1. **Purpose.** The purpose of this test is to determine the Gate equivalent series resistance (ESR) of power MOSFET semiconductor devices.

2. **Overview.** This test method provides a means to ensure switching consistency of power MOSFET devices. The Gate ESR measurement combined with Gate charge measurements provide an alternative to high-current high-speed measurements where MOSFET device fast switching characteristics are over-masked by test circuit stray elements.

2.1 **Test conditions.** This test method describes two test conditions (A and B) by which the Gate ESR of MOSFET devices can be determined. A description of the two test conditions of this test method are as follows:

a. Test condition A uses a LCR meter to determine Gate ESR.

b. Test condition B is a manual method to determine Gate ESR.

3. **Definitions.** The following symbols and terminology shall apply to this test method:

a. f Test frequency.

b. C_g Effective Gate capacitance.

c. C_{iss} Input capacitance (small-signal common-Source, short-circuit).

d. C_s Series capacitance.

e. I Source output current.

f. L Test circuit inductance.

g. R_g Gate equivalent series resistance (ESR).

h. R_s Series resistance.

i. V_{DS} Drain to source voltage.

j. V_{GS} Gate to Source voltage.

4. General requirements.

4.1 **Apparatus for condition A.** The apparatus required for test condition A shall include the following, configured as shown on figure 3402–1, as applicable to the specified test procedure:

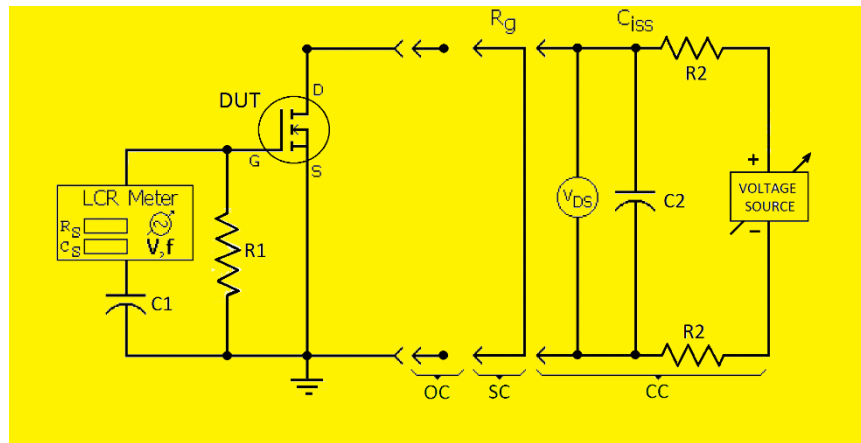
a. The Gate ESR test circuit, as shown in figure 3402–1.

(1) Drain and Source open mode test circuit (see load OC on figure 3402–1).

(2) Drain and Source short mode test circuit (see load SC on figure 3402–1).

(3) C_{iss} test circuit (see load CC on figure 3402–1).

b. **LCR meter.** The LCR meter shall be capable of supplying a sine wave signal with a magnitude up to 1 Volt (peak) and frequency of 1 MHz (typical). The LCR meter can also be used to measure R_s and C_s .



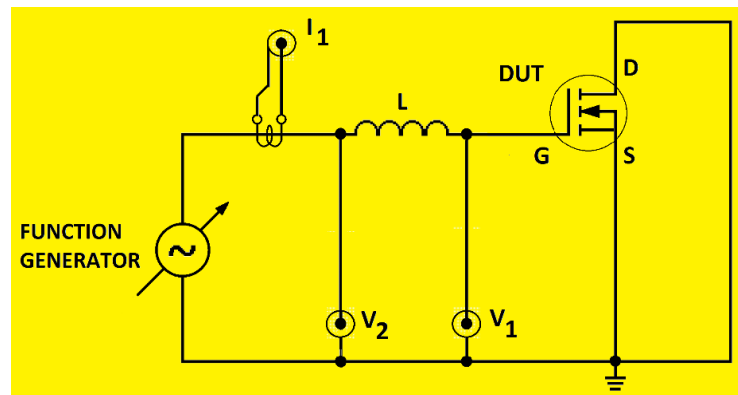
NOTES:

1. Capacitors C1 and C2 = 1 μ F.
2. Resistance R1 = 10M Ω and R2 = 33K Ω .

FIGURE 3402-1. Test circuit for condition A.

4.2 Apparatus for condition B. The apparatus required for test condition B shall include the following, configured as shown on figure 3402-2, as applicable to the specified test procedure:

- a. **The manual method** Gate ESR test circuit, as shown in figure 3402-2.
- b. A function generator source capable to supply the sine wave signal with magnitude up to 1 Volt (peak) and frequency of 1 MHz (typical).
- c. Current probe capable of high-frequency measurements.
- d. Oscilloscope capable of high-frequency measurements.



NOTES:

1. I₁ is the current sense output of current probe.
2. Inductor L = 50 μ H typical.
3. V₁ and V₂ are voltage sense inputs to oscilloscope.

FIGURE 3402-2. Test circuit for condition B.

5. Detailed requirements.

5.1 Procedure for condition A. With no DUT in the test circuit, the test begins with applying a test voltage consisting of a sine wave of frequency 1 MHz of less than 1 Volt (peak) and measuring stray capacitances of test circuit (figure 3402-1) and the empty socket where the DUT will be mounted in both Drain and Source OPEN mode (load test circuit OC) as well as Drain and Source SHORT mode (load test circuit SC). Next, using the load test circuit CC configuration, insert the DUT into the test circuit, reapply the test voltage and record R_s measurement. The measurement of C_s is optional. The values for R_g and C_g of the DUT are calculated by the LCR meter.

5.2 Procedure for condition B. With a DUT in the test circuit, the test begins with applying a test voltage consisting of a sine wave of frequency 1 MHz of less than 1 Volt (peak). Voltage V_1 is monitored and shall not to exceed the rated V_{GS} (typical ± 20 V). Adjust the test frequency f until the Source output voltage V_2 waveform and Source output current I_1 waveform are in phase. The DUT Gate ESR measurement can then be calculated using the following formula:

$$R_g = \frac{V_2}{I}$$

5.2.2 Notes.

- a. The value for C_g can also be calculated using the following formula:

$$C_g = \frac{1}{(2\pi f)^2 \times L}$$

- b. The inductor in the test circuit is normally 50 μ H in value; however, if the Gate resistance (or capacitance) is very high then the proper inductor value can be estimated using the following formula:

$$L = \frac{1}{2 \times (2\pi 10^6)^2 \times C_{iss}}$$

6. Notes.

6.1 Summary. The following conditions and details should be specified in the performance specification sheet or acquisition document.

6.1.1 Summary for condition A. The following conditions and limits should be specified for condition A:

- Test frequency (in MHz), typical 1 MHz.
- Gate ESR (in ohms), as R_s from LCR meter.
- Effective Gate capacitance (in picofarad), as C_s from LCR meter, optional.

d. Load test circuits:

(1) OC: Drain to Source open-circuit.

(2) SC: Drain to Source short-circuit.

(3) CC: C_{iss} circuit.

6.1.2 Summary for condition B. The following conditions and limit **should** be specified in for condition **B**:

- Test frequency (in MHz), **typical** 1 MHz.
- Series inductor value (in **μH**), if not 50 μH.
- Gate ESR (in ohms).
- Effective Gate capacitance (**in** picofarad), optional.

6.2 General notes.

- Even though the Gate ESR together with Gate charges helps better representing MOSFET in high speed applications and circuit simulations, the lumped R_g and effective C_g presentation does have its limitation. Some power MOSFET die in latest technology do not have symmetrical or uniform connecting conductances from Gate and Source terminations to each individual cell or stripe structures. The switching responses from the lumped R_g and effective C_g model may not be true responses. The correct series resistor and parallel capacitor model in these cases suggests a somewhat test frequency dependence in lumped R_g measurement.
- Because of DC bias and AC bias dependencies of C_g , the DC voltage induced from AC bias applying through LRC series resonant circuitry would cause C_g to be changed. The measured R_g with condition B at resonant frequency thus somewhat dependent of input signal.

Series resonant frequency:
$$W_0 = \frac{1}{\sqrt{LC_g}}$$

Series resonant characteristic impedance:
$$Z_0 = \sqrt{\frac{L}{C}}$$

7. Background. High-speed switching measurements of power **MOSFET** devices are sensitive and dependent to the stray elements (capacitive, inductive and resistive impedances) of the test circuit. As a result, switching data of identical **MOSFET** devices have difficult time reaching reasonable agreement. The ESR by design directly relates to die Gate processing such as polysilicon doping level, metallization, contact resistance, all of which affect high-speed performance. Since big process variation usually results in an ESR increase in significant magnitude, the **Gate** ESR test method provide an alternative for the industry to reach agreement on high speed switching measurements.

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METHOD 3402.1

MOSFET GATE EQUIVALENT SERIES RESISTANCE

1. **Purpose.** The purpose of this test is to determine the Gate equivalent series resistance (ESR) of power MOSFET semiconductor devices.

2. **Overview.** ~~This can be done in two ways, using either manual test circuit or LCR test equipment.~~ This test method provides a means to ensure switching consistency of power MOSFET devices. The Gate ESR measurement combined with Gate charge measurements provide an alternative to high-current high-speed measurements where MOSFET device fast switching characteristics are over-masked by test circuit stray elements.

2.1 **Test conditions.** This test method describes two test conditions (A and B) by which the Gate ESR of MOSFET devices can be determined. A description of the two test conditions of this test method are as follows:

a. Test condition A uses a LCR meter to determine Gate ESR.

b. Test condition B is a manual method to determine Gate ESR.

3. ~~2.~~ **Definitions.** The following symbols and terminology shall apply ~~for the purpose of~~ to this test method:

a. f Test frequency.

b. C_g Effective Gate capacitance.

c. C_{iss} Input capacitance (small-signal common-Source, short-circuit).

d. C_s Series capacitance.

e. I Source output current.

f. L Test circuit inductance.

g. R_g Gate equivalent series resistance (ESR).

h. R_s Series resistance.

i. V_{DS} Drain to source voltage.

j. V_{GS} Gate to Source voltage.

4. General requirements.

4.1 ~~3-4~~ **Apparatus for condition A.** The apparatus required for this test condition A shall include the following, configured as shown on figure 3402-1, as applicable to the specified test procedure:

a. ~~C_{iss}~~ The Gate ESR test circuit, as shown in figure 3402-1. ~~Capacitors C1 and C2 present short circuits at the test frequency; L1 and L2 present high ac impedance at test frequency for isolation; bridge has low dc resistance between its output terminals and capable of carrying test current without affecting the desired accuracy of measurement.~~

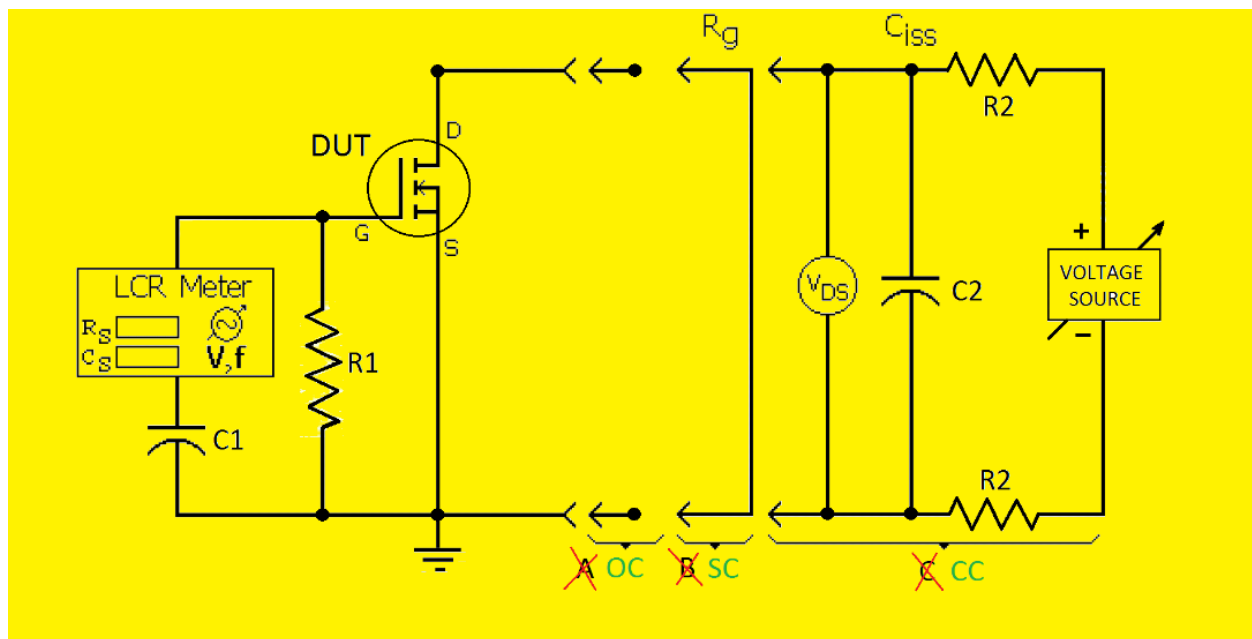
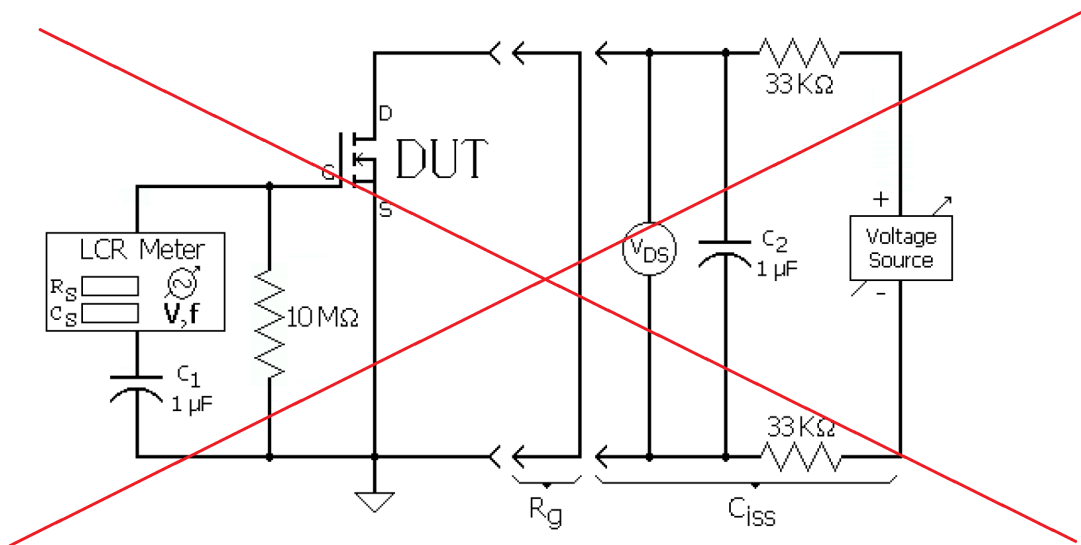
(1) Drain and Source open mode test circuit (see load OC on figure 3402-1).

(1 2) Drain and Source short mode test circuit (see load condition B SC on figure 3402-1)

(2 3) C_{iss} load test circuit (see load condition C CC on figure 3402-1).

b. **LCR meter.** The A LCR meter shall be capable to of supplying the a sine wave signal with a magnitude up to 1 Volt (peak) and frequency of 1 MHz (1MHz typical) and. The LCR meter can also be used to measure the series-resistance R_s and series-capacitance C_s .

METHOD 3402.1



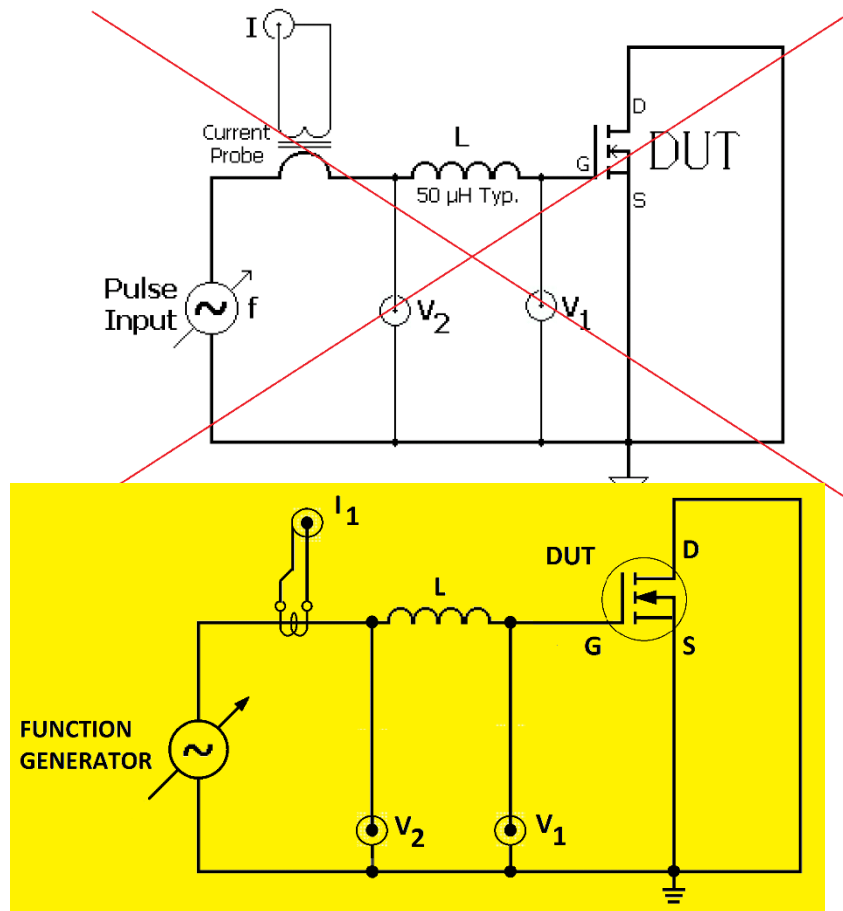
NOTES:

1. Capacitors C1 and C2 = 1 μ F.
2. Resistance R1 = 10M Ω and R2 = 33K Ω .

FIGURE 3402-1. ~~Gate ESR testing setup for MOSFETs—Condition B~~ Test circuit for condition A.

4.2 4.1 Apparatus for condition B. The apparatus required for this test condition B shall include the following, configured as shown on figure 3402-2, as applicable to the specified test procedure:

- The manual method Gate ESR test circuit, as shown in figure 3402-2.
- A function generator source capable to supply the sine wave signal with magnitude up to 1 Volt (peak) and frequency of 1 MHz (1 MHz typical).
- Current probe capable of high-frequency measurements.
- Oscilloscope capable of high-frequency measurements.



NOTES:

- I_1 is the current sense output of current probe.
- Inductor $L = 50 \mu\text{H}$ typical.
- V_1 and V_2 are voltage sense inputs to oscilloscope.

FIGURE 3402-2. ~~Gate ESR testing setup for MOSFETs—condition A~~ Test circuit for condition B.

5. Detailed requirements.

~~3. Condition A. This is the test in which a LCR meter is used with the C_{iss} test circuit. The test frequency is fixed at 1 MHz and the R_g & C_g of MOSFET device under test are calculated by the impedance analyzer.~~

5.1 ~~3.2~~ Procedure for condition A. With no DUT in the test circuit, the test begins with applying a test voltage consisting of a sine wave of frequency 1 MHz ~~sine-wave-voltage~~ of less than 1 Volt (peak) and measuring stray capacitances of test circuit (figure 3402-1) and the empty socket where the DUT will be mounted in both Drain and Source OPEN mode (load ~~condition A test circuit OC~~) as well as Drain and Source SHORT mode (~~short Drain and Source contacts prior to this measurement load condition B test circuit SC~~). Next, using the load ~~condition C test circuit CC~~ configuration, insert MOSFET device under test the DUT into the test circuit, reapply the test voltage and record R_s (C_s optional) measurements. The measurement of C_s is optional. The values for R_g and C_g of the DUT are calculated by the LCR meter.

~~3.3 Summary. The following conditions & limit shall be specified in detail specification for Condition A:~~

- ~~a. Test frequency (in MHz), typical 1MHz.~~
- ~~b. Gate ESR, as R_s from LCR meter (in Ohms).~~
- ~~c. Effective gate capacitance, as C_s from LCR meter (picofarad), optional.~~

~~4. Condition B. This is the test in which an external inductor is added in series with R_g & C_g of MOSFET device under test. The test frequency is then adjusted to get capacitive and inductive impedances cancelled out and thus pure resistance R_g can be measured.~~

5.2 ~~4.2~~ Procedure for condition B. With a DUT in the test circuit, the test begins with applying a test voltage consisting of a sine wave of frequency 1 MHz ~~sine-wave-voltage~~ of less than 1 Volt (peak). ~~V_1 Voltage V_1 is monitored and shall not to exceed the rated V_{GS} V_{GS} (typical ± 20 V). Adjust the test frequency f until the Source output voltage V_2 waveform and Source output current I_1 waveform are in phase. The MOSFET the DUT Gate ESR measurement can then be calculated from below using the following formula:~~

$$R_g = \frac{V_2}{I_1}$$

5.2.2 ~~4.3~~ Notes.

- a. The ~~effective Gate Capacitance~~ value for C_g can also be calculated ~~with below~~ using the following formula:

$$C_g = \frac{1}{(2\pi f)^2 \times L}$$

- b. The inductor in the ~~test~~ circuit is normally 50 μ H in value; however, if the Gate resistance (or capacitance) is very high then the proper inductor value can be estimated ~~with below~~ using the following formula:

$$L = \frac{1}{2 \times (2\pi 10^6)^2 \times C_{iss}}$$

6. Notes.

6.1 Summary. The following conditions and details should be specified in the performance specification sheet or acquisition document.

6.1.1 ~~3-3~~ Summary for condition A. The following conditions & and limits ~~shall~~ should be specified in ~~detail~~ specification for condition A:

- a. Test frequency (in MHz), typical 1 MHz.
- b. Gate ESR (in ohms), as R_s from LCR meter (~~in Ohms~~).
- c. Effective Gate capacitance (in picofarad), as C_s from LCR meter (~~picofarad~~), optional.
- d. Load ~~conditions~~ test circuits:

~~A~~ (1) OC: Drain to Source open-circuit.

~~B~~ (2) SC: Drain to Source short-circuit.

~~C~~ (3) CC: C_{ISS} circuit.

6.1.2 ~~4-4~~ Summary for condition B. The following conditions and limit ~~shall~~ should be specified in ~~detail~~ specification for condition ~~A~~ B:

- a. Test frequency (in MHz), ~~about~~ typical 1 MHz.
- b. Series inductor value (in ~~micro-Henry~~ μH), if not 50 μH .
- c. Gate ESR (in ohms).
- d. Effective Gate capacitance (in picofarad), optional.

6.2 ~~5-~~ General notes.

- a. Even though the Gate ESR together with Gate charges helps better representing MOSFET in high speed applications and circuit simulations, the lumped R_g and effective C_g presentation does have its limitation. Some power MOSFET die in latest technology do not have symmetrical or uniform connecting conductances from Gate and Source terminations to each individual cell or stripe structures. The switching responses from the lumped R_g and effective C_g model may not be true responses. The correct series resistor and parallel capacitor model in these cases suggests a somewhat test frequency dependence in lumped R_g measurement.
- b. Because of DC bias and AC bias dependencies of C_g , the DC voltage induced from AC bias applying through LRC series resonant circuitry would cause C_g to be changed. The measured R_g with condition B at resonant frequency thus somewhat dependent of input signal.

Series resonant frequency:
$$W_0 = \frac{1}{\sqrt{LC_g}}$$

Series resonant characteristic impedance:
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7. 4.4 Background. High-speed switching measurements of power MOSFET devices are sensitive and dependent to the stray elements (capacitive, inductive and resistive impedances) of the test circuit. As a result, switching data of identical MOSFET devices have difficult time reaching reasonable agreement. The ESR by design directly relates to die Gate processing such as polysilicon doping level, metallization, contact resistance, all of which affect high-speed performance. Since big process variation usually results in an ESR increase in significant magnitude, the Gate ESR test method provide an alternative for the industry to reach agreement on high speed switching measurements.

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KEY to HIGHLIGHTING:

- a. Text highlighted in yellow was added and red text with strike-out will be removed. These changes were included in the initial draft.

The source of these changes were from DLA Land and Maritime.

- b. Text or figures highlighted in green was added and red text with strike-out and highlighted in blue will be removed. These changes will be included in the initial draft for coordination of MIL-STD-750-3.

The source of these changes were from comments made to the initial draft.