

ENGINEERING PRACTICES STUDY

PROJECT NUMBER: 5961-2021-020

TITLE:

MIL-STD-750-3, TEST METHOD 3101

PROPOSED REVISION TO EMPHASIZE
THERMAL IMPEDANCE TESTING USING
AUTOMATIC TEST EQUIPMENT

27 AUGUST 2021

FINAL REPORT

STUDY CONDUCTED BY

DLA LAND AND MARITIME
DOCUMENT STANDARDIZATION DIVISION (VA)
ACTIVE DEVICE BRANCH (VAC)

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I. OBJECTIVES: The objective of this Engineering Practice (EP) study was to obtain comments or concurrence from the military services, device manufacturers, laboratories, OEMs, and the user community concerning a proposed revision to test method 3101 of MIL-STD-750-3 to change the way that thermal impedance testing is to be performed.

II. BACKGROUND: The current test method 3101.4 was last revised in November 2006. A draft of test method 3101 that changed the focus of how thermal impedance testing is to be performed in the method was submitted to DLA-VAC by the JEDEC 13.1 Technical 750 Test Method Review task group Chair. The major change in the proposed revision was to make the use of automatic test equipment (ATE) and techniques for performing thermal impedance testing the preferred method and to relegate the existing older thermal response methods as non-preferred. After performing a review of the content of the current wording of test method 3101, editorial issues were noted and were included in the initial draft of the proposed test method revision.

III. RESULTS: Essential and technical comments were received regarding the changes proposed by the revision. Those comments were resolved from a point of view to pursue the original focus of the project to emphasize ATE and techniques over thermal response techniques for thermal impedance testing. The changes made to the EP study test method draft (see attachment 1) reflect the original focus of the EP study.

IV. CONCLUSIONS: The preparing activity believes that the current thermal response testing procedures and support requirements that were proposed for relegating as non-preferred and partial removal from the method must be kept in method 3101 for legacy testing purposes. The preparing activity will attempt to restructure the current method to keep these legacy portions and the new proposed portions within the same method, but if that is not possible, then a new method will be created that contains the new proposals.

V. RECOMMENDATIONS: Attempt to include the general updates and the new ATE content, within the attached draft method, into the existing method 3101. If they are not able to be combined cohesively then include a revision of method 3101 which only addresses the editorial issues of method 3101 that were noted in the review in the next standardization action to MIL-STD-750-3. Also, the draft method included in this final report would then be included as a new test method in the next standardization action to MIL-STD-750-4.

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DRAFT DATE: 27 AUGUST 2021

METHOD XXXX

THERMAL IMPEDANCE TESTING OF DIODES

1. **Purpose.** The purpose of this test method is to determine the thermal performance of diodes (hereafter referred to as 'devices').

2. **Overview.** The test procedures covered by this method can also be applied to rectifier diodes, transient voltage suppressors, power Zener diodes, and some Zener, signal, and switching diodes.

2.1 **Introduction for steady-state thermal impedance and transient thermal impedance testing.** The thermal performance testing covered by this test method can determine two different characterizations: Steady-state thermal impedance (hereafter referred to as 'thermal resistance') or transient thermal impedance (hereafter referred to as 'thermal impedance') testing. Thermal resistance testing determines thermal performance of devices at long heating times (also see method 4081). Both thermal impedance and thermal resistance are measured in °C/W. A thermal impedance graph illustrates overall thermal performance from short transients to very long heating times. Thermal impedance with suitable heating times determines the ability of the device die-to-package interface to transfer heat from the die to the package and is a measure of the thermal quality of the die attachment. Also, thermal impedance testing may be done for production screening with ATE measured in °C/W where this quotient measures the change in junction temperature in degrees Centigrade as a result of a known power level in watts applied for a specific heating time. The junction temperature measurements are achieved by a temperature sensitive parameter (TSP) or what is often the forward diode voltage with a known temperature characteristic at a specific measuring current. See appendix A for procedures for measuring the TSP of devices. It is relevant to designs that use either headers, or heat conducting plugs, with mass and thermal conductivity allowing effective discrimination of poor die attachments. This is particularly true with power devices. Some Zener constructions, particularly when used with small junction area designs, cool too rapidly from the cessation of heating current to provide accurate measurement when forward (diode) current is used for this test. For such devices, a method is provided to apply currents in the Zener direction and make a measurement much closer to the termination of the heating current. In this way, no minority carriers are involved and inductive effects are minimized due to lower test current. This may be considered a laboratory measurement since cable lengths in an ATE may prevent accurate measurements so close to cessation of the heating current. This laboratory method is intended on initial Zener device design verification for correlation to forward direction thermal impedance testing (such as with an ATE) prior to establishing a production test limit. Correlation assurance should be provided in the forward direction production monitoring that thermal impedance in the reverse direction (Zener) does not exceed the specified limit. If this Zener test method exceeds the forward method by 10 percent or more, production monitoring (with an ATE in the forward direction) will require a lower limit, for some devices, than that required by the more accurate laboratory method (see 5.6.1). See appendix B for procedures for establishing testing conditions and acceptance limits of devices.

2.1.1 **Background and scope for thermal impedance.** Thermal impedance of devices is sensitive to the presence of voids in the die attachment material between the die and package since these voids impede the flow of heat from the die to the package. Due to the difference in the thermal time constants of the die and package, the measurement of thermal impedance is more sensitive to the presence of die attachment material voids than the measurement of thermal resistance. This is because the thermal time constant of the die is shorter than that of the package. Thus, the heating power pulse width can be selected so that only the die and the die-to-package interface are heated during the heating power pulse by using a pulse width somewhat greater than the die thermal time constant but less than that of the package. Heating power pulse widths ranging from 1 ms to 400 ms for various package designs have been found to satisfy this criterion. This enables the detection of die attachment material voids to be greatly enhanced, with the added advantage of not having to heat sink the DUT. Thus, the shorter heating times of thermal impedance testing using ATE make it more efficient than thermal resistance testing for production testing (manufacturing screen, process control, production monitoring) or incoming inspection for the thermal quality of internal die attachments near the device junction.

2.1.2 **Background and scope for thermal resistance testing.** Thermal resistance testing using very long heating times is typically performed in a laboratory environment in accordance with method 4081 of MIL-STD-750-4. Method 4081 tests the thermal quality from the device junction to a defined external reference point on the package.

2.2 Test procedures. The three thermal impedance test procedures covered by this test method are as follows:

- a. Thermal impedance characterization of single junction devices (see 5.2).
- b. Thermal impedance characterization of multiple junction devices (see 5.3).
- c. Thermal impedance production screening (see 5.4 and appendix C).

2.3 ATE versus discrete test instrumentation. The test procedures to determine thermal impedance can use either ATE or discrete test instrumentation. This revision of this test method has been restructured to emphasize the use of ATE over the legacy test procedures of previous revision which were based on the use of discrete test instrumentation.

3. DEFINITIONS

3.1 Abbreviations. The following abbreviations are used in this test method.

- a. FEA Finite element analysis.
- b. TCZ Temperature compensated Zeners.
- c. VTC Voltage-temperature coefficient.

3.2 Definition of terms. The following definitions apply to the terms used in this test method.

3.2.1 Header. A header is that portion of a sealed device that provides both support for the external terminal and a feedthrough into the internal portion of the device. Headers can be of two types: Solid metal and ceramic or glass filled. The ceramic or glass filled header provides insulation as well as support and feedthrough for the terminals.

3.2.2 K-factor. The K-factor is a thermal calibration factor equal to the reciprocal of VTC. The K-factor relates the changes in TSP voltage to changes in junction temperature (T_j). The relationship is determined by a K-factor measurement (i.e., calibration). See 3.5 for the K-factor equation and appendix A for examples, methods and procedures for calculating the K-factor.

3.2.3 Thermal impedance (general) (see symbol Z_{θ}). The following definitions are associated with the term "thermal impedance" as used in this test method. Thermal impedance is also known as 'transient thermal impedance'. The term "thermal impedance" will be used in lieu of the term "transient thermal impedance" in this test method.

3.2.3.1 Thermal impedance. The change in temperature difference between two specified points or regions such as die-to-package that occurs during a heating time interval divided by the step-function change in power dissipation that occurred at the beginning of the interval and caused the change in temperature difference measured in units of $^{\circ}\text{C}/\text{W}$. This important feature for thermal management is also often included in performance specifications as a thermal impedance curve versus heating time.

3.2.3.2 Thermal impedance testing. Thermal impedance, with suitable heating times and heating currents, determines the ability of the die-to-header interface to transfer heat from the die to the header.

3.2.4 Thermal resistance (general) (see symbol R_{θ}). The following definitions are associated with the term "thermal resistance" as used in this test method. Thermal resistance is also known as "steady-state thermal impedance". The term "thermal resistance" will be used in lieu of the term "steady-state thermal impedance" in this test method. The typical units for thermal resistance are $^{\circ}\text{C}/\text{W}$.

3.2.4.1 Thermal resistance. The temperature difference between two specified points or regions divided by the power dissipation, under conditions of thermal equilibrium. The typical units for thermal resistance are $^{\circ}\text{C}/\text{W}$.

3.2.4.2 Thermal resistance testing. Thermal resistance testing determines performance of devices at steady state operation.

3.2.5 Thermal impedance testers. Thermal impedance testers are now available as ATE for high volume efficient testing for short heating times in production screening. They may also be used for thermal resistance at steady state operation if so equipped when used with adequate heat sinking and/or heat sink temperature monitoring as described in method 4081.

3.2.6 TSP. An electrical parameter of a device that varies directly with junction temperature in a linear or very nearly linear fashion. TSP is the temperature sensitive parameter of V_F or V_Z . The TSP is measured over a temperature range similar to the test temperature range at an I_M or I_{M2} that will permit resolution at the highest temperatures reached during the test.

3.2.7 TSP junction. A TSP junction is the junction being heated during thermal characteristic testing.

3.2.8 VTC. The voltage-temperature coefficient is the reciprocal of K.

NOTE 1: See 3.3.2.g (α_{VF}) and 3.3.3.d (α_{VZ}) for symbols.

NOTE 2: The typical units for VTC are mV/°C.

3.3 Symbols and definitions. The symbols common with both the forward and reverse directions of testing of the TSP are listed in 3.3.1. The symbols associated with forward direction testing of the TSP are listed in 3.3.2. The symbols associated with reverse direction testing (using the Zener biased direction) of the TSP are listed in 3.3.3. See 3.3.4 for symbol substitution difference between the forward and reverse direction.

3.3.1 Common symbols. The following symbols are common for both the forward and reverse direction testing:

a. K A thermal calibration factor equal to the reciprocal of VTC.

NOTE 1: K must be measured over a temperature range similar to the test temperature range at an I_M that will permit resolution at the highest temperatures reached during the test.

NOTE 2: The typical units for K are °C/mV.

NOTE 3: The value of K will be substantially different when using the reverse (Zener bias) direction. Some difference will be observed between Zener devices with different nominal voltages.

NOTE 4: See 3.5 for an equation and appendix A for example calculations for the value of K.

b. P_H The heating power pulse applied to the DUT. The product of V_H and I_H (or V_{HZ} and I_{HZ}) during the heating power pulse.

NOTE: Also referred to as 'heating power' in this test method.

c. P_T The measurement power applied to the DUT ($V * I$). For forward direction testing, $P_T = (V_F * I_M)$.

d. $R_{\theta JA}$ Thermal resistance from device junction to the ambient T_A .

NOTE: The typical units for $R_{\theta JA}$ are °C/W.

e. $R_{\theta JC}$ Thermal resistance from device junction to a point on the outside surface of the case immediately adjacent to the device chip.

NOTE: The typical units for $R_{\theta JC}$ are °C/W.

f. $R_{\theta JX}$ Thermal resistance from device junction to a defined reference point.

NOTE: The typical units for $R_{\theta JX}$ are °C/W.

g. T_A Ambient or free-air temperature, the air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.

NOTE: Testing has historically been performed in an open lab or on the production floor subject to natural convection and air movement produced by HVAC (heating, ventilation and air conditioning) common to all industrial locations. Any air movement in excess of 1.0 m/s must be blocked.

h. T_{EC} The temperature of the end cap of a surface-mount package.

i. t_H The duration of P_H pulse applied to the DUT. Also referred to as 'heating time' in this test method.

j. theta A term sometimes used in place of the symbol Z_θ in some art and associated text in some MIL-PRF-19500 specification sheets. The symbol Z_{th} is also used in place of the symbol Z_θ .

k. T_J The junction temperature of the DUT.

l. t_M The measurement pulse time.

m. t_{MD} Measurement delay time is the time from the start of P_H removal to the start of the final V_F (or V_{ZL}) measurement time, referred to as t_{sw} .

NOTE 1: The symbols t_{md} or tmd are sometimes used in place of the symbol t_{MD} in some art and associated text in this test method.

NOTE 2: The typical units for t_{MD} are in microseconds (μs).

NOTE 3: Delay shall be sufficient in length to allow for attenuation of switching transients to occur. The delay time will vary according to the length of the cable to test fixture (shorter is always better), associated fixture inductances, package magnetic properties and die charge storage properties. See further clarification of the use of t_{MD} in appendix D.

n. t_{sw} The sample window time during which final V_F (or V_{ZL}) measurement is made.

NOTE: The value of t_{sw} should be small; it can approach zero if an oscilloscope is used for manual measurements.

o. $Z_{\theta JC}$ Thermal impedance from device junction to a point on the outside surface of the case immediately adjacent to the device.

NOTE 1: $Z_{\theta JC}$ is measured over a time interval equal to the thermal time constant of the device.

NOTE 2: The typical units for $Z_{\theta JC}$ are $^{\circ}C/W$.

p. $Z_{\theta JX}$ Thermal impedance from device junction to a time defined reference point.

NOTE 1: The typical units for $Z_{\theta JX}$ are $^{\circ}C/W$.

NOTE 2: Z_θ has been called "theta" in some art and associated text in this document.

3.3.2 Forward direction. The following symbols and definitions apply for the purpose of this test method in the forward direction.

- a. I_H The heating current applied to the DUT during the heating time in order to cause power dissipation.
- b. I_M The measurement current used to forward bias the TSP junction for measurement of V_F .
NOTE: See 3.3.3 and 3.3.4 when using the reverse (Zener biased) direction for the TSP.
- c. V_F The forward biased junction voltage of the DUT used for junction temperature sensing or the TSP.
NOTE: See 3.3.3 and 3.3.4 when using the reverse (Zener biased) direction for the TSP.
- d. V_{Ff} The final V_F value after application of P_H .
- e. V_{Fi} The initial V_F value before application of P_H .
- f. V_H The heating voltage resulting from the application of I_H to the DUT.
- g. α_{VF} The temperature coefficient of V_F with respect to T_J at a fixed value of I_M .
NOTE: The typical units for α_{VF} are mV/°C.
- h. ΔV_F The change in the TSP, V_F , due to the application of P_H to the DUT.

3.3.3 Reverse (Zener biased) direction. The following symbols and abbreviations apply for the purpose of this test method in the reverse direction.

- a. V_Z The reverse biased (Zener) junction voltage of the DUT used for junction temperature sensing or the TSP.
- b. V_{Zf} The final V_Z value after application of P_H .
- c. V_{Zi} The initial V_Z value before application of P_H .
- d. α_{VZ} The temperature coefficient of V_Z with respect to T_J at a fixed value of I_M .
NOTE: The typical units for α_{VZ} are mV/°C.
- e. ΔV_Z The change in the TSP, V_Z , due to the application of P_H to the DUT.

3.4 Variable substitutions when using the reverse (Zener bias) direction. When using the reverse (Zener bias) direction as the TSP, instead of the forward direction, the following changes shall further apply to the definitions and formulas in this test method whenever they appear in the text:

- a. Letter symbols

I_F	is replaced by	I_Z
V_F	is replaced by	V_Z
V_H	is replaced by	V_{ZH}
V_{Fi}	is replaced by	V_{Zi}
V_{Ff}	is replaced by	V_{Zf}
ΔV_F	is replaced by	ΔV_Z
V_{F1}	is replaced by	V_{Z1}
V_{F2}	is replaced by	V_{Z2}
- b. Wording: Forward bias is replaced by reverse bias. Forward direction is replaced by reverse direction.

3.5 K-factor equation. The K-factor is calculated in accordance with the following equation:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}} \right| \text{ } ^\circ\text{C/mV}$$

Where:

- a. T_{J1} = Initial junction temperature in $^\circ\text{C}$
- b. T_{J2} = Final junction temperature in $^\circ\text{C}$
- c. V_{F1} = Initial V_F voltage in mV
- d. V_{F2} = Final V_F voltage in mV

See [appendix A](#) for methods, procedures and examples of measuring the K-factor using the TSP.

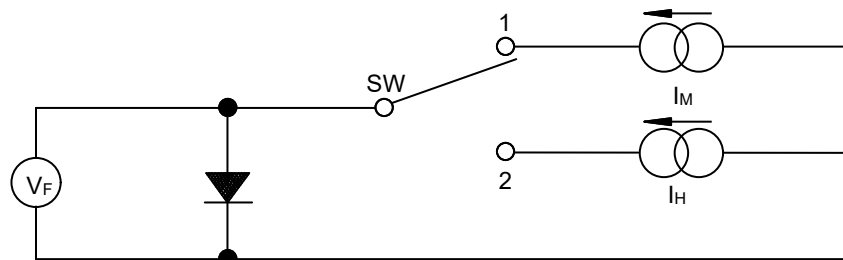
4. General requirements.

4.1 Apparatus. The apparatus required for this test shall include the following as applicable to the specified test procedures and techniques used.

4.1.1 ATE test instrumentation. When used, ATE test instrumentation shall be capable of establishing the required testing conditions and measuring the required electrical parameters to determine the thermal performance of the DUT.

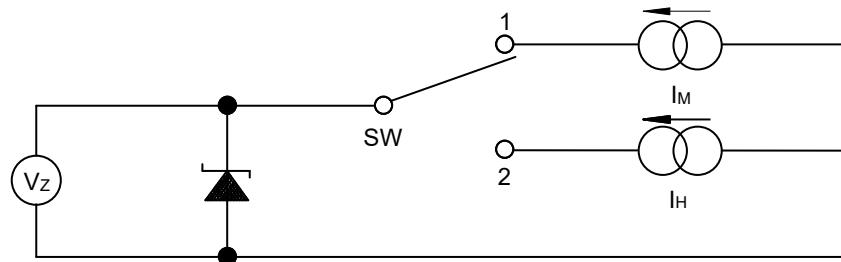
4.1.2 Discrete test instrumentation. When used, discrete test instrumentation shall be capable of applying the specified currents to the DUT and measuring the resulting parameters. The discrete test instrumentation required for this type of testing shall include the applicable test circuit as shown on figure XXXX-1 and the following, as applicable to the specified test procedure:

- a. A constant current source capable of adjustment to the desired value of I_H and able to supply the value of V_H required by the DUT. The constant current source should be able to maintain the desired value of I_H to within ± 2 percent during the entire length of heating time.
- b. A constant current source to supply the value of I_M with sufficient voltage compliance to turn the TSP junction fully on.
- c. An electronic switch capable of switching between the measurement conditions, the heating period conditions and the final measurement conditions in a time frame short enough to avoid DUT cooling during the transition; this typically requires switching in the microsecond or tens of microseconds range.
- d. A voltage measurement circuit capable of accurately making the V_{Ff} and V_{Fi} measurements within the time frame with millivolt resolution.



Thermal impedance test circuit for forward direction testing of diodes

FIGURE XXXX-1. Thermal impedance test circuit for diodes.



Thermal impedance test circuit for reverse direction testing of Zener diodes

FIGURE XXXX-1. Thermal impedance test circuit for diodes – continued.

4.1.3 **Temperature controlled environment.** The temperature controlled environment needed for measurement of TSP in appendix A shall be a liquid bath or oven chamber capable of maintaining the specified reference point temperature to within ± 1.0 °C of the preset (measured) value.

5. Detailed requirements.

5.1 **Thermal impedance test operation.** The use of ATE is the preferred method of determining thermal impedance of devices. The procedure of 5.2 covers single junction die, the procedure of 5.3 covers die with multiple junctions, and the procedure of 5.4 covers thermal impedance production screening.

5.1.1 **Forward direction.** The test procedures of 5.2 and 5.3 detail the use of discrete test instrumentation of 4.1.2 using the forward direction test circuit of figure XXXX-1 and waveform on figure XXXX-2.

5.1.2 **Reverse direction.** When using the reverse direction, correlation assurance shall be provided in the forward direction production monitoring that thermal impedance in the reverse (Zener bias) direction shall not exceed the specified limit.

5.2 Characterization of single junction devices.

5.2.1 **General.** The following details the requirements for thermal impedance testing devices with die that use a single junction design. See appendix B for guidelines on selecting values of I_H , I_M , t_H , and t_{MD} .

5.2.2 **Procedure.** The testing of single junction devices is summarized as follows:

- The test begins with the adjustment of I_M and I_H to the desired values (see figures XXXX-2 and XXXX-3). The value of I_H is usually at least 50 times greater than the value of I_M .
- Then with the electronic switch in position 1, the value of V_{FI} shall be measured.
- The switch is then moved to position 2 for a length of time equal to t_H and the value of V_H shall be measured.
- Finally, at the conclusion of t_H , the switch is again moved to position 1 and the value of V_{FI} is measured within a time period defined by t_{MD} (or $t_{MD} + t_{SW}$ depending on the definitions stated previously).
- The two current sources are then turned off at the completion of the test.

5.2.3 **Testing of devices with multiple junctions in series.** For the purposes of this test method, multiple in series P-N junctions oriented in the same direction (stacked-die) configurations shall be treated as a single element as be tested using the procedure in 5.2.2. The resulting thermal impedance measurement represents the entire die-stack assembly.

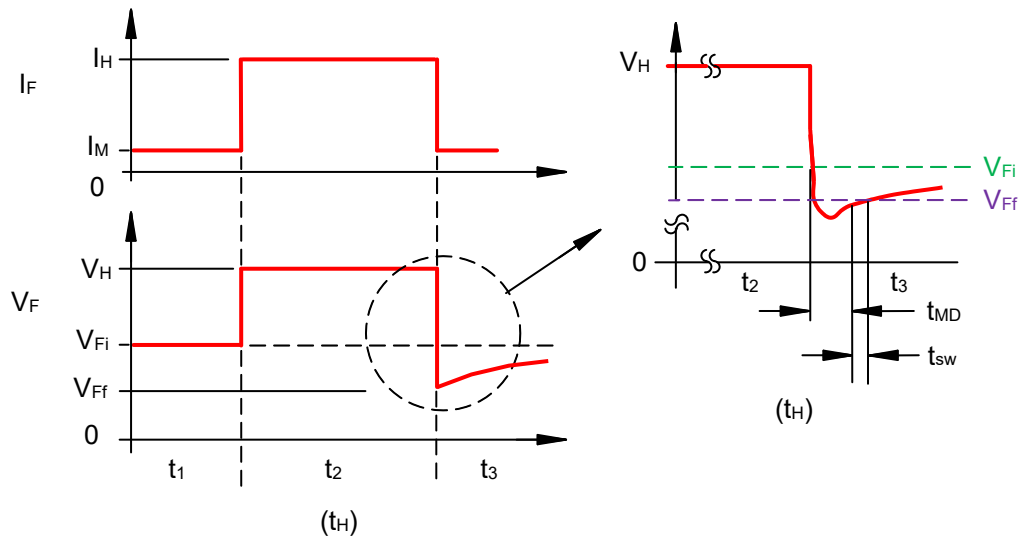


FIGURE XXXX-2. Thermal impedance testing waveforms for forward biased procedures.

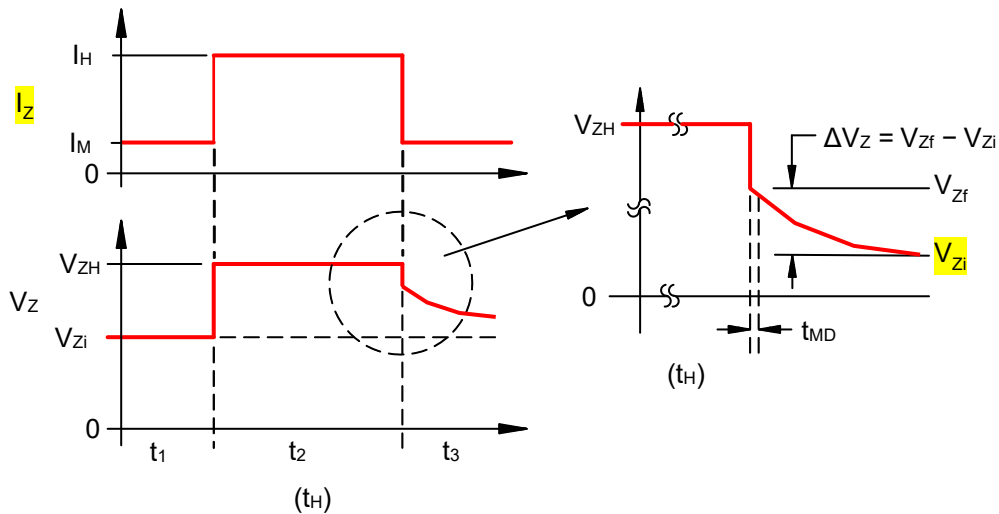


FIGURE XXXX-3. Thermal impedance testing waveforms for reverse (Zener) biased procedures.

5.3 Characterization of multiple parallel junction devices (dual, quad and arrays).

5.3.1 General. Traditionally, thermal impedance is required in device specification sheets without any clarification as to whether the values are for each element or all elements in parallel. While the assumption has been that the specification limits for thermal resistance apply to all elements in parallel, there has been no procedure on how to perform this. The thermal resistance test setup cannot directly parallel the devices because the junction with the lower V_F may draw some of the current away from the other elements. The test circuitry necessary for measuring thermal resistance and thermal impedance of devices with multiple parallel junctions can be prohibitive.

5.3.1.1 Thermal impedance. Thermal impedance shall be measured on each element individually while the other elements are un-powered as it is intended to assess die-to-header bond quality. These individual readings cannot be combined in any way to yield the total rating. This means that there is no universal method to measure the thermal impedance of dual, quad, or array as a whole and the individual device specification should not require such a measurement. Overall, power rating can be derived from similar packages employing single elements or by extensive computer modeling.

5.3.1.2 Thermal resistance. For thermal resistance only, measuring one junction while the other junctions are passively biased at the same power level does work. No power is to be applied until V_F has been measured; however, V_{F1} will likely be unaffected if the passively biased junctions are turned off a little late. The thermal resistance value for the measured junction is divided by the total number of junctions being biased to calculate an overall package thermal resistance.

5.3.2 Procedure. The testing of multiple parallel junction devices is summarized as follows:

- a. Begin thermal resistance test of one junction while others junctions are off.
- b. Power up remaining junctions to same current as the test junction.
- c. Power off remaining junctions only after the test junction reading has been acquired.
- d. Calculate total device thermal resistance by dividing the acquired reading of test junction by the total number of junctions in the package.

5.3.3 Limitations. This procedure is not recommended for determining thermal impedance for multiple parallel junction devices since short readings are not affected much by adjacent junction elements and the switching of the remaining junctions in such short time periods is prohibitive.

5.4 Thermal impedance production screening. The goal of thermal impedance production screening is to detect and remove any device that has defects that can affect reliability or performance. The key factors for this testing are as follows:

- a. Determine a K-factor and VTC for the DUT as described in appendix A. These parameters are normally measured at a current selected so that it does not affect the accuracy of the thermal impedance test.
- b. Determine a P_T measurement power and t_M measurement pulse time. The measurement pulse time should be sufficient to delineate the package layer being monitored. For example: 10 ms to 30 ms measures the die bond integrity and 100 ms to 300 ms measures both the die bond plus an additional die tab attach to the package header. See C.3 herein. The heating power pulse should be sufficient to heat the junction up at least 25 °C unless limited by a maximum power density rating of the junction or by I_H limitations of the test equipment (see B.3 step 3 and EXCEPTION therein).
- c. Determine a t_{MD} to provide the junction temperature.
- d. Deploy test equipment capable of applying the pulse determined in 5.4.b and providing an output that either directly calculates the peak junction temperature with the supplied K-factor and provides a thermal impedance reading in °C/W or provides a delta voltage change that can manually be converted to thermal impedance by multiplying by the K-factor and dividing by the P_T measurement power. This t_{MD} delay time is usually provided by the appropriate specification but extenuating circumstances such as die storage time or package magnetic resonance may dictate using a longer value of t_{MD} . This is permitted provided a correlation is established between the required value of t_{MD} and the specified value of t_{MD} .

The supplier shall notify DLA Land and Maritime of any specified measurement conditions that might fail to achieve the thermal impedance test method's primary goal of detecting and removing defective devices.

5.5 Notes. The following details apply to the test procedures of 5.2 and 5.3.

- a. ATE provides the value for $Z_{\theta JX}$ directly instead of using V_{FI} and V_{FT} for thermal impedance or thermal resistance calculations. This is also now the preferred method instead of using older "thermal response" methods with ΔV_F values in Volts. Record the value of $Z_{\theta JX}$.
- b. Alternative waveforms, as may be generated by ATE using the general principles of this method, may be used upon approval of the qualifying activity.
- c. The reverse direction (Zener biased) testing method in figure XXXX-3 illustrates a positive TSP when the Zener device is in avalanche breakdown. It is also possible to portray a negative TSP for low voltage Zener devices when they are in the field emission or tunneling mode. A near zero TSP can also result from these two off-setting factors of a specific operating current that shall be avoided by changing to a higher or lower current. Also see appendix A herein for methods and procedures for measuring the TSP. Note that for Zener devices, I_{M2} can be equal to I_{H2} provided the sense time for I_{M2} at the end of t_H is no more than 5 percent of the overall heating time (t_H) for I_{H2} . This 5 percent value will correlate to a thermal impedance reading that is no more than 5 percent lower than the true value. This is not unlike to the minor errors caused by the measurement delay time associated with the forward direction method.
- d. TCZ do not normally respond to the reverse direction (Zener biased) method of figure XXXX-3 since the Zener junction is compensated by a "stabistor". This compensation results in a near zero time constant for the reference voltage as desired where the TSP becomes ineffective in the normal operating direction for measuring thermal impedance. However, when the stabistor used is another Zener diode with a V_Z higher than the TCZ's own Zener, the device can be operated in its reverse direction using the stabistor as both the heat-generating and temperature sensitive element. This is especially true if the two junctions are part of the same die. When an independent stabistor die or multiple stabistor dice are employed, the results will be an average of all the dice. Also the K_F factor used for the thermal impedance measurement becomes the total of the stabistor(s) and the Zener in the TCZ device. Heating test times for TCZ thermal measurement in the range of 10 ms to 30 ms allows all the junctions to be proportionally activated.

5.6 Acceptance limits.

5.6.1 General discussion. Historically the variations in device characteristics from one manufacturer to another caused difficulty in establishing a single acceptance limit for all devices tested to a given specification sheet when only using a thermal response method with acceptance limit values for ΔV_F since different design, materials, and processes can alter the resultant ΔV_F value for a given set of test conditions. It has now been recognized absolute thermal impedance limits are required for best correlation of applied power to surge performance such as for Zener or rectifier diodes. In such examples, setting a limit for Zener diode construction with the forward direction (the usual ATE) method requires prior evaluation of $Z_{\theta JX}$ (and $R_{\theta JX}$, when desired) by the Zener biased method. If the Zener biased method result is more than 10 percent higher, the limit shall be based on the more accurate Zener biased measurement. In such a case, if it is desired to use the forward biased method for TSP, the limit ($Z_{\theta JX}$ or $R_{\theta JX}$) shall be reduced by the extent (percentage) difference between the two methods.

5.6.2 $Z_{\theta JX}$ limit. (For full characterization with the proper ATE.) The thermal impedance approach uses an absolute magnitude value specification that overcomes the problems associated with the other older approaches. Thermal impedance is time dependent and is calculated as follows:

$$Z_{\theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_F)}{(I_H)(V_H)} \right| \text{ } ^\circ\text{C/W}$$

5.6.3 $R_{\theta JX}$ limit. (For thermal resistance specification testing.) The thermal resistance to some defined point, such as the case ($R_{\theta JC}$), lead ($R_{\theta JL}$), or end cap ($R_{\theta JEC}$), is an absolute magnitude value specification used for equilibrium conditions. The t_H heating time shall therefore be extended to longer times. This may range from only 1 second on high power devices to 20 seconds or longer on low power axial-leaded devices where the thermal impedance curve flattens out for thermal resistance values when using well controlled reference point temperatures. In the example of $R_{\theta JC}$, $R_{\theta JL}$, or $R_{\theta JEC}$ measurements, the case, lead or end cap reference points shall be carefully stabilized and monitored in temperature which requires an infinite heat sink or careful monitoring for optimum results. The ΔT_J in the equation below is the difference in T_J to the case, lead, or end cap reference temperature as applicable by package type.

$$R_{\theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_F)}{(I_H)(V_H)} \right| \text{ } ^\circ\text{C/W}$$

METHOD XXXX

NOTE: Some ATE designed primarily for thermal impedance testing with short heating times (t_H) may not include capabilities of controlling or monitoring these reference temperatures for an accurate thermal resistance test measurement at long heating times. See method 4081 of MIL-STD-750-4 for further details on testing thermal resistance of diodes.

5.6.4 General comment for thermal impedance testing. One potential problem in using the thermal impedance testing approach lies in trying to make accurate enough measurements with sufficient resolution to distinguish between acceptable and nonacceptable devices. As the DUT current handling capability increases, the thermal impedance under transient conditions will become a very small value. This raises the potential for rejecting good devices and accepting bad ones. Higher I_H values shall be used in this case.

6. Summary. The following test conditions and measurements to be specified and recorded.

6.1 Thermal impedance and equilibrium measurements.

6.1.1 Test conditions. Specify the following test conditions:

- a. I_M measurement current ___mA
- b. I_H heating current ___A
- c. t_H heating time ___ms
- d. t_{MD} measurement time delay ___ μ s
- e. t_{SW} sample window time ___ μ s

6.1.2 Data. Record the value of $Z_{\theta JX}$.

6.2 K-factor calibration. (Optional for criteria 6.2.1.a or 6.2.1.b, mandatory for 6.2.1.c, 6.2.1.d, or 6.2.1.e.)

6.2.1 Test conditions. Specify the following test conditions:

- a. I_M measurement current ___ mA
- b. T_{J1} initial junction temperature ___°C
- c. V_{F1} initial V_F voltage ___mV
- d. T_{J2} final junction temperature ___°C
- e. V_{F2} final V_F voltage ___mV

6.2.2 K-factor. Calculate K-factor in accordance with the equation of 3.5.

K-factor ___°C/mV

6.3 Specification limit calculations. One or more of the following should be measured or calculated, as stated on the device specification sheet (see 5.6.1):

- a. $Z_{\theta JX}$ ___°C/W (For large variation in K among devices).
- b. $R_{\theta JX}$ ___°C/W

APPENDIX A

MEASUREMENT OF THE TSP

A.1 Scope. This appendix contains the methods and procedures for measuring the K-factor using the TSP of devices covered by this test method. This appendix is a mandatory part of the test method. The information contained herein is intended for compliance.

A.2 Measurement of the TSP V_F (or V_Z). The calibration of V_F versus T_J ($1/K$) is accomplished by monitoring V_F for the required value of I_M as the environmental temperature (and thus the DUT temperature) is varied by external heating. It is relevant to programming the ATE with the applicable K-factor in the acceptance criteria (see 5.6.2 and 5.6.3). The magnitude of I_M shall be chosen so that V_F is a linearly decreasing function over the normal T_J range of the device. I_M shall be large enough to ensure that the device junction is turned on but not large enough to cause significant self heating.

A.2.1 Example TSP measurement test setup. An example TSP measurement test setup is shown on figure XXXX-A1.

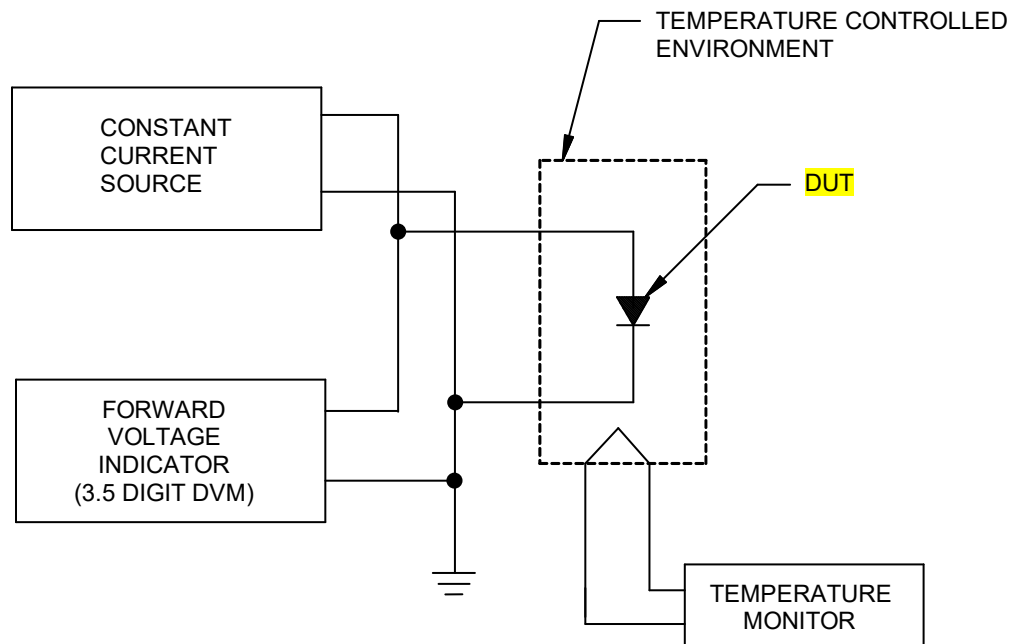


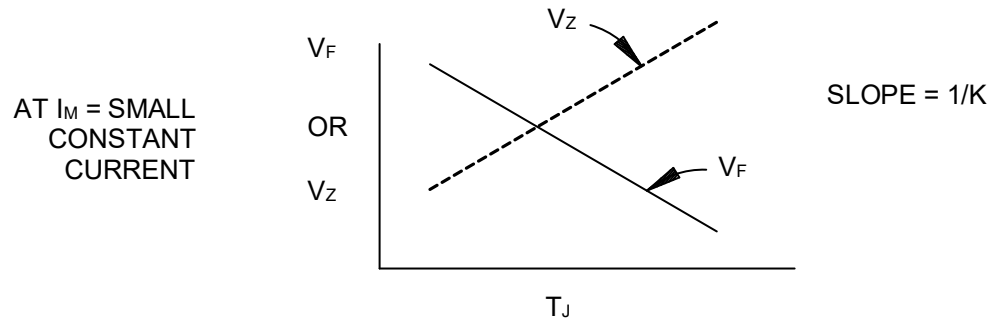
FIGURE XXXX-A1. Example TSP measurement test setup.

A.2.2 Example TSP measurement. An example of the TSP measurement method using the measurement test setup of figure XXXX-A1 is as follows:

- Step 1: Measure V_{F1} at T_{J1} using I_M
- Step 2: Measure V_{F2} at T_{J2} using I_M
- Step 3: Calculate the value of the K using the equation of 3.5.

The resulting calibration curve is shown on figure XXXX-A2.

APPENDIX A



NOTES:

1. I_M shall be large enough to overcome surface leakage effects but small enough not to cause significant self heating.
2. When using the reverse (Zener) direction, the I_M may also require adjustment to avoid a near zero TSP where the avalanche breakdown effects are offset by tunneling or field emission (see 5.4.c).
3. T_J is externally applied: (e.g., via oven, liquid) environment.

FIGURE XXXX-A2. Example calibration curve of V_F (or V_Z) versus T_J .

A.3 K-factor.

A.3.1 K-factor calculation. A calibration factor K (which is the reciprocal of the slope of the curve on figure XXXX-A2) can be calculated using the K-factor equation of 3.5.

A.3.2 Temperature considerations. It is required that the range of temperatures that K -factor is measured over approximately correlates to the range of temperature used for thermal measurements. It is important to characterize the device at least once over a broad temperature range using increments of 25 °C as well as over several values of I_M . This is especially true for room ambient thermal resistance measurements where the recorded value can be deceptively lower when the device is operated close to its maximum T_J . Some devices, especially gold doped devices, can have a saturation current at these elevated temperatures that can overwhelm the I_M current. Characterization is required as it might reveal that a higher value of I_M will be needed.

A.3.3 Sample size considerations. It has been found experimentally that the K -factor variation for all devices within a given device type class is small. The usual procedure is to perform a K -factor calibration on a 10 to 12 piece sample from a device lot and determine the average value of K and standard deviation (σ). If σ is less than or equal to 3 percent of the average value of K , then the average value of K can be used for all devices within the lot. If σ is greater than 3 percent of the average value of K , then all the devices in the lot shall be calibrated and the individual values of K shall be used in determining device acceptance.

A.4 Alternative to using individual values of K . As an alternative to using individual values of K , the manufacture may establish internal limits unique to their product that ensures atypical device removal from the population (lot-to-lot and within-the-lot). The manufacture shall use statistic techniques to establish the limits to the satisfaction of the Government.

APPENDIX B

ESTABLISHMENT OF TESTING CONDITIONS AND ACCEPTANCE LIMITS

B.1 Scope. This appendix covers establishment of testing conditions and acceptance limits for devices covered by this test method. This appendix is a mandatory part of the test method. The information contained herein is intended for compliance.

B.2 General. This procedure describes how to set up the test conditions and determine the acceptance limits for implementing the thermal impedance test for die attachment evaluation using the apparatus and definitions stated in appendix A. It can also be used for thermal characterization purposes of various devices. The following details apply:

- a. This procedure thermally characterizes the device out to a point in heating time required to ensure heat propagation through the internal die attachments. An appropriate heat sink should also be used or the external case or reference point temperature also monitored where heating times can be very short for heat propagation to the external mounting point such as for case mounted power devices or very close proximity solder pads to the internal die element.
- b. When using the procedure for taking thermal resistance measurements, the value for I_H shall be equal to the value specified in the device specification sheets, typically at rated current or higher. The values for t_H , t_{MD} , and heat sink conditions shall be also taken from the device specification sheets. Also the external reference point temperature shall be measured at the conclusion of the heating time and used in the thermal resistance calculation shown in method 4081.

B.3 Initial device testing procedure. From a sample of 20 to 25 devices, select any one device to start the initial device testing procedure as follows:

Step 1: Set up the test apparatus as follows:

$I_H = 1.0 \text{ A}$	(Or some other desired value near the DUTs normal operating current: Typically higher for power diodes, and lower for Zener diodes, when measured in the Zener direction.)
$t_H = 10 \text{ to } 50 \text{ ms}$	Unless otherwise specified, for most devices rated up to 15 W power dissipation. See the notes of figures XXXX-B1 and XXXX-B2 for best heating time selection.
50 to 100 ms	Unless otherwise specified, for most devices rated up to 200 W power dissipation.
$\geq 250 \text{ ms}$	For thermal resistance measurement. The pulse shall be shown to correlate to steady-state conditions before it can be substituted for steady-state condition. See test method 4081 of this multipart test method standard for further details on testing thermal resistance of diodes.
$t_{MD} = 100 \text{ } \mu\text{s max}$	For nonmagnetic or non-inductive lead/package where inductive delay or stored charge do not influence the reading, $t_{MD} = 70 \text{ } \mu\text{s}$ is a good choice. A larger value may be required on power devices with magnetic/inductive package elements that generate non-thermal electrical transients; unless otherwise specified, this would be observed in the t_3 region on figure XXXX-3. If, however, a value of t_{MD} greater than 300 μs is required in order to be able to test outside of the inductive switching region, then correlation shall be made back to 70 μs from whatever value of t_{MD} is required for a stable test.

APPENDIX B

Refer to [appendix D](#) for a technique for measuring devices that cannot be measured at $t_{MD} = 70 \mu s$ maximum because of stored charge or package magnetic effects. The method will involve measuring at $t_{MD} =$ a higher value and then following a simple calculation to correct the reading. The qualifying activity shall be notified if this alternate t_{MD} method is to be used.

$I_M = 10 \text{ mA}$

(Or some nominal value approximately two percent, or less, of I_H .)

IMPORTANT: Diodes like Schottky and gold doped switching rectifiers can have enough saturation current so that the K-factor varies with temperature at lower values of I_M . It is safest to have previously measured at least once for each family type, the K-factor at 25 °C increments from 25 °C up to at least 150 °C (or T_J max) plus vary the current over a decade. Pick an I_M value where K-factor remains fairly consistent over temperature. If K-factor is inconsistent, then use the K-factor that corresponds with the actual T_J achieved in the thermal impedance test (may require some iterations to calculate this value).

Step 2: Insert device into the apparatus test fixture and initiate a test. (For best results, a test fixture that offers some form of heat sinking would be desirable. Heat sinking is not needed if either the power dissipation during the test is well within the [DUT's](#) free-air rating or the maximum heating time is limited to less than that required for the heat to propagate through the [package](#).)

Step 3: Based on the value of ΔV_F , proceed forwards or go back using the following criteria:

- a. If ΔV_F is less than 50 mV, return to step 1 and increase heating power into device by increasing I_H .
- b. If ΔV_F is in the 50 to 300 mV range, or ΔV_{ZL} is equivalent to the same ΔT_J , then proceed to step 4. This range approximately corresponds to a junction temperature change of roughly +25 °C to +150 °C and is sufficient for initial comparison purposes.

EXCEPTION (for when the maximum DUT or test equipment rated I_H has been reached): In this case, the accuracy associated with using a smaller ΔV_F shall be accepted. Test equipment shall have at least 100 μV resolution for ΔV_F . Higher resolution test equipment can easily compensate if ΔV_F is less than 50 mV. If ΔV_F is greater than 150 mV, approximately corresponding to a junction temperature change greater than +75 °C, it would probably be desirable to reduce the heating power by returning to step 1 and reducing I_H .

NOTE: Some ATE automatically guards against this problem.

NOTE: The test equipment shall be capable of resolving ΔV_F to within 5 percent. If not, the higher value of ΔV_F shall be selected until the 5 percent tolerance is met. Two different devices can have the same T_J rise even when P_H is different, due to widely differing V_H . Within a given lot, however, a higher V_H is more likely to result in a higher T_J rise.

Step 4: Test each of the sample devices and record the data detailed in [6](#).

Step 5: Select the devices with the highest and lowest values of $Z_{\theta JX}$ and put the remaining devices aside. These two device will be used to generate data needed to create thermal impedance curves.

Step 6: Using the devices with the highest and lowest values from step 5, collect data for the two devices to plot thermal impedance curves similar to the examples shown on figure [XXXX-B1](#).

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Step 7: Interpretation of the heating curves is the next step. Realizing that the thermal characteristics of identical **dice** should be the same if the t_H is equal to or less than the thermal time constant of the **die**, the two curves should start out the same for the low values of t_H . Non-identical **dice** (thinner or smaller in cross section) will have **higher or lower values of thermal impedance** at the smaller values of t_H , **but they typically exhibit the same slope where thermal impedance decreases by one decade for every two decades the heating time decreases on a log-log plot**. As the value of t_H is increased, thereby exceeding the **die** thermal constant, heat will have propagated through the **dice** into the die attachment **material** region. Since the **thermal impedance** curve devices of step 5 were specifically chosen for their difference, the curves of figures **XXXX-B1** and **XXXX-B2** diverge after t_H reaches a value where the die attachment **material** variance has an **effect** on the device T_J and $Z_{\theta JX}$ as best observed on figure **XXXX-B2** for a log-log plot. Increasing t_H further will eventually result in a flattening of the curve as the heating propagates in the device package and thermal impedance approaches the thermal resistance value of the device. If the device package has little thermal mass and is not well mounted to a good heat sink, the curve will not flatten very much, but will show a definite change in slope.

Step 8: Using the **thermal impedance** curve, select the appropriate value of t_H to correspond to the inflection point in the transition region between heat in the **die** and heat in the package.

If there are several different elements in the heat flow path: **Die**, die attachment **material**, substrate, substrate attach, and package for example in a hybrid, there will be several plateaus and transitions in the **thermal impedance** curve. **An** appropriate selection of t_H will optimize evaluation sensitivity to other attachment areas.

Step 9: Return to the apparatus and set t_H equal to the value determined from step 8.

Step 10: Because the selected value of t_H is much less than that for thermal equilibrium, it is possible to significantly increase the P_H without degrading or destroying the device. The increased power dissipation within the DUT will result in higher ΔV_F or CU values that will make determination of acceptable and unacceptable devices much easier.

Step 11: The pass/fail limit, the cut-off point between acceptable and nonacceptable devices, can be established in a variety of ways:

- Correlation to other die attachment evaluation methods, such as die shear and X-ray. While these two methods have little actual value from a thermal point of view, they do represent standardization methods as described in various standards.
- Maximum allowable junction temperature variations between devices. Since the relationship between ΔT_J and ΔV_F is about $0.5^\circ\text{C}/\text{mV}$ for forward bias testing, or a measurable equivalent for **reverse bias** testing, the T_J spread **among** devices can be easily determined. The T_J predicts reliability. Conversely, the T_J spread necessary to meet the reliability projections **could previously** be translated to a ΔV_F or CU value for pass/fail criteria. **The more definitive $Z_{\theta JX}$ is now the preferred method for pass/fail limits.**

To fully utilize this approach, it will be necessary to calibrate the devices for exact value of the T_J to V_F characteristic. The characteristic's slope, commonly referred to as **K-factor**, is easily measured on a sample basis using a voltmeter, environmental chamber, temperature **monitor**, and a power supply setup as described in **appendix A** herein. A simple set of equations yield the T_J once K and ΔV_F are known:

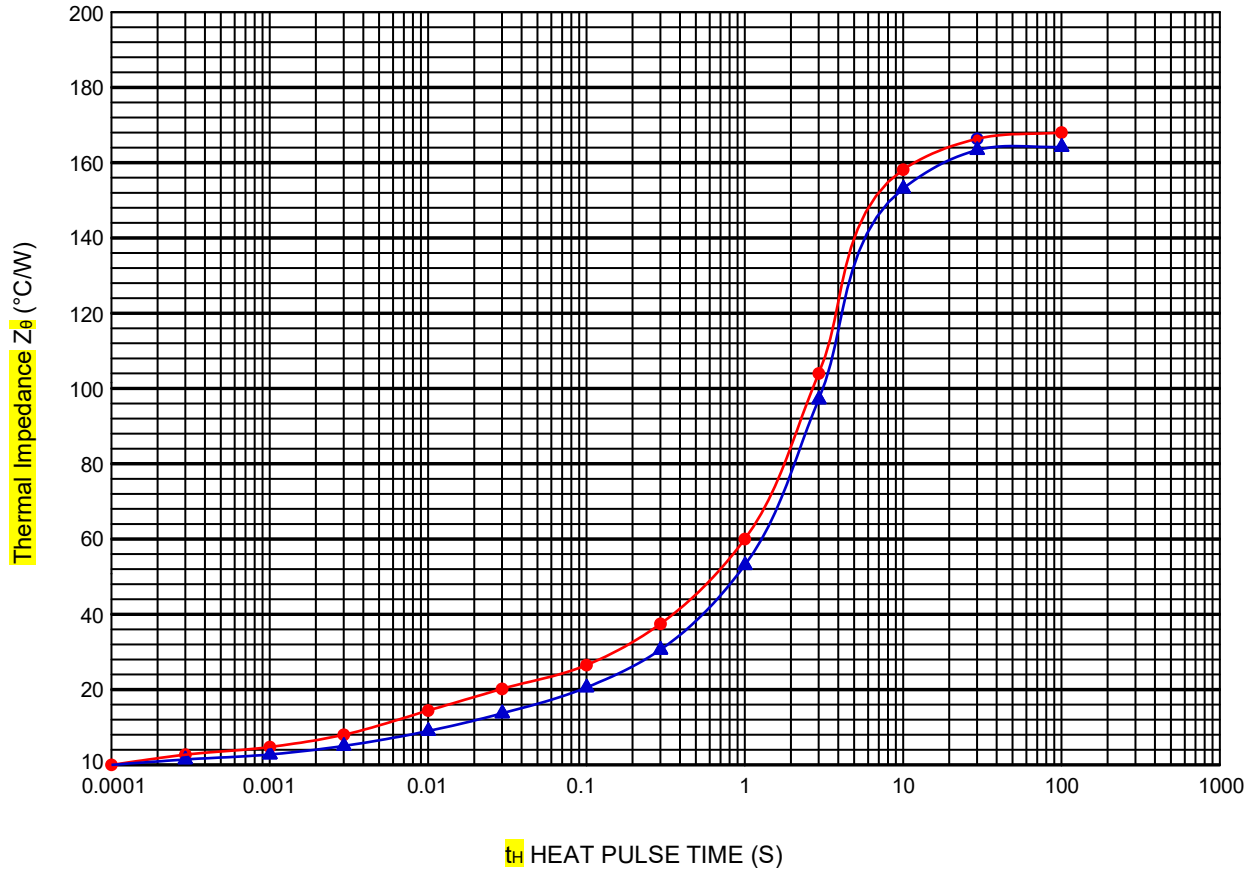
$$\Delta T_J = (K) (\Delta V_F)$$

$$T_J = T_A + \Delta T_J$$

where T_A is the ambient or reference temperature. For thermal **impedance** test conditions **with short heating times relative to heat propagation to the distant external reference point on the device**, the T_A is usually equivalent to lead temperature (T_L) for axial lead devices.

APPENDIX B

THERMAL IMPEDANCE AT $T_{EC} = 25\text{ }^{\circ}\text{C}$
36D DO-35 / UR GLASS MELF DIODE EXAMPLE



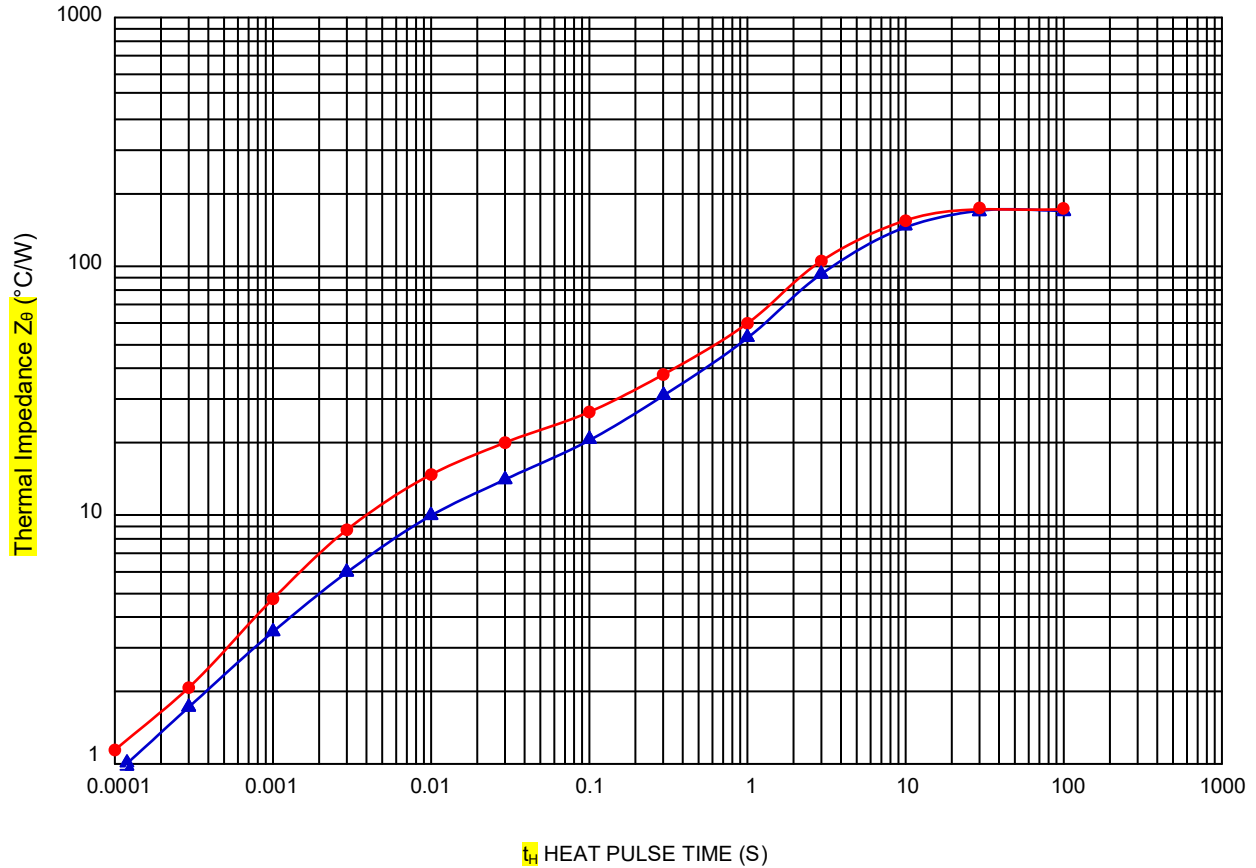
NOTES:

1. Log-linear plot. The time period when the two curves (lower in blue best versus upper in red worst) are farthest apart is the best heating time to use for thermal impedance die bond testing. Note that since the range from 10 ms to 100 ms in this example are nearly parallel, any place in that region is acceptable; however, 10 ms to 30 ms results in faster testing so that would be the logical choice. While log-log plots are requested for use in the device specification sheet, log-linear plots may be substituted with approval of the Qualifying Activity. See figure XXXX-B2 for a log-log example.
2. Both figures XXXX-B1 and XXXX-B2 are plots of the same data.
3. The log-linear incorrectly leads one to believe that maximum void test sensitivity is available anywhere above 10ms.
4. For tight resolution at long test times, the log-linear can provide better resolution. However, for short pulse operation, the log-log is far superior.

FIGURE XXXX-B1. Thermal impedance curves for two extreme devices (log-linear plot).

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THERMAL IMPEDANCE AT $T_{EC} = 25\text{ }^{\circ}\text{C}$
36D DO-35 / UR GLASS MELF DIODE EXAMPLE



NOTES:

1. **Log-log plot.** The log-log plot (preferred) illustrates the ability of short test pulses during thermal impedance to detect poor die bonds. The time period when the two curves (lower in blue best versus upper in red worst) are farthest apart is the best time to use for thermal impedance die bond testing. Note that since the range from 10 ms to 100 ms in this example are nearly parallel, any place in that region is acceptable; however, 10 ms to 30 ms results in faster testing so that would be the logical choice. Each construction design may have a different "sweet zone". For example, many double plug diodes are very near 10 ms for optimum heating times.
2. Both figures XXXX-B1 and XXXX-B2 are plots of the same data.
3. The log-log curve deals with resolution accuracy just like any automatic tester. Here the log-log curve makes it clear that you will lose resolution accuracy above 100ms.

FIGURE XXXX-B2. Thermal impedance curves for two extreme devices (log-log plot).

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Step 11 – Continued.

- c. Statistically, from a 20 to 25 device sample, the distribution of ΔV_F or $Z_{\theta JX}$ values should be a normal one with defective devices out of the normal range. Figure XXXX-B3 shows a ΔV_F or $Z_{\theta JX}$ distribution for a sample lot of diodes.

NOTE: The left-hand side of the histogram envelope is fairly well defined but the other side is greatly skewed to the right. This is because the left-hand side is constrained by the absolute best heat flow that can be obtained with a given die assembly material and process unless a test method error is introduced. The other side has no such constraints because there is no limit as to how poorly a die is mounted.

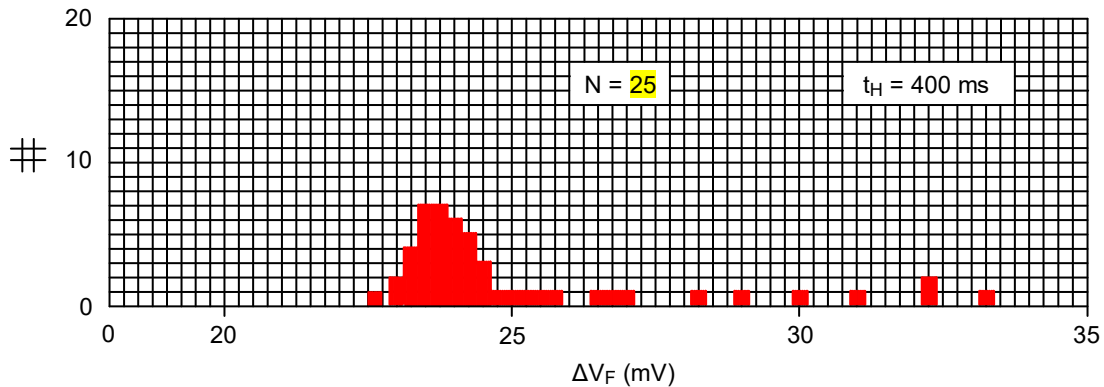


FIGURE XXXX-B3. Typical ΔV_F or $Z_{\theta JX}$ distribution with asymmetrical histogram distribution.

The usual rule of thumb in setting the maximum limit for $Z_{\theta JX}$ is to use the distribution average value and three standard deviations (σ). For example:

$$\left| (Z_{\theta JX}) \right| \Big|_{\substack{\text{high} \\ \text{limit}}} = \overline{Z_{\theta JX}} + X\sigma$$

Where $X = 3$ in most cases and $\overline{Z_{\theta JX}}$ is the average distribution values.

The statistical data required is obtained by testing 25 or more devices under the conditions of step 11.

The maximum limit determined from this approach should be correlated to the diode's specified thermal resistance. This will ensure that the limits do not pass DUTs that would fail the thermal resistance or thermal impedance requirements.

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Step 12: Once the test conditions and pass/fail limit have been determined, it is necessary only to record this information for future testing requirements of the same device in the same package. It is also recommended that a minimum limit is established to ensure a test method error or other anomaly is investigated.

Step 13: After the pass/fail limits are established, there shall be verification that they correlate to good and bad bonded devices or the electrical properties such as surge.

The 13 steps listed above are summarized in table XXXX-1.

TABLE XXXX-1. Summary of test procedure steps.

General description		Steps	Comments
A	Initial setup	1 through 4	Approximate instrument settings to find variations among devices in 10 to 15 piece sample.
B	Thermal impedance curve generation	5 through 6	Using highest and lowest reading devices, generate thermal impedance curves.
C	Thermal impedance curve interpretation	7 through 9	Thermal impedance curve is used to find more appropriate value for t_H corresponding to heat in the die attachment area (for some other desired interface in the heat flow path).
D	Final setup	10	Heating power applied during t_H is increased in order to improve measurement sensitivity to variations among devices.
E	Pass-fail determination	11 through 12	A variety of methods is available such as JEDEC JESD 34 for setting the fail limit; the statistical approach is the fastest and easiest to implement.
F	Verification	13	Mechanical / electrical correlation

B.4 Routine device thermal impedance testing procedure. Once the proper control settings have been determined for a particular device type from a given manufacturing process or vendor, repeated testing of that device type simply requires that the same testing conditions be used as previously determined.

B.5 Heat flow distance versus elapsed time plot. This section is provided to assist in determining the t_H for heating or measurement time required to adequately propagate heat and delineate a particular interface. The graph on figure XXXX-B4 shows effective how far heat travels in the time shown in the X-axis.

The example listed on the graph shows that heat passing through 10 mils of silicon takes 1.05 ms to reach the back side. During the 1.05 ms, the heat has remained inside the die, has not passed through the die bond interface, and is too short a time to measure the die bond interface. Multiply by at least 7 to get a minimum test time.

The example continues to show that it would take 7.92 ms for heat to reach through the silicon die, across the braze layer that is being evaluated and through but not outside of the tab the die is mounted on. Based on this, 7.92 ms would work as a t_H that would maximize sensitivity to bad bonds but not be influenced by anything beyond the first tab. This is where the popular default value of 10 ms came from.

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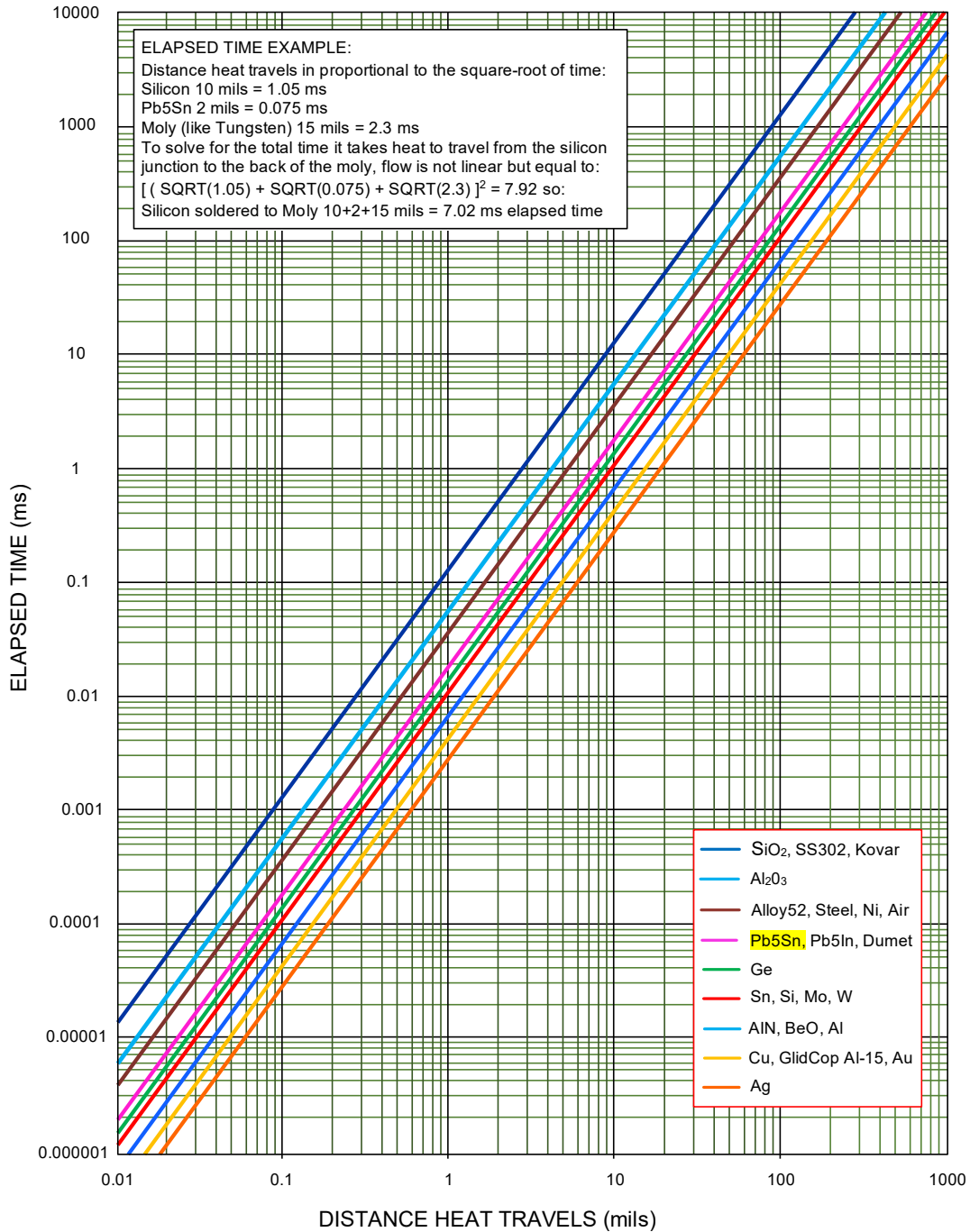


FIGURE XXXX-B4 Heat flow distance versus elapsed time plot.

APPENDIX C

THERMAL IMPEDANCE PRODUCTION SCREENING GUIDELINES

C.1 Scope. This appendix covers thermal impedance production screening guidelines for devices covered by this test method. This appendix is not a mandatory part of the test method. The information contained herein is intended for compliance only when specified by the specification sheet or acquisition documentation.

C.2 Applying the thermal impedance test to production product testing. Every device type is likely to respond differently in readings to thermal impedance tests. The intent here is not to compare dissimilar devices but, rather, to compare devices within a single lot to each other (statistical comparison), to a specification maximum limit (when applicable) and, if at all possible, to a design ideal value. The following rules shall be applied:

- a. Any device failing the specification maximum limit (if one exists) is an automatic reject.
- b. Any device falling outside of a normal distribution of thermal impedance readings in a histogram is subject to reject. In order to successfully use thermal impedance to detect and remove any devices that have defects that can affect reliability or performance, the histogram for individual lot testing shall be different from that used for end-point testing. For end-point testing, this distribution should be documented over the course of five inspection or screening lots. If each lot has a similar distribution, then the average distribution and pass-fail limits of the combination of all five lots may be used to establish permanent screening limits. If the K-factor does not vary more than 10 percent from lot-to-lot, then it is permissible to establish a constant K-factor for this particular part number or die family. Otherwise, the K-factor may need to be re-established for every lot. In general, this process should establish a maximum limit for evaluating that particular device type, and while it may not be used to successfully screen manufacturing defects, no individual lot evaluations should allow limits higher than the end-point limit.
- c. Since a number of factors impact the thermal impedance results, in order to use thermal impedance testing to remove defects, all other influences of thermal impedance shall be held as uniform as possible. This can only be done by evaluating each production or manufacturing lot before these lots are combined into inspection or screening lots. In this case, it is necessary to treat each production or manufacturing lot on a stand alone basis by calculating a K-factor and screening limits from a sample for that specific lot.
- d. Upper and lower pass-fail limits cannot be determined by using ± 3 -sigma. This is because in most cases (except where you have achieved near perfection), the distribution is an asymmetrical histogram bell curve where the right (high-side) of the curve extends farther away from center normal than the left (low-side). This is because making devices less than perfect (extends right) is easy but making devices better than perfect (extends left) is far less likely. The upper and lower limits can be set one of two ways:
 - 1) Split Histogram curve in half at the center peak value and calculate separate 3-sigma limits, one for the upper side and one for the lower side.
 - 2) Engineering should visually review the Histogram curve and select appropriate limits based upon what looks normal and what does not.

The value of a lower pass-fail limit is to catch changes in the device that might otherwise go undetected. For example: Braze preform is suddenly too thin, die size was just changed, or package design was changed by package vendor. Since the original design-value for thermal impedance remains the one constant through all testing, this is an excellent tool to confirm that thermal impedance is giving meaningful readings and that the design is being executed correctly by production.

- e. The design-value should fall somewhere in the lower region of the histogram curve or slightly below the curve. Major deviations indicate that one or the other is in error, or that the measurement conditions cannot give an absolute accurate value (though relative values for statistical screening may continue to be usable for screening).

APPENDIX D

BACKWARD t_{MD} PROJECTOR CALCULATION METHOD

D.1 Scope. This appendix covers the backward t_{MD} projector calculation method that can assist in performing thermal impedance measurements described by this test method. This appendix is not a mandatory part of the test method. The information contained herein is intended for compliance only when specified by the specification sheet or acquisition documentation.

D.2 General. While the thermal impedance test method tells us to make allowances for devices that have either magnetic or stored charge issues that hinder using delay times under 100 μs , this "backward t_{MD} projector calculation method" details a method to make the allowance. Generally this correction is only needed for thermal resistance because it is thermal resistance that usually has an absolute specification maximum. Short-pulse-width thermal impedance used only for SPC purposes and for screening out poor die bond problems is just as effective regardless of the value of t_{MD} used. However, if an absolute value of thermal impedance accuracy is required, then a minimum delay time is still required for correlation reference such as for thermal impedance curves often included in performance specifications.

D.3 Example analysis of a thermal impedance tester. Figure XXXX-D1 illustrates what a thermal impedance tester displays when a test is performed. The first reading (V_F) is always the easiest to take. The second reading (V_F) can be misled by ferro-magnetic resonant delay, stored charge, etc. and must be delayed until the device has stabilized. When the device stabilized within the 100 μs t_{MD} time period, no further compensation is required.

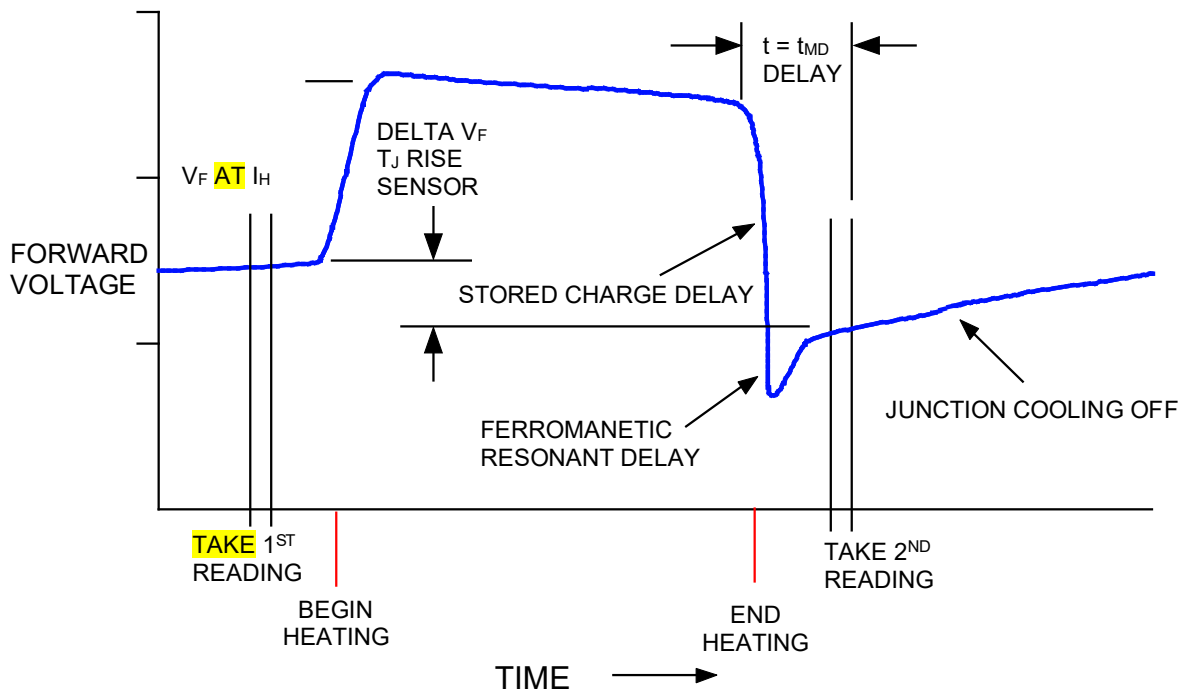


FIGURE XXXX-D1. Analysis of Z_θ test.

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D.4 The backward t_{MD} projector calculation. However, when a much longer t_{MD} is required to avoid the interference caused by magnetics and stored charge, the backward t_{MD} projector calculation method detailed below can be used.

D.4.1 Definitions. The following symbols shall apply:

- t_{MD} = Specification delay time for Z_{θ} (such as 70 μ s when it otherwise cannot be measured directly).
- t_{MD1} = Delay time that can be measured (such as 1000 μ s) for $Z_{\theta1}$.
- t_{MD2} = Forced 2nd delay time = (approximately two to three times t_{MD1}) for $Z_{\theta2}$.

(Any units for t_{MD} and Z_{θ} can be used, but be consistent throughout).

D.4.2 Constants. The following constants shall apply:

- $c = (Z_{\theta1} - Z_{\theta2}) / [\sqrt{t_{MD1}} - \sqrt{t_{MD2}}]$
- $k = Z_{\theta1} - c * \sqrt{t_{MD1}}$

D.4.3 Calculation. Using the constants from D.4.2, solve for $Z_{\theta(t_{MD})}$ where:

$$Z_{\theta(t_{MD})} = k + c * \sqrt{t_{MD}}$$

NOTE: For ideal Z_{θ} value, set $t_{MD} = 0$ in the equation, which yields the value of just k.

D.4.4 Calculating a one-time correction factor. While it is possible to have a thermal impedance tester programmed to do this automatically, it is also possible to calculate a one-time correction factor that can be applied to the test limit and allow testing using t_{MD1} and θ_{1} to adjusted limits.

Calculate the correction factor for a given design and use it instead:

$$\text{Factor} = Z_{\theta(t_{MD})} / Z_{\theta1},$$

$$\text{Factor} = [k + c * \sqrt{t_{MD}}] / [k + c * \sqrt{t_{MD1}}]$$

So that the correct $Z_{\theta(t_{MD})}$ = measured $Z_{\theta1}$ at t_{MD1} * Factor.

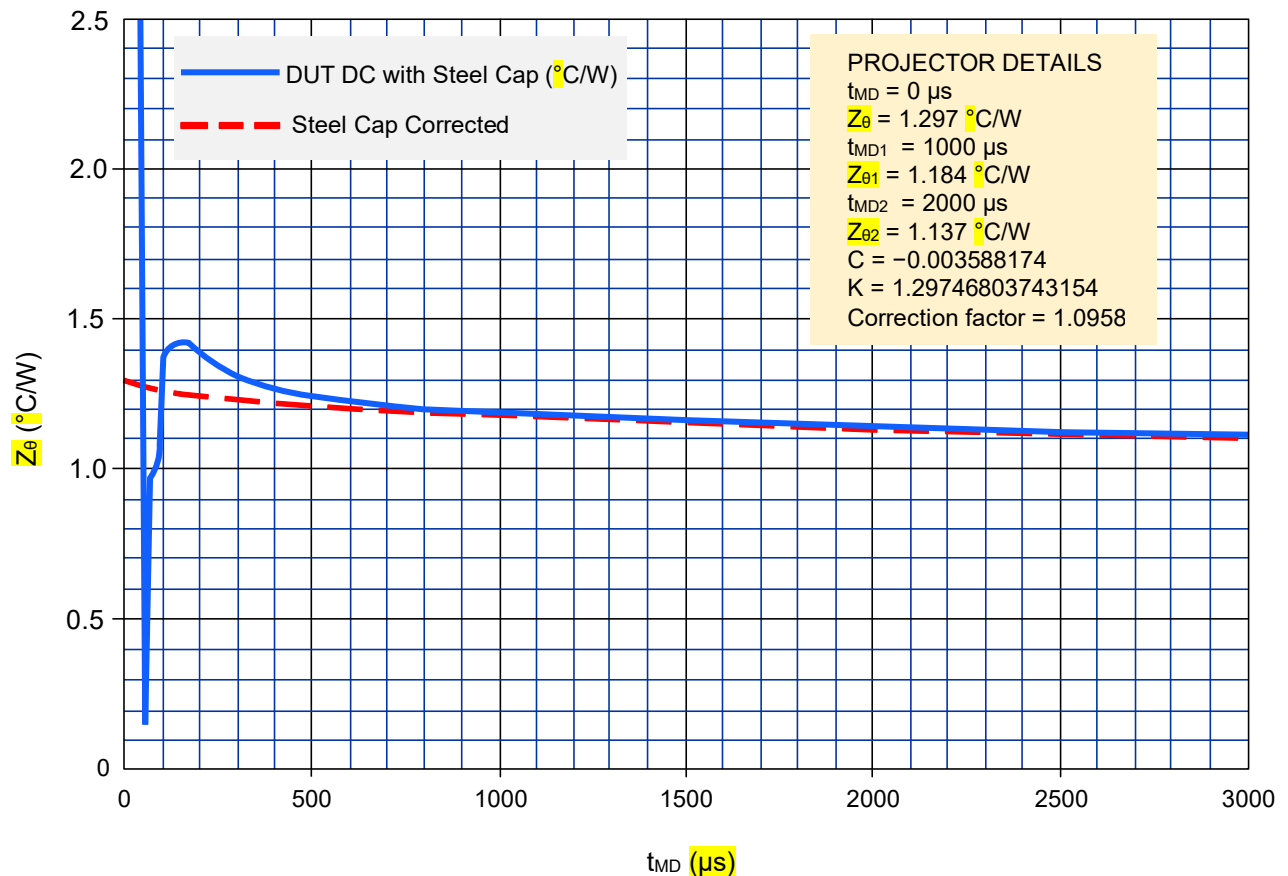
Likewise, the new screening max $Z_{\theta1}$ limit using t_{MD1} becomes $Z_{\theta(t_{MD})} / \text{Factor}$.

This "Factor" value can be used to apply to any one design (same die, same package) using the same test setup conditions (I_H , I_M , etc.) without the need to do any future re-calculations.

D.5 Z_{θ} versus t_{MD} plot examples. Figures XXXX-D2 through XXXX-D4 shows examples of a device that benefits immensely from the use of the backward t_{MD} projector (plus the same device with the "trouble maker" steel cap removed) and a device that doesn't require the "projector" at all. Note that using the "projector" for a device that does not require the "projector" does not cause any error. The point is also made that the backward t_{MD} projector can work for any device including bipolar transistors, field-effect transistors, and diodes:

APPENDIX D

D.5.1 Plot for an example device that requires correction. Figure XXXX-D2 is a plot of a device that is very much in need of correction. This particular example is for a rectifier but this "projector" method works equally well for diodes and bipolar transistors. The dashed line is the output of the "projector" where the value of t_{MD} is varied from zero out to t_{MD2} . The magnetic (due to steel cap) and stored charge perturbations end between 700 μs and 800 μs .



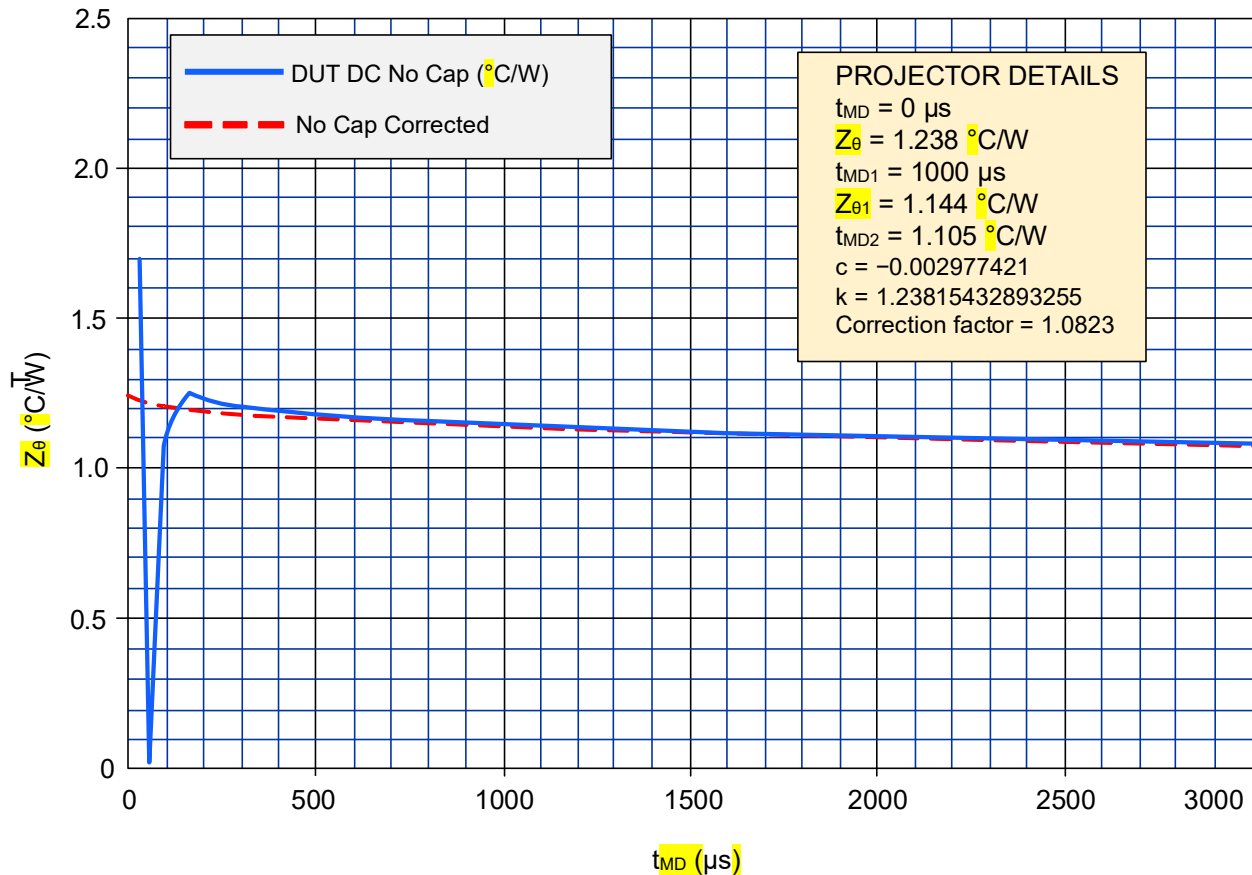
NOTE: Observe closely on the curve above that if the "projector" had not been used, e.g. $t_{MD} = 50 \mu s$ had been used instead, a Z_{θ} value less than 25 percent of the actual Z_{θ} value would have been measured. The next measurement would have likely been erratic and your SPC charts would be plotting setup errors and not product integrity.

FIGURE XXXX-D2. Z_{θ} versus t_{MD} plot for an example device that requires correction.

APPENDIX D

D.5.2 Plot for example device in D.5.1 with no steel cap. Figure XXXX-D3 is a plot of the identical device depicted in figure XXXX-D2 except that the steel cap, the cause of much of the magnetic perturbations, has been removed. The perturbations are quite natural since the current carrying terminals pass through the cap creating an artificial magnetic core in which to store energy.

Figure XXXX-D3 does show that other problems can cause unnatural oscillations (especially at these high currents) where error begins to creep in below 400 μs .

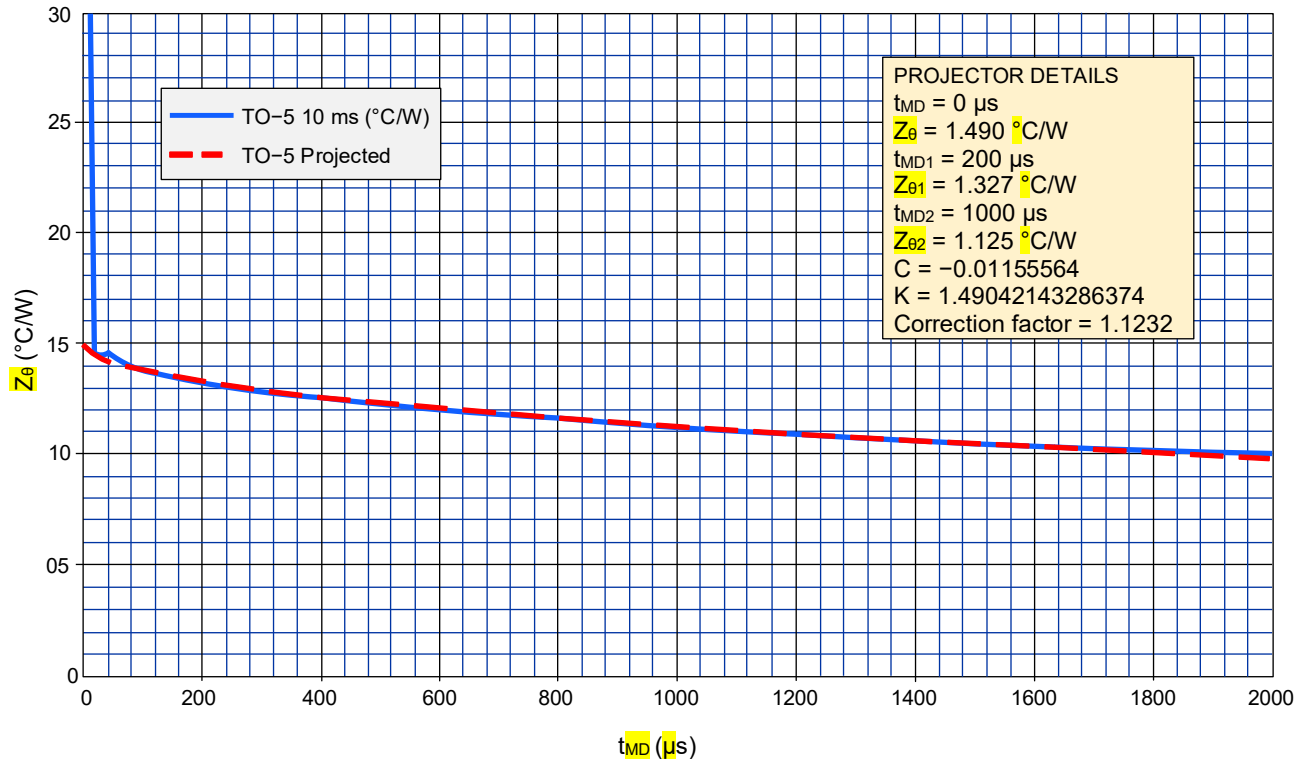


NOTE: With the magnetic disturbances removed, there only remains the effects of stored charge and/or recovery delay in the thermal resistance tester as, in this case, the power source shall switch from $I_H = 60 \text{ A}$ to $I_M = 50 \text{ mA}$.

FIGURE XXXX-D3. Z_{θ} versus t_{MD} plot for an example device with no steel cap.

APPENDIX D

D.5.3 Plot for an example device that requires almost no correction. Figure XXXX-D4 is a plot of a device that requires almost no correction at all. The plot shows measured thermal impedance essentially tracking with the "projector" plot. One of the reasons this device performs so well is that the test current is very low (1 A), the die is very fast, and the case has very little magnetic influence.



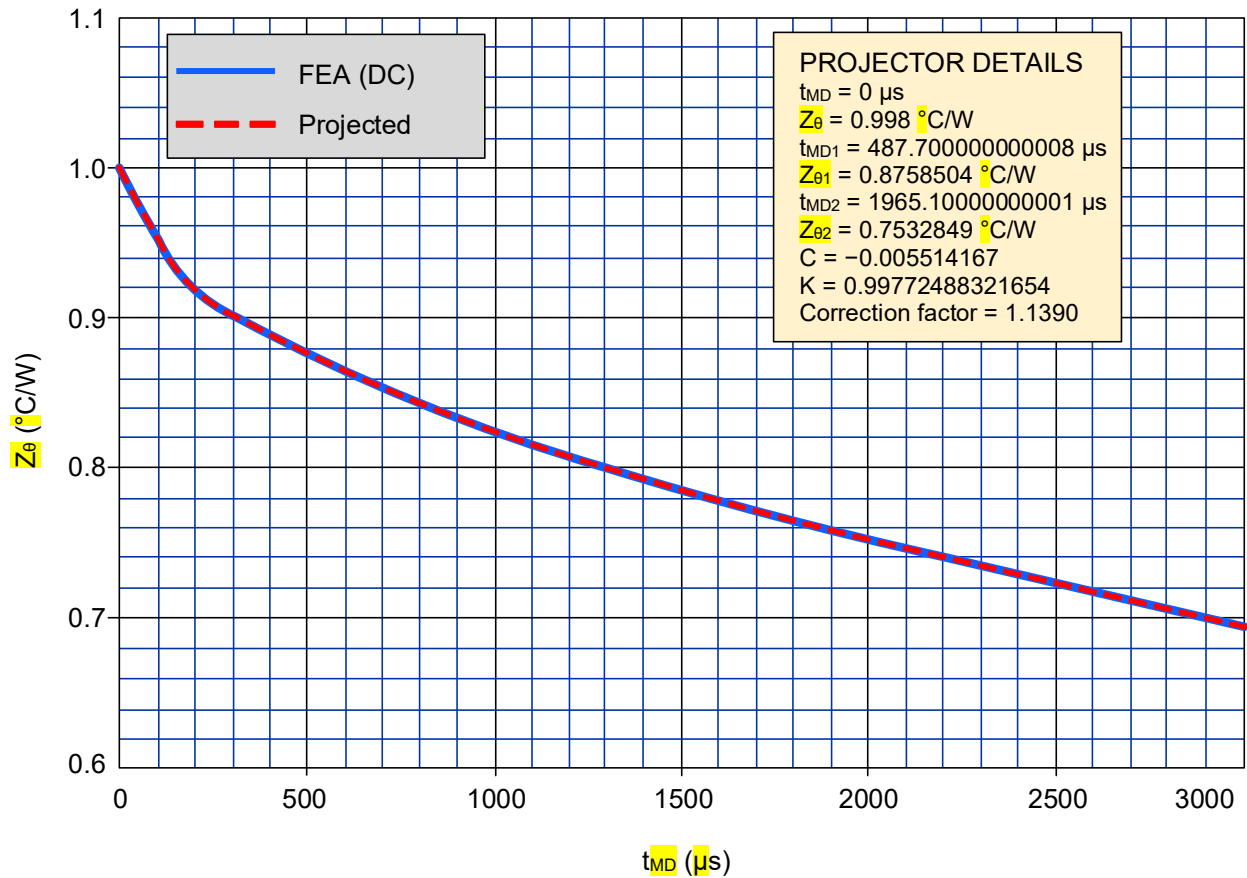
NOTES:

1. Knowing exactly how to select t_{MD1} and t_{MD2} is important.
2. t_{MD1} shall be selected just past the point where various perturbations occur and this can be accomplished by making "cooling plots" like the plots used for this figure.
3. For t_{MD2} , usually pick a value between 2 to 3 times t_{MD1} .

FIGURE XXXX-D4. Z_{θ} versus t_{MD} plot for an example device that requires almost no correction.

APPENDIX D

D.6 FEA cooling plot. Figure XXXX-D5 shows a FEA cooling plot. This FEA plot has been prepared in which the thermal resistance at $t_{MD} = 0$ is known by definition. This cooling plot provides evidence that the "projector" actually shows what is happening at $t_{MD} = 0$.



NOTES:

1. The selection of "odd" values of t_{MD1} and t_{MD2} is because these were provided by the computer. It can be seen that the FEA output (solid line) and the "projector" overlay each other perfectly.
2. Be aware that when measuring thermal resistance, the "projector" works very easily with very little guess work. When used for pulsed thermal impedance, some error can creep in if t_{MD1} and/or t_{MD2} is selected carelessly. Again, be prepared with the appropriate cooling plot curve for a given semiconductor family.
3. It has always been believed that measuring Z_{θ} at $t_{MD}=0$ was impossible. With this method, it can be done.

FIGURE XXXX-D5. Z_{θ} versus t_{MD} FEA cooling plot.