

ENGINEERING PRACTICE STUDY

PROJECT NUMBER: 5961-2024-020

TITLE:

MIL-STD-750-2, TEST METHOD 2073

"VISUAL INSPECTION FOR UNENCAPSULATED SEMICONDUCTOR DIODE DIE"

PROPOSAL TO DEVELOP A DRAFT TO ADDRESS
FORMAT CONSISTENCY, UPDATE FIGURES, AND TO
ADD REQUIREMENTS CONCERNING FOREIGN MATERIAL

9 MAY 2024

FINAL RERORT

STUDY CONDUCTED BY

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ATTACHMENTS 2

I. **OBJECTIVES:** The objective of this Engineering Practice (EP) Study was to obtain input from users (military services, device manufacturers, laboratories, and user community) concerning a proposed revision to test method 2073 of MIL-STD-750-2.

II. **BACKGROUND:** The preparing activity for MIL-STD-750 (DLA-VAC) received a request from a user to add requirements concerning foreign material to the test method. DLA-VAC prepared an initial draft of a proposed 2073.3 that added requirement for foreign material based on similar type of requirements from other visual inspection test methods in MIL-STD-750-2 (methods 2069, 2070, 2072, and 2078). The proposed revision of the test method also includes a new figure, modifies current figures, corrects editorial issues, and reorganizes the test method format.

III. **RESULTS:** All comments received from the initial draft during the review period regarding the proposed changes in content and format were accepted and have been incorporated into the drafts for the final report.

Both a clean reader draft (see attachment 1) and mark-up source draft (see attachment 2, which contains both additions and deletions) have been included for comparison, reviewing, and documenting the results of this study. A key that identifies the changes that were made in the initial draft versus the changes that were made in the final report draft has been included at the top of the first page of each attachment.

IV. **CONCLUSIONS:** The highlighted changes to the test method (see attachment 1) should be proposed for incorporation into the next standardization document change action to MIL-STD-750-2.

V. **RECOMMENDATIONS:** Prepare an initial draft of MIL-STD-750-2 using the results of this study for the draft of test method 2073.3.

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KEY to changes:

Text that was added to the Initial Draft are highlighted in yellow.

Text that was added for the Final Report as a result of comments to the Initial Draft are highlighted in green.

Text that was proposed to be deleted in the Initial Draft and Final Report are not shown in this attachment, but can be viewed in attachment 2 of this final report.

ATTACHMENT 1 to FINAL REPORT for Project 5961-2024-020

MIL-STD-750-4

METHOD 2073.3

VISUAL INSPECTION FOR UNENCAPSULATED SEMICONDUCTOR DIODE DIE

1. Purpose. The purpose of this test method is to verify the quality and workmanship of unencapsulated semiconductor diode die (hereafter referred to as "die") for compliance with the requirements contained herein and the individual performance specification sheet or acquisition document.

1.1 Application. All examinations and inspections shall be performed to identify and reject those die with defects that could lead to device failures. This test method will normally be used prior to die installation on a 100 percent inspection basis. This test method may also be employed on a sampling basis prior to encapsulation to determine the effectiveness of the manufacturer's quality control and handling procedures.

1.2 Exclusions and limitations. Excludes die designs with both anode and cathode on the same surface and stacked dice assemblies.

2. Apparatus. The apparatus for this test method shall consist of the following:

- a. Optical equipment (monocular, binocular, or stereo microscope) capable of the magnifications specified herein.
- b. Light sources to illuminate the devices being inspected.
- c. Adequate fixturing for handling the die during examination without causing contamination or damage.
- d. Adequate covered storage and transportation containers to protect die from mechanical damage and environmental contamination.
- e. Visual standards (e.g., gauges, drawings, photographs) necessary to perform an effective examination and enable the inspector to make objective decisions on the acceptability of the die being examined.

3. Definitions. The following definitions shall apply:

- a. Active area: Any area where electrical contact may be made on the "P" or "N" regions of the die.
- b. Active region: Region covered by passivation that supports electrical activity and junction geometries.
- c. Foreign material:
 1. Conductive foreign material is defined as any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspections.
 2. Nonconductive foreign material is defined as any substance that appears translucent under those conditions of lighting and magnification used in routine visual inspections.
- d. Junction: The boundary between "P" and "N" type semiconductor material.

NOTE: In the case of a Schottky diode, there is no actual junction other than the guard ring. Schottky diodes have a barrier that exists at the metal-silicon contact, however, for the purposes of this test method the barrier will be treated as a junction.

- e. Passivation: Silicon oxide, silicon nitride, or other insulating material that is grown or deposited directly over the "P-N" junction or the Schottky guard ring "P-N" junction.

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f. **Particles.** Semiconductor material chips shall be treated as conductive particles. The following classifications apply:

1. **Embedded particles:** Particles which are attached by more than one half of their largest dimension.
2. **Non-embedded particles:** Particles which are attached by less than one half of their largest dimension.

g. **Probe marks.** Probe marks are indentations, mars or scratches on the bond pads made by probes during electrical measurements.

4. **General requirements.**

4.1 **Procedure.** The die shall be examined in a suitable sequence of operations and at the specified magnifications to determine compliance with the requirements of the individual specification sheet or acquisition document and the criteria of this test methods figures and associated textual criteria. The sequence of examinations required may be varied at the discretion of the manufacturer.

4.1.1 **Die inspections.** These inspections shall apply to alloy, diffused mesa, epitaxial mesa, planar, and epitaxial planar construction techniques. Unless otherwise specified, inspections shall be made on a random selection of the applicable side or sides (see 4.2) of each die being inspected. If a lot fails, 100-percent inspection of the total lot shall be performed.

4.1.2 **Magnification.** Unless otherwise specified by the individual specification sheet or acquisition document, the die magnifications requirements specified in table 2073-I shall be used for visual inspection. The following details apply:

- a. **Examinations** shall be performed perpendicular to the die surface with normal incident illumination.
- b. The inspection shall be performed under suitable illumination.
- c. Binocular and stereo microscopes shall have each eyepiece individually focused for the inspector

TABLE 2073-I. **Die magnification requirements.**

Die size ^{1/}	High power magnification	Low power magnification
.030 inch (0.76 mm) or less	100X to 200X	30X to 50X
.031 to .060 inch (0.78 to 1.52 mm)	75X to 150X	30X to 50X
.061 inch to .150 inch (1.55 to 3.81 mm)	35X to 120X	20X to 30X
Greater than .150 inch (3.81 mm)	25X to 75X	20X to 30X

^{1/} Length of shortest dimension.

4.2 Examination options. After dice sample selection for visual inspection, the manufacturer may elect either of two options as follows.

- a. Option A: Front side visual inspection with sample size specified by individual specification sheet or acquisition document. If no sample size is specified, 100-percent visual is assumed.
- b. Option B: Both front side and back side inspection. Backside visual inspection shall be conducted with sample size specified by individual specification sheet or acquisition document. If no sample size is specified, use sample size 22 for quality level H or sample size 45 for quality level K. For both quality levels, reject on 1 or more failures.

NOTE: If no examination option is specified by the individual performance specification sheet or acquisition document, then option A shall be the default examination option.

4.3 Removal of foreign material on die surface. Removal of foreign material or particles on the die surface may be attempted by using a nominal gas blow of approximately 20 psi (138 kPa).

5. Acceptability (accept and reject criteria).

5.1 General. The die shall be examined in accordance with the applicable figure or figures, as needed, for the die design, construction, topography involved, and associated textual criteria.

5.1.1 Selecting representative figure(s). Determine type of die being examined by comparing it to figures 2073-1 through 2073-8 and select a representative figure. An exact match of die to figure is not necessary. If a single figure does not represent the die being inspected, then features from more than one figures can be aggregated to form an inspection baseline. If a representative figure or figures cannot be determined, then contact the die vendor source for assistance in matching an appropriate figure or figures.

NOTE: Hexagonal shaped die shall be inspected to the same criteria as the square die shown herein.

5.1.2 Die figures. The following figures depict the design, construction, and topography of square die:

a. The figures for front side visual inspection (options A and B) are as follows:

- a. Button contact diodes. figure 2073-1.
- b. High voltage planar diode I. figure 2073-2.
- c. High voltage planar diodes II. figure 2073-3.
- d. Inside moat mesa diodes. figure 2073-4.
- e. Low voltage contact overlay diodes. figure 2073-5.
- f. Low voltage planar diode. figure 2073-6.
- g. Outside moat mesa diodes. figure 2073-7.
- h. Schottky barrier diodes. figure 2073-8.

b. The figure for backside visual inspection (applicable to option B only) is figure 2073-9.

5.2 Foreign material. Die inspections for foreign material shall be performed at low magnification.

5.2.1 Defects. Die that exhibits any of the following conditions shall not be acceptable:

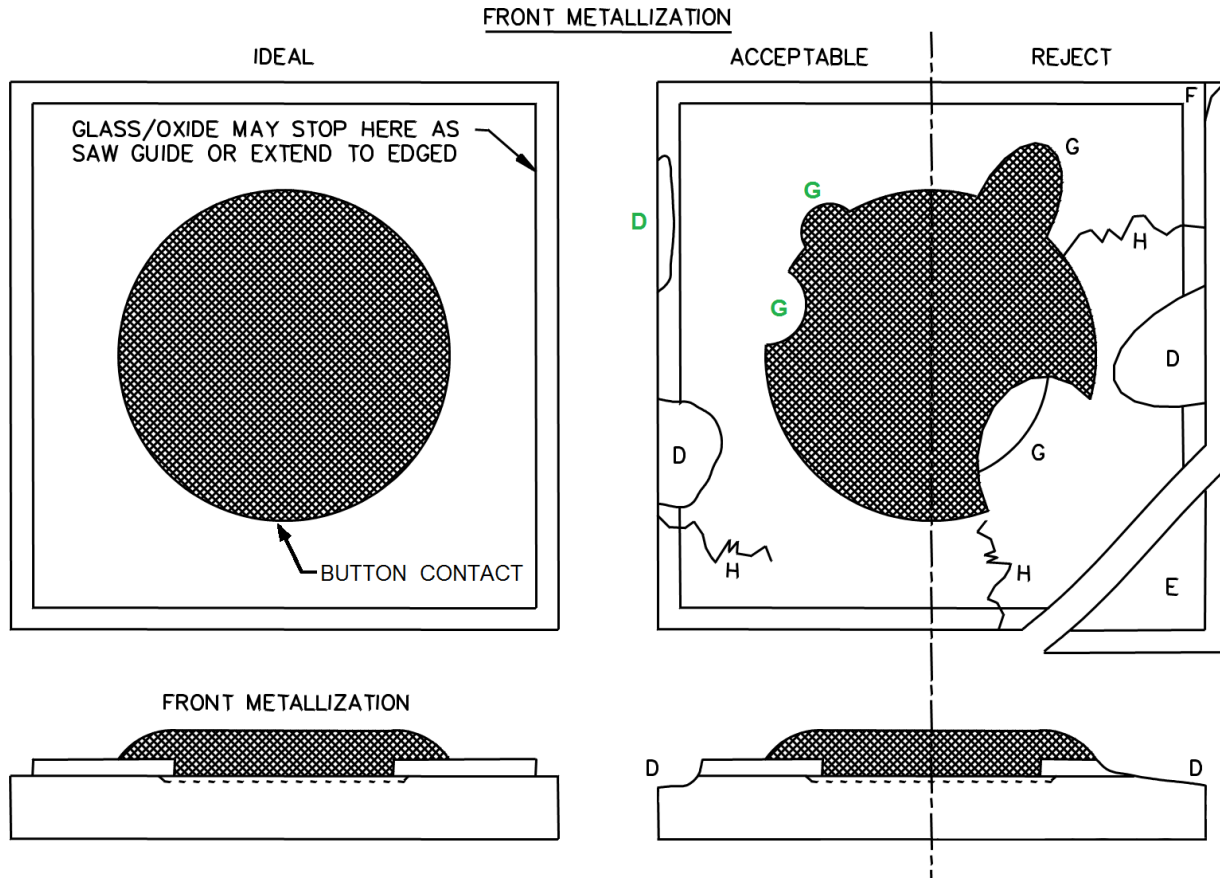
- a. Embedded particles on the surface of the die that bridge semiconductor junctions, or any combination of metallization or junction.
- b. Loosely attached conductive particles on the surface of the die that are large enough to bridge the narrowest unglassivated active circuit element spacing.
- c. Non-embedded particles on the surface of the die that are large enough to bridge the narrowest unglassivated active metal spacing.
- d. Ink, paint or similar blemish on the surface of the die that covers more than 25 percent of the bonding area or pad area or that bridges any combination of unglassivated metallization or bare semiconductor material (silicon areas) (see figure 2073-12 new figure based off figure 2072-43).

5.2.2 Foreign material or particle removal. If present, attached conductive foreign material or particles may be removed in accordance with 4.3.

5.3 Probe marks. Probe marks shall not penetrate the contact metal and expose any non-passivated active region.

6. Summary. The following conditions should be specified in the applicable document (performance specification sheet or drawing):

- a. Examination option letter.
- b. Any additional requirements for design, construction and topography.



Reject criteria:

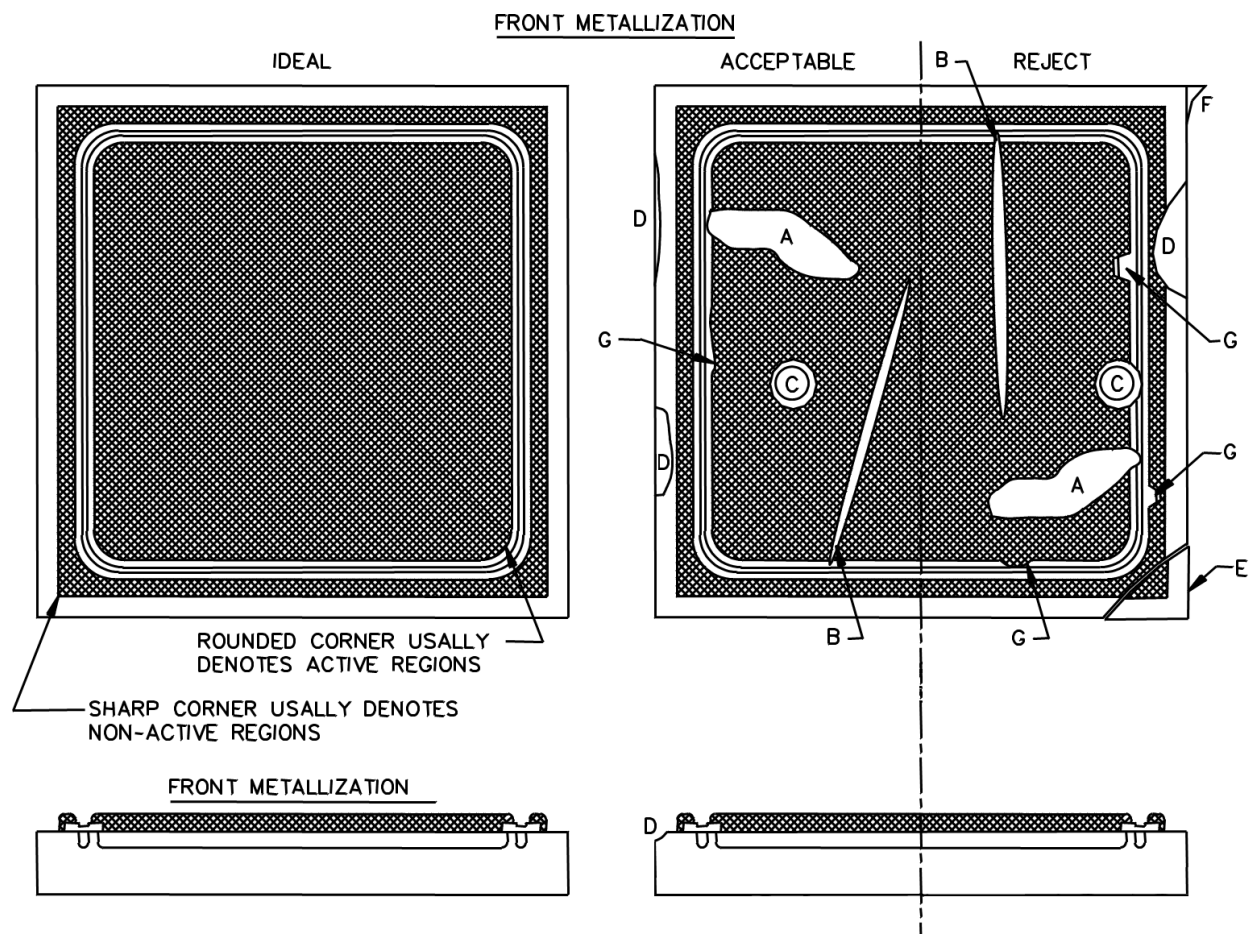
1. Edge chipping (D) shall not extend more than 50 percent to metallization.
2. Missing pieces (E) extending beyond 50 percent to junction boundary shall not be acceptable.
3. Additional attached pieces (F) defined by an incomplete cut or scribe line shall not be acceptable.
4. Additional front metallization extending 50 percent or more to the next geometric boundary (G) or pulled back to reveal contact area or any non-passivated active region shall not be acceptable.
5. Cracks (H) shall not extend near the metallized button closer than 50 percent and shall not be directed toward button such that additional propagation would intersect the button.

NOTES:

1. The cross-sectional views are for reference only.
2. For button contact diodes, the metal button overlays the junction and active area.

FIGURE 2073-1. Button contact diodes.

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**Reject criteria:**

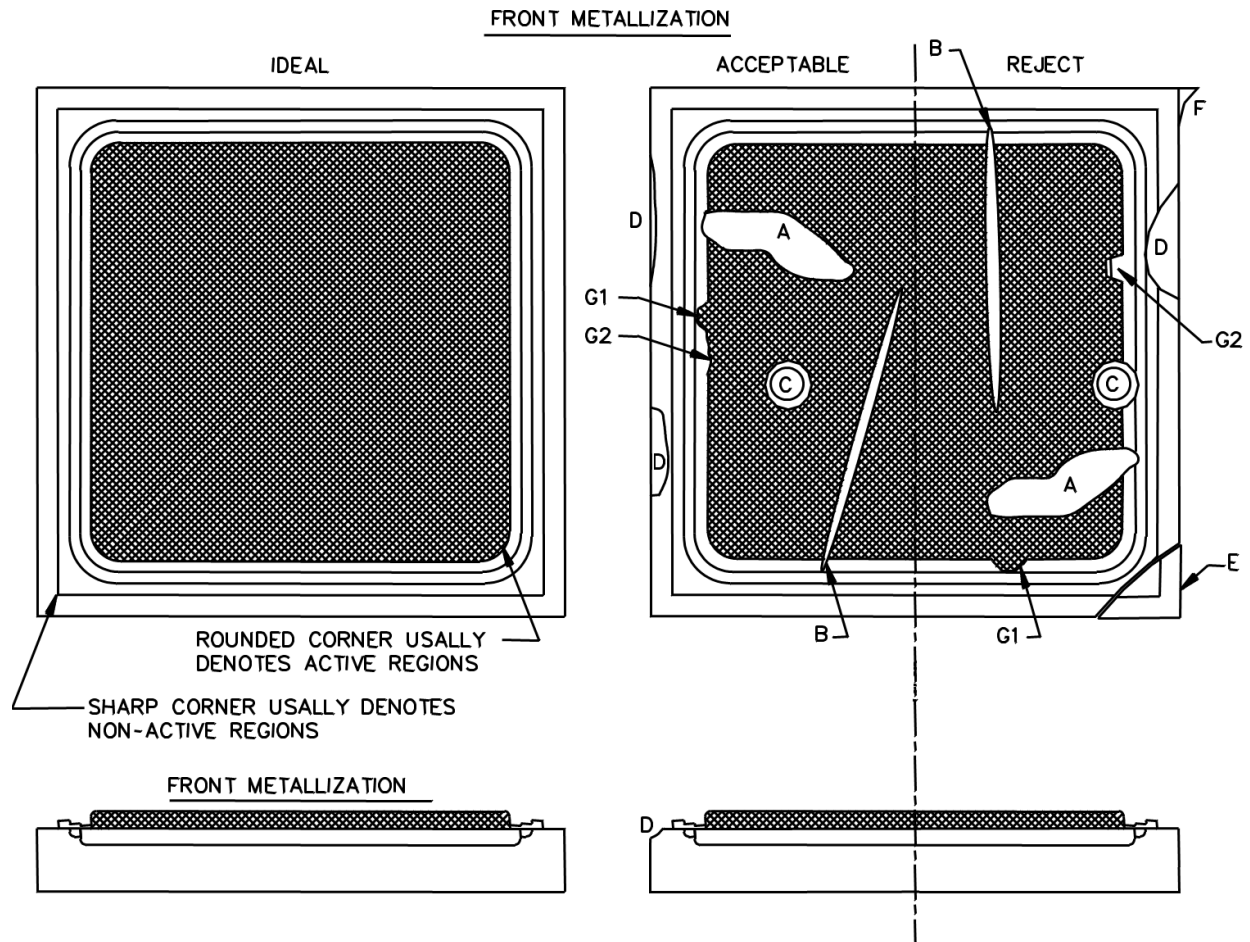
1. Smears (A), scratches (B) or probe marks (C) **shall** not extrude metal such that it covers any guard rings.
2. Edge chipping or cracks (D) **shall** not extend into outside metallization ring (or if absent, 50 percent of distance between chip edge and nearest active ring.)
3. Missing pieces (E) extending into outside metal ring or additional attached pieces (F) defined by an incomplete cut or scribe line **all not be acceptable**.
4. Additional front metallization extending over nearest ring boundary (G) or pulled back to reveal contact area or any non-passivated region **shall not be acceptable**.
5. Cracks (not illustrated) **shall** not extend under the metallized areas and **shall** not be present inside any of the active regions.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-2. High voltage planar diode I (guard ring(s) and outside metal oxide edge cover or field plate).

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**Reject criteria:**

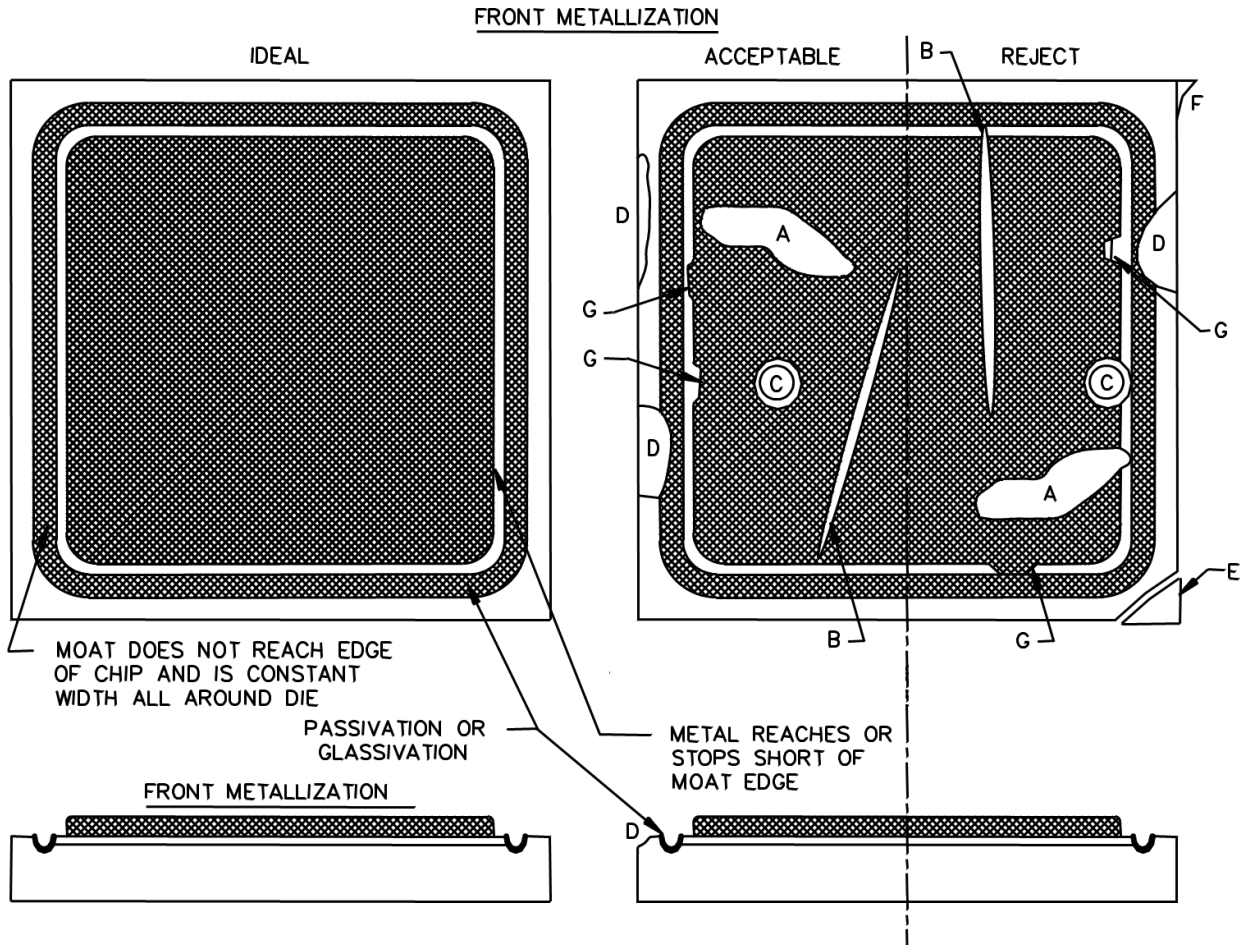
1. Smears (A), scratches (B) or probe marks (C) **shall** not extrude metal such that it extends over the next geometric boundary (covers the P-guard ring area).
2. Edge chipping or cracks (D) **shall** not extend into outside metallization ring (or if absent, 50 percent of distance between **die** edge and active ring boundary.)
3. Missing pieces (E) extending 50 percent of distance between chip edge and nearest ring boundary or additional attached pieces (F) defined by an incomplete cut or scribe line **shall not be acceptable**.
4. Additional front islands of metallization crossing any diffusion line (G1) or pulled back to reveal contact area or any non-passivated region (G2) **shall not be acceptable**. Note that G2 does not apply to **die** designed without requiring metal-passivation overlay. In this latter exception, much or all of the oxide window will be exposed as a legal part of the design.
5. Cracks (not illustrated) **shall** not extend under the metallized areas and **shall** not be present inside any of the active regions.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-3. High voltage planar diodes II (integrated P-minus guard ring).

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**Reject criteria:**

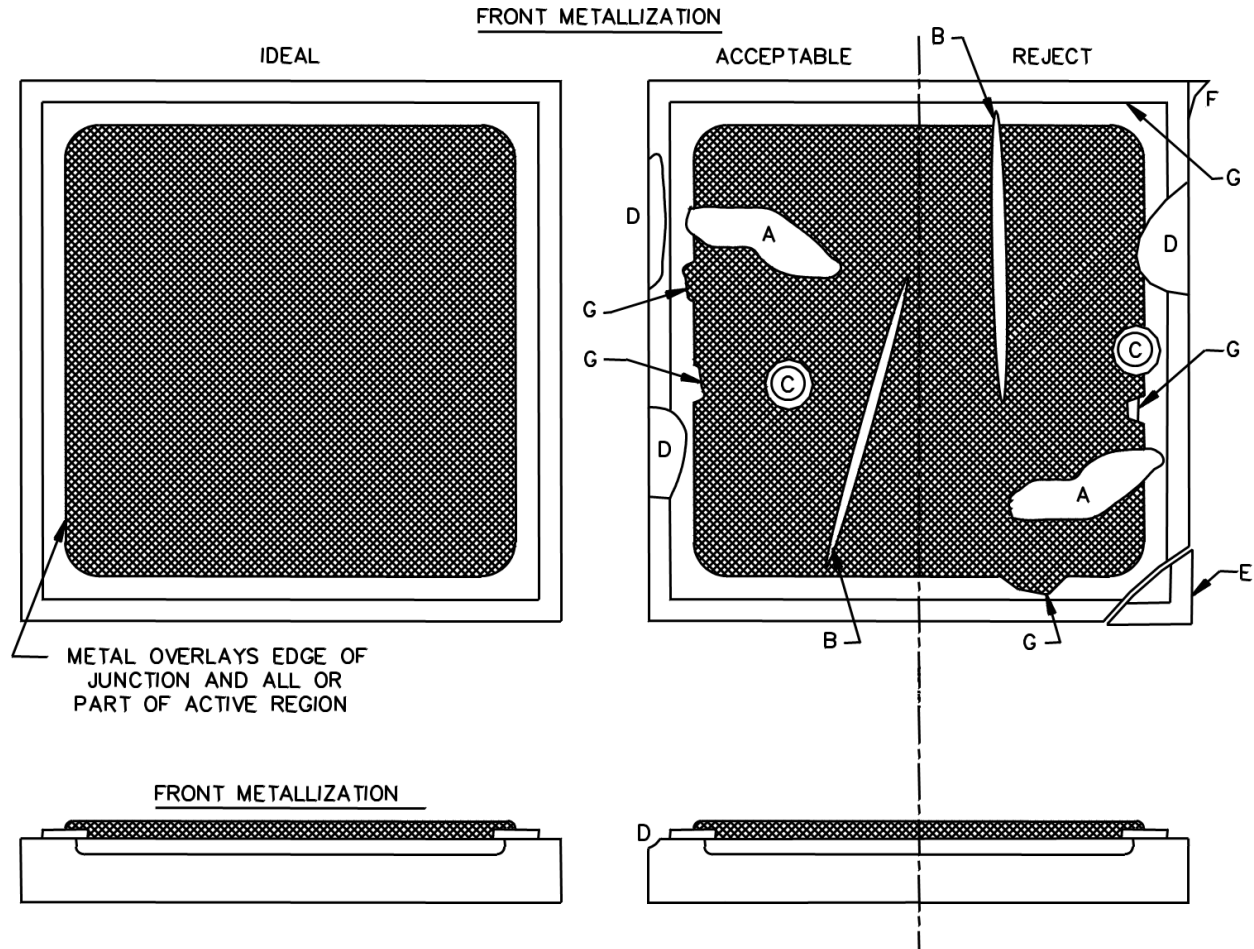
1. Smears (A), scratches (B) or probe marks (C) **shall** not extrude metal outside metallized region over moat edge.
2. Edge chipping or cracks (D) **shall** not extend into moat area.
3. Missing pieces (E) extending 50 percent of distance between chip edge and the moat or additional attached pieces (F) defined by an incomplete cut or scribe line **shall not be acceptable**.
4. Additional front metallization extending into the moat (G) or pulled back to reveal contact area or any non-passivated region **shall not be acceptable**.
5. Cracks (not illustrated) **shall** not extend under the metallized areas nor more than 50 percent of the way across the moat from the outside.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-4. Inside moat mesa diodes (passivated moat does not extend to edge of die).

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Reject criteria:

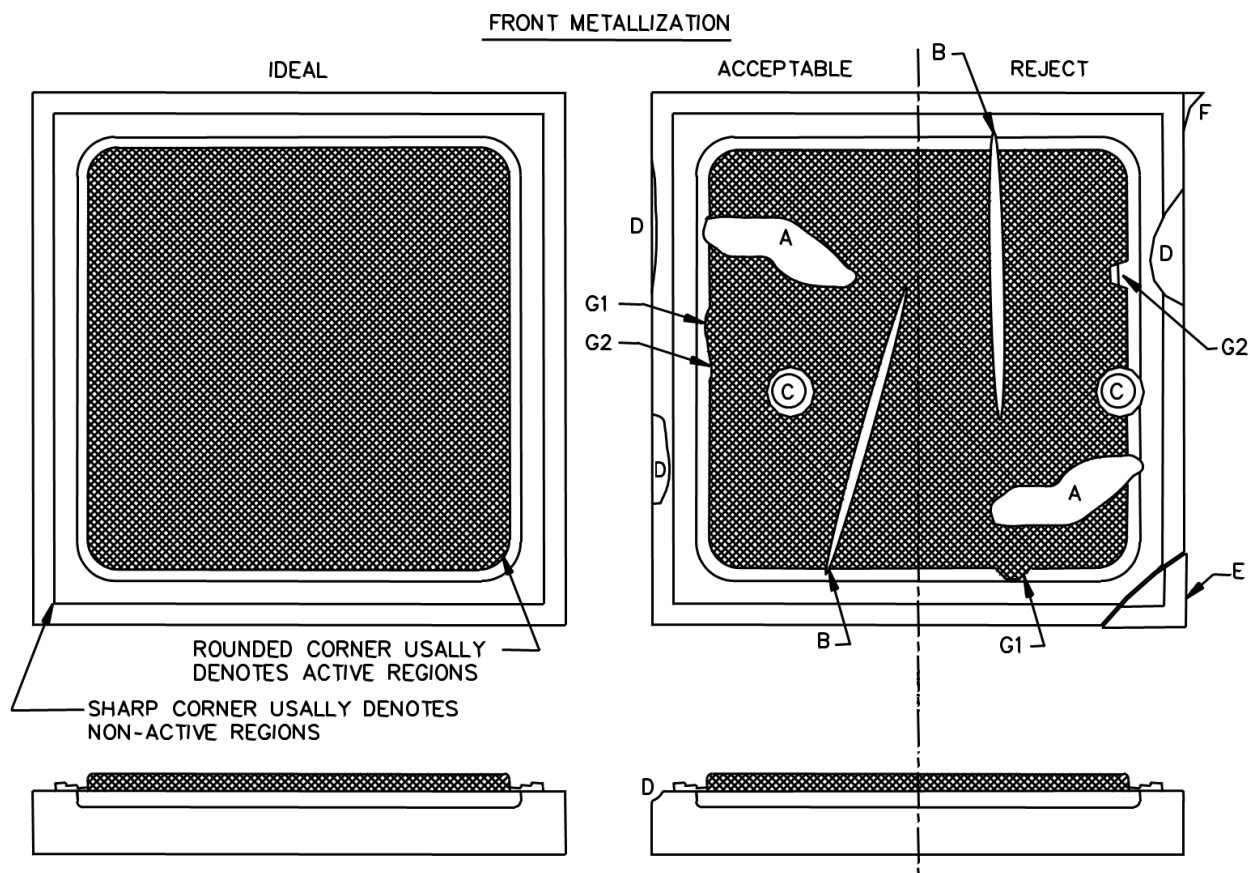
1. Smears (A), scratches (B) or probe marks (C) **shall** not extrude metal outside metalized region more than 50 percent of the way to the next boundary.
2. Edge chipping (D) **shall** not extend into metallization.
3. Missing pieces (E) extending beyond 50 percent to metal boundary or additional attached pieces (F) defined by an incomplete cut or scribe **shall not be acceptable**.
4. Additional front metallization extending 50 percent or more to the next geometric boundary (G) or pulled back to reveal contact area or any non-passivated active region **shall not be acceptable**.
5. Cracks (not illustrated) **shall** not extend under the metalized areas and **shall** not be present inside any of the active regions.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-5. Low voltage contact overlay diodes (metal overlays junction and active area field plate).

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**Reject criteria:**

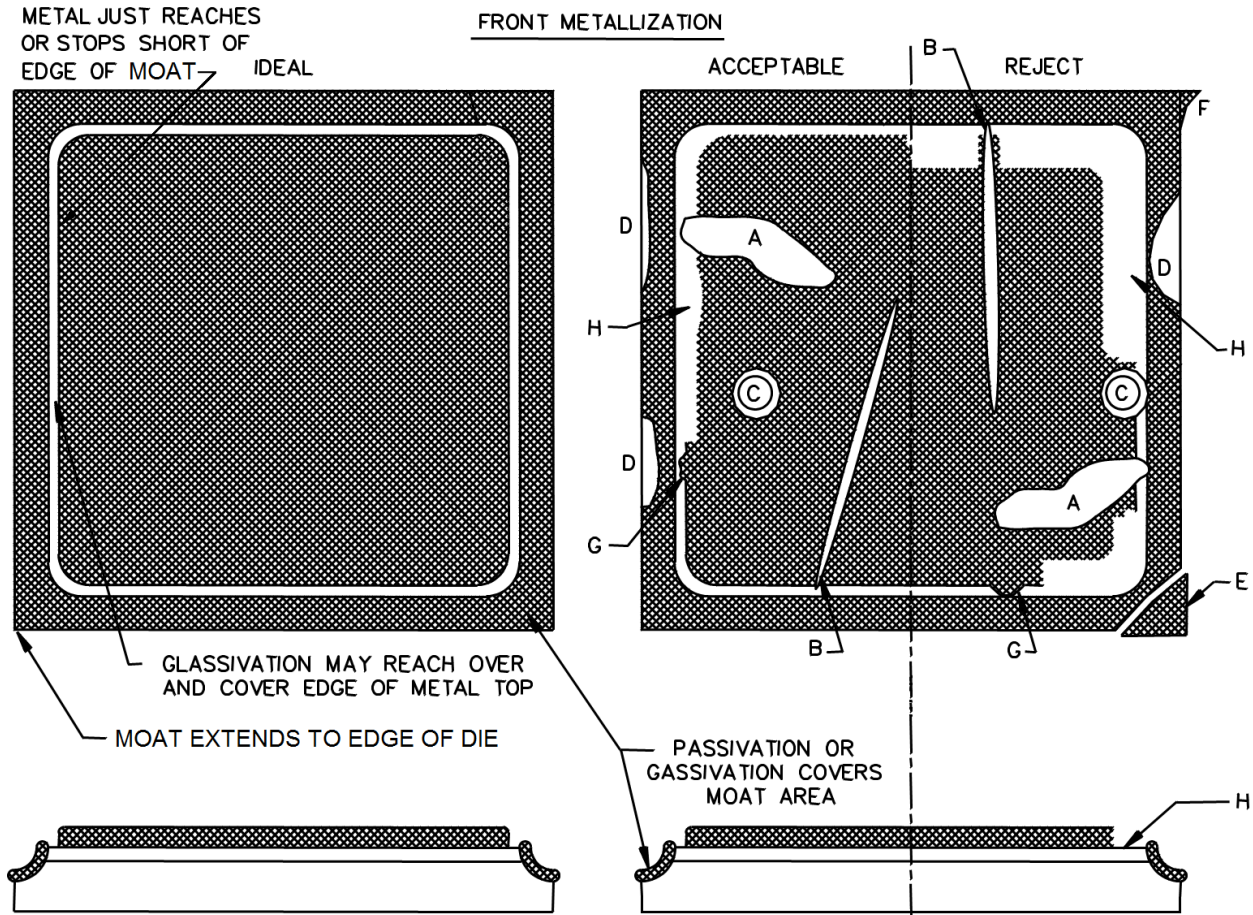
1. Smears (A), scratches (B) or probe marks (C) shall not extrude metal outside junction boundary region.
2. Edge chipping or cracks (D) shall not extend beyond 50 percent between chip edge and junction boundary.
3. Missing pieces (E) extending beyond 50 percent to junction boundary or additional attached pieces (F) defined by an incomplete cut or scribe line shall not be acceptable.
4. Additional front islands of metallization crossing any diffusion line (G1) or pulled back to reveal contact area or any non-passivated region (G2) shall not be acceptable. Note that G2 does not apply to die designed without requiring metal passivation overlay. In this latter exception, much or all of the oxide window will be exposed as a legal part of the design.
5. Cracks (not illustrated) shall not extend under the metallized areas and shall not be present inside any of the active regions.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.
3. Sharp corner usually denotes non-active regions.

FIGURE 2073-6. Low voltage planar diode.

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Reject criteria:

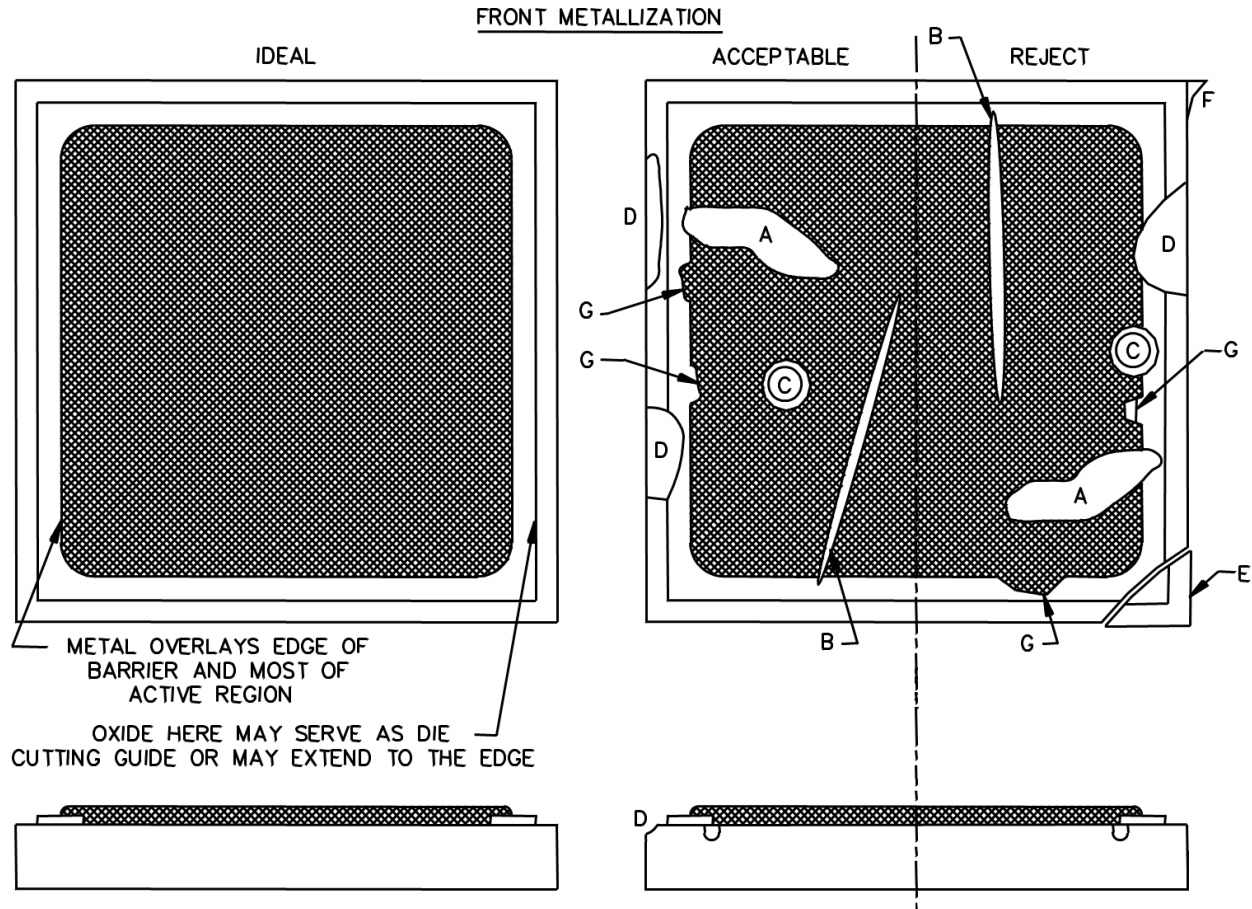
1. Smears (A), scratches (B) or probe marks (C) **shall** not extrude metal outside metalized region over moat edge.
2. Edge chipping (D) **shall** not extend into moat area more than 50 percent.
3. Missing pieces (E) extending beyond 50 percent across moat or additional attached pieces (F) defined by an incomplete cut or scribe line **shall not be acceptable**.
4. Additional front metallization extending over into the moat (G) or missing front metal (H) exceeding 5 percent of total mesa area **shall not be acceptable**.
5. Cracks (not illustrated) **shall** not extend under the metalized area no more than 50 percent of the way across the moat from the outside.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-7. Outside moat mesa diodes (moat extends from mesa to edge of die).

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**Reject criteria:**

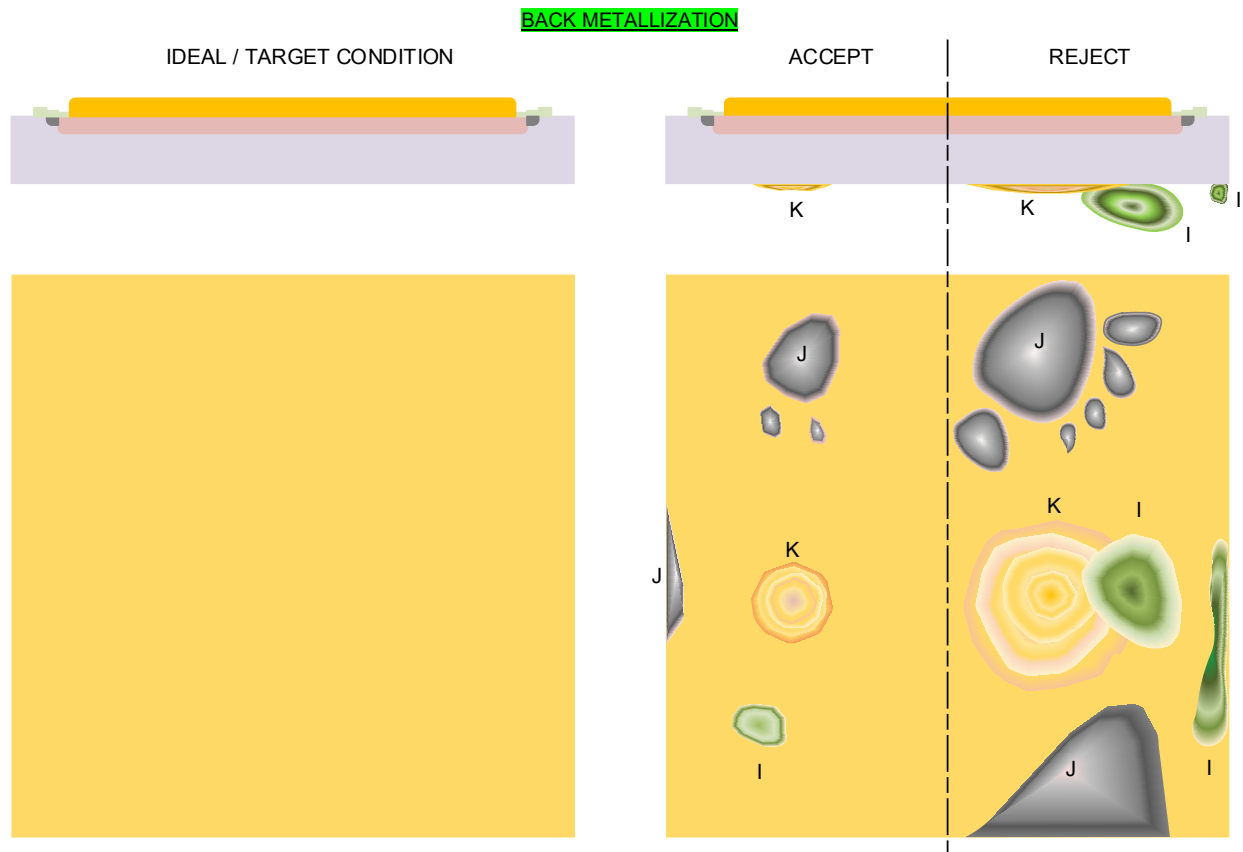
1. Smears (A), scratches (B) or probe marks (C) **shall** not extrude metal outside metalized region more than 50 percent to the next geometric boundary.
2. Edge chipping (D) **shall** not extend into metallization.
3. Missing pieces (E) extending more than 50 percent of distance from chip edge and metallization or additional attached pieces (F) that exceed **die** dimensional specifications **shall not be acceptable**.
4. Additional front metallization extending 50 percent or more to the next geometric boundary (G) or pulled back to reveal contact area or any non-passivated barrier region **shall not be acceptable**.
5. Cracks (not illustrated) **shall** not extend under the metalized areas and **shall** not be present inside any of the active regions.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-8. Schottky barrier diodes (metal overlays barrier edge and active area field plate).

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Reject criteria:

1. Backside contamination and foreign material (I), either firmly or loosely attached, exceeding 10 percent of total area.
2. Missing backside metal (J) exceeding 20 percent of total area.
3. Blisters (K) in metallization exceeding 10 percent of total area.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-9. Back side (bottom) inspection criteria.

KEY to changes:

Text that was added to the Initial Draft are highlighted in yellow.

Text that was added for the Final Report as a result of comments to the Initial Draft are highlighted in green and marked with green vertical bars.

ATTACHMENT 2 to FINAL REPORT for Project 5961-2024-020

METHOD 2073.2 3

VISUAL INSPECTION FOR UNENCAPSULATED DIE (SEMICONDUCTOR DIODE) DIE

1. Purpose. The purpose of this test method is to check verify that the quality and workmanship of unencapsulated semiconductor diode die (hereafter referred to as "die") for compliance with the requirements of contained herein and the individual performance specification sheet or acquisition document.

1.1 Application. All examinations and inspections shall be performed to detect identify and eliminate reject those die with defects that could lead to device failures. This test method will normally be used prior to die installation on a 100 percent inspection basis. This test method may also be employed on a sampling basis prior to encapsulation to determine the effectiveness of the manufacturer's quality control and handling procedures.

1.2 Exclusions and limitations. Excludes die designs with both anode and cathode on the same surface and stacked dice assemblies.

2 3. Apparatus. a. The apparatus for this test method shall include consist of the following:

- a. Optical equipment (monocular, binocular, or stereo microscope) capable of the magnifications specified herein.
- b. Light sources to illuminate the devices being inspected.
- c. Adequate fixturing shall be provided for handling the die during examination without causing contamination or damage during examination.
- d. Adequate covered storage and transportation containers to protect devices die from mechanical damage and environmental contamination.
- e. and Any Visual standards (e.g., gauges, drawings, photographs) necessary to perform an effective examination and enable the examiner inspector to make objective decisions on the acceptability of the die being examined.

3. 2 Definitions. The following definitions shall apply:

- a. Active area: Any area where electrical contact may be made on the "N" "P" or "P" "N" regions of the die.
- b. Active region: Region covered by passivation that supports electrical activity and junction geometries.
- c. Foreign material (attached): Any conductive or nonconductive material that is not part of the die construction.
 1. Conductive foreign material is defined as any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspections.
 2. Therefore, Nonconductive foreign material is defined as any substance that appears transparent translucent under those conditions of lighting and magnification used in routine visual inspections.
- d. Junction: The boundary between "P" and "N" type semiconductor material.

NOTE: In the case of a Schottky diode, there is no actual junction other than the guard ring. Schottky diodes have a barrier that exists at the metal-silicon contact, however, for the purposes of this test method the barrier will be treated as a junction.

- e. Passivation: Silicon oxide, silicon nitride, or other insulating material that is grown or deposited directly over the "P-N" junction or the Schottky guard ring "P-N" junction.

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f. Particles. Semiconductor material chips shall be treated as conductive particles. The following classifications apply:

1. Embedded particles: Particles which are attached by more than one half of their largest dimension.
2. Non-embedded particles: Particles which are attached by less than one half of their largest dimension.

g. Probe marks. Probe marks are indentations, mars or scratches on the bond pads made by probes during electrical measurements.

4. General requirements.

4.1 ~~4.~~ Procedure. The die shall be examined in a suitable sequence of operations and at the specified magnifications to determine compliance with the requirements of the individual specification sheet or acquisition document and the criteria of this test methods figures and associated textual criteria ~~the specified test conditions~~. The sequence of examinations required may be varied at the discretion of the manufacturer.

4.1.1 ~~4.1~~ Die inspections. These inspections shall apply to alloy, diffused mesa, epitaxial mesa, planar, and epitaxial planar construction techniques. Unless otherwise specified, inspections shall be made on a random selection of ~~at least one side~~ the applicable side or sides (see 4.2) of each die being inspected. If a lot fails, 100-percent inspection of the total lot shall be performed.

4.1.2 Magnification. ~~b.~~ Unless otherwise specified by the individual specification sheet or acquisition document ~~procuring activity~~, the die magnifications requirements specified in table 2073-I shall be used for visual inspection. The following details apply:

- a. Visual inspection Examinations shall be performed ~~with a monocular, binocular, or stereo microscope and shall be performed~~ perpendicular to the die surface with normal incident illumination.
- b. The inspection shall be performed under suitable illumination.
- c. Binocular and stereo microscopes shall have each eyepiece individually focused for the ~~examiner~~ inspector

TABLE 2073-I. Die magnification requirements.

Chip Die size 1/	High power magnification	Low power magnification
.030 inch ~~30 mils~~ (0.76 mm) or less	100X to 200X	30X to 50X
.031 ~~31~~ to .060 inch ~~60 mils~~ (0.78 to 1.52 mm)	75X to 150X	30X to 50X
.061 inch ~~61~~ to .150 inch ~~150 mils~~ (1.55 to 3.81 mm)	35X to 120X	20X to 30X
Greater than .150 inch ~~150 mils~~ (3.81 mm)	25X to 75X	20X to 30X

1/ Length of shortest dimension.

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4.2 Examination options. ~~Examine die according to the appropriate figure, its' illustrations, and associated textual criteria.~~ After dice sample selection for visual inspection, the manufacturer may elect either of two options as follows.

- a. Option A: Front side visual inspection with sample size specified by individual specification sheet or acquisition document ~~procuring activity~~. If no sample size is specified, 100-percent visual is assumed.
- b. Option B: Both front side and back side ~~visual in addition to front side visual inspection~~. Backside visual ~~is~~ inspection shall be conducted with sample size specified by individual specification sheet or acquisition document ~~procuring activity~~. If no sample size is specified, use sample size 22 for ~~class~~ quality level H or sample size 45 for ~~class~~ quality level K. For both quality levels, ~~and~~ reject on 1 or more failures.

NOTE: If no examination option is specified by the individual performance specification sheet or acquisition document ~~procuring activity~~, then option A shall ~~apply~~ be the default examination option.

4.3 Removal of foreign material on die surface. Removal of foreign material or particles on the die surface may be attempted by using a nominal gas blow of approximately 20 psi (138 kPa).

5. Acceptability (accept and reject criteria).

5.1 General. ~~4.1.1 Type of die examined.~~ The die shall be examined in accordance with the applicable figure or figures, as needed, for the die design, construction, topography involved, ~~Examine die according to the appropriate figure, its' illustrations, and associated textual criteria.~~

5.1.1 Selecting representative figure(s). Determine type of die being examined by ~~referring~~ comparing it to figures 2073-1 through 2073-8 and select a representative figure. An exact match of die to figure is not necessary. ~~select a representative figure~~. If a single figure does not represent the die being inspected, then features from more than one figures can be aggregated to form an inspection baseline. If a representative figure or figures cannot be ~~discerned~~ determined, ~~perhaps elements of different figures will apply~~ then contact the die vendor source for assistance in matching an appropriate figure or figures.

NOTE: Hexagonal shaped die ~~will~~ shall be inspected to the same criteria as the square die shown herein.

5.1.2 Die figures. The following figures depict the design, construction, and topography of square die:

- a. The figures for front side visual inspection (options A and B) are as follows:

- a. Button contact diodes. figure 2073-1.
- b. High voltage planar diode I. figure 2073-2.
- c. High voltage planar diodes II. figure 2073-3.
- d. Inside moat mesa diodes. figure 2073-4.
- e. Low voltage contact overlay diodes. figure 2073-5.
- f. Low voltage planar diode. figure 2073-6.
- g. Outside moat mesa diodes. figure 2073-7.
- h. Schottky barrier diodes. figure 2073-8.

- b. The figure for backside visual inspection (applicable to option B only) is figure 2073-9.

5.2 ~~4.3 Foreign material.~~ ~~Examine die for attached conductive foreign material. No detailed illustration is~~

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provided for this due to the random nature of such material. The examiner is expected to use their own judgment in this matter. Die inspections for foreign material shall be performed at low magnification.

5.2.1 Defects. Die that exhibits any of the following conditions shall not be acceptable:

- a. Embedded particles on the surface of the die that bridge semiconductor junctions, or any combination of metallization or junction.
- b. Loosely attached conductive particles on the surface of the die that are large enough to bridge the narrowest unglassivated active circuit element spacing.
- c. Non-embedded particles on the surface of the die that are large enough to bridge the narrowest unglassivated active metal spacing.
- d. Ink, paint or similar blemish on the surface of the die that covers more than 25 percent of the bonding area or pad area or that bridges any combination of unglassivated metallization or bare semiconductor material (silicon areas) (see figure 2073-12 new figure based off figure 2072-43).

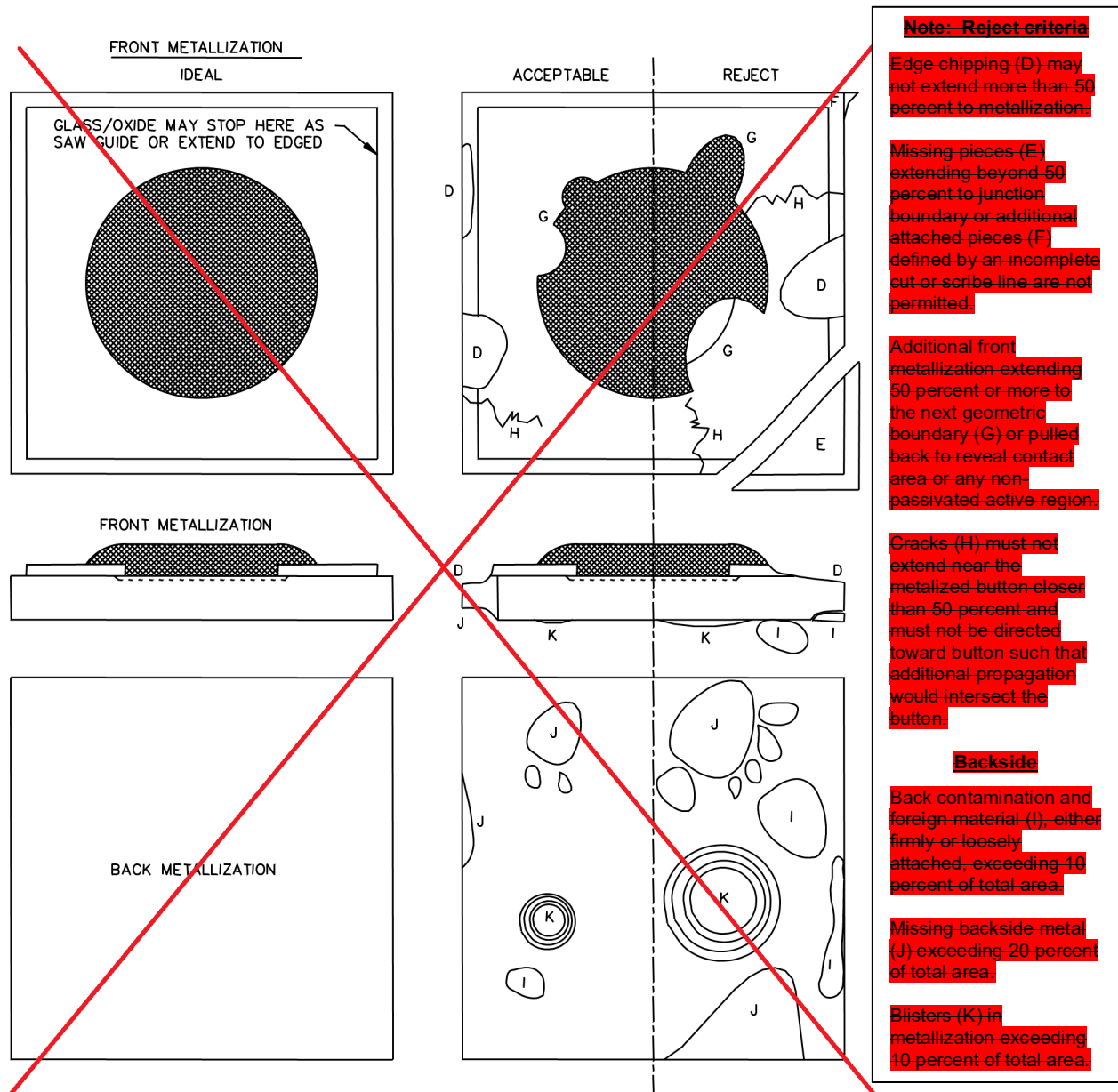
5.2.2 Foreign material or particle removal. If present, attached conductive foreign material or particles may be removed in accordance with 4.3.

5.3 ~~4.4~~ Probe marks. Probe marks shall not penetrate the contact metal and expose any non-passivated active region.

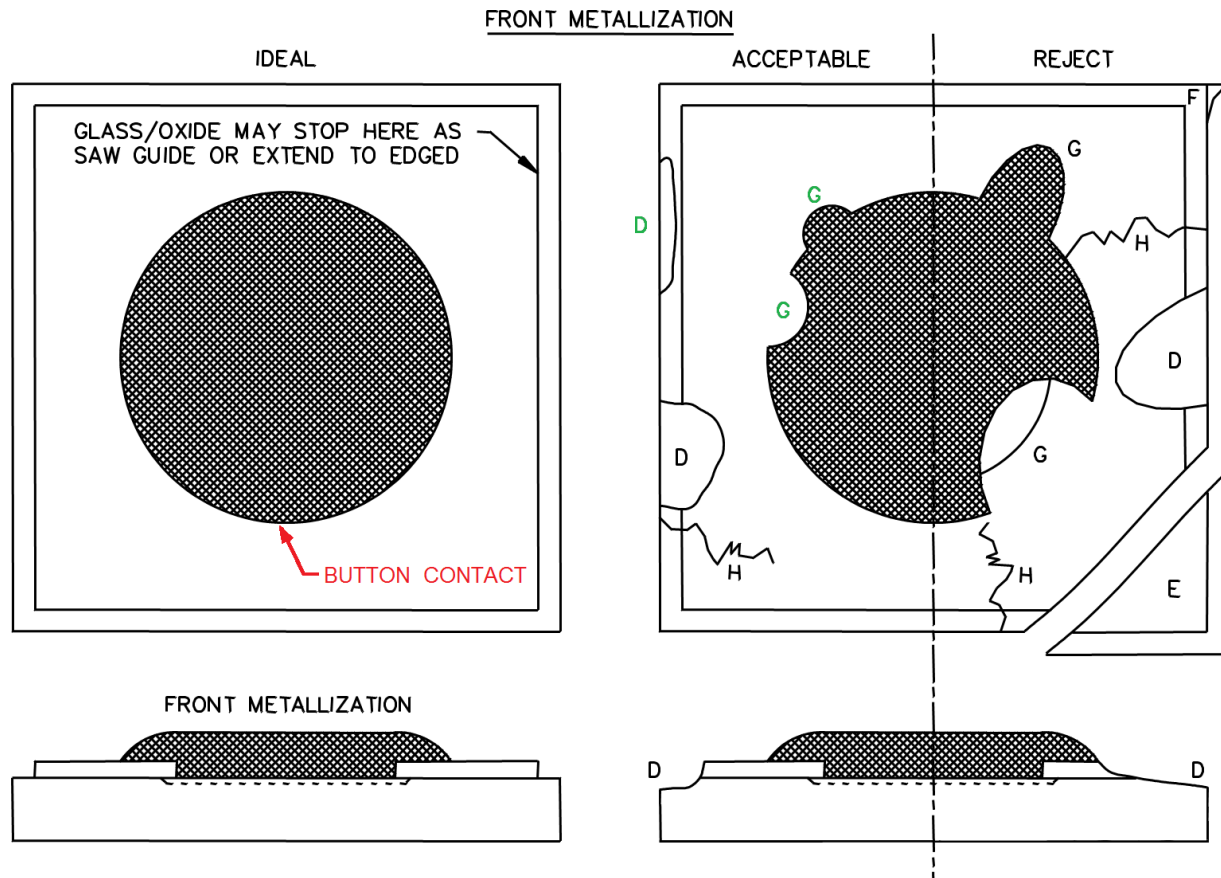
6. Summary. The following conditions should be specified in the applicable document (performance specification sheet or drawing):

- a. Examination option letter.
- b. Any additional requirements for design, construction and topography.

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FIGURE 2073-1. Button contact diodes (metal button overlays junction and active area).

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**Reject criteria:**

1. Edge chipping (D) **may shall** not extend more than 50 percent to metallization.
2. Missing pieces (E) extending beyond 50 percent to junction boundary **or shall not be acceptable.**
3. Additional attached pieces (F) defined by an incomplete cut or scribe line **are not permitted shall not be acceptable.**
4. Additional front metallization extending 50 percent or more to the next geometric boundary (G) or pulled back to reveal contact area or any non-passivated active region **shall not be acceptable.**
5. Cracks (H) **must shall** not extend near the metalized button closer than 50 percent and **must shall** not be directed toward button such that additional propagation would intersect the button.

NOTES:

1. The cross-sectional views are for reference only.
2. For button contact diodes, the metal button overlays the junction and active area.

FIGURE 2073-1. Button contact diodes **(metal button overlays junction and active area).**

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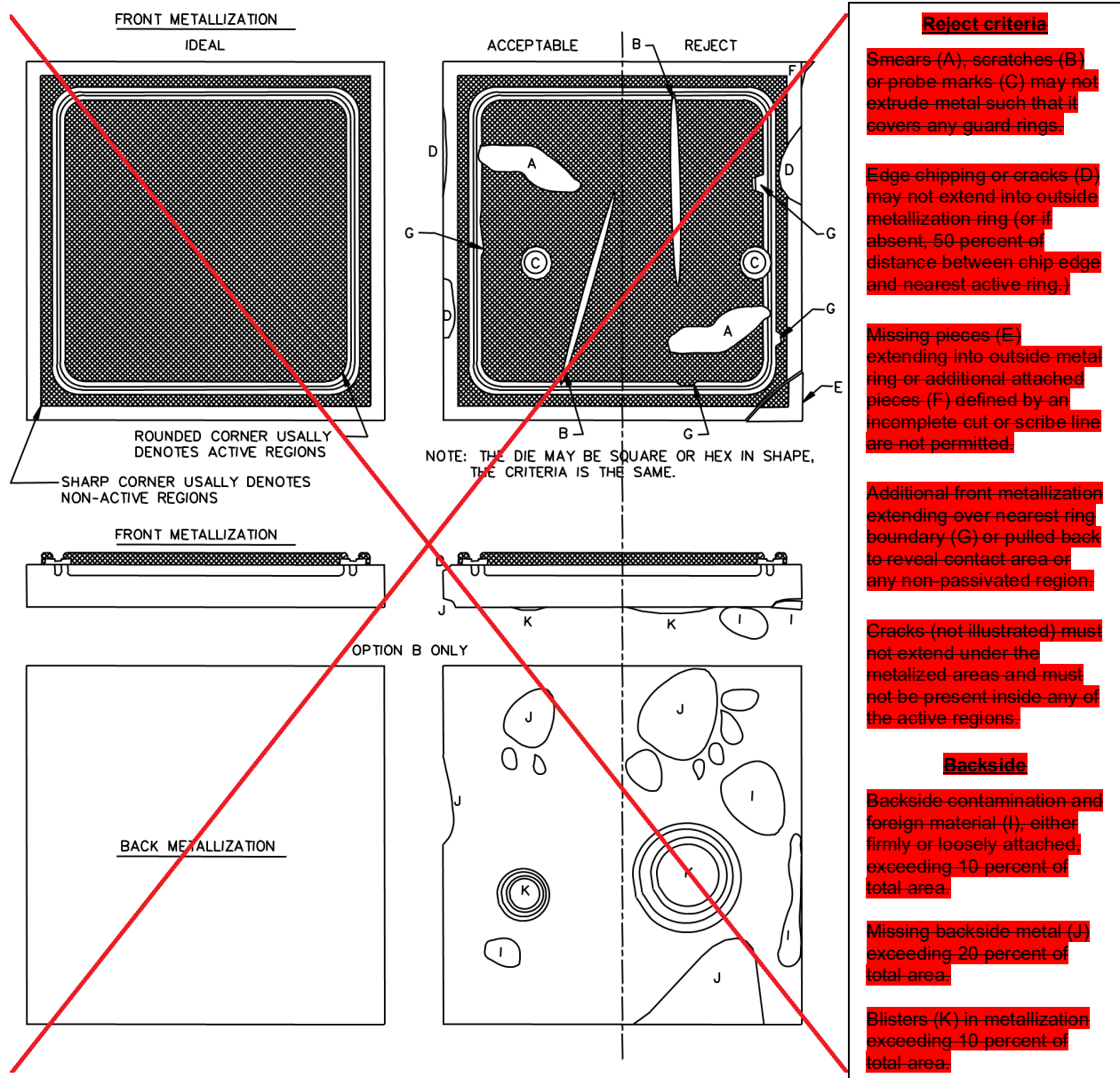
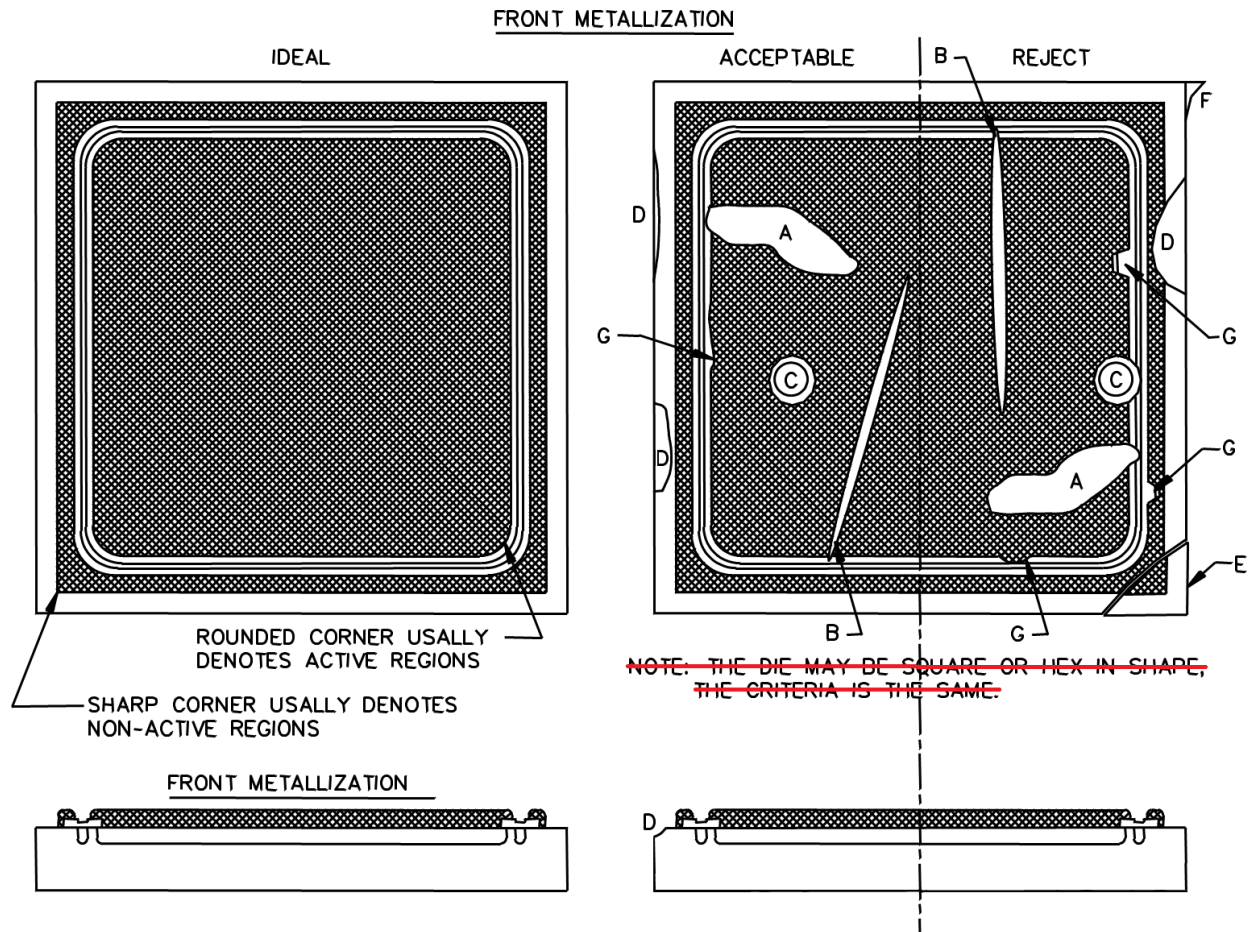


FIGURE 2073-2. High voltage planar diode I (guard ring(s) and outside metal oxide edge cover or field plate).

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**Reject criteria:**

1. Smears (A), scratches (B) or probe marks (C) **may shall** not extrude metal such that it covers any guard rings.
2. Edge chipping or cracks (D) **may shall** not extend into outside metallization ring (or if absent, 50 percent of distance between chip edge and nearest active ring.)
3. Missing pieces (E) extending into outside metal ring or additional attached pieces (F) defined by an incomplete cut or scribe line **are not permitted shall not be acceptable**.
4. Additional front metallization extending over nearest ring boundary (G) or pulled back to reveal contact area or any non-passivated region **shall not be acceptable**.
5. Cracks (not illustrated) **must shall** not extend under the metalized areas and **must shall** not be present inside any of the active regions.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-2. High voltage planar diode I (guard ring(s) and outside metal oxide edge cover or field plate).

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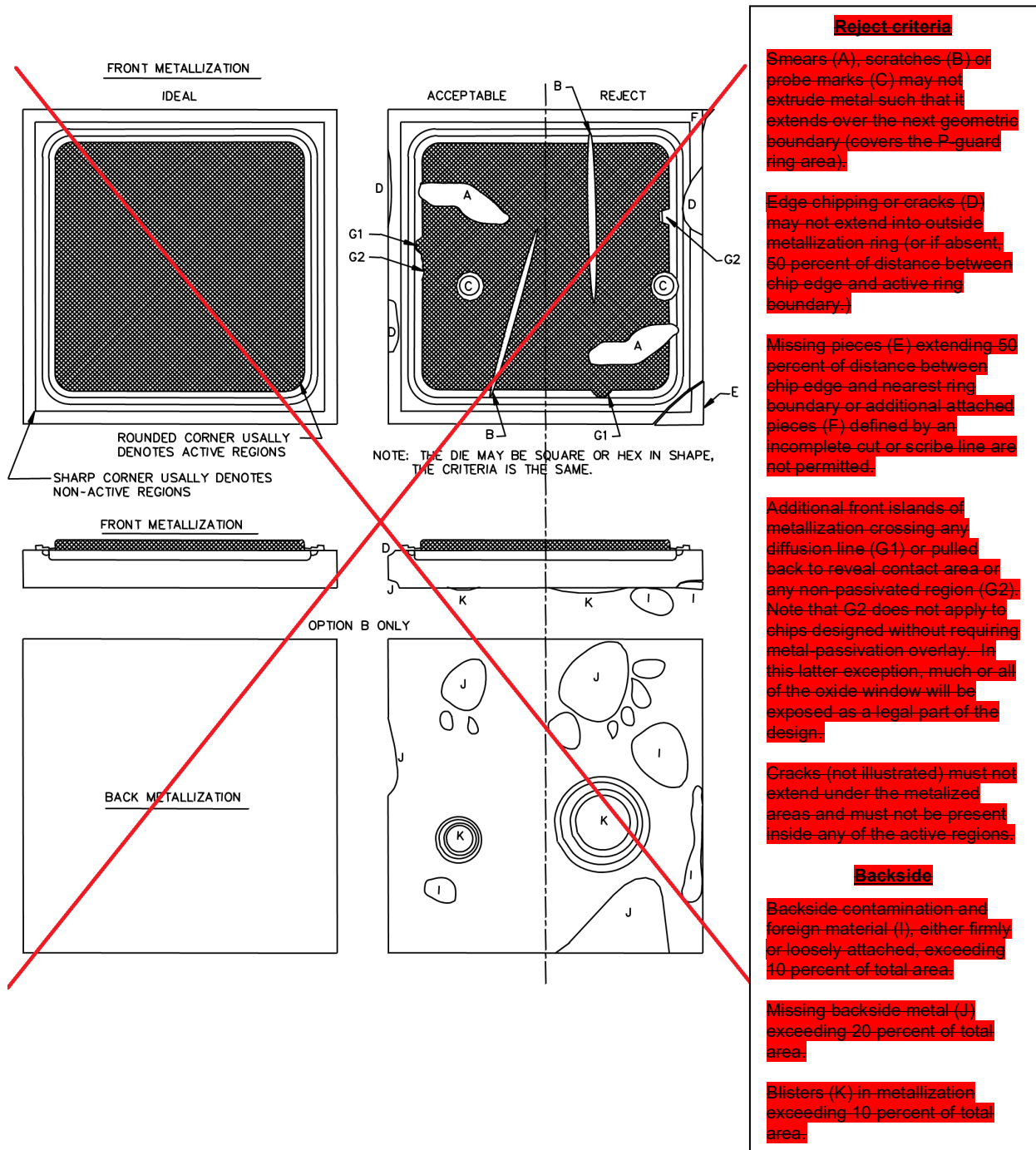
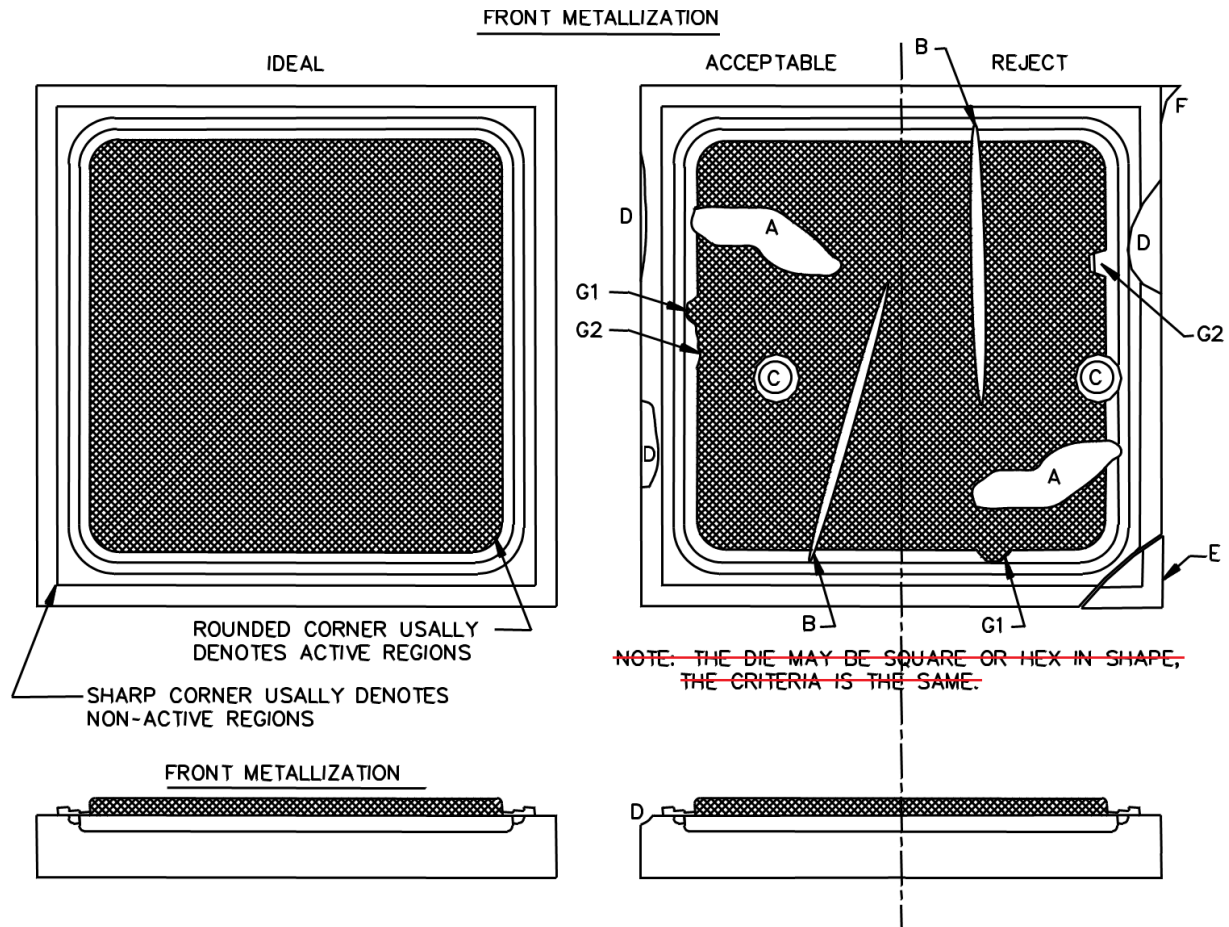


FIGURE 2073-3. High voltage planar diodes II (integrated P-minus guard ring).

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**Reject criteria:**

1. Smears (A), scratches (B) or probe marks (C) **may shall** not extrude metal such that it extends over the next geometric boundary (covers the P-guard ring area).
2. Edge chipping or cracks (D) **may shall** not extend into outside metallization ring (or if absent, 50 percent of distance between chip edge and active ring boundary.)
3. Missing pieces (E) extending 50 percent of distance between chip edge and nearest ring boundary or additional attached pieces (F) defined by an incomplete cut or scribe line **are not permitted shall not be acceptable**.
4. Additional front islands of metallization crossing any diffusion line (G1) or pulled back to reveal contact area or any non-passivated region (G2) **shall not be acceptable**. Note that G2 does not apply to **ships die** designed without requiring metal-passivation overlay. In this latter exception, much or all of the oxide window will be exposed as a legal part of the design.
5. Cracks (not illustrated) **must shall** not extend under the metalized areas and **must shall** not be present inside any of the active regions.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-3. High voltage planar diodes II (integrated P-minus guard ring).

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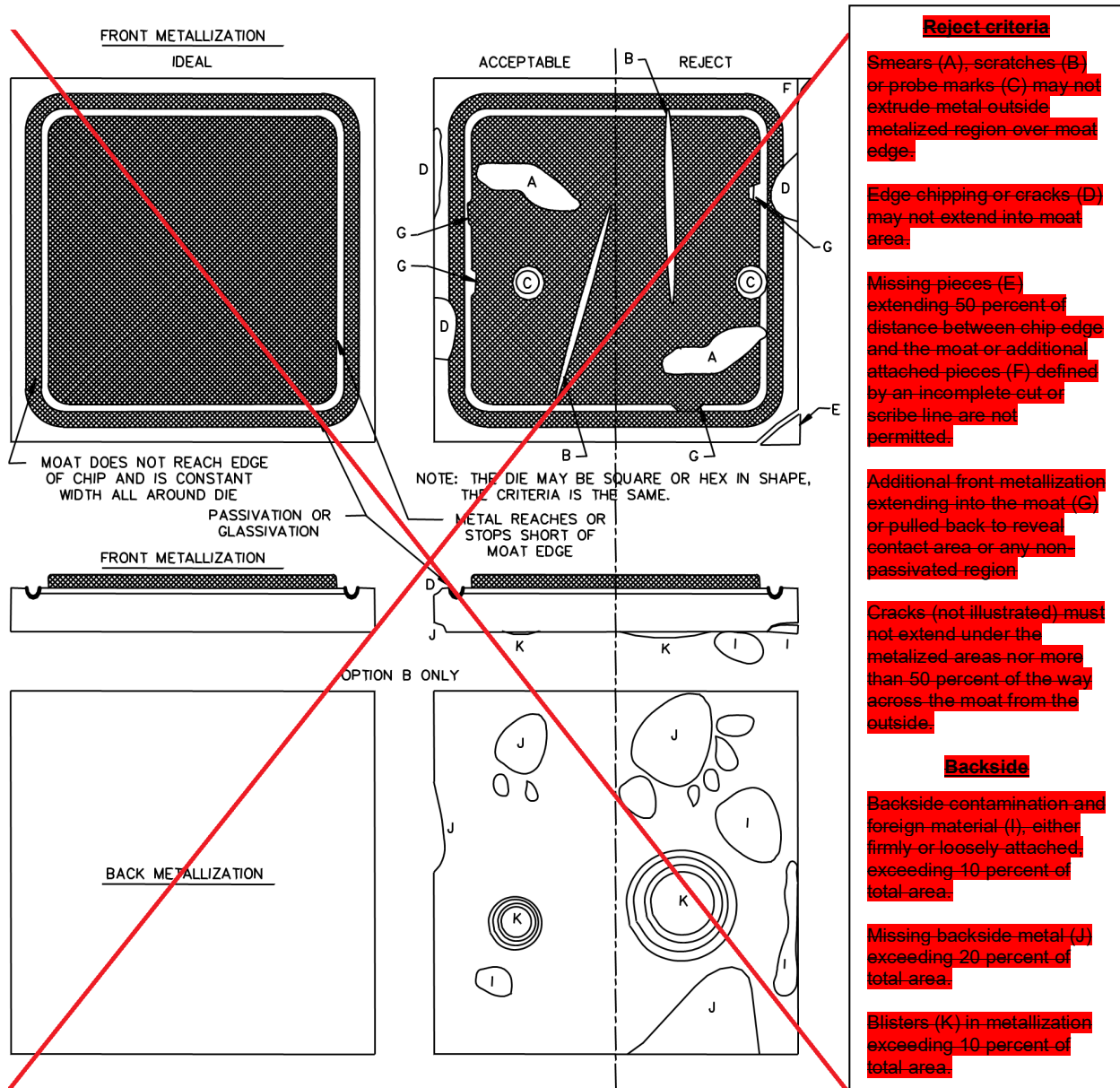
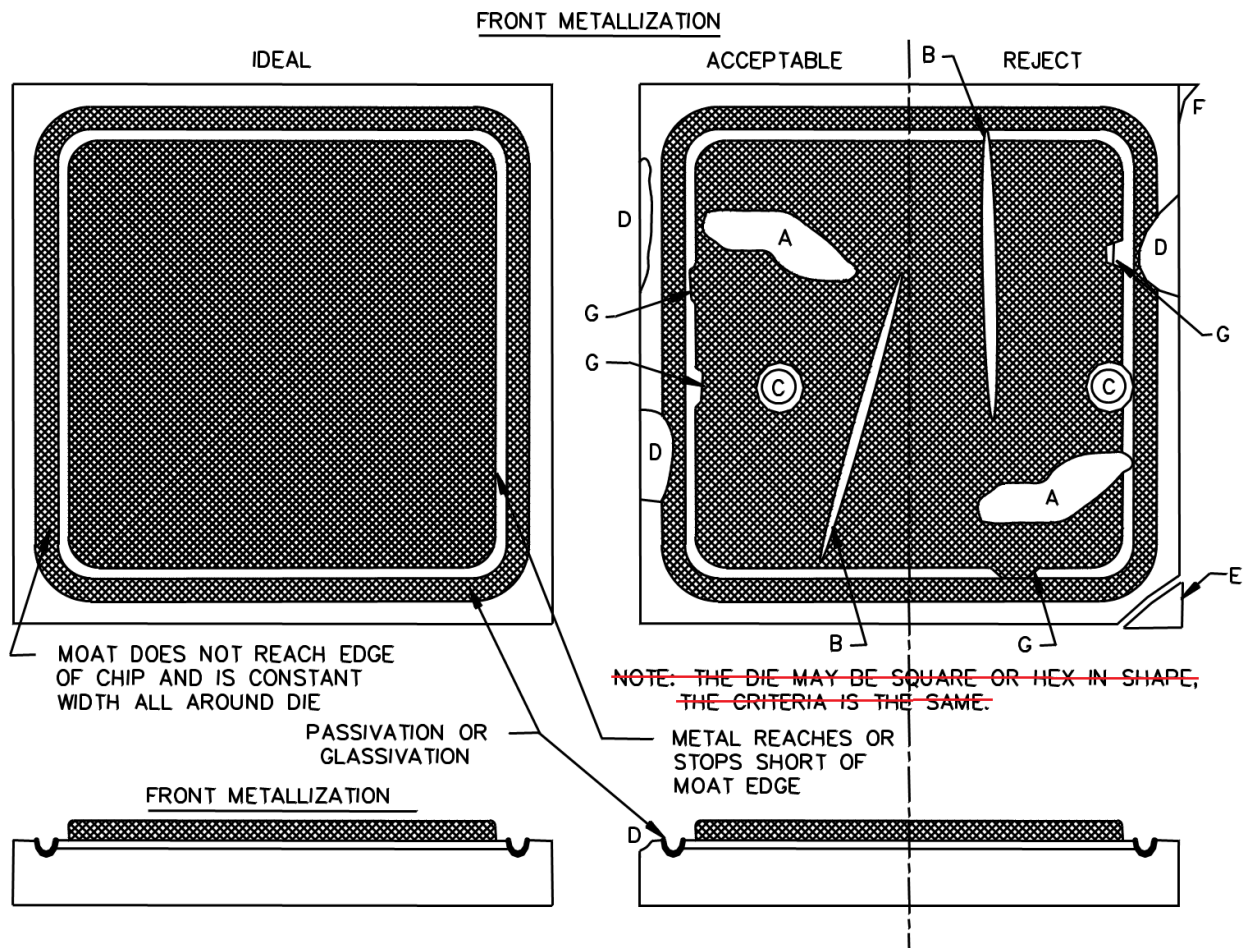


FIGURE 2073-4. Inside moat mesa diodes (passivated moat does not extent to edge of die).

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**Reject criteria:**

1. Smears (A), scratches (B) or probe marks (C) **may shall** not extrude metal outside metalized region over moat edge.
2. Edge chipping or cracks (D) **may shall** not extend into moat area.
3. Missing pieces (E) extending 50 percent of distance between chip edge and the moat or additional attached pieces (F) defined by an incomplete cut or scribe line **are not permitted shall not be acceptable**.
4. Additional front metallization extending into the moat (G) or pulled back to reveal contact area or any non-passivated region **shall not be acceptable**.
5. Cracks (not illustrated) **must shall** not extend under the metalized areas nor more than 50 percent of the way across the moat from the outside.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-4. Inside moat mesa diodes (passivated moat does not extent to edge of die).

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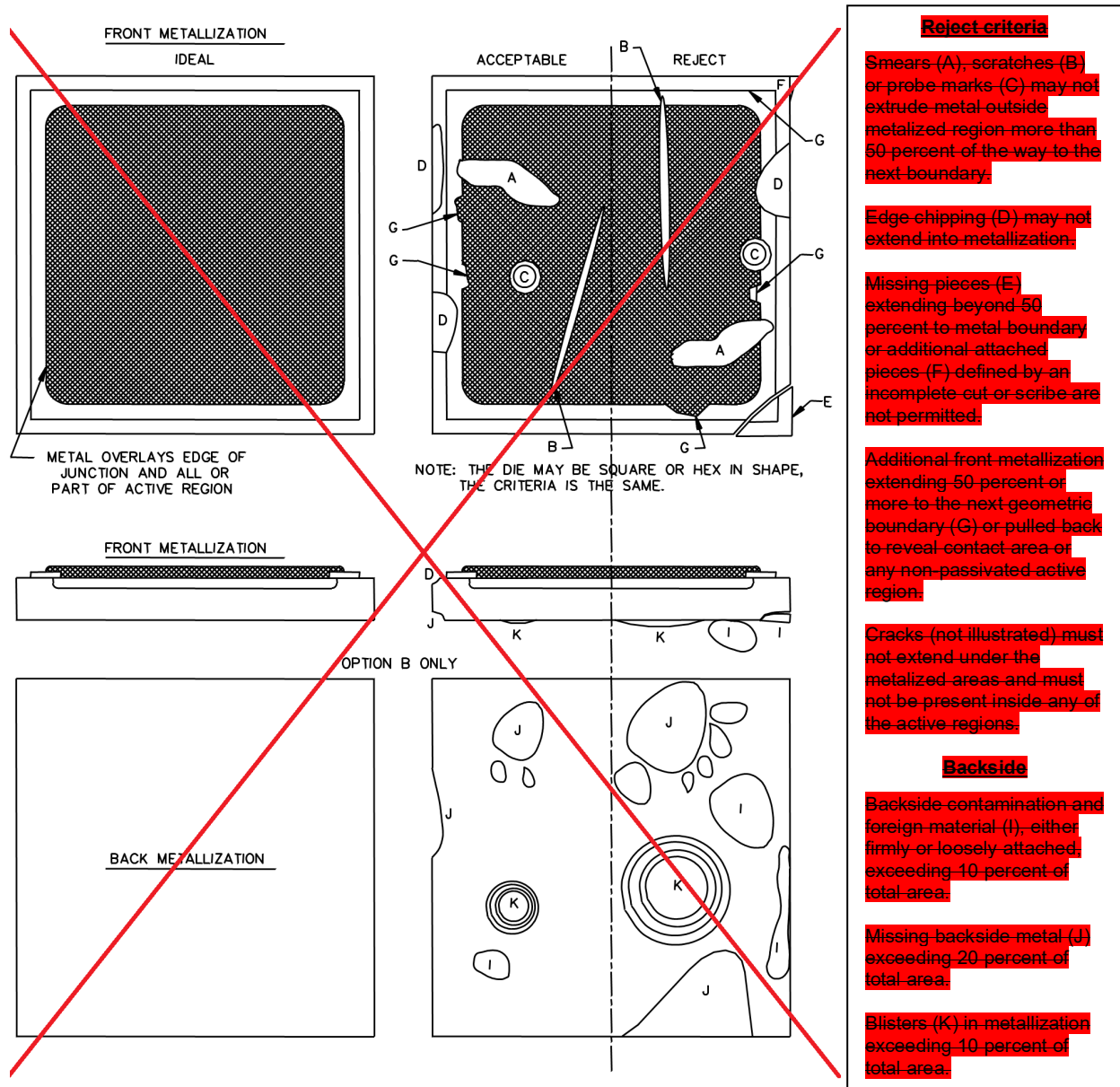
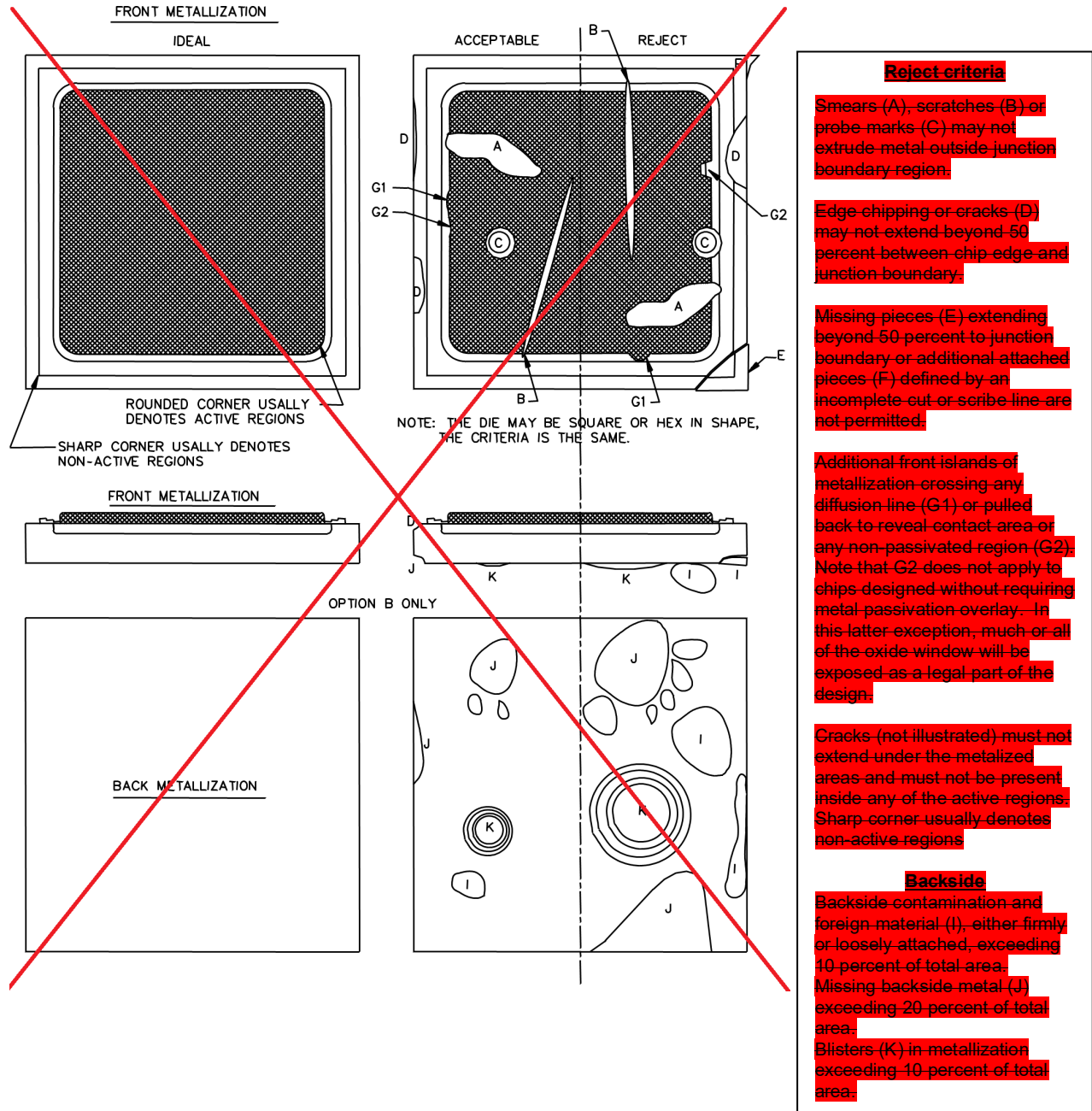


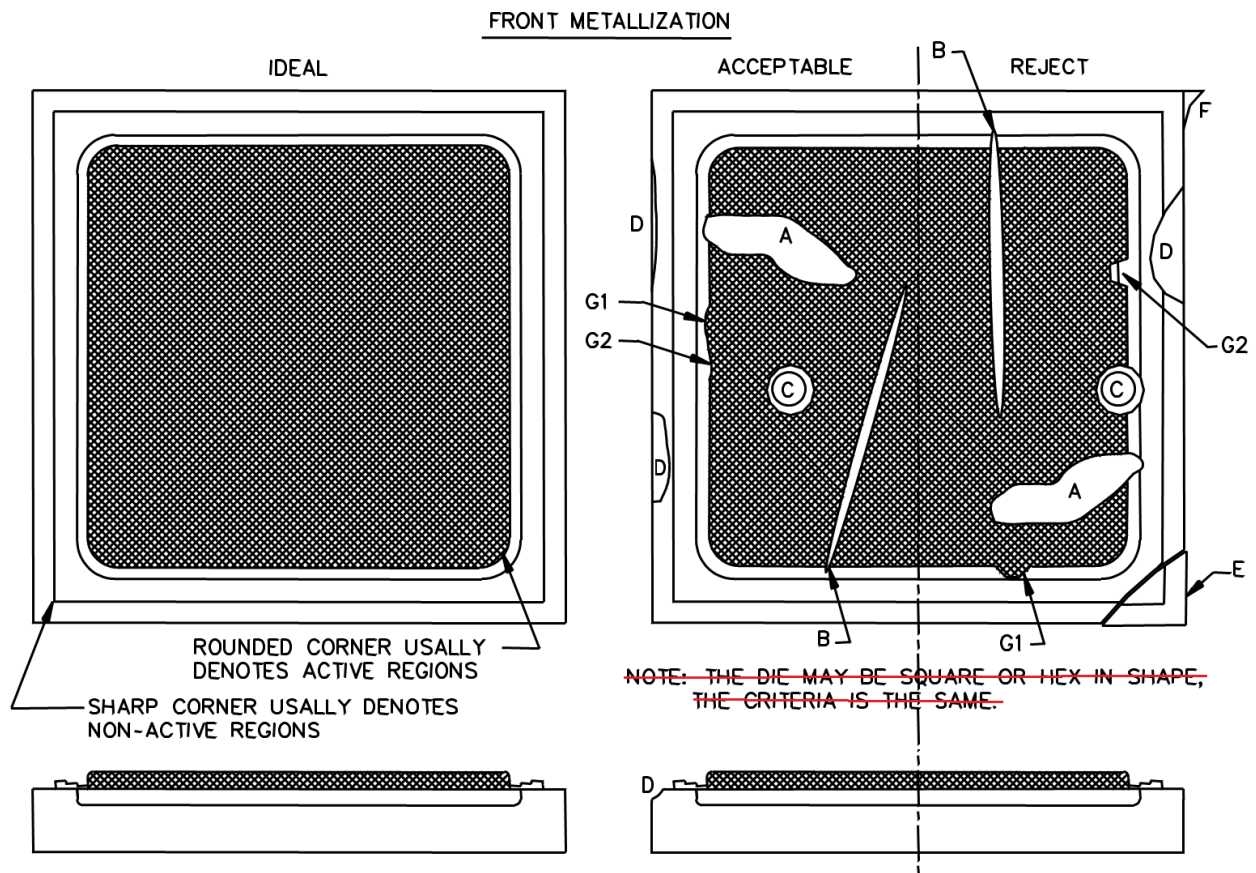
FIGURE 2073-5. Low voltage contact overlay diodes (metal overlays junction and active area field plate).



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FIGURE 2073-6. Low voltage planar diode

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**Reject criteria:**

1. Smears (A), scratches (B) or probe marks (C) **may shall** not extrude metal outside junction boundary region.
2. Edge chipping or cracks (D) **may shall** not extend beyond 50 percent between chip edge and junction boundary.
3. Missing pieces (E) extending beyond 50 percent to junction boundary or additional attached pieces (F) defined by an incomplete cut or scribe line **are not permitted shall not be acceptable**.
4. Additional front islands of metallization crossing any diffusion line (G1) or pulled back to reveal contact area or any non-passivated region (G2) **shall not be acceptable**. Note that G2 does not apply to die designed without requiring metal passivation overlay. In this latter exception, much or all of the oxide window will be exposed as a legal part of the design.
5. Cracks (not illustrated) **must shall** not extend under the metallized areas and **must shall** not be present inside any of the active regions.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.
3. Sharp corner usually denotes non-active regions.

FIGURE 2073-6. Low voltage planar diode.

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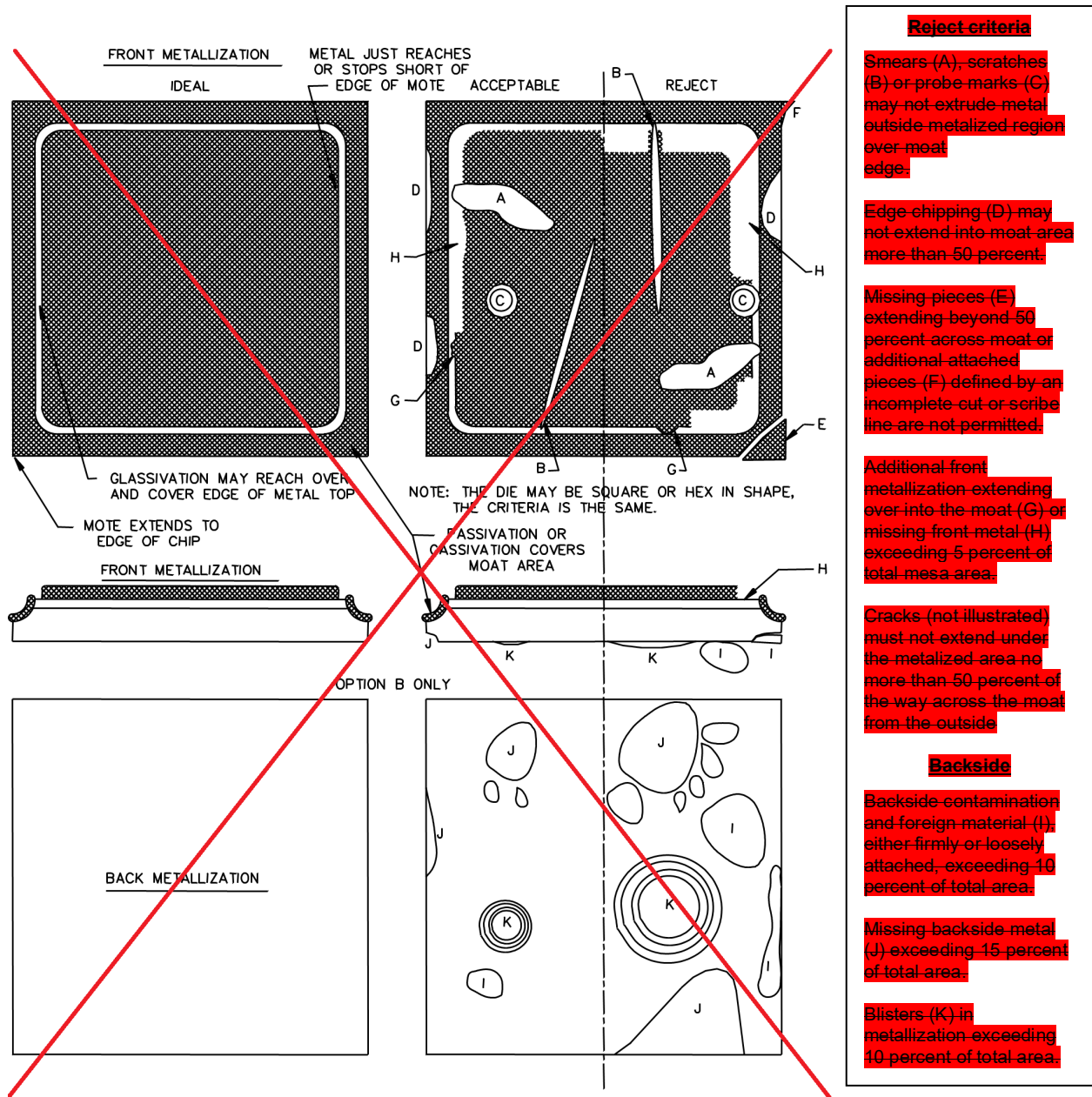
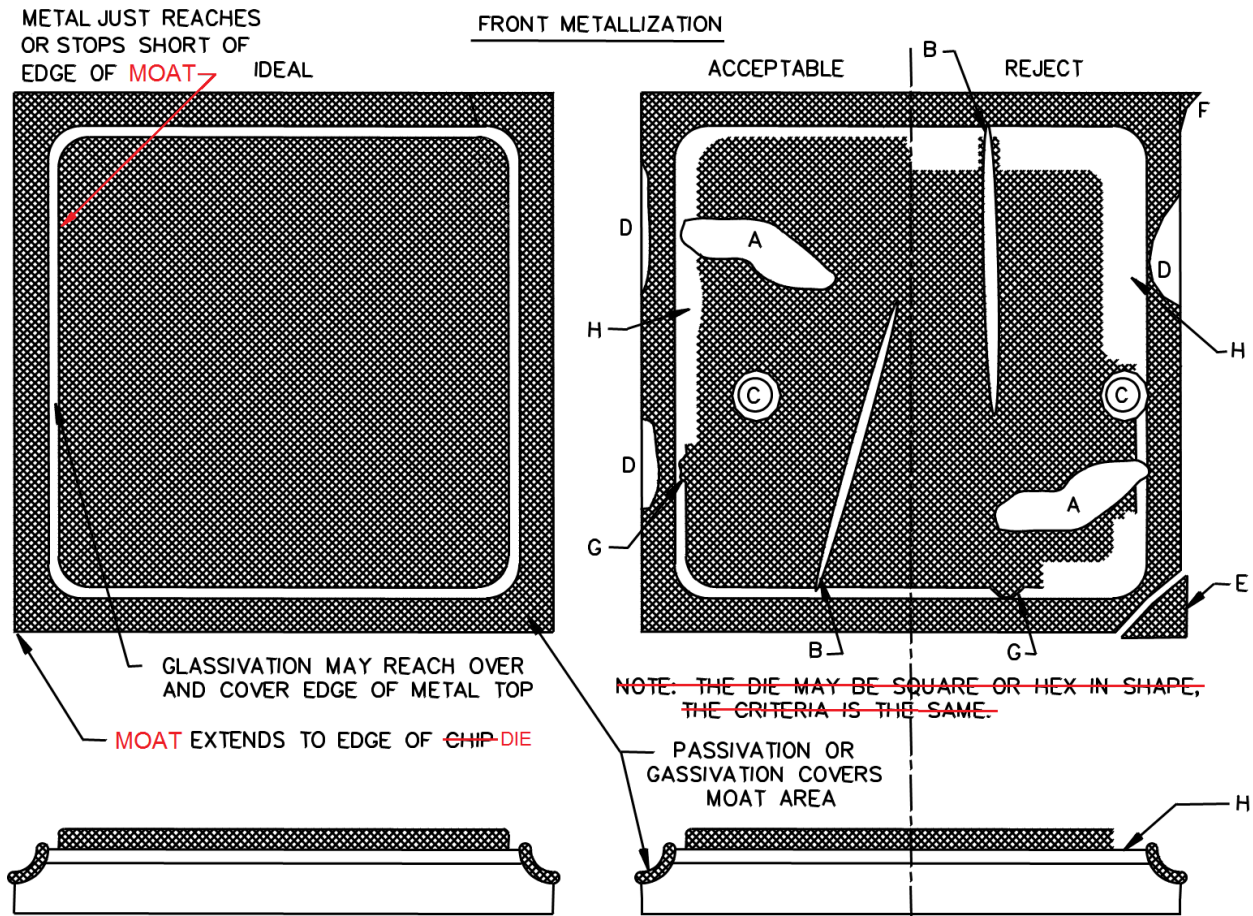


FIGURE 2073-7. Outside moat mesa diodes (moat extends from mesa to edge of die).

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**Reject criteria:**

1. Smears (A), scratches (B) or probe marks (C) **may shall** not extrude metal outside metallized region over moat edge.
2. Edge chipping (D) **may shall** not extend into moat area more than 50 percent.
3. Missing pieces (E) extending beyond 50 percent across moat or additional attached pieces (F) defined by an incomplete cut or scribe line **are not permitted shall not be acceptable**.
4. Additional front metallization extending over into the moat (G) or missing front metal (H) exceeding 5 percent of total mesa area **shall not be acceptable**.
5. Cracks (not illustrated) **must shall** not extend under the metallized area no more than 50 percent of the way across the moat from the outside.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-7. Outside moat mesa diodes (moat extends from mesa to edge of die).

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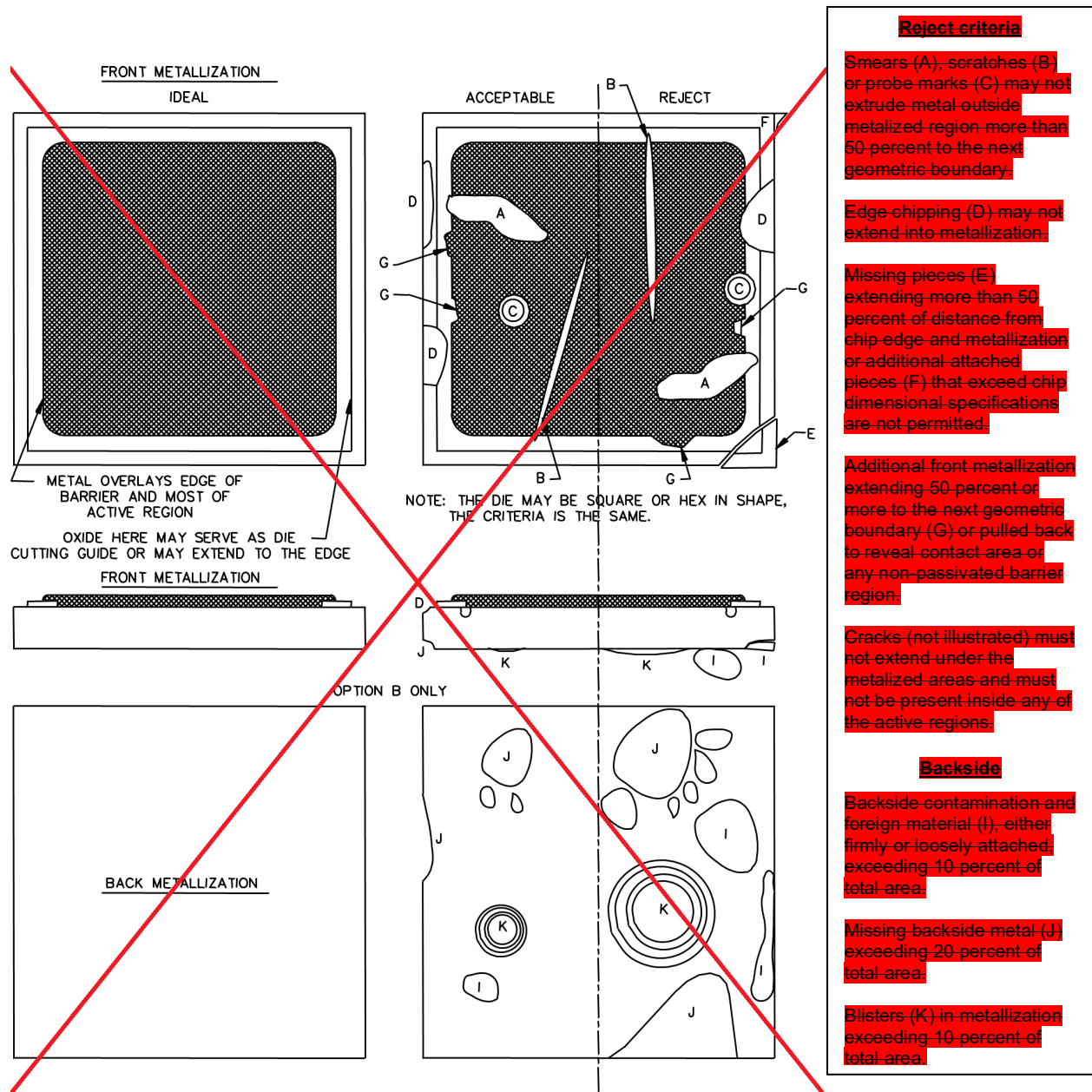
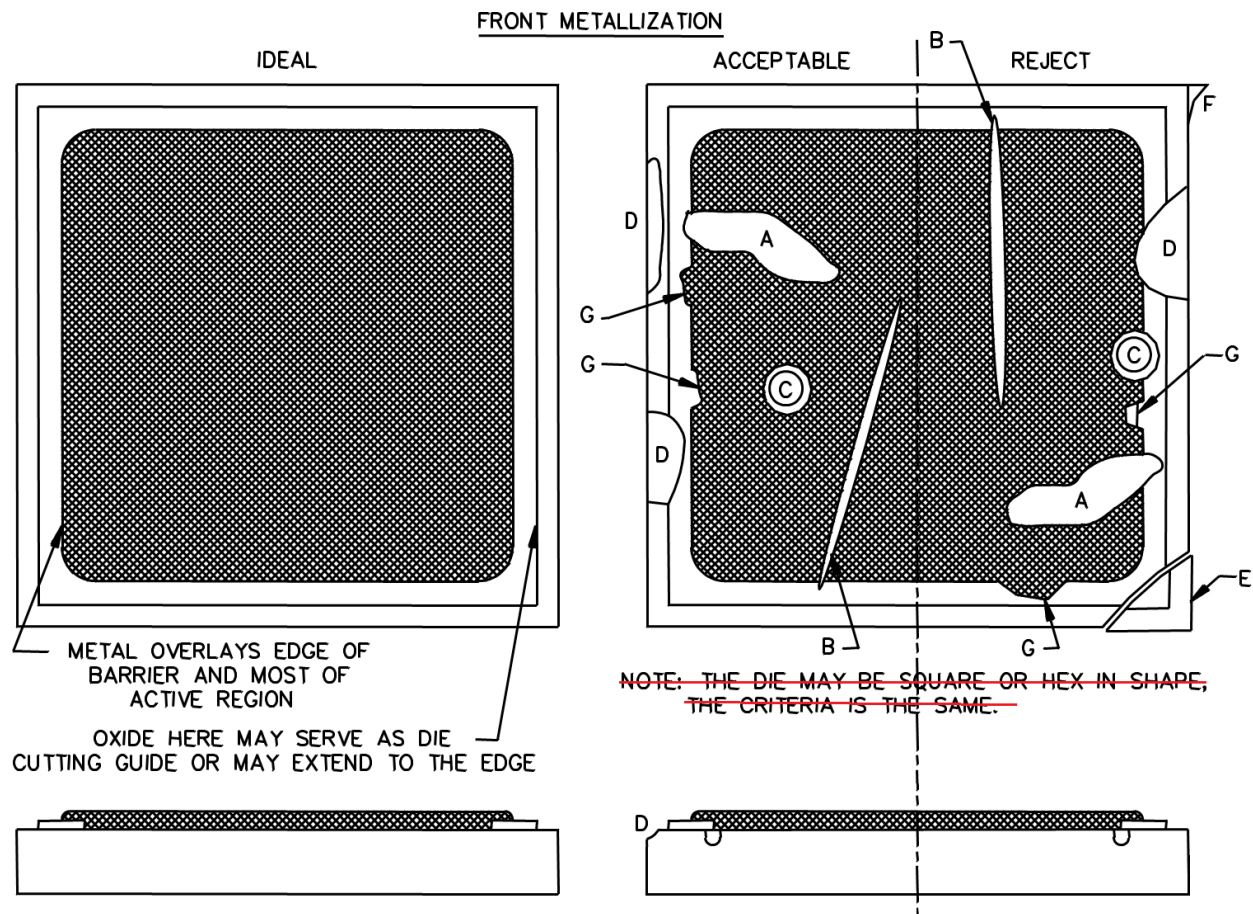


FIGURE 2073-8. Schottky barrier diodes (metal overlays barrier edge and active area field plate).

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**Reject criteria:**

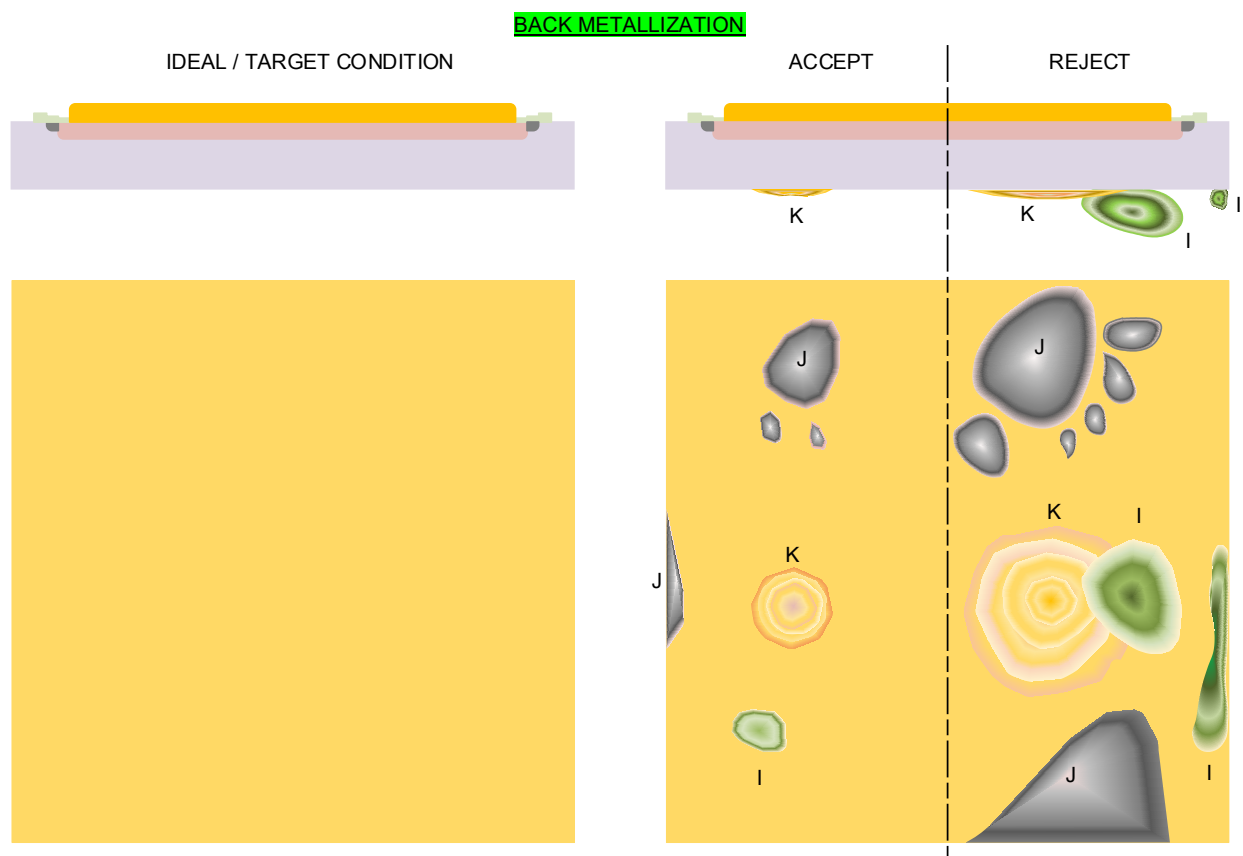
1. Smears (A), scratches (B) or probe marks (C) **may shall** not extrude metal outside metalized region more than 50 percent to the next geometric boundary.
2. Edge chipping (D) **may shall** not extend into metallization.
3. Missing pieces (E) extending more than 50 percent of distance from chip edge and metallization or additional attached pieces (F) that exceed **chip die** dimensional specifications **are not permitted shall not be acceptable**.
4. Additional front metallization extending 50 percent or more to the next geometric boundary (G) or pulled back to reveal contact area or any non-passivated barrier region **shall not be acceptable**.
5. Cracks (not illustrated) **must shall** not extend under the metalized areas and **must shall** not be present inside any of the active regions.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-8. Schottky barrier diodes (metal overlays barrier edge and active area field plate).

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Reject criteria:

1. Backside contamination and foreign material (I), either firmly or loosely attached, exceeding 10 percent of total area.
2. Missing backside metal (J) exceeding 20 percent of total area.
3. Blisters (K) in metallization exceeding 10 percent of total area.

NOTES:

1. The cross-sectional views are for reference only.
2. The die may be square or hexagonal in shape. The acceptance criteria are the same.

FIGURE 2073-9. Back side (bottom) inspection criteria.